Application Note

Detailed Explanation of S-Parameters and the FPD-Link Channel Specification

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ABSTRACT

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With the rapid advancement of Advanced Driver Assistance Systems (ADAS) and In-Vehicle Infotainment (IVI) systems, the number of onboard sensors—such as cameras, radars, and displays—along with their associated bandwidth requirements, has grown exponentially. FPD-Link, a high-speed serializer/deserializer (SerDes) technology developed by Texas Instruments specifically for automotive video transmission, supports data rates of up to several gigabits per second over coaxial cables or shielded twisted pairs (STP). It is widely deployed in infotainment, ADAS camera links, and automotive radar transmission. As FPD-Link evolves from the third generation (FPD-Link III, 4.16Gbps) to the fourth generation (FPD-Link IV, 7.55Gbps and beyond), the challenges associated with signal integrity and link design have become increasingly significant.

S-parameters (Scattering Parameters) are a fundamental tool for characterizing the performance of RF and high-speed digital links, providing a comprehensive description of a transmission channel's reflection characteristics (return loss, S_{11} or S_{22}) and transmission characteristics (insertion loss, S_{21} or S_{12}). In FPD-Link automotive applications, S-parameters are utilized throughout the entire product lifecycle—from chip design and board development to cable/connector selection and full-vehicle validation. They serve as a critical basis for channel budget allocation, fault diagnosis, and link margin assessment.

This paper, targeting FPD-Link automotive applications as the ultimate objective, provides a systematic and in-depth analysis of S-parameter theory, physical interpretation, and key specifications in the context of the FPD-Link Channel Specification. It details Vector Network Analyzer (VNA) measurement methodologies and focuses on the practical application of S-parameters in vehicle-level channel budget allocation, PCB material selection, and connector and harness testing standards. Furthermore, drawing on typical debugging case studies, this paper offers diagnostic strategies and troubleshooting approaches for common S-parameter anomalies, enabling engineers to develop comprehensive S-parameter analysis capabilities in ADAS and IVI system development, thereby ensuring signal integrity in high-speed serial links from theory to measurement.

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1 Fundamentals of S-Parameter Theory

In Advanced Driver Assistance Systems (ADAS) and In-Vehicle Infotainment (IVI) systems, as the data rates of high-speed serializer/deserializer (SerDes) technologies such as FPD-Link continue to increase, the demand for high-frequency signal simulation, testing, and evaluation has become increasingly prominent. S-parameters (Scattering Parameters), as the core metrics for characterizing high-speed signal channel performance, are a primary consideration for FPD-Link users. This chapter starts with characteristic impedance and progressively analyzes insertion loss, return loss, and multi-port network models.

1.1 Characteristic Impedance Explained

Characteristic Impedance (Z_0) is the "wave impedance" exhibited by the interaction between electric and magnetic fields as an electromagnetic wave propagates through a transmission line medium. At high frequencies, when the conductor length exceeds 1/10 of the signal wavelength, the conductor can no longer be treated as an ideal conductor and must be analyzed using a distributed parameter model (RLCG model).

Theoretical Basis: According to the Telegrapher's Equations, characteristic impedance is determined by the distributed inductance (L) and distributed capacitance (C) of the transmission line. For an ideal lossless line, it is calculated as:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{1}$$

In PCB layout design, the following factors affect characteristic impedance:

1. Trace Width (W): The conductor width directly affects the capacitance component. As trace width increases, the capacitance between the conductor and the reference plane increases, resulting in lower characteristic impedance. For example, when a microstrip line width increases from 5mil to 10mil, under the same dielectric conditions, characteristic impedance may decrease from 70Ω to 35Ω.
2. Dielectric Thickness (H): The distance between the signal layer and the reference plane. Increasing dielectric thickness reduces the capacitance per unit length, thereby increasing characteristic impedance. For example, increasing dielectric thickness from 4 mil to 8mil may raise characteristic impedance from 50Ω to 70Ω.
3. Copper Thickness (T): Conductor thickness affects the fringing field distribution. As copper thickness increases, the fringing capacitance effect intensifies, and characteristic impedance decreases slightly. Typically, 1oz copper (1.4mil) results in characteristic impedance approximately 2–3Ω lower than 0.5oz copper (0.7mil).
4. Dielectric Constant (ε_r): An inherent property of the dielectric material. Higher ε_r values result in greater capacitance per unit length and lower characteristic impedance. For example, under the same geometric dimensions, FR4 material with ε_r = 4.5 yields characteristic impedance approximately 15% lower than high-frequency material with ε_r = 3.5.

There are two PCB trace models: microstrip line and stripline.

1. Microstrip Line

   Structural Characteristics: The signal conductor is located on the PCB surface, with the dielectric substrate and reference plane beneath.

   Characteristics: Partially exposed to air, the effective dielectric constant lies between that of air and the substrate material.

   Typical Applications: High-speed signal routing on outer layers.

   Advantages: Easy routing and testing.

   Impedance Calculation Formula:

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right) \tag{2}$$

2. Stripline

Structural Characteristics: The signal conductor is completely embedded in the dielectric between two reference planes.

Characteristics: Fully surrounded by dielectric, with a more uniform electric field distribution compared to microstrip.

Typical Applications: High-speed signal routing on inner layers.

Advantages: Better electromagnetic shielding performance.

Impedance Calculation Formula:

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{1.9(2H+T)}{0.8W+T}\right) \quad (3)$$

In automotive applications, to achieve maximum power transfer and minimize reflections, impedance control standards are strictly defined: Coaxial Cable (Coax): Standard single-ended impedance is 50Ω. Shielded Twisted Pair (STP): Standard differential impedance is 100Ω. Any impedance discontinuities—such as connectors, vias, or trace width changes—cause signal reflections, thereby affecting signal integrity.

1.2 Reflection Coefficient Explained

The reflection coefficient Γ describes the degree of reflection at an impedance discontinuity, defined as:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (4)$$

where Z_L is the load impedance and Z_0 is the characteristic impedance of the transmission line.

Physical Mechanism of Reflection: When a signal propagates to an impedance discontinuity, a portion of the energy is reflected back to the source, while the remaining energy continues to propagate forward. The magnitude of reflection depends on the degree of impedance mismatch. For example: When $Z_L = Z_0$, Γ = 0 — ideal condition, all signal energy is transmitted, no reflection.

When $Z_L = \infty$ (open circuit), Γ = 1 — all signal energy is reflected.

When $Z_L = 0$ (short circuit), Γ = −1 — all signal energy is reflected, and the reflected energy is phase-inverted relative to the incident energy.

In practical applications, common causes of non-ideal transmission include:
1. Impedance discontinuities at connector pads and interfaces.
2. Inductive effects introduced by vias.
3. Additional capacitive loading from stubs.
4. Transition points where different transmission line types join.

1.3 Insertion Loss Explained

Insertion Loss (S_{21}) refers to the energy loss of a signal during transmission through the link, expressed in dB. For a passive system, S12 = S21; therefore, this document only describes forward insertion loss S21, hereinafter referred to as insertion loss. It is a key metric for measuring power loss when a signal passes through a transmission channel. In FPD-Link systems, insertion loss directly determines the maximum transmission distance and link margin.

Contributing Factors: S_{21} loss is primarily composed of the following four mechanisms:
1. Conductor Loss: Caused by the skin effect. At high frequencies, current concentrates near the conductor surface, reducing the effective conduction area and increasing resistance. Copper foil roughness (e.g., VLP copper vs. standard ED copper) has a significant impact on this loss.
2. Dielectric Loss: Caused by polarization hysteresis in dielectric materials. It is proportional to frequency and determined by the loss tangent (tanδ). High-frequency laminates (such as Rogers RO4003C) have a tanδ much lower than that of standard FR4.

3. Radiation Loss: At high frequencies, microstrip lines radiate a portion of energy into the surrounding space in the form of electromagnetic waves.
4. Mismatch Loss: Caused by energy reflection due to impedance discontinuities at connection points. Although this is primarily reflected in S_{11}, it indirectly affects the measured S_{21} values.

Key Considerations in Actual Development:

1. Frequency Dependence: Insertion loss increases with frequency. For example, at 10GHz, the loss of FR4 material is several times higher than at 1GHz. Developers must pay closer attention to PCB trace design and simulation at high frequencies.
2. Link Budget: When designing FPD-Link channels, it is essential to ensure that S_{21} at the Nyquist frequency still meets the receiver (deserializer) sensitivity requirements, and it is recommended to maintain a 3dB link margin.

1.4 Return Loss Explained

Return Loss (S_{11}) characterizes the degree of impedance matching on a transmission line. It is the dB representation of the reflection coefficient (Γ) and directly reflects the amount of signal energy reflected back to the source during transmission.

The relationship between return loss and reflection coefficient Γ is:

$$RL = 20 \cdot \log_{10}(|\Gamma|) \quad [dB] \tag{5}$$

A larger absolute value of S_{11} (i.e., a more negative value, for example, −20dB is better than −10 dB) indicates less reflection and better matching. Voltage Standing Wave Ratio (VSWR): Another common representation of return loss, defined as the ratio of the maximum to minimum voltage on the transmission line:

$$VSWR = \frac{1 + |\Gamma|}{1 - |\Gamma|} \tag{6}$$

A VSWR closer to 1 indicates better impedance matching.

In automotive environments, connector mating/unmating, component pads on PCBs, PCB manufacturing tolerances, and cable bending all introduce impedance discontinuities. The FPD-Link Channel Specification typically requires that the overall link S_{11} be better than −10 dB within the target frequency band (−12dB recommended for PCB) to ensure efficient signal energy transfer to the receiver and to avoid intersymbol interference (ISI) caused by multiple reflections.

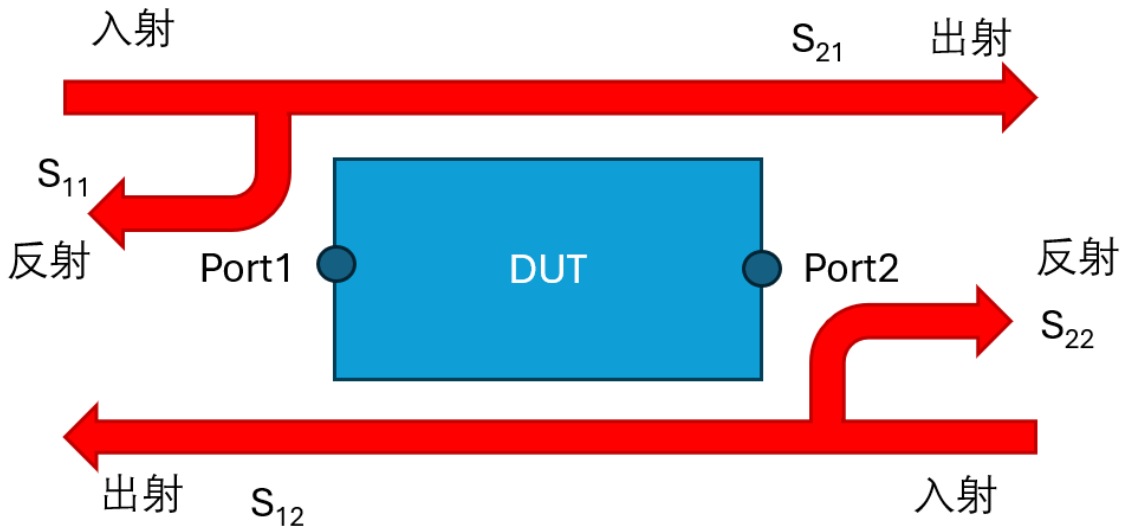

Figure 1-1. S-Parameter Diagram

1.5 Two-Port and Four-Port S-Parameters Explained

S-parameters establish a mathematical model for high-frequency networks by describing the relationship between incident waves (a) and reflected waves (b). Based on the signal transmission mode, they are primarily divided into two-port (single-ended) and four-port (differential) models.

In automotive industry applications: Two-Port Network (Single-Ended Mode): Applicable to coaxial cable (COAX) signal analysis. Four-Port Network (Differential Mode): Applicable to shielded twisted pair (STP) signal analysis.

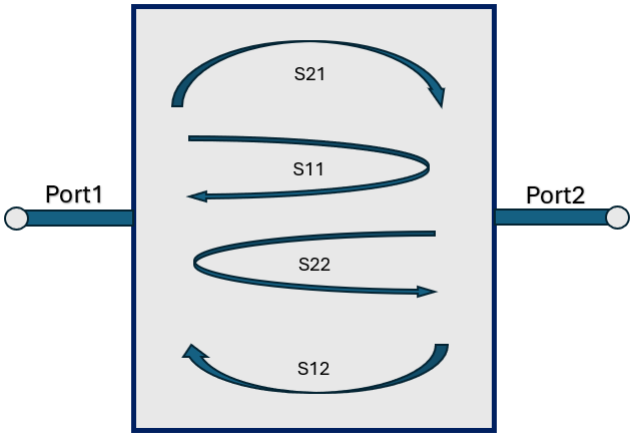

Figure 1-2. Two-Port Transmission Diagram

A four-port network, which consists of the incident and reflected ports for a differential pair, is typically converted to mixed-mode S-parameters for analysis: S_{DD} (Differential-Differential): Differential-mode signal transmission and reflection.

SDD_{21}: Differential insertion loss — core performance metric.

SDD_{11}: Differential return loss — measures differential pair matching.

S_{CC} (Common-Common): Common-mode signal transmission and reflection — related to EMI characteristics.

S_{DC} (Differential to Common): Mode conversion — a core metric for measuring differential pair asymmetry. Low S_{DC} values indicate good symmetry and effective common-mode noise suppression.

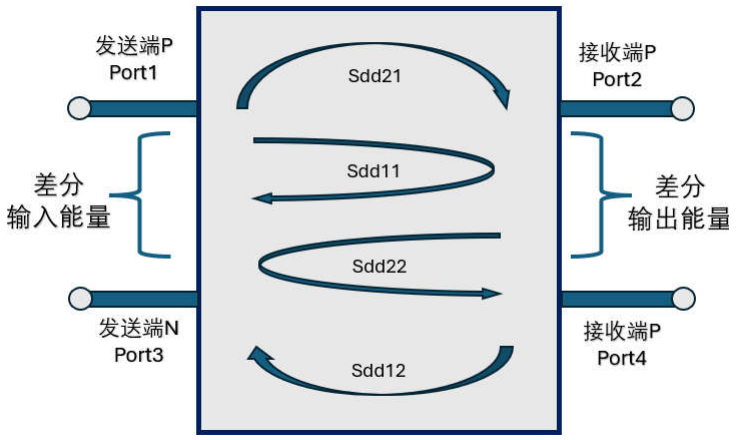

Figure 1-3. Four-Port Transmission Diagram

2 S-Parameter Measurement Methods and Calibration Techniques

2.1 Introduction to Vector Network Analyzer Principles

The Vector Network Analyzer (VNA) is the core instrument for measuring the network parameters (primarily S-parameters) of RF and microwave devices. Its basic operating principle involves generating a known-frequency and known-amplitude stimulus signal via an internal signal source and feeding it into the Device Under Test (DUT). The VNA incorporates high-precision receivers capable of simultaneously measuring the magnitude and phase information of incident, reflected, and transmitted waves.

By comparing the received signals with the reference signal, the VNA computes S-parameters in complex form. Modern VNAs typically employ a four-receiver architecture, enabling simultaneous measurement of forward (S_{11}, S_{21}) and reverse (S_{22}, S_{12}) transmission and reflection characteristics in a single connection setup. In high-speed digital applications such as FPD-Link, the broadband capability of the VNA (typically requiring coverage up to the 3rd to 5th harmonics of the SerDes data rate) is critical for accurately assessing channel loss and impedance continuity.

The core strength of the VNA lies in its ability to separate incident and reflected waves, which is accomplished through directional couplers or bridges. A directional coupler allows signals to flow from the source to the load (forward direction) while simultaneously coupling off a small portion of the reflected signal. By measuring the ratios of the reference channel (R) to the test channels (A, B), the VNA eliminates the effects of source power fluctuations, thereby achieving highly accurate measurement results. Furthermore, the dynamic range of the VNA determines the minimum measurable loss and maximum isolation, which is particularly crucial for evaluating far-end crosstalk (FEXT) in high-speed SerDes channels.

2.2 TDR Measurement Explained

Time Domain Reflectometry (TDR) is a technique that utilizes reflection principles to characterize transmission line properties. Although VNAs primarily operate in the frequency domain, modern VNAs can emulate TDR functionality through the Inverse Fast Fourier Transform (IFFT), converting frequency-domain S-parameters into time-domain responses.

The operating principle of TDR is analogous to radar: a fast-rise-time step stimulus or pulse signal is sent into the transmission line. When the signal propagates along the transmission line and encounters an impedance change (discontinuity), a portion of the energy is reflected back to the source. By analyzing the amplitude and time delay of the reflected signal, the location and nature of the impedance discontinuity can be determined.

From the reflection coefficient formula derived in Section 1.2, it follows that: if the reflected voltage is positive, the impedance increases (inductive behavior, e.g., vias, connectors); if the reflected voltage is negative, the impedance decreases (capacitive behavior, e.g., oversized pads, stubs).

Locating Impedance Mismatch Distance: The distance *D* to the fault point can be calculated using the formula $D = \left(c \cdot t\right) / \left(2 \cdot \sqrt{\varepsilon_r}\right)$, where *c* is the speed of light, *t* is the round-trip time, and ε_r is the dielectric constant of the medium.

During TDR testing, the system must first be calibrated to eliminate errors introduced by cables and connectors, and the TDR edge rate must be set according to the signal frequency being tested (for FPD-Link IV devices, 35ps is recommended). The instrument then precisely locates the physical distance to the fault or discontinuity by analyzing the time difference of the reflected pulse return (using the formula: distance = propagation velocity × round-trip time / 2); simultaneously, the polarity and amplitude of the reflected waveform are used to determine the nature of the fault—a positive reflection (waveform upward) indicates an increase in impedance, while a negative reflection (waveform downward) indicates a decrease in impedance. Through this non-destructive testing approach, engineers can intuitively obtain an impedance profile of the entire channel, enabling rapid assessment of signal integrity and precise localization of physical defects.

Application in FPD-Link: TDR is the "gold standard" for diagnosing impedance matching issues in automotive harnesses and PCBs. It provides an intuitive impedance profile of the entire channel—from the SerDes chip pad through PCB traces and connectors to the cable—helping engineers quickly pinpoint the specific physical locations that are causing signal integrity problems.

2.3 VNA Calibration Operating Procedure

To eliminate errors introduced by the test system (cables, connectors, adapters), calibration must be performed prior to measurement. The following is a standard SOLT (Short-Open-Load-Thru) calibration procedure using a Keysight VNA:

Instrument Warm-up and Setup: Turn on the VNA and allow it to warm up to ensure thermal stability of the internal source and receivers. Set the start frequency, stop frequency, and the number of sweep points.

Select Calibration Kit: In the VNA software, select the calibration kit definition that corresponds to the actual calibration standards being used (e.g., 85052D or N4691E electronic calibration module). This step is critical, as different calibration standards have distinct mechanical dimensions and electrical models.

One-Port Calibration: Sequentially connect the Open, Short, and Load standards to the test port and execute the calibration routine in the instrument.

Two-Port Calibration: In addition to the steps above, connect a Thru standard between Port 1 and Port 2 and execute the instrument calibration. The calibration process automatically calculates and stores the error terms (directivity, source match, reflection tracking, etc.).

Calibration Verification: After calibration is complete, connect a known verification standard and observe the S_{11} and S21 curves. Using an open circuit as an example: if S_{11} is flat (close to 0dB) and S21 is extremely low (close to the instrument's noise floor), the calibration is considered successful.

2.4 Test Methods for S_{11} and S_{21}

This section uses single-ended cable S-parameter measurement as an example. For differential cables, S-parameter measurements are typically performed using a four-port VNA or a two-port VNA with an optional upgrade.

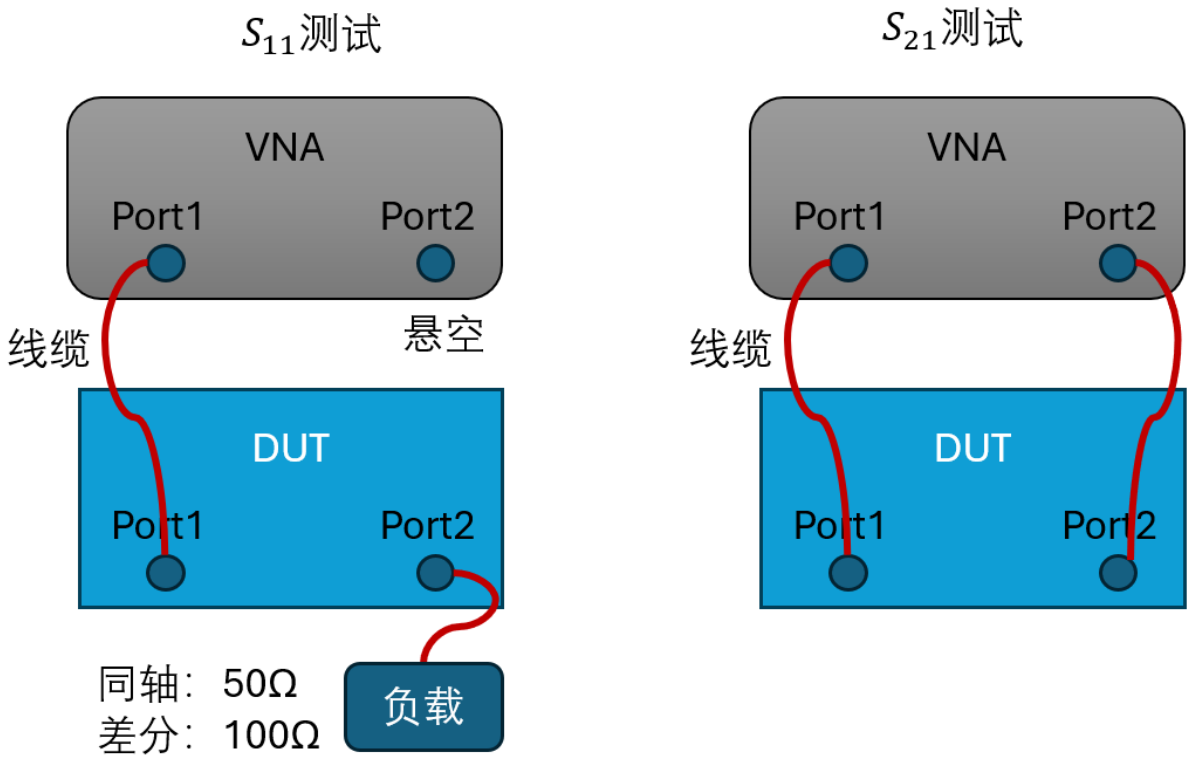

Figure 2-1. S_{11} and S_{21} Connection Diagram

S_{11} Test:

As shown in Figure 2-1, the connection configuration is as follows: VNA Port 1 is connected to the DUT input, and the DUT output must be terminated with a precision 50Ω load (or 100Ω differential load for differential lines). Locate the S_{11} trace icon on the instrument and select it; the S_{11} measurement curve will then be displayed. Data Analysis: The primary focus is on whether the return loss across the entire frequency band meets the Channel Specification requirements (e.g., less than -10dB). Periodic ripples on the S_{11} curve typically indicate impedance discontinuities or stub effects along the transmission line.

S_{21} Test:

As shown in Figure 2-1, the connection configuration is as follows: VNA Port 1 is connected to the DUT input, and Port 2 is connected to the DUT output. Similarly, locate the S_{21} trace icon on the instrument and select it; the S_{21} measurement curve will then be displayed. Data Analysis: The primary focus is on whether the insertion loss at each frequency point across the entire frequency band meets the Channel Specification. The slope of the S_{21} curve reflects the combined effects of skin effect and dielectric loss. In FPD-Link systems, it is essential to ensure that the S_{21} curve is smooth and free of abnormal notches; otherwise, the equalizer (EQ) at the deserializer receiver may fail to converge.

Note

For FPD-Link applications, it is imperative to ensure that the FPD-Link channel specification is met across the entire Nyquist frequency range, rather than only at a single Nyquist frequency point.

3 FPD-Link Channel Specification Analysis

3.1 Overview of Total Link, PCB, and Cable Channel Specifications

In FPD-Link automotive applications, as illustrated in Figure 3-1, the Channel Specification typically provides requirements and reference standards for the total link, PCB, and cable separately. This differentiation is primarily driven by the needs of vehicle-level signal integrity budget allocation and practical engineering implementation.

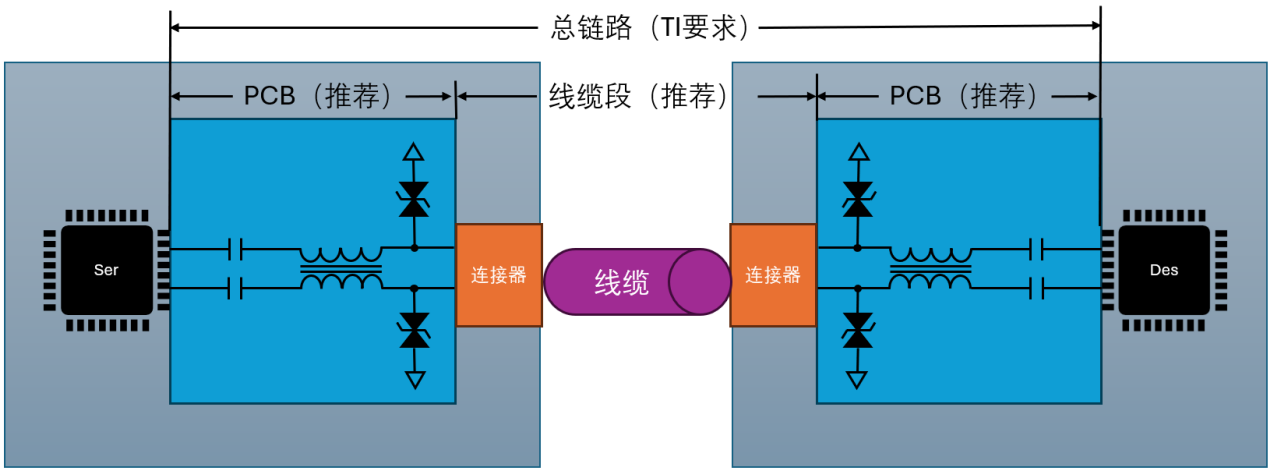

Figure 3-1. FPD-Link Total Channel, PCB, and Cable Diagram

As shown in Figure 3-1, the Total Channel encompasses the complete physical path from the transmitter (Serializer) device pin to the receiver (Deserializer) device pin. It represents the true end-to-end signal transmission path within the vehicle, including PCB traces, connectors, harnesses, and all interface-related physical effects. Note: The Total Channel Specification is the fundamental requirement for ensuring normal and stable FPD-Link operation; therefore, it constitutes a mandatory requirement on the link, not a recommendation.

PCB and Cable: In vehicle design and manufacturing, PCB fabrication and harness manufacturing are typically handled by separate suppliers. The separation of PCB and Cable Specifications facilitates independent quality control and testing of components from different vendors. For instance, PCB material loss and cable shielding performance each require individual metrics to ensure that after all components are assembled into the complete vehicle, the total channel performance still meets the requirements. Since the PCB and cable are constituent parts of the overall channel, and for the FPD-Link chip, stable and normal operation is guaranteed as long as the total channel specification is satisfied, the PCB and Cable Specifications are therefore recommended guidelines rather than mandatory requirements.

3.2 Channel Specification Analysis

In high-speed serial link design, the Total Channel Requirement is a mandatory hard specification that the entire high-speed link (PCB + cable) must strictly comply with. The system's final insertion loss, return loss, and other parameters must meet this specification to ensure signal integrity and proper communication between chips.

In addition to the Total Channel Requirement, two additional columns of data are typically provided: the PCB Budget and the Cable Assembly Budget. These are recommended reference values derived from engineering experience. It is important to emphasize that these two recommended values are not mandatory absolute targets, regardless of how the loss is actually distributed between the PCB and the cable in practical testing. In actual design, these two portions follow a "trade-off" budget allocation principle.

- If the PCB trace is long and results in higher loss, this can be compensated by selecting a high-quality, low-loss cable;
- Conversely, if the cable loss is relatively high, the PCB design must adopt lower-loss dielectric materials or shorter trace lengths.

As long as the combined loss of the PCB and cable, when summed, still meets the overall budget of the Total Channel Requirement, the design is deemed compliant.

Additionally, in the 98x Channel Specification, due to the higher data rates at which 98x devices operate, there are often scenarios in the design phase where it is difficult for the PCB to meet the recommended PCB targets specified in the Channel Specification. To address this, the 98x Channel Specification provides two alternative reference standards: PCB Focus and Cable Focus. The core distinction lies in how the total budget is flexibly allocated between the board and the cable. In system design, customers need only satisfy one of the two approaches to meet the recommended values of the 98x Channel Specification and comply with TI's design recommendations.

3.3 Key Design and Test Considerations for the FPD-Link Channel Specification

To ensure stable operation of FPD-Link links in the complex automotive environment, beyond the fundamental S-parameter metrics, special attention must be paid to the following critical engineering variables when defining and validating the Channel Specification:

1. Importance of Test Environment Calibration: When performing high-precision S-parameter measurements, proper calibration of the Vector Network Analyzer (VNA) and its test fixtures is essential. Appropriate calibration methods (such as SOLT or TRL) must be employed to accurately extend the reference plane to the ports of the Device Under Test (DUT). If the test setup cannot calibrate out the fixtures simultaneously, de-embedding of the fixtures is required; otherwise, the additional loss and phase delay introduced by the test fixtures or cables will be incorrectly factored into the Channel Specification, leading to misinterpretation of link performance or even masking genuine signal integrity issues.
2. Impact of Repeated Connector Mating Cycles on S-Parameters: In automotive electronics, connectors undergo numerous mating and unmating cycles during assembly, repair, and testing. Repeated mechanical insertion can cause contact wear, spring fatigue, or micro-deformation, which alters contact impedance and exacerbates impedance discontinuities. When defining the Specification, the degradation of high-frequency electrical performance (particularly return loss and insertion loss) over the connector's lifecycle due to mechanical durability should be taken into account, ensuring that signal transmission requirements are still met after multiple mating cycles.
3. Effect of Harness Bending Radius on Performance: During vehicle wiring, harnesses inevitably undergo bending and routing. An excessively small bending radius alters the physical geometry of coaxial cables or twisted pairs, disrupting their original uniform transmission line characteristics, leading to localized characteristic impedance discontinuities and degraded shielding effectiveness. Therefore, Channel Specification validation must include performance testing of the harness under actual installation bending radius, ensuring that insertion loss and crosstalk remain within safe margins under extreme routing conditions.
4. Influence of Temperature Variation on Dielectric Constants: Automotive operating environments experience extreme temperature ranges (typically -40°C to +85°C or even higher). The dielectric constant (Dk) of PCB materials and cable insulating dielectrics drifts with temperature, directly causing the characteristic impedance of transmission lines to vary with temperature fluctuations, thereby affecting S_{11} (return loss) and phase stability of signal transmission. When designing the Channel Specification, environmental factors must be incorporated into the evaluation, with impedance variation across the full temperature range assessed to prevent communication bit errors caused by excessive signal reflection under extreme temperature conditions.

4 Conclusion

The evolution of FPD-Link technology has imposed stringent challenges on the design of high-speed in-vehicle links, making S-parameter analysis a core methodology for ensuring signal integrity. This paper begins with the fundamental theories of characteristic impedance, reflection, and transmission loss, and systematically elaborates on the physical meaning and measurement methods of S-parameters. It also clarifies the differences between total links and component-level specifications within the FPD-Link channel specification. In engineering practice, by following the test guidelines and precautions presented herein, designers can accurately achieve the signal integrity metrics required for the designed and tested links, thereby ensuring the stable operation of high-speed data links.

5 References

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2. Texas Instruments, FPD-Link-IV-ADAS-ChannelSpec-Rev1p2_FPD4Coax, FPD-Link Application note.
3. Texas Instruments, Channel Requirements-DS90Ux98x_Rev1p2, FPD-Link Application note.

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