EVM User's Guide: ADS122S14EVM

SNSR-DUAL-ADC-EVM Evaluation Module

1 Description

The SNSR-DUAL-ADC-EVM is a low-power, precision sensor measurement design comprised of two ADS122S14 analog-to-digital converters (ADC) and a single MSPM0G1507 microcontroller (MCU). The ADS122S14 is a precision, low-power, 8-channel, 24-bit delta-sigma ADC. The MSPM0G1507 is a 32-bit MCU on the enhanced Arm® Cortex®-M0+ 32-bit core platform operating at clock speeds up to 80MHz.

2 Features

- 2x ADS122S14 24-bit precision ADCs
- MSPM0G1507 32-bit ARM MCU
- 8-pin analog input header supporting:
  - Resistive bridge measurement
  - NTC and PTC measurement
  - 2-, 3-, and 4-wire RTD measurement
  - Thermocouple measurement
- 4-pin header with excitation options including:
  - IDAC
  - REFOUT
  - VDD
- JTAG connector for programming the MCU
- Isolated USB for terminal communication in a 4-20mA loop
- Connection terminal for TI Loop Control AFE Transmitter
- 8-pin analog input header
- SPI communication header for digital signal monitoring

3 Applications

- Field transmitters:
  - Temperature
  - Pressure
  - Flow
  - Strain
- General sensor system analysis

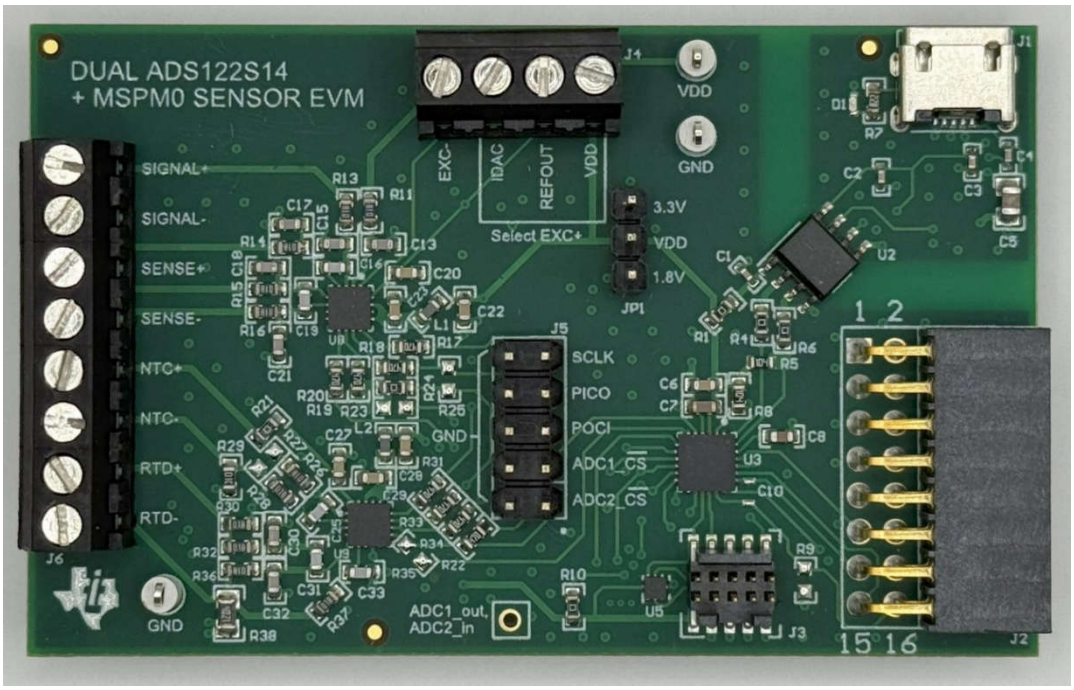

Figure 4-1. SNSR-DUAL-ADC Evaluation Module

4 Evaluation Module Overview

4.1 Introduction

The SNSR-DUAL-ADC-EVM is a platform for evaluating a low-power, small size, precision ADC + MCU reference design for sensor measurement applications. The SNSR-DUAL-ADC-EVM board includes two ADS122S14 ADCs for sensor signal acquisition and a single MSPM0G1507 MCU as the system controller. The SNSR-DUAL-ADC-EVM enables communication between the ADCs and the MCU using either a daisy-chain configuration or independent operation using dedicated chip select ($\overline{CS}$) pin.

This users' guide describes the characteristics, operation and the use of the SNSR-DUAL-ADC-EVM. The SNSR-DUAL-ADC-EVM eases the evaluation of the device in precision field transmitter as well as any systems that require multiple ADCs. This users' guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the SNSR-DUAL-ADC-EVM.

4.2 Kit Contents

The SNSR-DUAL-ADC-EVM evaluation module kit includes the following features:

- Hardware required for diagnostic testing as well as accurate performance evaluation of a low-power, precision field transmitter using the ADS122S14 and the MSPM0G1507.
- Windows® 10 and 11 operating systems support.
- An A-to-Micro-B USB Cable

4.3 SNSR-DUAL-ADC-EVM Specifications

Table 4-1 provides the SNSR-DUAL-ADC-EVM board specifications.

Table 4-1. SNSR-DUAL-ADC-EVM Specifications

PARAMETER	CONDITIONS	VALUE
Temperature	Recommended operating free-air temperature range, T_A	15°C ≤ T_A ≤ 35°C
VDD (Recommended voltage range, external source)	VDD to GND	1.74V ≤ VDD ≤ 3.6V
Power supply current range (external power supply)	Supply current range $\|I_S\|$	$\|I_S\|$ ≤ 0.1A
Analog input voltage range	Gain = 0.5 to 10	GND ≤ VIN ≤ VDD - 0.35V
	Gain = 16 to 256	GND + 0.35 ≤ VIN ≤ VDD - 0.4V
ADC digital communication	Communication to the ADCs using SPI Header	1.8V or 3.3V
JTAG VDD	VDD supplied through the LaunchPad™ JTAG	3.295 - 3.305V
JTAG communication	Digital communication level	3.3V

4.4 Device Information

The ADS122S14 is a precision, low-power, 24-bit delta-sigma ADC that offers many integrated features to reduce system cost and component count including:

- Eight analog inputs through a flexible multiplexer that enables measurement of multiple sensor types with one device.
- Low noise programmable gain amplifier that enables precise sensor measurements.
- External VREF inputs for external ratiometric sensors.
- Two programmable current sources to bias sensors including RTDs and resistive bridges.
- Internal programmable voltage reference.
- Four General Purpose I/Os(GPIOs) that are configurable as push-pull or open drain outputs.

The ADS122S14 can be connected in a daisy-chain configuration to reduce the number of SPI connections in systems that require simultaneous measurement of multiple signals. The daisy-chain connection links together the SPI output (SDO) of one device to the SPI input (SDI) of the next device so that the devices in the chain appear as a single logical device to the controller. There is no special programming required for daisy-chain operation. Apply additional shift clocks to access all devices in the chain.

Table 4-2. ADS122S14 Device Specifications

ADS122S14 SPECIFICATION	VALUE
Package size (WQFN)	3.00mm × 3.00mm
Package size (DSBGA)	2.00mm × 2.00mm
Operating temperature range	-40°C to 125°C
AVDD to GND supply voltage	1.74V to 3.6V
DVDD to GND supply voltage	1.65V to 3.6V
Voltage reference inputs	0.5V to AVDD
Absolute input current	-2nA to 2nA
Programmable gain	0.5 to 256

The MSPM0G1507 is a 32-bit MCU on the enhanced Arm® Cortex®-M0+ 32-bit core platform operating at clock speeds up to 80MHz frequency. The MCU provides up to 128KB embedded flash program memory and up to 32KB SRAM. The MSP also incorporates a memory protection unit for memory isolation, 7-channal DMA, math accelerator for linearization and a variety of analog peripherals.

Table 4-3. MSPM0G1507 Device Specifications

MSPM0G1507 SPECIFICATION	VALUE
Package size (24-pin VQFN)	4.00mm × 4.00mm
Operating temperature range	-40°C to 125°C
VDD to GND supply voltage	1.62V to 3.6V
MCLK frequency	Up to 80MHz
ULPCLK frequency	Up to 40MHz

4.5 Getting Started With the SNSR-DUAL-ADC-EVM

The following list of steps provides an overview to quickly get the SNSR-DUAL-ADC-EVM setup and operational. The subsequent sections in this document expand on each step and explain in detail the SNSR-DUAL-ADC-EVM available features. Links are provided to navigate from this quick-start guide to the appropriate section at each step, where applicable:

1. Remove the SNSR-DUAL-ADC-EVM and USB cable from the box.
2. Connect the A-to-Micro-B USB cable from EVM directly to a USB port on the computer. Do not connect the cable through a USB hub. A green LED on the EVM indicates a valid connection.
3. Power the EVM using one of the power connection options in Table 5-1.
4. Connect sensors or signals to the input terminal block J6 and the excitation terminal block J4.
   a. Measuring a Voltage-Excited 6-wire Bridge Using ADC1 and a Low-side Bias Resistor Using ADC2
   b. Measuring a Voltage-Excited 6-wire Bridge Using ADC1 and a Current-Excited 2-wire RTD Using ADC2
   c. Measuring a Current-Excited 4-wire Bridge Using ADC1 and a Voltage-Excited Thermistor Using ADC2
   d. Measuring a Thermocouple Using ADC1 and an NTC for Cold-Junction-Compensation Using ADC2
   e. Measuring One 3-wire RTD Using ADC1 and One 3-wire RTD Using ADC2
   f. Measuring One 4-wire RTD Using ADC1 and One 4-wire RTD Using ADC2
   g. Measuring Generic Voltage or Current Inputs
5. Open a terminal program.
   a. Use the integrated serial terminal in Code Composer Studio if a terminal program is not installed.
6. The EVM arrives with firmware programmed and is therefore ready to use out of the box. Data can be captured and streamed from the system without any additional components or boards.
   a. The Software section describes these programmed functions.

Optional: The latest version of the SNSR-DUAL-ADC-EVM software can be downloaded at https://github.com/TexasInstruments/precision-adc-examples.

5 Hardware

5.1 Hardware Overview

The SNSR-DUAL-ADC-EVM provides a field transmitter reference design that integrates two ADS122S14 ADCs with an MSPM0G1507 controller. Several interface options provide the user multiple ways to configure, control, and receive data from the EVM. Use a TI LP-MSPM0G3507 or other equivalent LaunchPad to program the onboard MSPM0G1507. Use the Loop Control AFE Transmitter for analog output transmitter systems, such as a 4-20mA industrial loop.

Figure 5-1 shows the hardware components required to interface with the EVM and highlights optional external interface equipment in red.

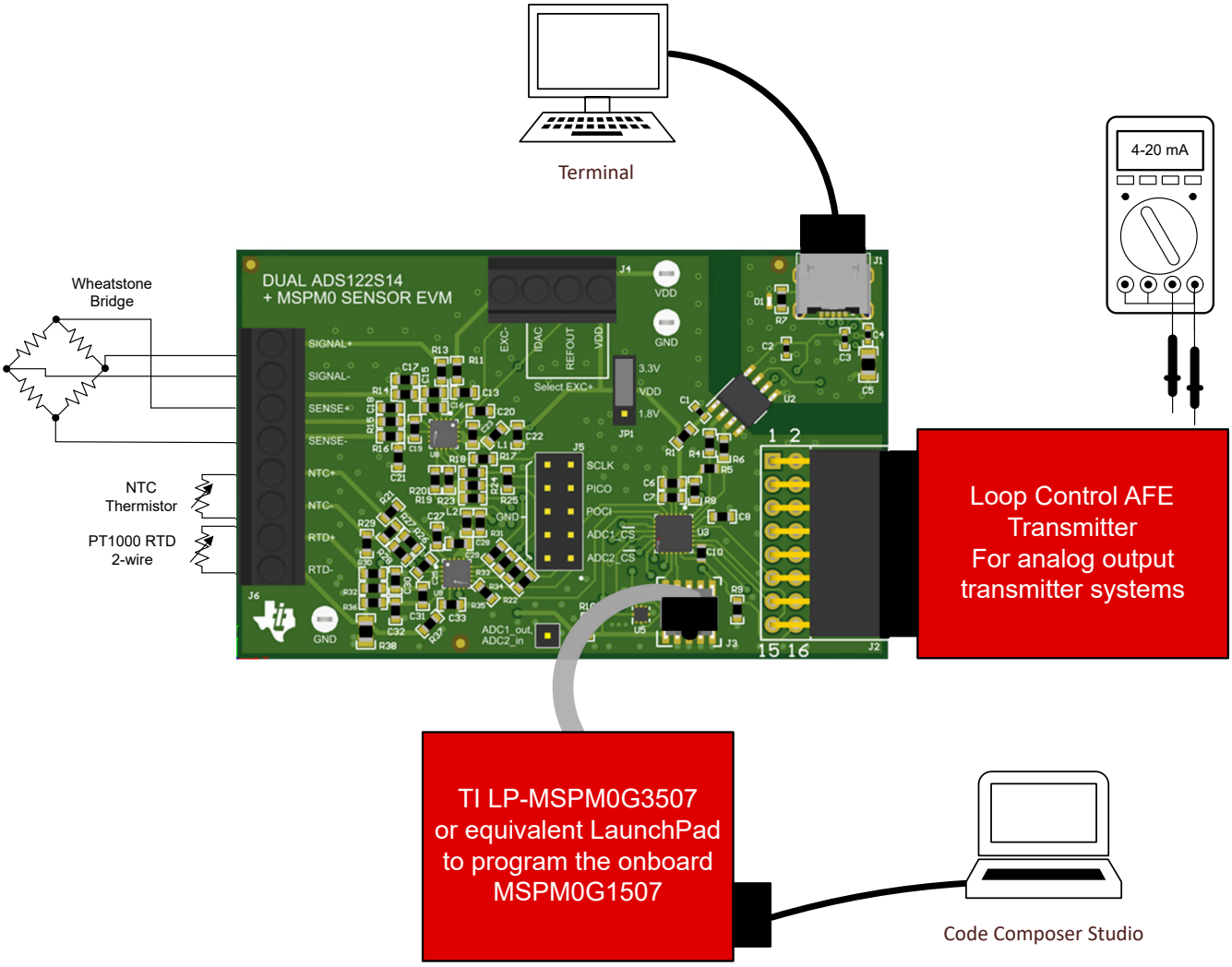

Figure 5-1. SNSR-DUAL-ADC-EVM Interface Options

5.2 Power Requirements

The SNSR-DUAL-ADC-EVM requires external power using one of three source options: external power supply, JTAG connector, or a TI Loop Control AFE transmitter board. Table 5-1 summarizes the SNSR-DUAL-ADC-EVM power connection options.

Table 5-1. Power Connection Options

Power Source	Description
External bench supply	VDD test point, can be used as external power connection VDD: 1.74V -3.6V
	2x GND test points, can be used as external ground connection to the EVM
JTAG	JTAG header to program and power the EVM.
Transmitter header	16-pin header used with Texas Instruments Loop Control AFE Transmitter boards. Jumper 1 (JP1) selects a VDD voltage of either 1.8V or 3.3V from the transmitter board

Measure total system power consumption with an external meter connected to the VDD and GND test points. Figure 5-2 shows the power connection options.

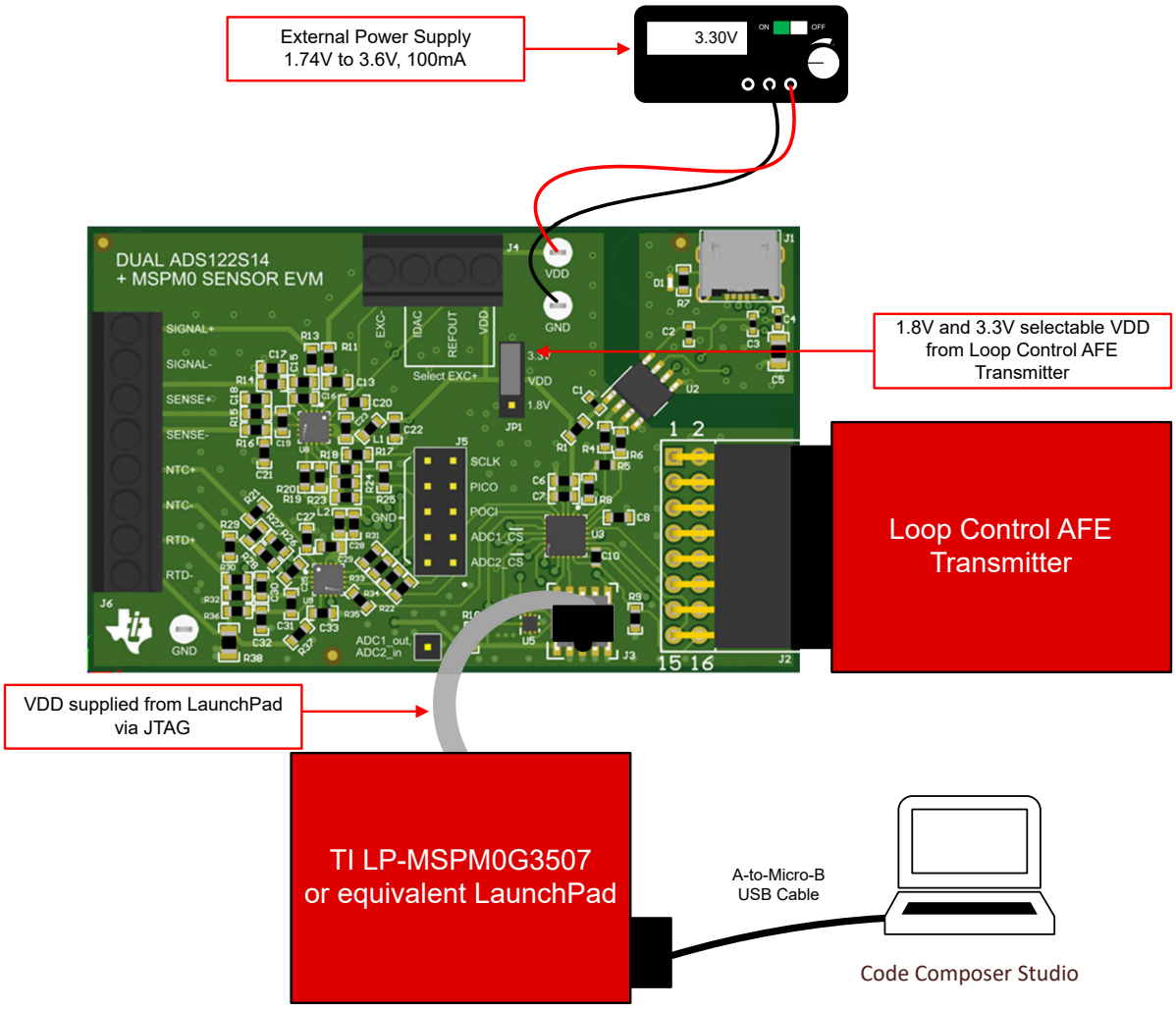

Figure 5-2. Power Connection Options

Note that JP1 functions as a selectable VDD only when the Loop Control AFE Transmitter board powers the EVM; otherwise, JP1 has no effect.

5.3 ADC Connections and Decoupling

Figure 5-3 shows the connections to both ADS122S14 data converters (U8 and U9). Each power supply connection (AVDD and DVDD) includes two 100nF decoupling capacitors and an inductor in a pi-filter configuration. This filter helps remove any high-frequency noise from the power supply. Alternatively, replace the inductor with a 2Ω to 3Ω resistor to avoid the current-choking effects of the inductor. Furthermore, each reference output pin includes a 100nF decoupling capacitor. Place all capacitors close to the device pins and verify a solid connection to the GND plane.

Each digital pin includes a 47Ω series resistor. These resistors smooth digital signal edges to minimize overshoot and ringing

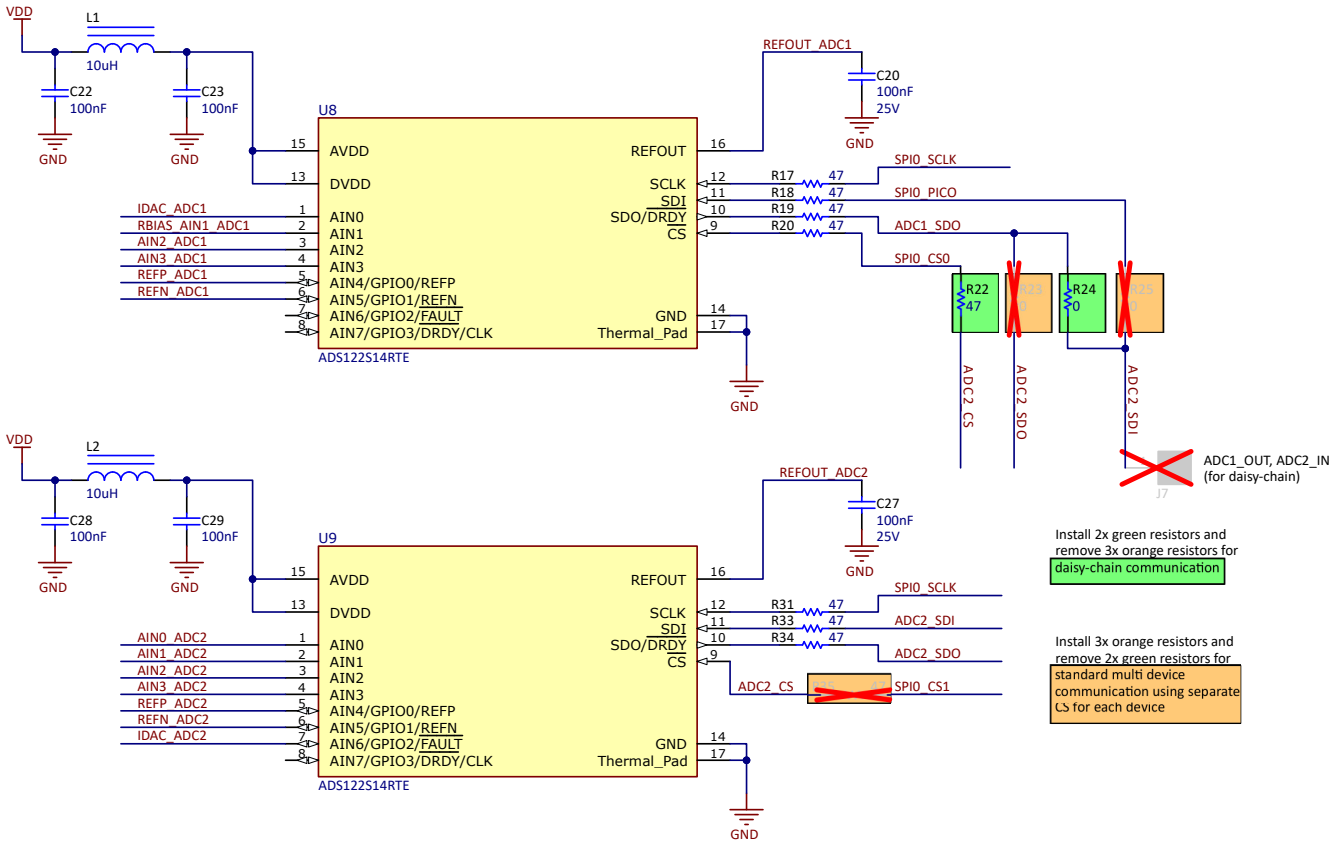

Figure 5-3. ADC Connections and Decoupling

The SNSR-DUAL-ADC-EVM supports both daisy-chain and multi-device (dedicated $\overline{CS}$ pins) communication between the ADCs and MCU. Figure 5-3 shows that the default EVM configuration uses daisy-chain communication through the resistors highlighted in green. Use multi-device communication by removing the resistors highlighted in green and installing the resistors highlighted in orange. Table 5-2 lists the two configurations on the EVM board and the corresponding installed resistors. Figure 5-3 identifies each resistor.

Table 5-2. Digital Communication Configuration Options for Installed Resistors

Resistor Number	Daisy-chain Communication	Multi device Communication
R22	**Installed**	Not Installed
R23	Not Installed	**Installed**
R24	**Installed**	Not Installed
R25	Not Installed	**Installed**
R35	Not Installed	**Installed**

5.4 Analog Inputs

ADC1 Analog Inputs and ADC2 Analog Inputs provide an overview of the analog inputs of the two ADS122S14 ADCs on the SNSR-DUAL-ADC-EVM.

5.4.1 ADC1 Analog Inputs

The SNSR-DUAL-ADC-EVM default settings configure ADC1 to measure the output signals of a resistive bridge. However, the user can configure the channels to measure general purpose sensor signals. Figure 5-4 shows the analog input filtering and additional circuitry connected to ADC1.

AIN2 and AIN3 form a differential pair that measures the input signals between SIGNAL+ and SIGNAL-. The default EVM settings configure AIN4 and AIN5 as the reference between SENSE+ and SENSE-. The user can also configure AIN4 and AIN5 as a differential pair to measure input signals. The default EVM settings configure AIN1 as the excitation source return path from an external bridge circuit. However, AIN1 can also be used as a single-ended measurement input when resistor R12 is removed.

ADC1 supports resistive bridge, thermocouple, 3- and 4-wire resistance temperature detectors (RTDs), and generic voltage and current input measurements. See Analog Sensor Connections for additional details regarding how to connect sensors to the SNSR-DUAL-ADC-EVM board.

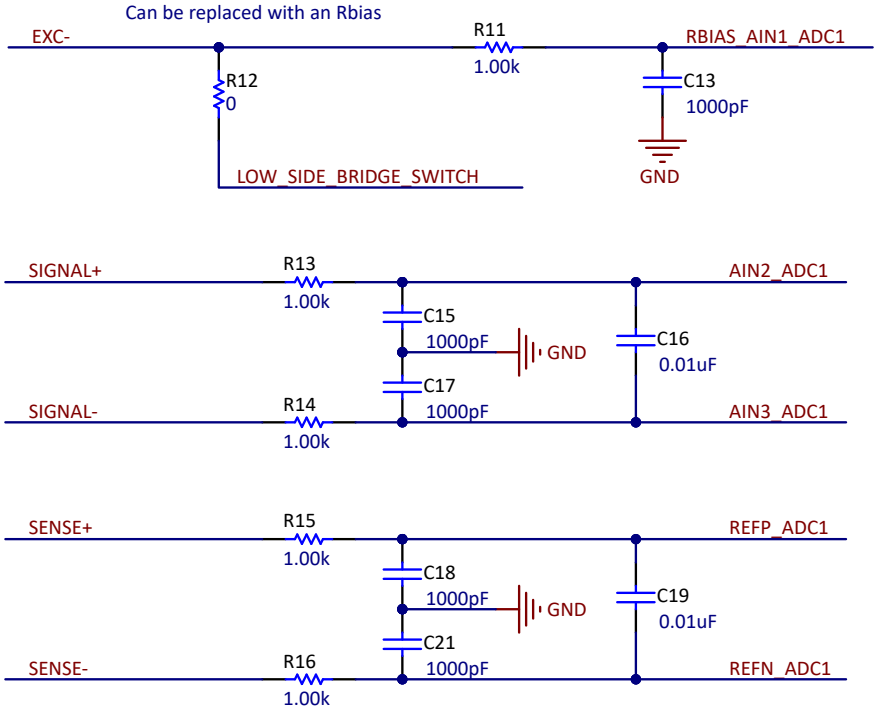

Figure 5-4. ADC1 Analog Front End

The ADC1 analog inputs include first-order resistor-capacitor filters that limit aliasing and noise effects. The differential pairs include an additional common-mode capacitor that filters common-mode noise. Equation 1 shows the calculation for the differential cut-off frequency. Equation 2 shows the calculation for the common-mode cut-off frequency.

$$f_{c_{diff}} = 1/[2\pi \times (R1 + R2) \times C_{diff}] = 1/ [2\pi \times (1000 + 1000) \times 0.01\mu F] \cong 8kHz \quad (1)$$

$$f_{c_{cm}} = 1/[2\pi \times R \times C_{cm}] = 1/ [2\pi \times 1000 \times 1000pF] \cong 160kHz \quad (2)$$

5.4.2 ADC2 Analog Inputs

The SNSR-DUAL-ADC-EVM default settings configure ADC2 to measure the output signals of both an external NTC and an external 2-wire RTD. However, the user can reconfigure the channels to measure general purpose input signals. Figure 5-5 shows the analog input filtering and additional circuitry connected to ADC2.

Inputs NTC+ and NTC- form a differential input pair that is intended to measure an external thermistor (NTC or PTC). The thermistor is part of a resistor divider with a 10kΩ bias resistor (Rbias) that is excited by REFOUT of ADC2. Populate the 10kΩ resistor in parallel with the thermistor to support analog linearization if desired. Inputs RTD+ and RTD- form a differential pair designed to interface directly with different RTD types. A populated 4.02kΩ reference resistor provides the ratiometric reference voltage for the RTD measurement.

Remove R21, R29, R30, R37, and R38 to create two general purpose differential pairs. NTC+ and NTC- form a differential pair between AIN0 and AIN1, while RTD+ and RTD- form a differential pair between AIN2 and AIN3.

ADC2 supports 2-, 3- and 4-wire RTD, external thermistor, and generic voltage and current input measurements. See Analog Sensor Connections for additional details regarding how to connect sensors to the SNSR-DUAL-ADC-EVM board.

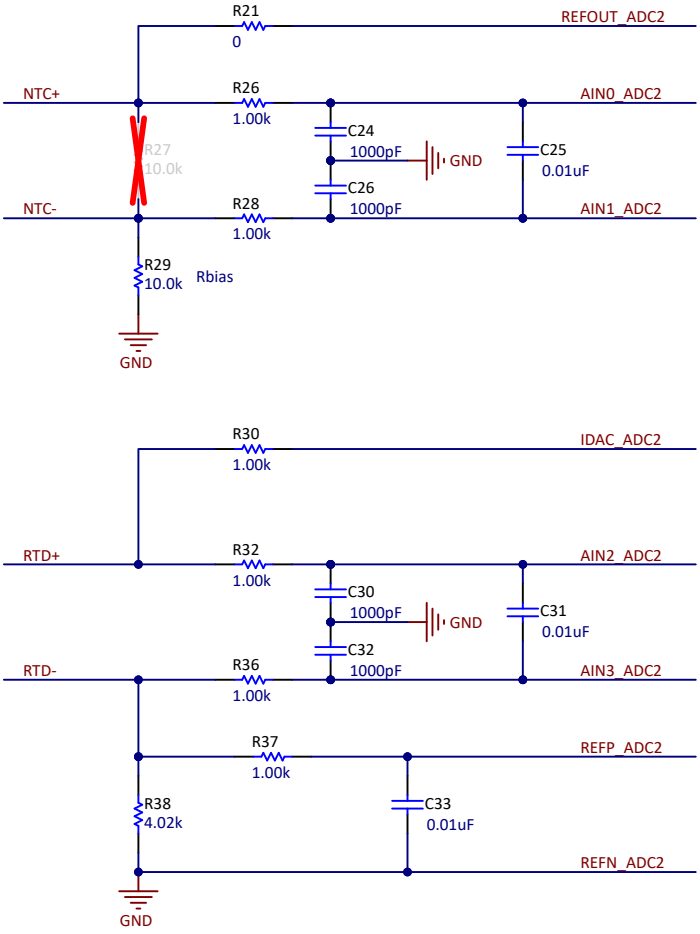

Figure 5-5. ADC2 Analog Front End

The ADC2 analog inputs include first-order resistor-capacitor filters that limit aliasing and noise effects. The differential pairs include an additional common-mode capacitor that filters common-mode noise. Equation 1 shows the calculation for the differential cut-off frequency. Equation 2 shows the calculation for the common-mode cut-off frequency.

$$f_{c_{diff}} = 1/[2\pi \times (R1 + R2) \times C_{diff}] = 1/ [2\pi \times (1000 + 1000) \times 0.01\mu F] \cong 8kHz \quad (3)$$

$$f_{c_{cm}} = 1/[2\pi \times R \times C_{cm}] = 1/ [2\pi \times 1000 \times 1000pF] \cong 160kHz \quad (4)$$

5.5 Excitation Connections and Low Side Bridge Switch

Figure 5-6 shows the sensor excitation circuitry. Header J4 functions as both an output and an input to the EVM. This header supports multiple sensor excitation sources, including VDD, REFOUT_ADC1, and IDAC_ADC1. EXC- completes the bridge connection to ground through the TMUX1219, which acts as a low-side bridge switch. The MSPM0G1507 controls the low-side bridge switch to either provide the bridge excitation with a path to ground or disconnect the bridge for power savings. Refer to Section 6.3.2.6 for additional information regarding how to operate the low side bridge switch.

In a current excitation bridge circuit, replace the 0Ω resistor R12 with a bias resistor to establish a valid common mode voltage for the bridge output. Additionally, this bias resistor provides a return path for the excitation current source.

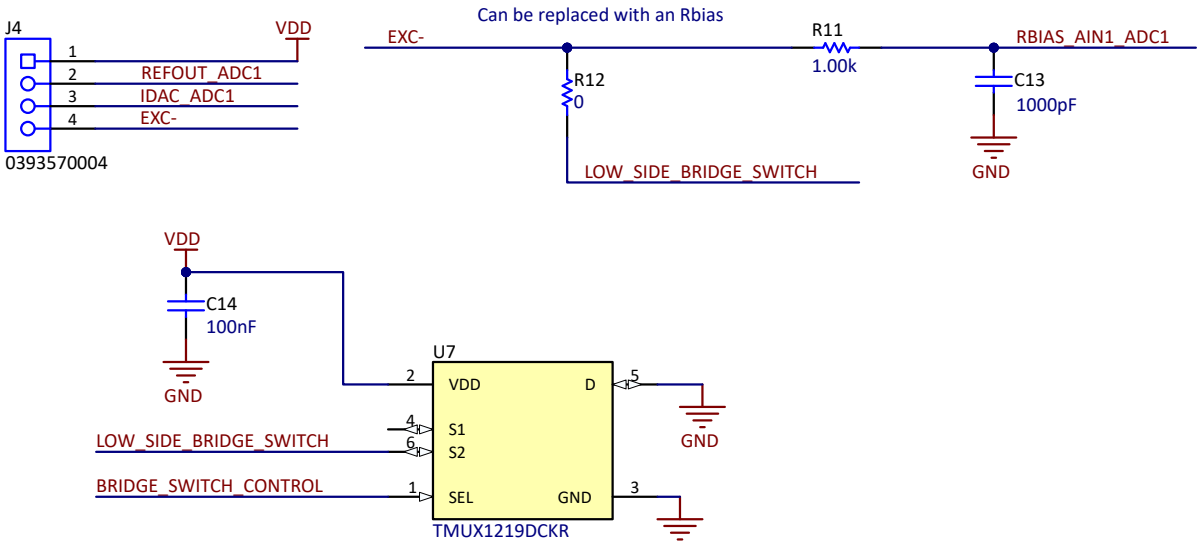

Figure 5-6. Excitation Header and Low Side Bridge Switch

5.6 Analog Sensor Connections

The SNSR-DUAL-ADC-EVM can be configured to use many different analog sensors. The following subsections show how to connect different combinations of sensors to the EVM. Additionally, each subsection includes a table of important ADC register settings for that configuration as well as each register's preloaded value. These tables use PURPLE cells to indicate ADC settings that are fixed by the hardware, and YELLOW cells to indicate ADC settings that the user must select based on the system requirements.

- Pressure Sensor (Resistive Bridge) Application Examples
  - Measuring a Voltage-Excited 6-wire Bridge Using ADC1 and a Low-side Bias Resistor Using ADC2
  - Measuring a Voltage-Excited 6-wire Bridge Using ADC1 and a Current-Excited 2-wire RTD Using ADC2
  - Measuring a Current-Excited 4-wire Bridge Using ADC1 and a Voltage-Excited Thermistor Using ADC2
- Temperature Sensor Application Examples
  - Measuring a Thermocouple Using ADC1 and an NTC for Cold-Junction-Compensation Using ADC2
  - Measuring One 3-wire RTD Using ADC1 and One 3-wire RTD Using ADC2
  - Measuring One 4-wire RTD Using ADC1 and One 4-wire RTD Using ADC2
- General Purpose Application Examples
  - Measuring Generic Voltage or Current Inputs

Table 5-3 shows the SNSR-DUAL-ADC-EVM header pin connection to the respective ADC pin.

Table 5-3. SNSR-DUAL-ADC-EVM Header to ADC Pin

ADC	SNSR-DUAL-ADC-EVM Header Pin	ADC Pin
ADC1	VDD	AVDD / DVDD
	REFOUT	REFOUT
	IDAC	AIN0
	EXC-	AIN1
	SIGNAL+	AIN2
	SIGNAL-	AIN3
	SENSE+	AIN4 / REFP
	SENSE-	AIN5 / REFN
ADC2	NTC+	AIN0
	NTC-	AIN1
	RTD+	AIN2
	RTD-	AIN3

5.6.1 Pressure Sensor (Resistive Bridge) Application Examples

Common pressure sensor applications use a low-noise ADC with an integrated PGA to measure the low-level signals from a pressure-sensitive resistive bridge. Additionally, many systems also measure the pressure sensor temperature to correct for temperature drift errors. The EVM allows for both the measurement of a resistive bridge and bridge temperature using an external temperature sensor. Refer to A Basic Guide to Bridge Measurements application note for additional information about measuring resistive bridges with precision ADCs.

Figure 5-7 shows a block diagram of the SNSR-DUAL-ADC-EVM analog front end with example sensors connected to the input and excitation terminal blocks. Note that one analog input header is used for both the ADC1 and ADC2 analog inputs and that ADC1 generates the REFOUT and IDAC excitation sources.

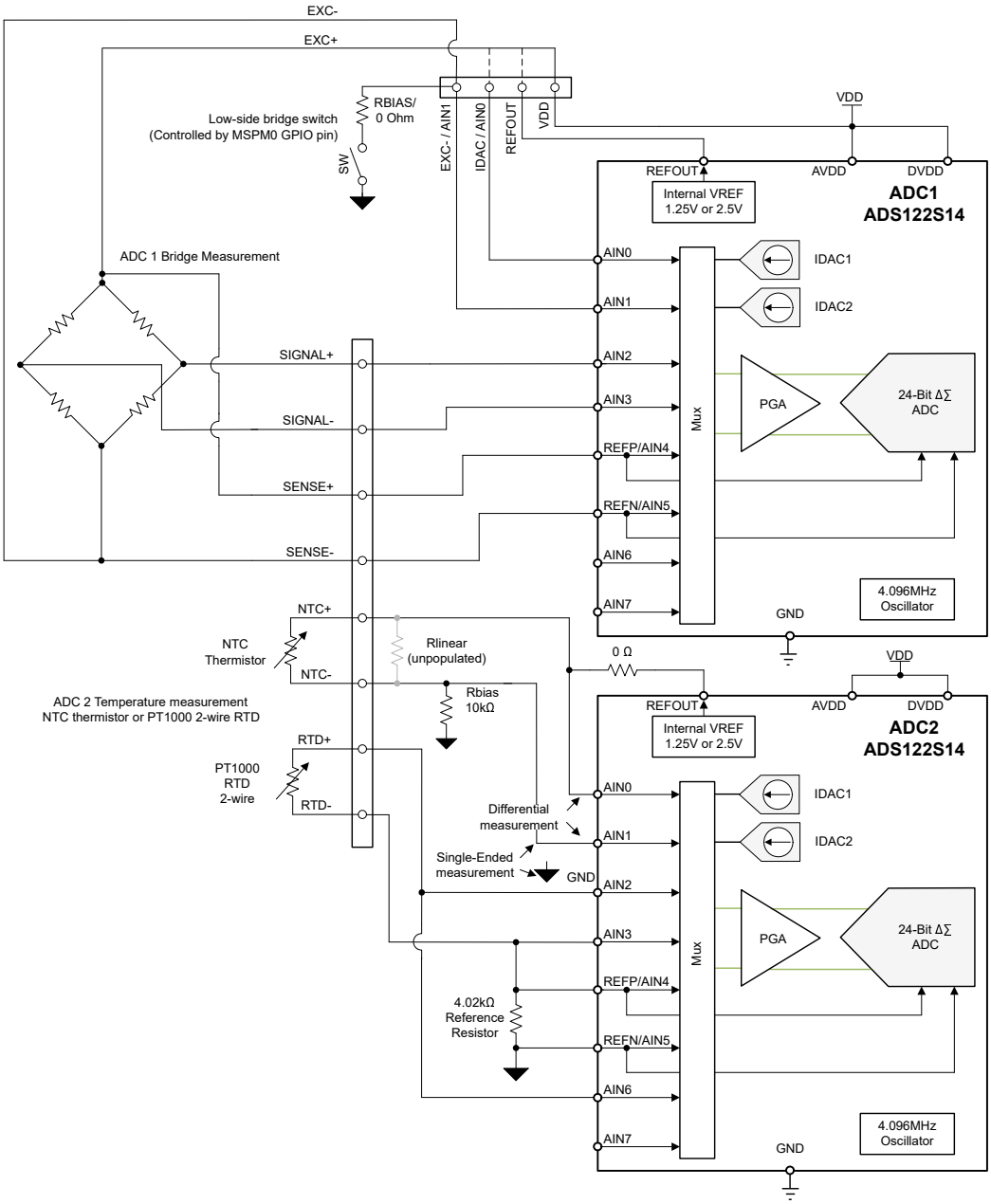

Figure 5-7. SNSR-DUAL-ADC-EVM Block Diagram with Pressure Sensor, Thermistor, and RTD Connected

5.6.1.1 Measuring a Voltage-Excited 6-wire Bridge Using ADC1 and a Low-side Bias Resistor Using ADC2

Figure 5-8 shows the EVM connection diagram to measure a voltage-excited 6-wire resistive bridge using ADC1 and a low-side bias resistor using ADC2.

1. Connect the positive and negative bridge leads to SIGNAL+ and SIGNAL- on the input header, respectively.
2. Connect the positive and negative bridge reference or sense leads to SENSE+ and SENSE- on the input header, respectively.
3. Connect the positive bridge excitation lead to VDD on the excitation header.
4. Connect a series R_{Bias} resistor across RTD+ and RTD- on the input header to determine bridge resistance.
5. Connect an external wire from RTD- to EXC- on the excitation header to connect to the low-side bridge switch.

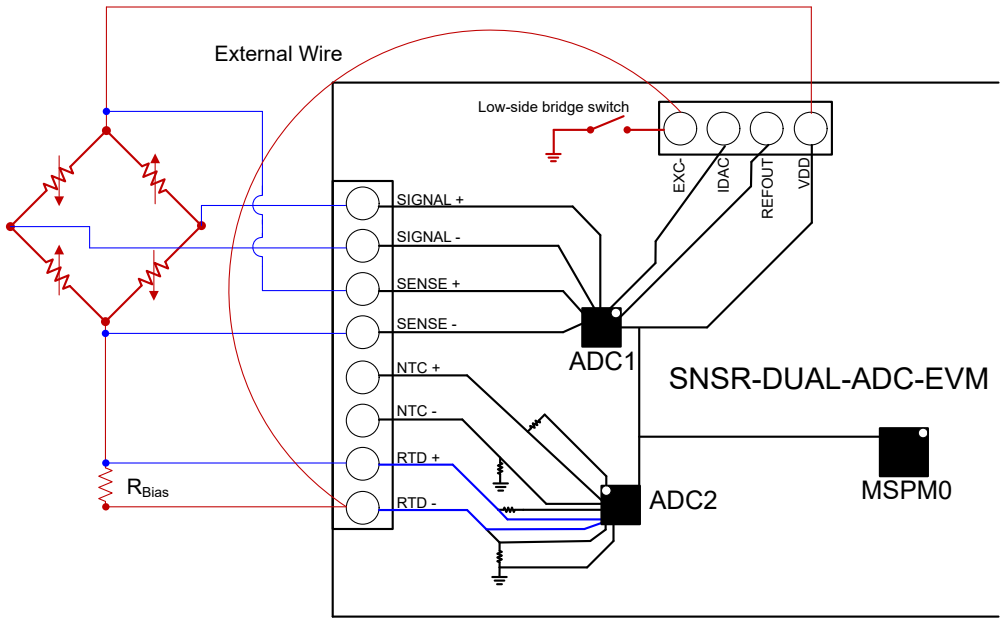

Figure 5-8. Measuring a Voltage-Excited 6-wire Bridge Using ADC1 and a Low-side Bias Resistor Using ADC2

The red lines indicate the sensor bias path and the blue lines indicate the sensor measurement path in Figure 5-8. Table 5-4 describes the applicable register settings to measure a voltage-excited 6-wire resistive bridge using ADC1 and a low-side bias resistor using ADC2. Recall that purple cells indicate ADC settings that are fixed by the hardware and yellow cells indicate ADC settings that the user must select.

Table 5-4. Suggested Register Settings for Application

ADC	REGISTER (1)	Value	Description
ADC1	MUX_CFG (07h)	0x23h	AINP = AIN2, AINN = AIN3
	GAIN_CFG (08h)	0x0Dh	Gain = 128
	REFERENCE_CFG (09h)	0x21h	REFP_BUF_EN, REF_SEL = External Reference
ADC2	MUX_CFG (07h)	0x01h	AINP = AIN0, AINN = AIN1
	GAIN_CFG (08h)	0x01h	Gain = 1
	REFERENCE_CFG (09h)	0x00h	REFOUT = 1.25V, Internal Reference

(1) See ADC1 and ADC2 Power-on and *adc reset* Register Settings for default EVM firmware settings.

5.6.1.2 Measuring a Voltage-Excited 6-wire Bridge Using ADC1 and a Current-Excited 2-wire RTD Using ADC2

Figure 5-9 shows the EVM connection diagram to measure a voltage-excited 6-wire resistive bridge using ADC1 and a current-excited 2-wire RTD using ADC2.

1. Connect the positive and negative bridge leads to SIGNAL+ and SIGNAL- on the input header, respectively.
2. Connect the positive and negative bridge reference or sense leads to SENSE+ and SENSE- on the input header, respectively.
3. Connect the positive and negative bridge excitation leads to REFOUT and EXC- on the excitation header, respectively.
4. Connect a 2-wire PT1000 RTD directly to the RTD+ and RTD- on the input header. The onboard 4.02kΩ reference resistor (R38) enables a ratiometric reference voltage configuration for ADC2.

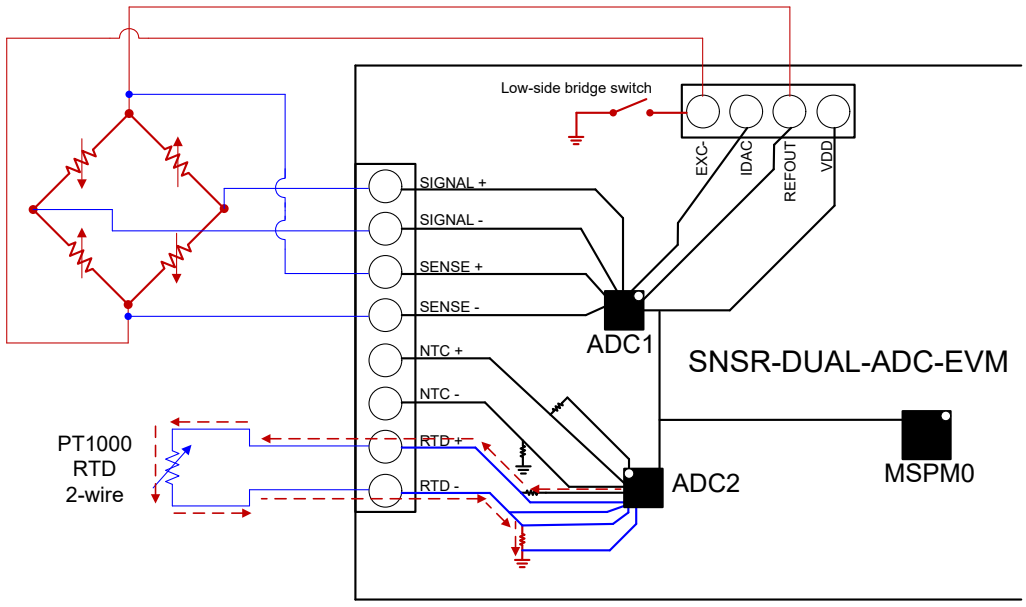

Figure 5-9. Measuring a Voltage-Excited 6-wire Bridge Using ADC1 and a Current-Excited 2-wire RTD Using ADC2

The red lines indicate the sensor bias path and the blue lines indicate the sensor measurement path in Figure 5-9. Table 5-5 describes the applicable register settings to measure a voltage-excited 6-wire resistive bridge using ADC1 and a current-excited 2-wire RTD using ADC2. Recall that purple cells indicate ADC settings that are fixed by the hardware and yellow cells indicate ADC settings that the user must select.

Table 5-5. Suggested Register Settings for Application

ADC	REGISTER (1)	Value	Description
ADC1	MUX_CFG (07h)	0x23h	AINP = AIN2, AINN = AIN3
	GAIN_CFG (08h)	0x0Dh	Gain = 128
	REFERENCE_CFG (09h)	0x23h	REFP_BUF_EN, REF_VAL=2.5V, REF_SEL = External Reference
	IDAC_MUX_CFG (0Eh)	0x80h	IDAC Unit = 10µA
			I1MUX = AIN0
ADC2	MUX_CFG (07h)	0x23h	AINP = AIN2, AINN = AIN3
	GAIN_CFG (08h)	0x01h	Gain = 1
	REFERENCE_CFG (09h)	0x21h	REFP_BUF_EN = 1b, REF_SEL = External Reference
	IDAC_MAG_CFG (0Dh)	0x0Ah	IDAC1 Magnitude 90x IUNIT
	IDAC_MUX_CFG (0Eh)	0x86h	IDAC Unit = 10µA
			I1MUX = AIN6

(1) See ADC1 and ADC2 Power-on and *adc reset* Register Settings for default EVM firmware settings.

5.6.1.3 Measuring a Current-Excited 4-wire Bridge Using ADC1 and a Voltage-Excited Thermistor Using ADC2

Figure 5-10 shows the EVM connection diagram to measure a current-excited 4-wire resistive bridge using ADC1 and a voltage-excited NTC using ADC2.

1. Connect the positive and negative bridge leads to SIGNAL+ and SIGNAL- on the input header, respectively.
2. Connect external jumper wires to SENSE+ and SENSE- from the input signal header to the IDAC and EXC- on the excitation header, respectively.
3. Connect the positive and negative bridge excitation leads to IDAC and EXC- on the excitation header.
4. Install an appropriately-sized bias resistor at R12 to establish the correct common-mode output voltage from the current-excited bridge
5. Connect thermistor across NTC+ and NTC- for a differential measurement or NTC+ and GND for a single-ended measurement. The onboard 10kΩ (R29) bias resistor creates a voltage divider with the external thermistor.

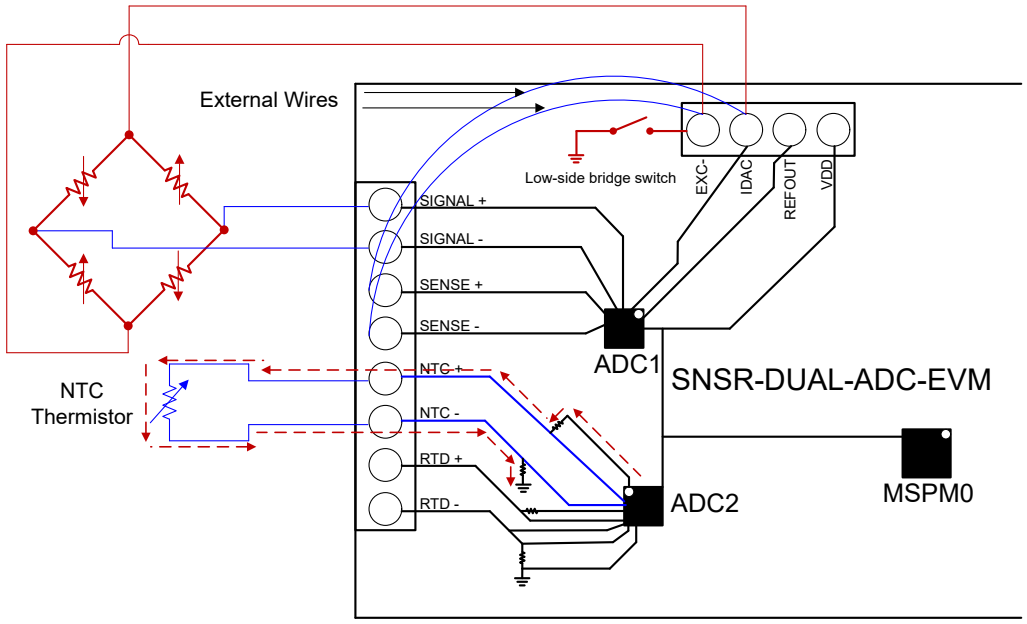

Figure 5-10. Measuring a Current-Excited 4-wire Bridge Using ADC1 and a Voltage-Excited Thermistor Using ADC2

The red lines indicate the sensor bias path and the blue lines indicate the sensor measurement path in Figure 5-10. Table 5-6 describes the applicable register settings to measure a current-excited 4-wire resistive bridge using ADC1 and a voltage-excited NTC using ADC2. Recall that purple cells indicate ADC settings that are fixed by the hardware and yellow cells indicate ADC settings that the user must select.

Table 5-6. Suggested Register Settings for Application

ADC	REGISTER (1)	Value	Description
ADC1	MUX_CFG (07h)	0x23h	AINP = AIN2, AINN = AIN3
	GAIN_CFG (08h)	0x0Dh	Gain = 128
	REFERENCE_CFG (09h)	0x21h	REFP_BUF_EN, REF_SEL = External Reference
	IDAC_MAG_CFG (0Dh)	0x0Bh	IDAC1 Magnitude 100x IUNIT
	IDAC_MUX_CFG (0Eh)	0x80h	IDAC Unit = 10µA,
			I1MUX = AIN0
ADC2	MUX_CFG (07h)	0x01h	AINP = AIN0, AINN = AIN1
	GAIN_CFG (08h)	0x01h	Gain = 1
	REFERENCE_CFG (09h)	0x00h	REFOUT = 2.5V, Internal Reference

(1) See ADC1 and ADC2 Power-on and *adc reset* Register Settings for default EVM firmware settings.

5.6.2 Temperature Sensor Application Examples

Thermocouple measurements rely on a voltage difference created between two dissimilar metals exposed to different temperatures. The cold-junction compensation corrects for the reference junction temperature to accurately represent the true temperature at the sensing junction. Refer to A Basic Guide to Thermocouple Measurements application note for additional information about measuring thermocouples with precision ADCs.

RTDs are among the most accurate temperature sensors available, covering wide temperature ranges. RTDs operate on the principle that the resistance of certain metals increases predictably with temperature. Refer to A Basic Guide to RTD Measurements application note for additional information about measuring RTDs with precision ADCs.

Figure 5-11 shows a block diagram of the SNSR-DUAL-ADC-EVM analog front end with example sensors connected to the input and excitation terminal blocks. Note that one analog input header is used for the analog inputs for both ADC1 and ADC2 and that ADC1 generates the REFOUT and IDAC excitation sources.

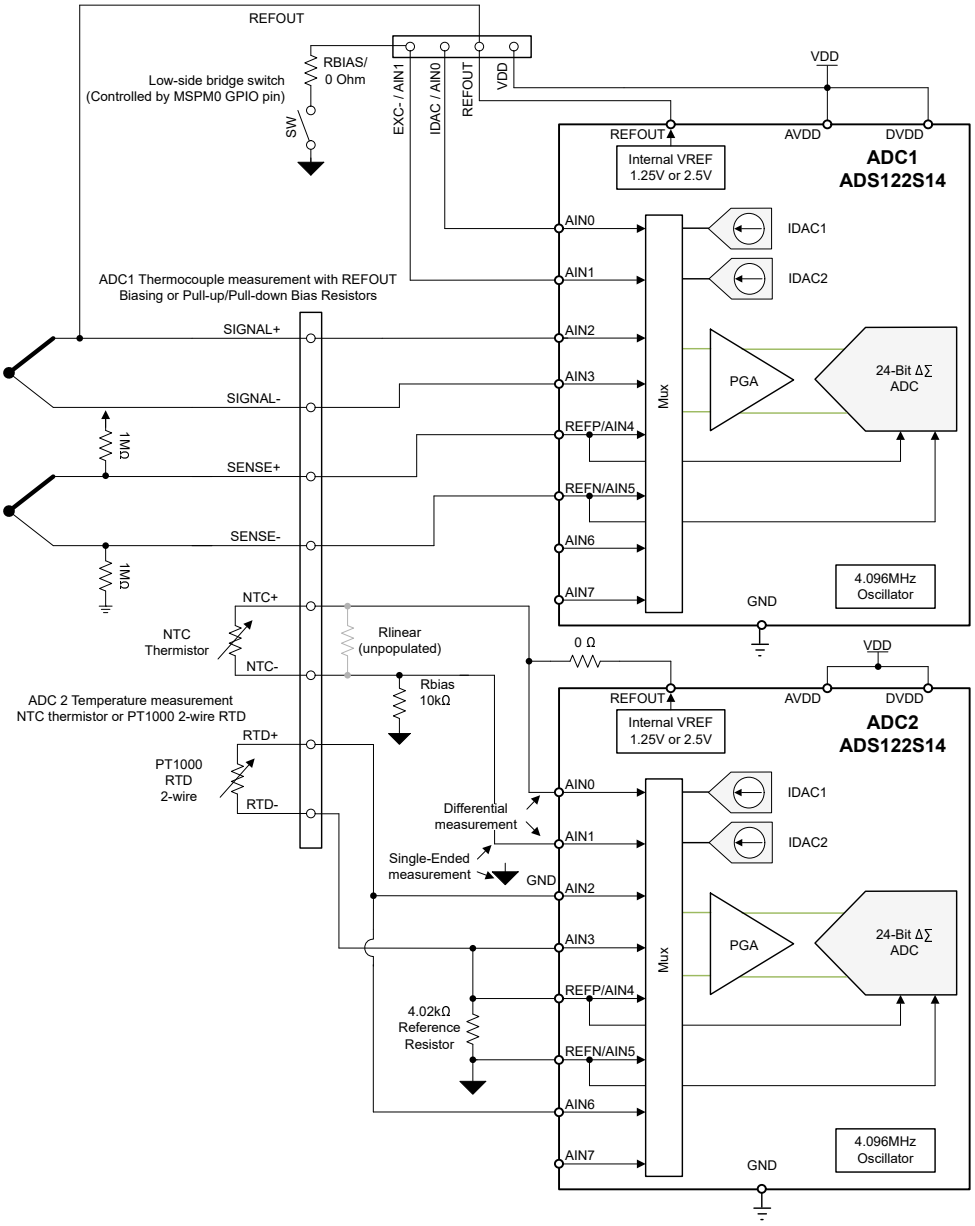

Figure 5-11. SNSR-DUAL-ADC-EVM Block Diagram With Thermocouples, Thermistor, and RTD Connected

5.6.2.1 Measuring a Thermocouple Using ADC1 and an NTC for Cold-Junction-Compensation Using ADC2

Figure 5-12 shows the EVM connection diagram to measure a thermocouple using ADC1 and an NTC for cold junction compensation using ADC2.

1. Bias the thermocouple with external pullup and pulldown resistors to set a common mode voltage at mid supply. Alternatively, bias the thermocouple through an external wire from the REFOUT pin to SIGNAL+.
2. Connect an external thermistor to the NTC+ and NTC- pins on the input header for cold-junction compensation of the thermocouple.
3. Connect an external thermistor across NTC+ and NTC- for a differential measurement or NTC+ and GND for a single-ended measurement. The onboard 10kΩ (R29) bias resistor creates a voltage divider with the external thermistor.

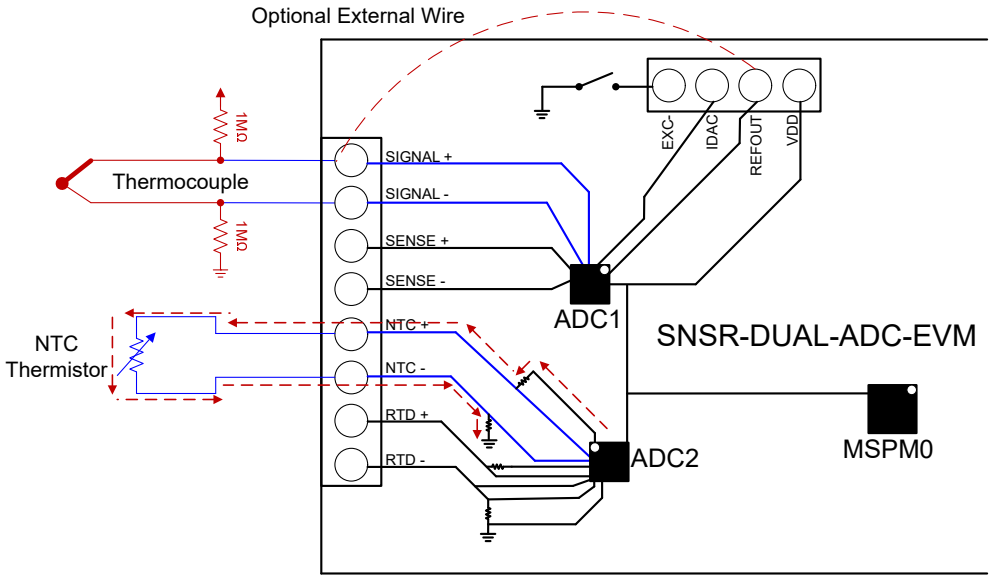

Figure 5-12. Measuring a Thermocouple Using ADC1 and an NTC for Cold-Junction-Compensation Using ADC2

The red lines indicate the sensor bias path and the blue lines indicate the sensor measurement path in Figure 5-12. Table 5-7 describes the applicable register settings to measure a thermocouple and an NTC for cold junction compensation. Recall that purple cells indicate ADC settings that are fixed by the hardware and yellow cells indicate ADC settings that the user must select.

Table 5-7. Suggested Register Settings for Application

ADC	REGISTER (1)	Value	Description
ADC1	MUX_CFG Register (07h)	0x23h	AINP = AIN2, AINN = AIN3
	GAIN_CFG (08h)	0x0Dh	Gain = 128
	REFERENCE_CFG (09h)	0x00h	REFOUT = 1.25V, Internal Reference
ADC2	MUX_CFG Register (07h)	0x01h	AINP = AIN0, AINN = AIN1
	GAIN_CFG (08h)	0x01h	Gain = 1
	REFERENCE_CFG (09h)	0x03h	REFOUT = 2.5V, Internal Reference

(1) See ADC1 and ADC2 Power-on and *adc reset* Register Settings for default EVM firmware settings.

5.6.2.2 Measuring One 3-wire RTD Using ADC1 and One 3-wire RTD Using ADC2

Figure 5-13 shows the EVM connection diagram to measure one 3-wire RTD using ADC1 and one 3-wire RTD using ADC2.

1. Connect RTD1 leads 1, 2, and 3 as shown such that ADC1 measures the RTD output across SIGNAL+ and SIGNAL- on the input header.
2. Connect an external RTD reference resistor (R_{REF}) across SENSE+ and SENSE- to enable a ratiometric reference voltage configuration for ADC1.
3. Connect additional jumper wires from IDAC to SIGNAL+ and from SENSE- to EXC-.
4. Connect RTD2 leads 1, 2, and 3 as shown such that ADC2 measures the RTD output across NTC+ and NTC- on the input header. The onboard 4.02kΩ reference resistor (R38) enables a ratiometric reference voltage configuration for ADC2.
5. Connect an additional external wire between RTD+ and NTC+ pins.

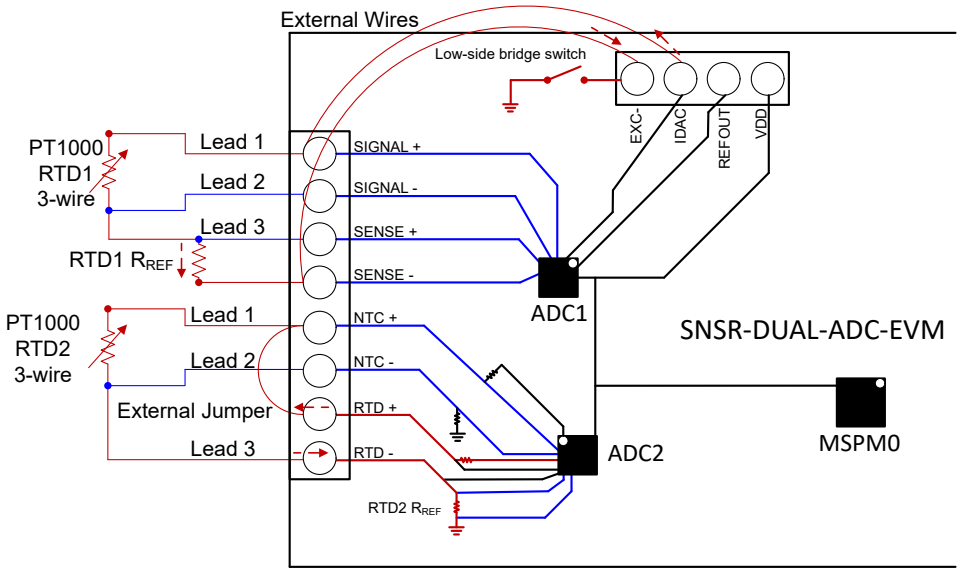

Figure 5-13. Measuring One 3-wire RTD Using ADC1 and One 3-wire RTD Using ADC2

The red lines indicate the sensor bias path and the blue lines indicate the sensor measurement path in Figure 5-13. Table 5-8 describes the applicable register settings for measuring two 3-wire RTDs. Recall that purple cells indicate ADC settings that are fixed by the hardware and yellow cells indicate ADC settings that the user must select.

Table 5-8. Suggested Register Settings for Application

ADC	REGISTER (1)	Value	Description
ADC1	MUX_CFG Register (07h)	0x23h	AINP = AIN2, AINN = AIN3
	GAIN_CFG (08h)	0x01h	Gain = 1
	REFERENCE_CFG (09h)	0x21h	REFP_BUF_EN, REF_SEL = External Reference
	IDAC_MAG_CFG (0Dh)	0x0Ah	IDAC1 Magnitude 90x IUNIT
	IDAC_MUX_CFG (0Eh)	0x80h	IDAC Unit = 10µA
			I1MUX = AIN0
ADC2	MUX_CFG Register (07h)	0x01h	AINP = AIN0, AINN = AIN1
	GAIN_CFG (08h)	0x01h	Gain = 1
	REFERENCE_CFG (09h)	0x21h	REFP_BUF_EN, REF_SEL = External Reference
	IDAC_MAG_CFG (0Dh)	0x0Ah	IDAC1 Magnitude 90x IUNIT
	IDAC_MUX_CFG (0Eh)	0x86h	IDAC Unit = 10µA
			I1MUX = AIN6

(1) See ADC1 and ADC2 Power-on and *adc reset* Register Settings for default EVM firmware settings.

5.6.2.3 Measuring One 4-wire RTD Using ADC1 and One 4-wire RTD Using ADC2

Figure 5-14 shows the EVM connection diagram to measure one 4-wire RTD using ADC1 and one 4-wire RTD using ADC2.

1. Connect RTD1 leads 1, 2, 3, and 4 as shown such that ADC1 measures the RTD output across SIGNAL+ and SIGNAL- on the input header.
2. Connect an external RTD reference resistor (R_{REF}) across SENSE+ and SENSE- to enable a ratiometric reference voltage configuration for ADC1.
3. Connect an additional external wire from SENSE- on the input header to EXC- on the excitation header.
4. Connect RTD2 leads 1, 2, 3, and 4 as shown such that ADC2 measures the RTD output across NTC+ and NTC- on the input header. The onboard 4.02kΩ reference resistor (R38) enables a ratiometric reference voltage configuration for ADC2.

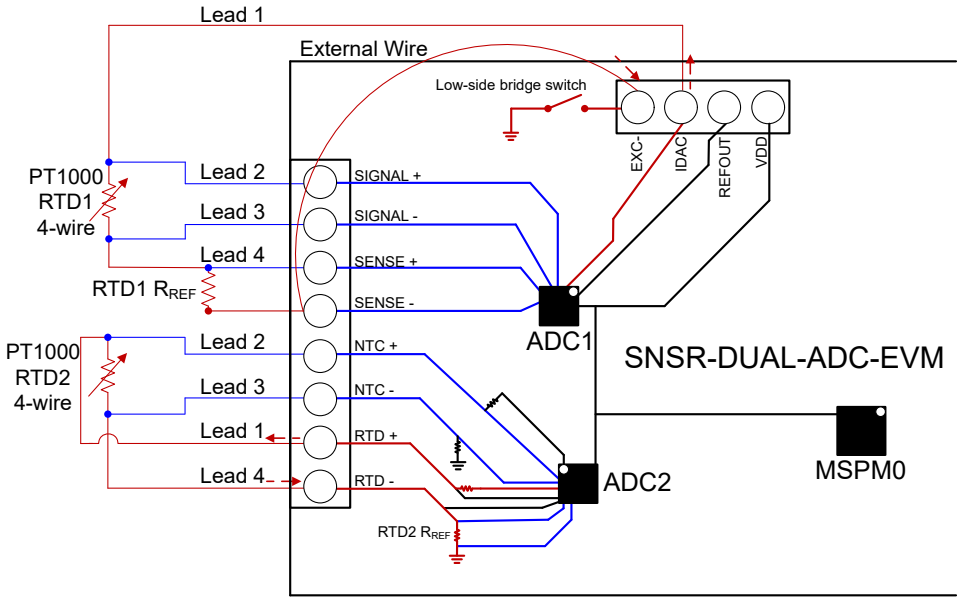

Figure 5-14. Measuring One 4-wire RTD Using ADC1 and One 4-wire RTD Using ADC2

The red lines indicate the sensor bias path and the blue lines indicate the sensor measurement path in Figure 5-14. Table 5-9 describes the applicable register settings for measuring two 4-wire RTDs. Recall that purple cells indicate ADC settings that are fixed by the hardware and yellow cells indicate ADC settings that the user must select.

Table 5-9. Suggested Register Settings for Application

ADC	REGISTER (1)	Value	Description
ADC1	MUX_CFG (07h)	0x23h	AINP = AIN2, AINN = AIN3
	GAIN_CFG (08h)	0x01h	Gain = 1
	REFERENCE_CFG (09h)	0x21h	REFP_BUF_EN, REF_SEL = External Reference
	IDAC_MAG_CFG (0Dh)	0x0Ah	IDAC1 Magnitude 90x IUNIT
	IDAC_MUX_CFG (0Eh)	0x80h	IDAC Unit = 10µA
			I1MUX = AIN0
ADC2	MUX_CFG Register (07h)	0x01h	AINP = AIN0, AINN = AIN1
	GAIN_CFG (08h)	0x01h	Gain = 1
	REFERENCE_CFG (09h)	0x21h	REFP_BUF_EN, REF_SEL = External Reference
	IDAC_MAG_CFG (0Dh)	0x0Ah	IDAC1 Magnitude 90x IUNIT
	IDAC_MUX_CFG (0Eh)	0x86h	IDAC Unit = 10µA
			I1MUX = AIN6

(1) See ADC1 and ADC2 Power-on and *adc reset* Register Settings for default EVM firmware settings.

5.6.3 General Purpose Application Examples

The SNSR-DUAL-ADC-EVM can be used for general evaluation of both ADS122S14 precision ADCs and is not restricted for sensor measurement applications. Each ADC can measure two differential inputs, four single-ended inputs, or a combination of both input types. Verify all input signals meet the requirements in Table 4-1.

5.6.3.1 Measuring Generic Voltage or Current Inputs

Figure 5-15 shows the EVM connection diagram to measure generic voltage or current inputs using ADC1 and ADC2. As shown, ADC1 measures a differential voltage source and a single ended current source. ADC2 measures a differential current source and a single ended voltage source. However, any combination of source types is possible. Enabling certain channels for generic input measurement can require removing passive components. Refer to the Schematics to identify any such components.

The red lines indicate the sensor bias path and the blue lines indicate the sensor measurement path in Figure 5-15. Table 5-10 describes the applicable register settings for generic voltage and current measurements. Recall that purple cells indicate ADC settings that are fixed by the hardware and yellow cells indicate ADC settings that the user must select.

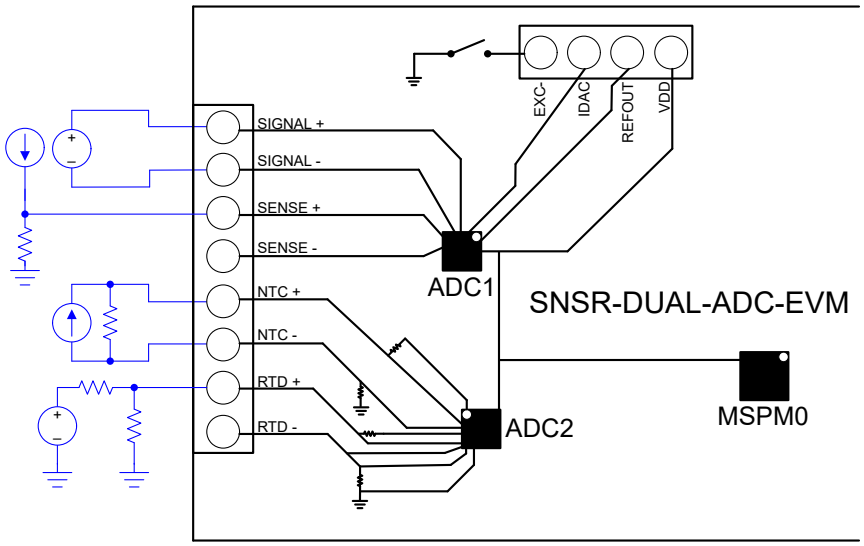

Figure 5-15. Measuring Generic Voltage or Current Inputs

Table 5-10. Suggested Register Settings for Application

ADC	REGISTER (1)	Value	Description
ADC1	MUX_CFG Register (07h)	0x23h	AINP = AIN2, AINN = AIN3
	GAIN_CFG (08h)	0x01h	Gain = 1
ADC2	MUX_CFG Register (07h)	0x01h	AINP = AIN0, AINN = AIN1
	GAIN_CFG (08h)	0x01h	Gain = 1

(1) See ADC1 and ADC2 Power-on and *adc reset* Register Settings for default EVM firmware settings.

5.7 MSPM0G1507

The SNSR-DUAL-ADC-EVM uses the MSPM0G1507 to communicate with and receive data from both ADS122S14 ADCs. The MCU is programmable through JTAG and can be controlled through the isolated USB. The MCU comes preloaded with firmware to use the EVM in a pressure sensor application using an external resistive bridge connected to ADC1 and a two-wire RTD for temperature compensation connected to ADC2. The Software section gives a high level overview of the functions available on the program. Refer to the PADC GitHub website for the most up-to-date firmware.

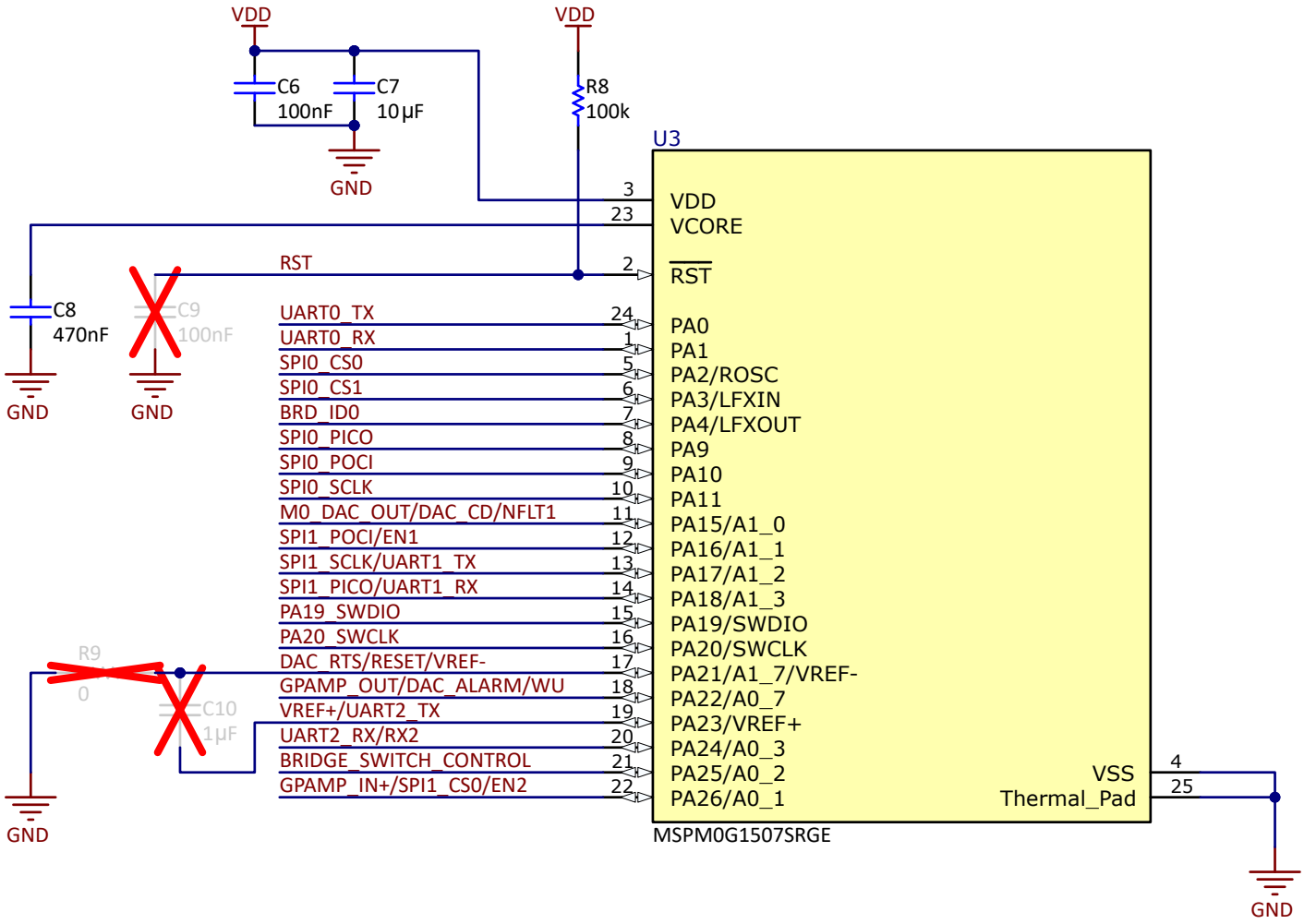

Figure 5-16. SNSR-DUAL-ADC-EVM MSPM0G1507 Circuitry

5.8 Digital Interfaces

Figure 5-17 shows the three digital interfaces used by the SNSR-DUAL-ADC-EVM. Connect the provided USB cable to header J1 to communicate with the preloaded EVM firmware using a PC terminal program. The EVM specifically supports isolated USB to enable configuration of the ADC registers while the board is operating in a 4-20mA loop. Refer to the Software section for more information on controlling the EVM through a terminal program. Header J3 is a JTAG connector for programming the MSPM0G1507 with any Texas Instruments LaunchPad or other debugging platform. Header J2 is used for the serial communication between two boards when the SNSR-DUAL-ADC-EVM connects to the Loop Control AFE Transmitter or other compatible output boards.

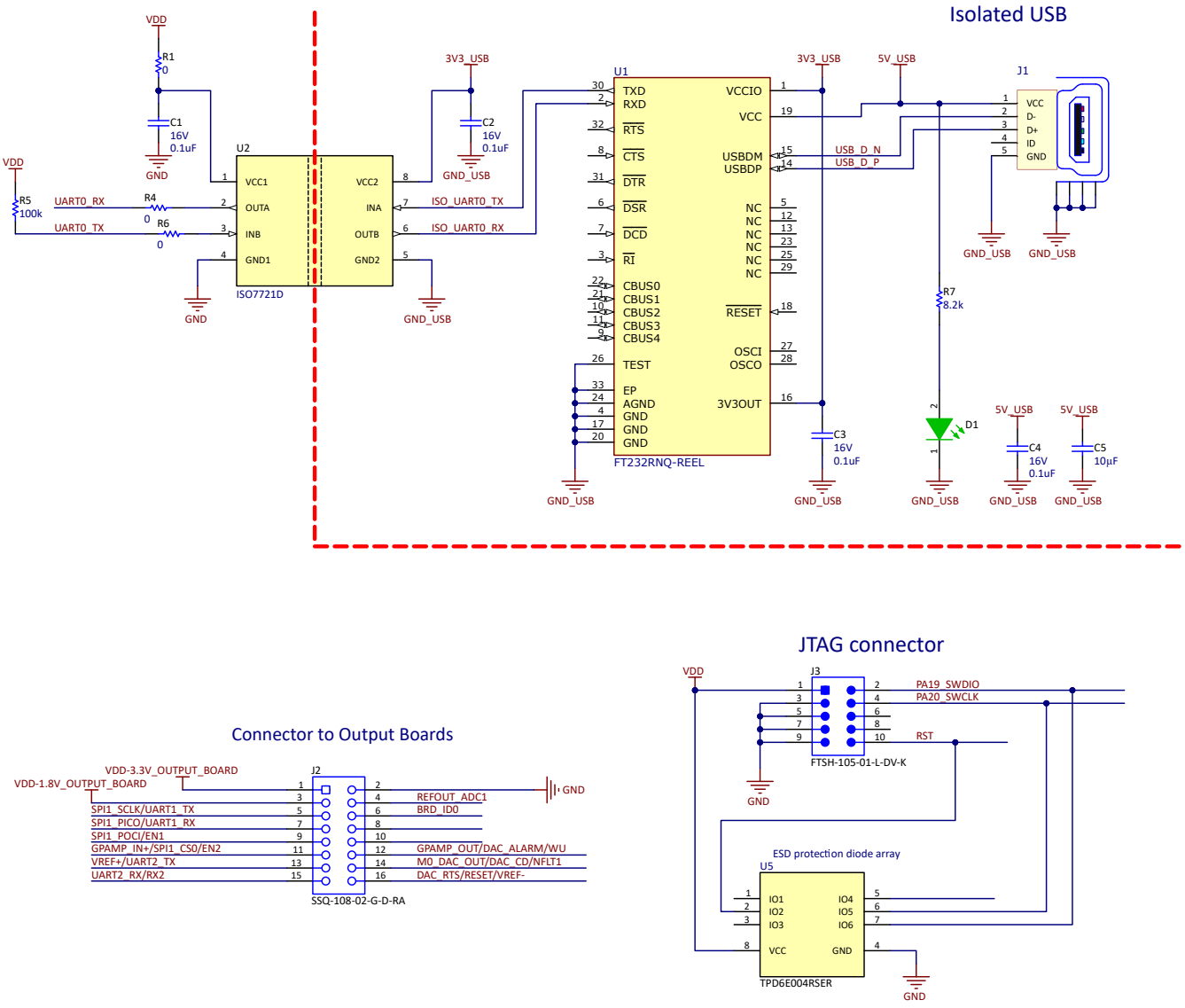

Figure 5-17. SNSR-DUAL-ADC-EVM Digital Interfaces

Table 5-11 shows the pinout for header J2 that is used to interface with compatible output boards. Pin one is marked on the PCB.

Table 5-11. J2 Header Pins

Pin	Description
1	VDD-3.3V from output board
2	GND
3	VDD-1.8V from output board
4	ADC1 REFOUT
5	SPI1 SCLK / UART1 TX
6	Output board ID
7	SPI1 PICO / UART1 RX
8	Not used
9	SPI1 POCI / EN 1
10	Not used
11	GPAMP IN+ / SPI1 CS / EN2
12	GPAMP OUT / DAC ALARM / WU
13	VREF+ / UART2 TX
14	M0 DAC OUT / DAC CD / NFLT1
15	UART2 RX / RX2
16	DAC RTS / RESET / VREF-

5.9 Digital Connection Headers

Figure 5-18 shows that headers J5 and J7 provide test points to measure digital signals or connect the SNSR-DUAL-ADC-EVM to an external controller if desired. Header J5 includes the communication signals: SCLK, PICO, POCI, CS0, and ADC2 CS for multi-device communication. Header J7 can be used to monitor the daisy-chain communication from the SDO of ADC1 to SDI of ADC2. By default, the EVM does not populate header J7.

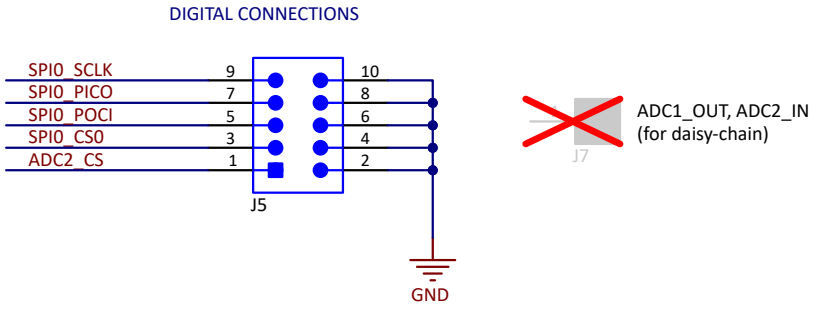

Figure 5-18. Digital Connection Headers

5.10 Shift Register

Figure 5-19 shows the shift register communication circuit. Each EVM variant has a unique identifier derived from the voltages applied to the shift register A:H pins. The MCU reads this board ID at start-up to determine which boards are connected and therefore which configuration settings and functions to execute. After start-up the firmware switches the TMUX1219 multiplexer from SHIFT_REGISTER to ADC2_SDO because the shift register is no longer required.

This shift register circuit is a unique function to the sensor transmitter reference design boards and is not a necessary circuit to replicate in an actual system.

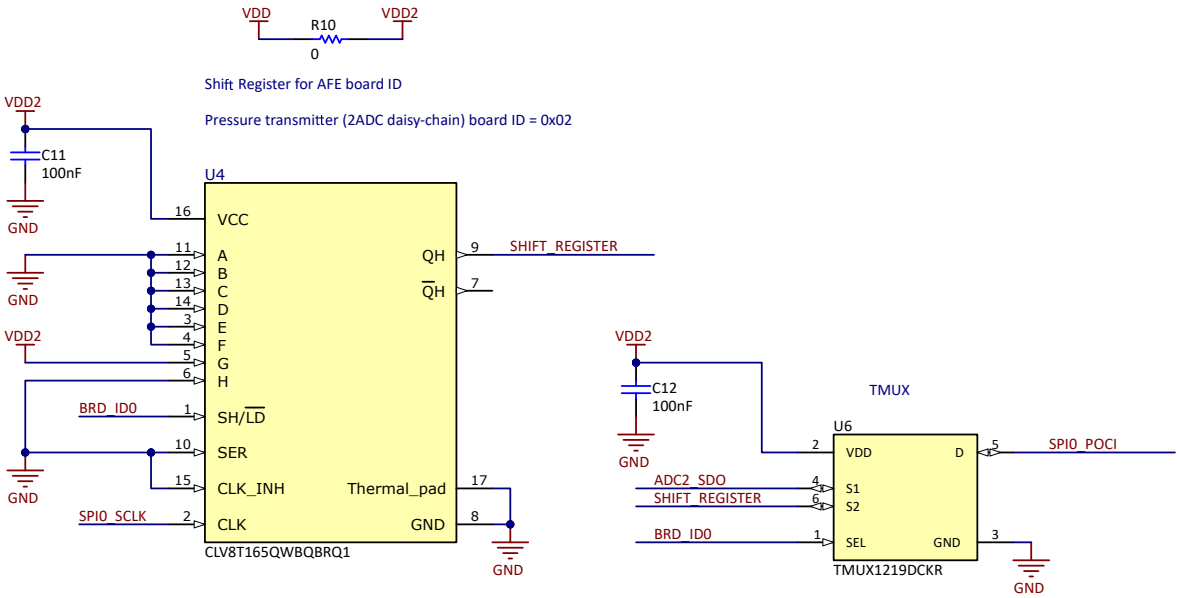

Figure 5-19. Identification Shift Register With Specific SNSR-DUAL-ADC-EVM Board ID Shown

5.11 Connecting External Output Boards to Header J2

The SNSR-DUAL-ADC-EVM can interface with several external output boards to model a complete field transmitter system. These companion PCB reference designs include both digital output and analog output options, including 4-20mA and 0-10V. For example, the Loop Control AFE Transmitter is a Texas Instruments reference design that includes a low-power, precision DAC and an output stage to generate a 4-20mA signal in a loop-powered transmitter application. In this configuration, the 4-20mA loop provides power to the Loop Control AFE Transmitter board, which in turn provides power to the SNSR-DUAL-ADC-EVM. Select the appropriate VDD voltage level using jumper JP1 on the SNSR-DUAL-ADC-EVM.

Figure 5-20 shows the SNSR-DUAL-ADC-EVM connected to the Loop Control AFE Transmitter with a 4-20mA output. Refer to TIDA-010982 for more information about the Loop Control AFE Transmitter and how the transmitter can be used with the SNSR-DUAL-ADC-EVM.

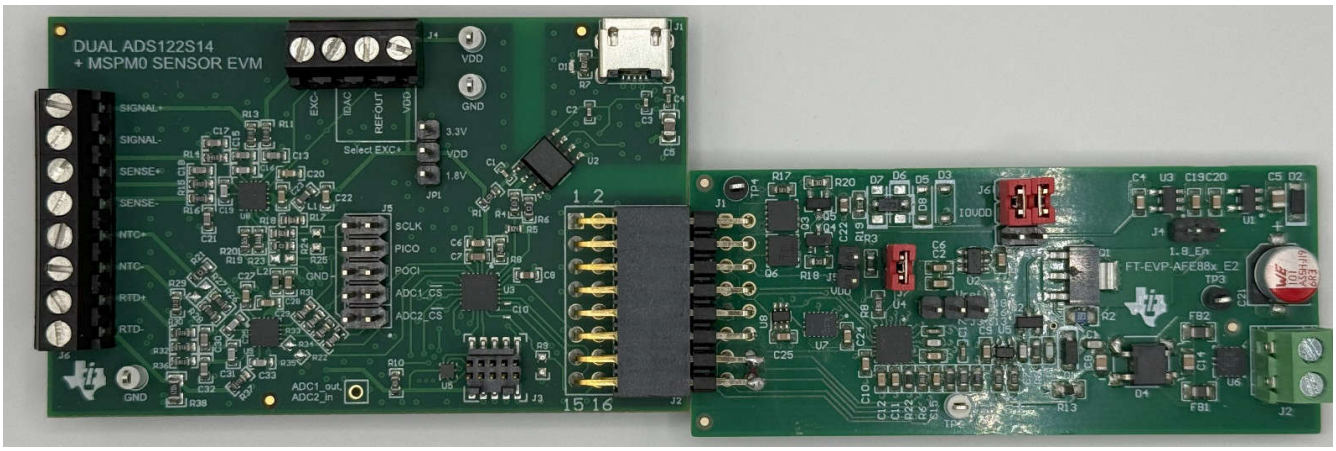

Figure 5-20. Loop Control AFE Transmitter Board Connected to the SNSR-DUAL-ADC-EVM

6 Software

The SNSR-DUAL-ADC-EVM includes preloaded firmware that users can access with a terminal program through the isolated USB. Download the example code from the Precision ADC GitHub® to modify the script beyond the commands listed below.

6.1 Top Level Menu

The SNSR-DUAL-ADC-EVM software uses nested menus. Access the top-level menu with the *help* command. In any sub-menu, use the *help* command by typing the sub-menu name followed by "help". The top-level *help* function lists all accessible subsystem menus. Figure 6-1 illustrates the top-level *help* menu of the EVM.

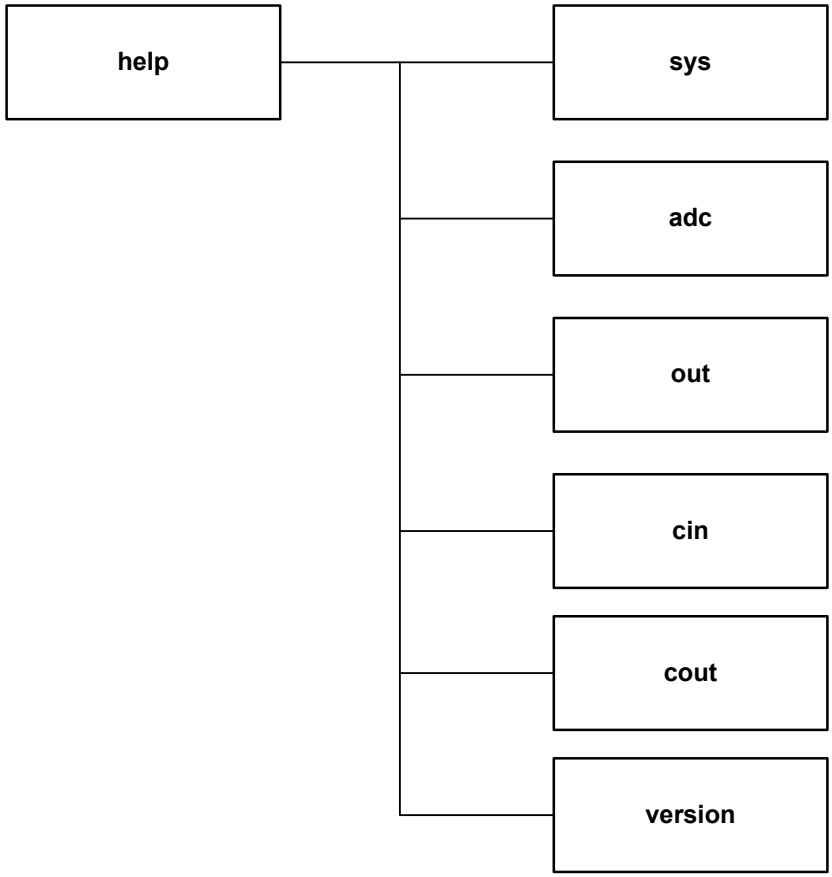

Figure 6-1. Top Level *Help* Menu

6.1.1 Top-level Help Menu Terminal

Figure 6-2 shows the terminal view of the *help* command.

```
FT Platform Oct 31 2025 07:38:59
Running at 32 MHz
Using ADS122S14 in daisy chain for pressure sensing
initialized...
help
help
sys     - 0x4ae1 - configure system
adc     - 0x545d - configure adc subsystem
out     - 0x5fed - configure output subsystem
cin     - 0x5f6d - configure adc data conditioning system
cout    - 0x6da9 - configure output data conditioning system
help    - 0x6659 - show this message
version - 0x45f5 - show information about software and hardware version
ret: 0
```

Figure 6-2. Terminal Top-Level *Help* Menu

6.2 System Sub Menu

Each subsystem menu has additional functionality menus. For example, writing *sys help* opens the help menu for configuring the *sys* subsystem and includes descriptions to use each menu. Figure 6-3 shows the functions that are available on the *sys* level.

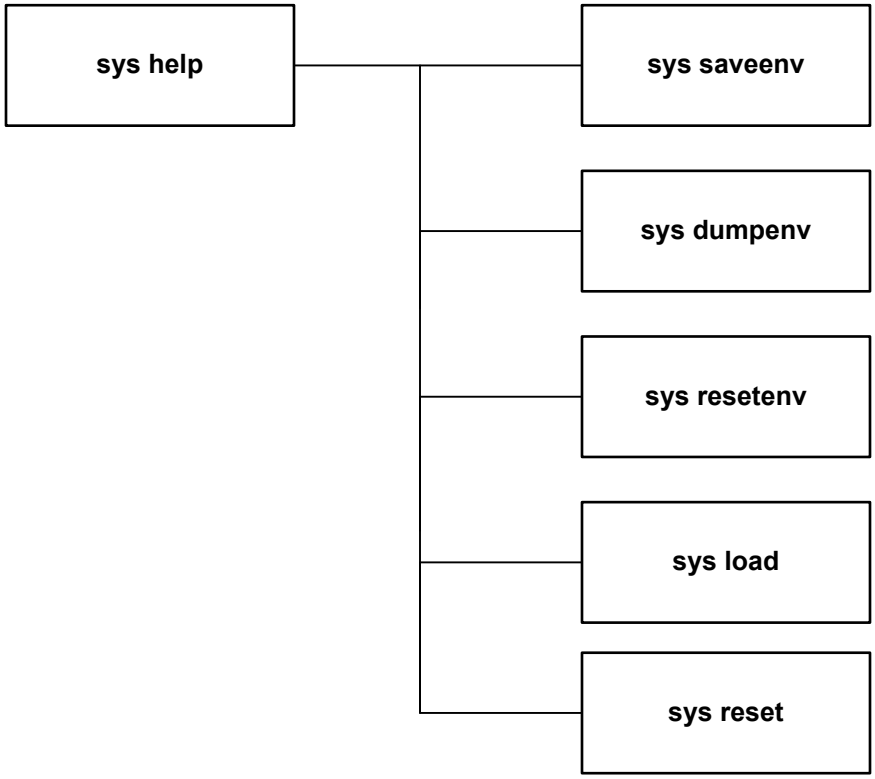

Figure 6-3. Sub-Level *sys help* Menu

6.2.1 SYS Help Menu Output

Figure 6-4 shows the terminal view of the *sys help* command.

```
sys help
sys help
All commands must start with sys
help       - 0x5501 - show this message
saveenv    - 0x166d - writes current configuration to flash
dumpenv    - 0x26f5 - dumps current configuration to screen
resetenv   - 0x7805 - dumps current configuration to screen
load       - 0x7d2d - read processing time of signal chain
reset      - 0x7d45 - restart the cpu
ret: 0
```

Figure 6-4. Terminal Sub-level *sys help* Menu

6.3 ADC Sub Menu

Each subsystem menu has additional functionality menus. For example, writing *adc help* opens the help menu for configuring the ADC subsystem and includes descriptions to use each menu. Figure 6-5 shows the *adc help* menu functions that are available for each ADS122S14.

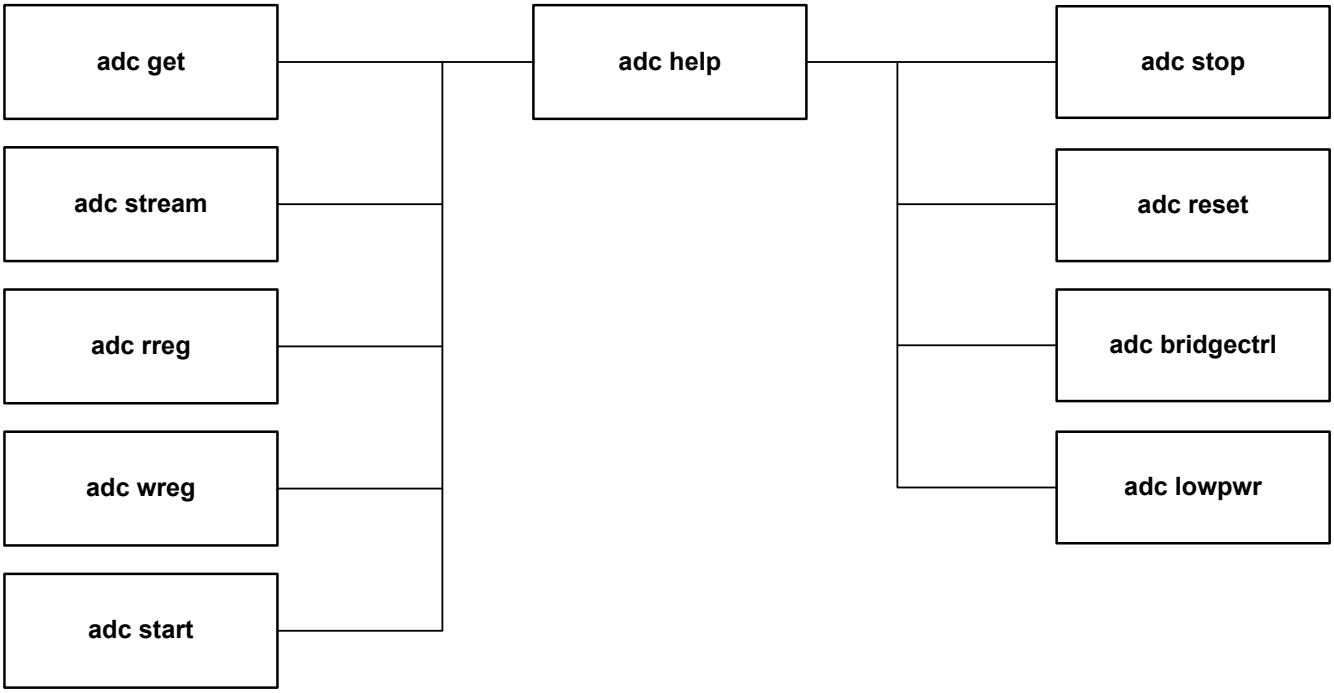

Figure 6-5. Sub-Level *adc help* Menu

6.3.1 ADC Help Menu Output

Use the *adc help* command to view the list of commands that can configure and control the ADCs. Figure 6-6 shows the terminal view of the *adc help* command.

```
adc help
adc help
All commands must start with adc
help       - 0x6605 - show this message
get        - 0x790d - return one raw reading
stream     - 0x7689 - starts/stops streaming raw readings
rreg       - 0x62ad - read register on both ADCs - rreg reg
wreg       - 0x52a9 - write register to ADC1 - wreg 1 reg value
                    - write register to ADC2 - wreg 2 reg value
start      - 0x79bd - start conversion
stop       - 0x79d9 - stop conversion
reset      - 0x6059 - rewrite default EVM adc config
bridgectrl - 0x4ef9 - Enable/disable bridge and bridge status readback - bridgectrl [on|off]
lowpwr     - 0x1f35 - operate bridge and ADC in duty cycle mode - enter time between power-ups in ms
cm_test    - 0x2c29 - production test for manufacturer
ret: 0
```

Figure 6-6. Terminal Sub-level *adc help* Menu

6.3.2 adc help Menu Input and Output Examples

The following sections provide examples for using several of the commands shown in Figure 6-6. Each section includes the input to the terminal to execute the command as well as a logic analyzer capture to show the expected output.

- *adc reset* Example
- *adc wreg* Daisy-Chain Example (Writing to a Single ADC)
- *adc wreg* Daisy-Chain Example (Writing to Both ADCs)
- *adc rreg* Daisy-Chain Example
- *adc stream* Example
- *adc lowpwr* Example

The SNSR-DUAL-ADC-EVM default behavior always transmits ten data frames per communication cycle in daisy-chain mode. The preloaded firmware receives two status bytes followed by three data bytes from each ADC regardless of the transmitted command or data. Refer to the ADS122S14 data sheet for details on daisy-chain operation.

Figure 6-7 shows an example logic analyzer capture of the EVM response frame to read out conversion data. Use Figure 6-7 as a guide to understand the logic analyzer captures in subsequent sections.

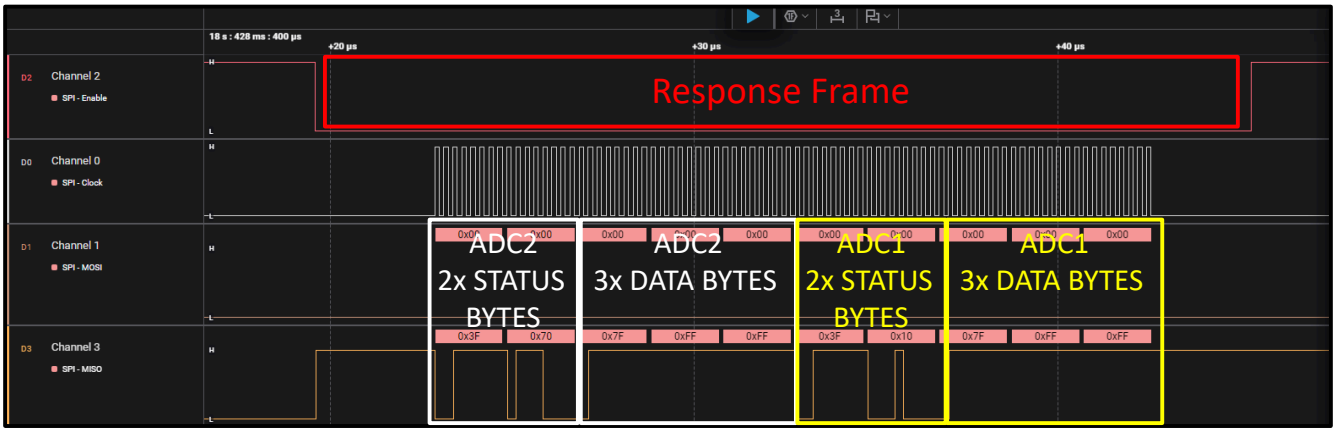

Figure 6-7. Example Logic Analyzer ADC Data Frame

6.3.2.1 *adc reset* Example

Use the *adc reset* command to reset both ADC1 and ADC2 to the preloaded-firmware default settings, which can be different than the device default settings. Figure 6-8 shows an example of the proper terminal syntax to reset ADC1 and ADC2 to the firmware defaults. The *adc reset* command always resets both ADCs in the default daisy-chain configuration such that resetting a single ADC is not possible.

Figure 6-8. Terminal Input to Reset Both ADC1 and ADC2 to Default Firmware Values (*adc reset*)

Syntax: *adc reset*

Table 6-1 shows the default SNSR-DUAL-ADC-EVM ADC1 and ADC2 register settings that are set on both power-up or using the *adc reset* command.

Table 6-1. ADC1 and ADC2 Power-on and *adc reset* Register Settings

ADC	REGISTER (Address)	VALUE
ADC1	DEVICE_CFG (05h)	0x00
	DATA_RATE_CFG (06h)	0x07
	MUX_CFG (07h)	0x23
	GAIN_CFG (08h)	0x01
	REFERENCE_CFG (09h)	0x21
	DIGITAL_CFG (0Ah)	0x10
	IDAC_MUX_CFG (0Eh)	0x80
ADC2	DEVICE_CFG (05h)	0x00
	DATA_RATE_CFG (06h)	0x07
	MUX_CFG (07h)	0x23
	GAIN_CFG (08h)	0x01
	REFERENCE_CFG (09h)	0x21
	DIGITAL_CFG (0Ah)	0x10
	IDAC_MAG_CFG (0Dh)	0x04
	IDAC_MUX_CFG (0Eh)	0xF6

All other ADC registers not included in Table 6-1 are the default value as specified in the ADS122S14 data sheet.

6.3.2.2 *adc wreg* Daisy-Chain Example (Writing to a Single ADC)

Use the *adc wreg* command followed by either a 1 or 2 to write to ADC1 or ADC2 respectively, while writing a null command to the other ADC. Complete the command by adding the one byte register address and the one byte register value after the ADC number. Figure 6-9 shows an example of the proper terminal syntax to write to register 08 (GAIN_CFG) to set the ADC1 gain to 128: *adc wreg 1 08 0D*.

Syntax: *adc wreg [ADC] [register address] [value]*

```
adc wreg 1 08 0D
adc wreg 1 08 0D
ret: 0
```

Figure 6-9. Terminal Input to Set ADC1 Gain to 128 (*adc wreg 1 08 0D*)

Figure 6-10 shows an example logic analyzer capture of the *adc wreg 1 08 0D* command with the input to ADC2 in the white box and the input to ADC1 in the yellow box. The white box shows that the controller sends the null command to ADC2 and the yellow box shows that the controller sends the write command to ADC1.

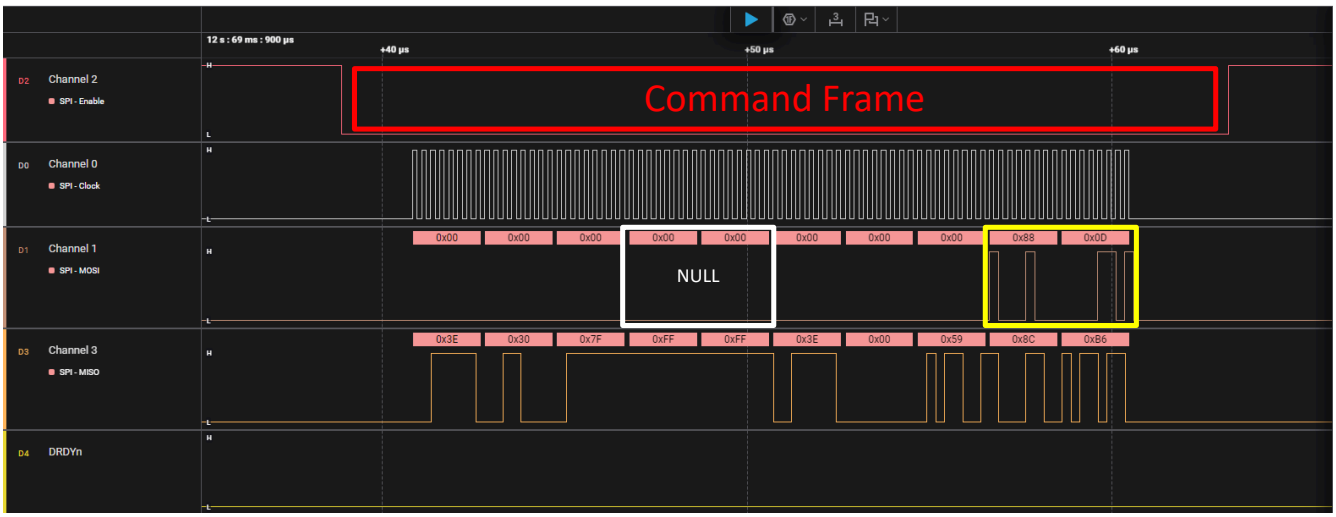

Figure 6-10. *adc wreg 1 08 0D* Logic Analyzer Capture

6.3.2.3 *adc wreg* Daisy-Chain Example (Writing to Both ADCs)

Use the *adc wreg* command followed by the one byte register address and one byte register value to write to both ADC1 and ADC2. Figure 6-11 shows an example of the proper terminal syntax to write to register 06 (DATA_RATE_CFG) to set ADC1 and ADC2 OSR = 16: *wreg 06 00*.

Syntax: *adc wreg [register address] [value]*

```
adc wreg 06 00
adc wreg 06 00
ret: 0
```

Figure 6-11. Terminal Input to Set ADC1 and ADC2 OSR to 16 (*adc wreg 06 00*)

Figure 6-12 shows an example logic analyzer capture of the *adc wreg 06 00* command with the input to ADC2 in the white box and the input to ADC1 in the yellow box. The white box shows the write command to ADC2 and the yellow box shows the write command to ADC1.

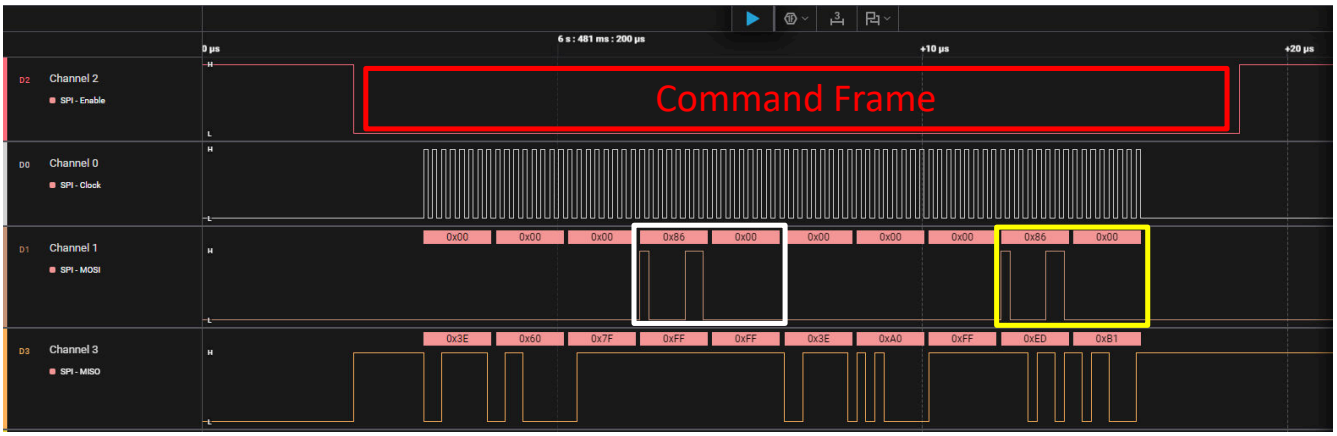

Figure 6-12. *adc wreg 06 00* Logic Analyzer Capture

6.3.2.4 *adc rreg* Daisy-Chain Example

Use the *adc rreg* command followed by the one byte register address to read the register value of both ADC1 and ADC2. Figure 6-13 shows an example of the proper terminal syntax and response to read register 05 (DEVICE_CFG): *adc rreg 05*.

Syntax: *adc rreg [register address]*

Response: *Reg [register address], 0x[ADC1 register value] 0x[ADC2 register value]*

```
adc rreg 05
adc rreg 05
Reg 0x5, 0x0 0x0
ret: 0
```

Figure 6-13. Terminal *adc rreg 05*

Figure 6-14 shows an example logic analyzer capture of the *adc rreg 05* command with the input to and response from ADC2 included in the white boxes while the input to and response from ADC1 is included in the yellow boxes. The 10-byte command frame shows the read command written to both ADCs. The 10-byte response frame reads out the register data from both ADCs. The *adc rreg* command always reads data from both ADCs in the default daisy-chain configuration such that reading data from a single ADC is not possible.

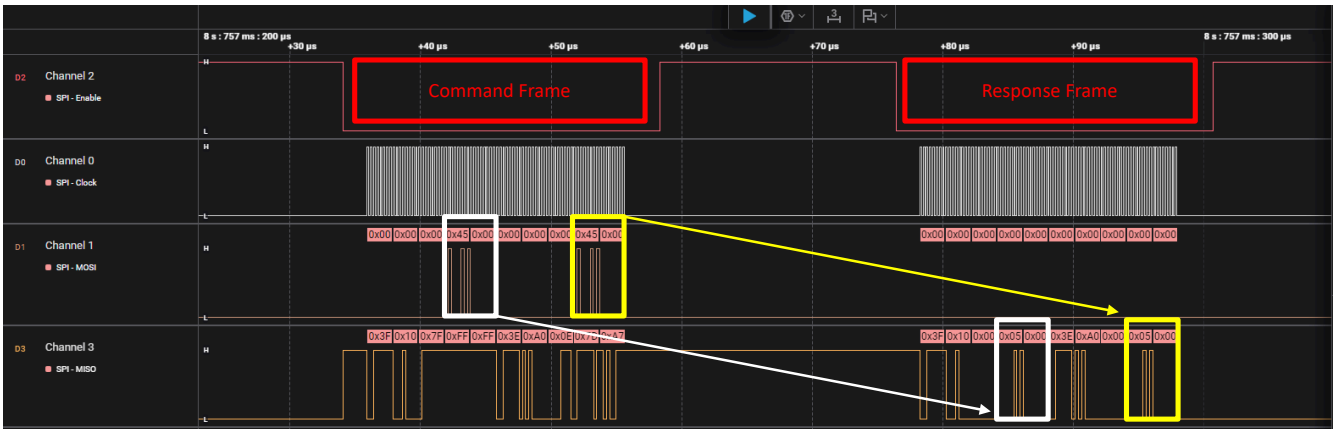

Figure 6-14. *adc rreg 05* Logic Analyzer Capture

6.3.2.5 *adc stream* Example

Use the *adc stream* command to stream out ADC1 and ADC2 data directly to the terminal. Figure 6-15 shows an example of the proper terminal syntax and response of the *adc stream* command.

```
adc stream
adc stream
ret: 0
0xl734cf 0x7feecf
0xl73527 0x7feeae
0xl73448 0x7feecb
0xl734a3 0x7feed7
a0xl7366b 0x7fefl5
0xl7348e 0x7feefe
0xl7358e 0x7feed4
d0xl73499 0x7feef8
0xl734f8 0x7feecc
0xl73424 0x7feef3
0xl73371 0x7feeea
c0xl7353b 0x7feed4
0xl734lc 0x7feef7
 0xl73455 0x7feebe
0xl735a7 0x7feecb
0xl7334f 0x7feef2
s0xl734cf 0x7feedb
0xl736e4 0x7feed8
0xl7352c 0x7feed7
t0xl73497 0x7fefl0
0xl73545 0x7feeea
r0xl73367 0x7feee8
0xl733a2 0x7feeb3
0xl7337e 0x7feedf
e0xl7364e 0x7feee1
0xl734bl 0x7feee3
a0xl73495 0x7feeb2
0xl73479 0x7feed3
```

Figure 6-15. Terminal *adc stream*

Figure 6-16 shows an example logic analyzer capture of the *adc stream* command.

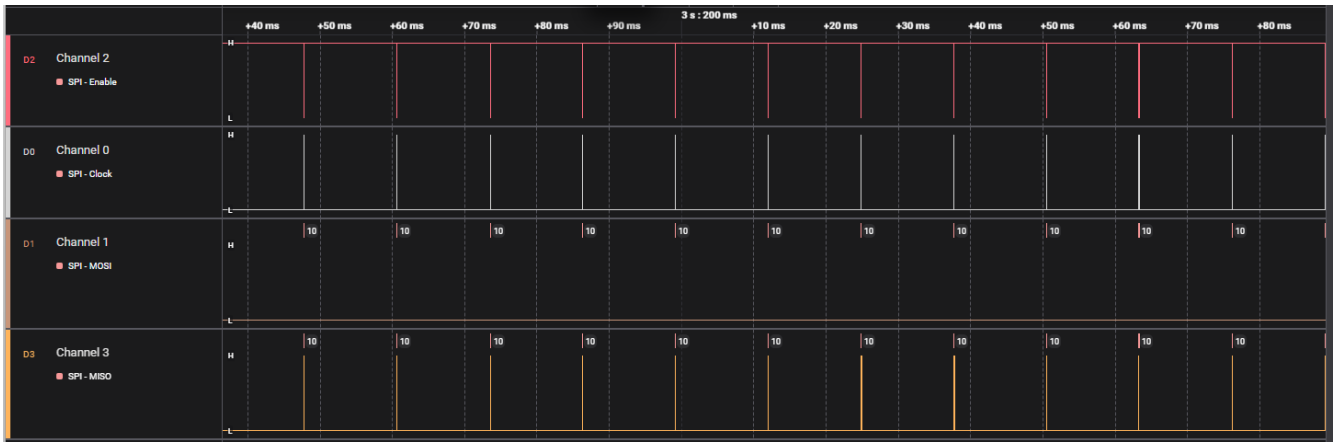

Figure 6-16. *adc stream* Logic Analyzer Capture

6.3.2.6 *adc lowpwr* Example

Use the *adc lowpwr* command to collect periodic sensor readings while minimizing power consumption. The firmware minimizes power consumption by cycling the MCU, both ADCs, and the bridge power between conversions. Figure 6-17 shows the timing diagram for the *adc lowpwr* command including the bridge power, ADC power, and the MCU power during one complete sensor cycle period.

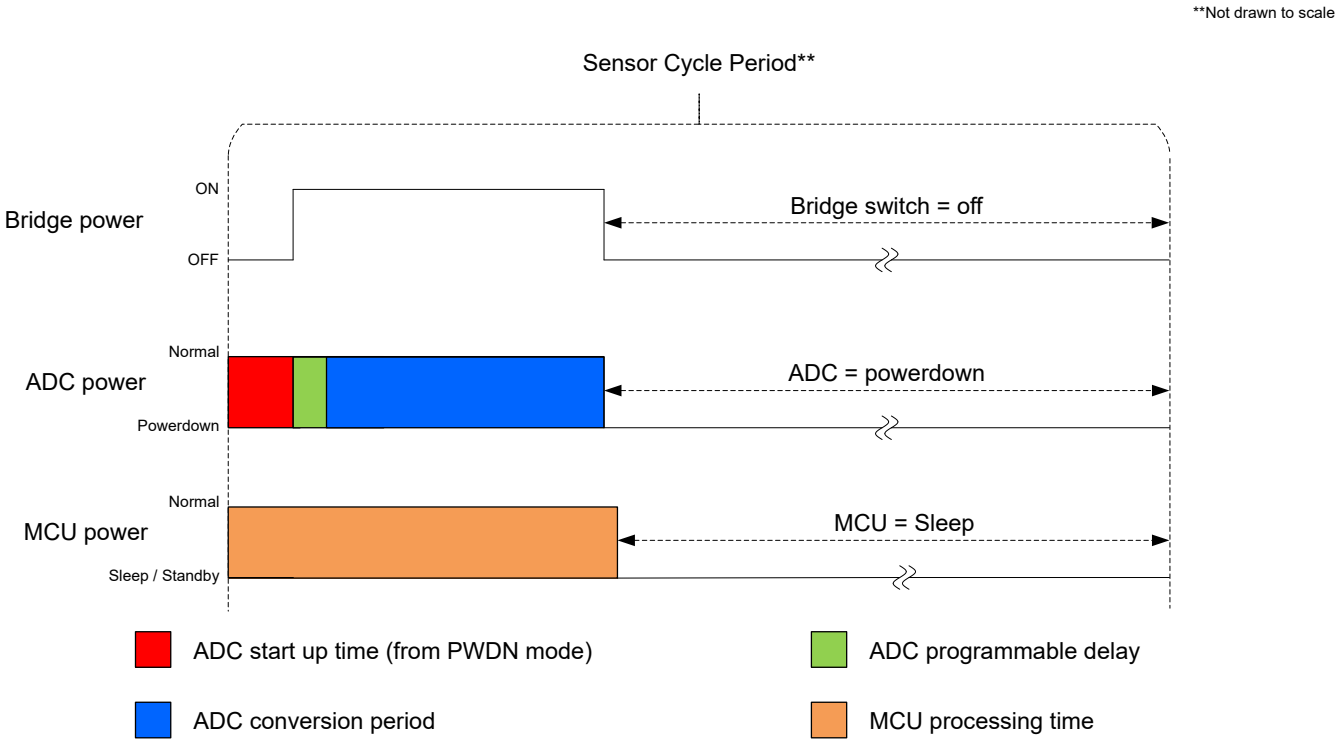

Figure 6-17. *adc lowpwr* Example Timing Diagram

As Figure 6-17 shows, the system on-time is effectively the sum of the ADC start up, ADC delay, and ADC conversion times, though the MCU must stay active slightly longer to process the received data and put the ADC in powerdown mode. The user must verify that the selected ADC settings result in an on-time that is less than the sensor cycle period. Figure 6-18 shows an example of the proper terminal syntax and response to get one reading from ADC1 and ADC2 every 1000ms: *adc lowpwr 1000*.

Syntax: *adc lowpwr [sensor cycle period]*

```
adc lowpwr 1000
adc lowpwr 1000
Mode: 0 | f_MOD: 32000 Hz | OSR: 0x07h | Start up: 10.0 ms | Delay: 0.0000 ms | Conv: 55.33 ms | Duty Cycle: 6.5%
ADC Low power bridge cycling streaming every 1000 ms. Type 'adc lowpwr stop' to halt.

ADC1: 0x7fffff ADC2: 0x7fedf5
ADC1: 0x7fffff ADC2: 0x7fef21
ADC1: 0x7fffff ADC2: 0x7feeld
ADC1: 0x7fffff ADC2: 0x7fef8f
ADC1: 0x7fffff ADC2: 0x7fef67
ADC1: 0x7fffff ADC2: 0x7ff07f
ADC1: 0x7fffff ADC2: 0x7feea9
ADC1: 0x7fffff ADC2: 0x7feedb
ADC1: 0x7fffff ADC2: 0x7fef99
ADC1: 0x7fffff ADC2: 0x7feeef
ADC1: 0x7fffff ADC2: 0x7feeb3
ADC1: 0x7fffff ADC2: 0x7fef99
ADC1: 0x7fffff ADC2: 0x7fee4f
ADC1: 0x7fffff ADC2: 0x7feea9
```

Figure 6-18. *adc lowpwr 1000* Terminal Input Example

The firmware uses the current ADC settings set by the user to derive timing parameters and execute the *adc lowpwr* command. This command displays the applicable, user-configured ADC settings and derived timing parameters for reference. Table 6-2 shows the output from the *adc lowpwr* command.

Table 6-2. *adc lowpwr* Response

Parameter	Description	Type	Applicable ADS122S14 Register
MODE	Current ADC speed mode	User Configured	DEVICE_CFG (0x05h)
f_MOD	MODE modulator frequency	Response	N/A
OSR	OSR register bits	User Configured	DATA_RATE_CFG (0x06h)
START UP	ADC START UP time from Powerdown mode, see ADS122S14 data sheet Electrical Characteristics Table	Response	N/A
DELAY	Programmable delay, use to account for external analog settling if necessary	User Configured	DATA_RATE_CFG (0x06h)
CONV	Total conversion time, includes DELAY	Response	N/A
DUTY CYCLE	Percentage of [(START UP + CONV) / sensor cycle period]	Response	N/A

Figure 6-19 shows an example logic analyzer capture of the *adc lowpwr 1000* command over a four-second period.

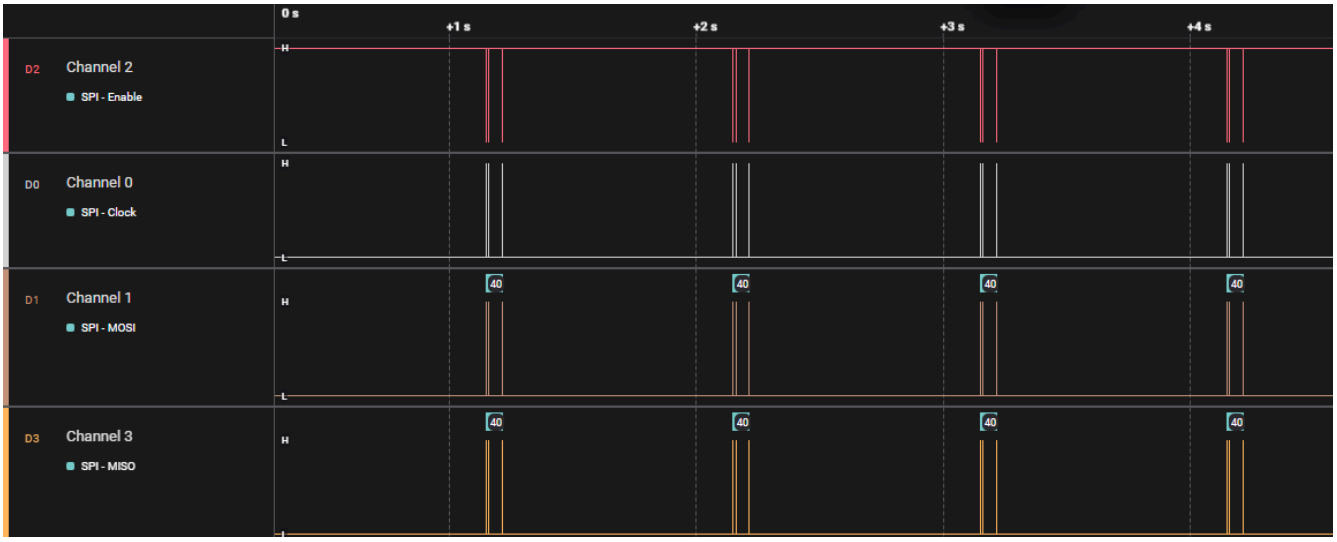

Figure 6-19. *adc lowpwr 1000* Logic Analyzer Capture

Figure 6-20 shows an example terminal output when the ADC active period exceeds 90% of the user-input sensor cycle period. The terminal displays the minimum sensor cycle period based on the current ADC settings.

```
adc lowpwr 50
adc lowpwr 50
Sensor cycle period too short for settings(min time: 73.19 ms). Please adjust inputs.
ret: 1
```

Figure 6-20. *adc lowpwr* Sensor Cycle Period Too Short

Figure 6-21 shows an example of the proper syntax and response to stop the *adc lowpwr* stream mode: *adc lowpwr stop*.

Syntax: *adc lowpwr stop*

```
adc lowpwr stop
Stopping ADC Low power bridge cycling stream...
ADC Low power bridge cycling stream stopped.
ret: 0
```

Figure 6-21. *adc lowpwr stop* Terminal Input Example

Figure 6-22 shows the total SNSR-DUAL-ADC-EVM supply current using the *adc lowpwr 1000* command over a four-second period. The bridge switch is disabled, the ADS122S14 ADCs enter power-down mode, and the MSPM0 enters Sleep Mode during the low part of the duty cycle. This power cycling reduces the average current consumption over the 1000ms sampling period by 48%, from 4.5mA to 2.34mA. Save additional average power by reducing the conversion time, increasing the sensor cycle period, or putting the MCU into a lower power state.

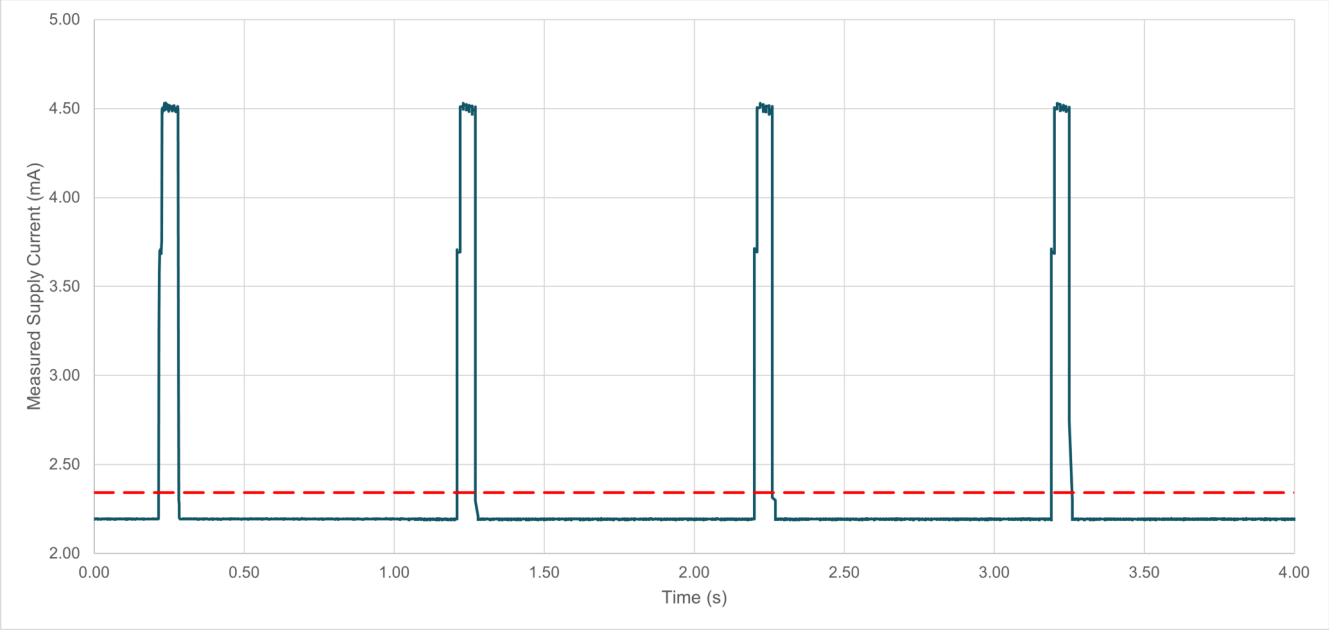

Figure 6-22. SNSR-DUAL-ADC-EVM Supply Current Over Time Using the *adc lowpwr 1000* Command

Figure 6-23 shows a breakdown of the supply current consumption of ADC1, ADC2, a 1.5kΩ (nominal) Wheatstone bridge, and the MSPM0 during normal operation of the SNSR-DUAL-ADC-EVM using the settings shown in Figure 6-18.

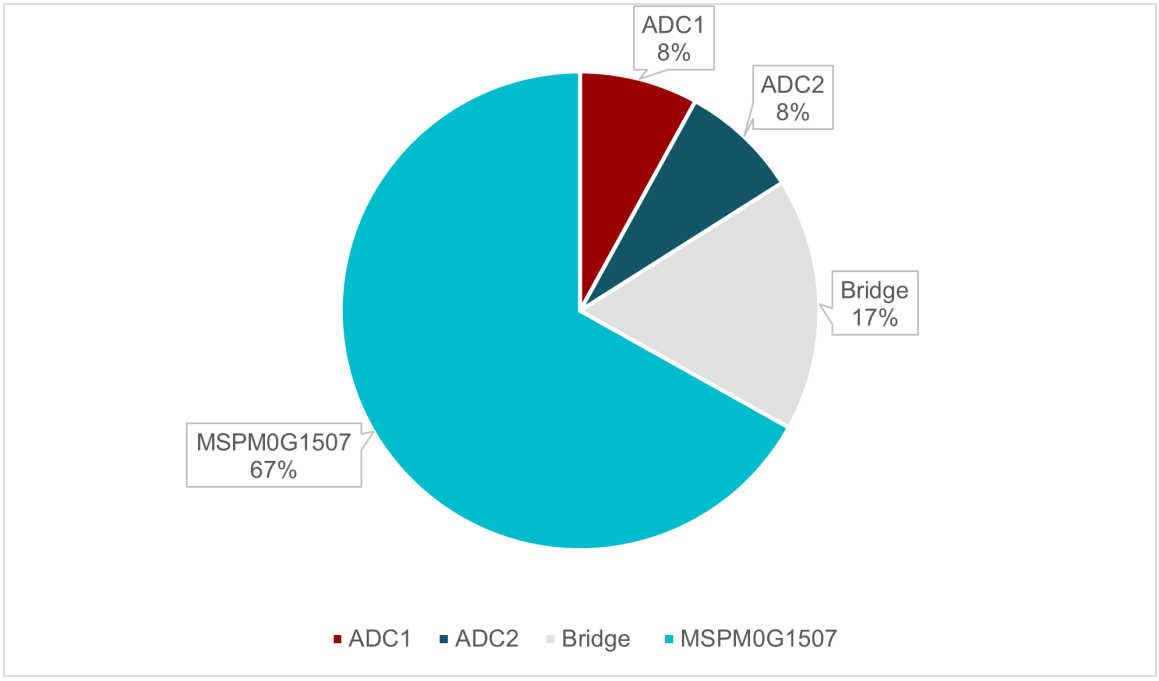

Figure 6-23. Supply Current During Normal Operation by Device

7 Hardware Design Files

The following section contains the SNSR-DUAL-ADC-EVM board schematic, printed-circuit-board (PCB) layout, and bill of materials (BOM).

7.1 Schematics

Figure 7-1 to Figure 7-3 show the SNSR-DUAL-ADC-EVM schematics.

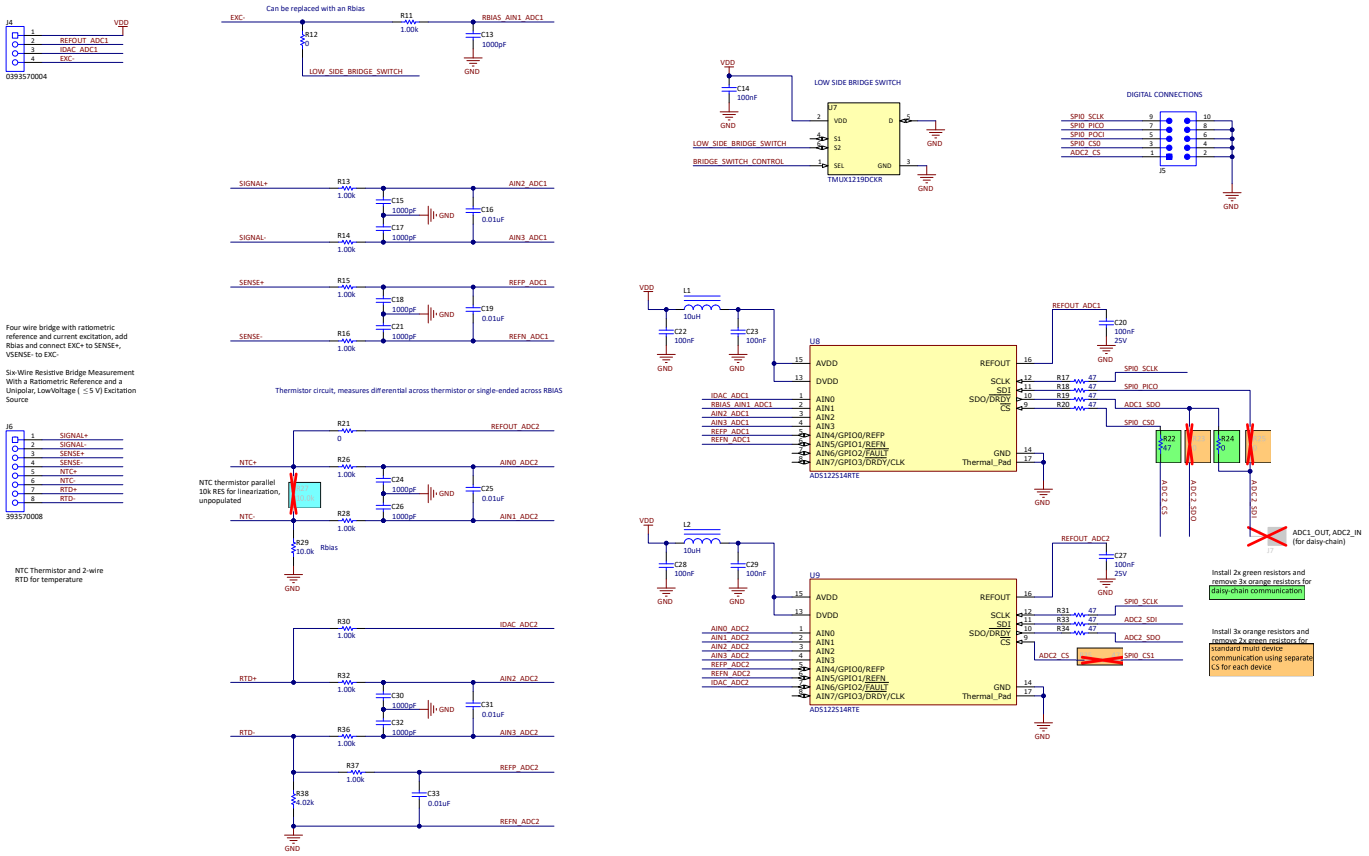

Figure 7-1. SNSR-DUAL-ADC-EVM Analog Front End

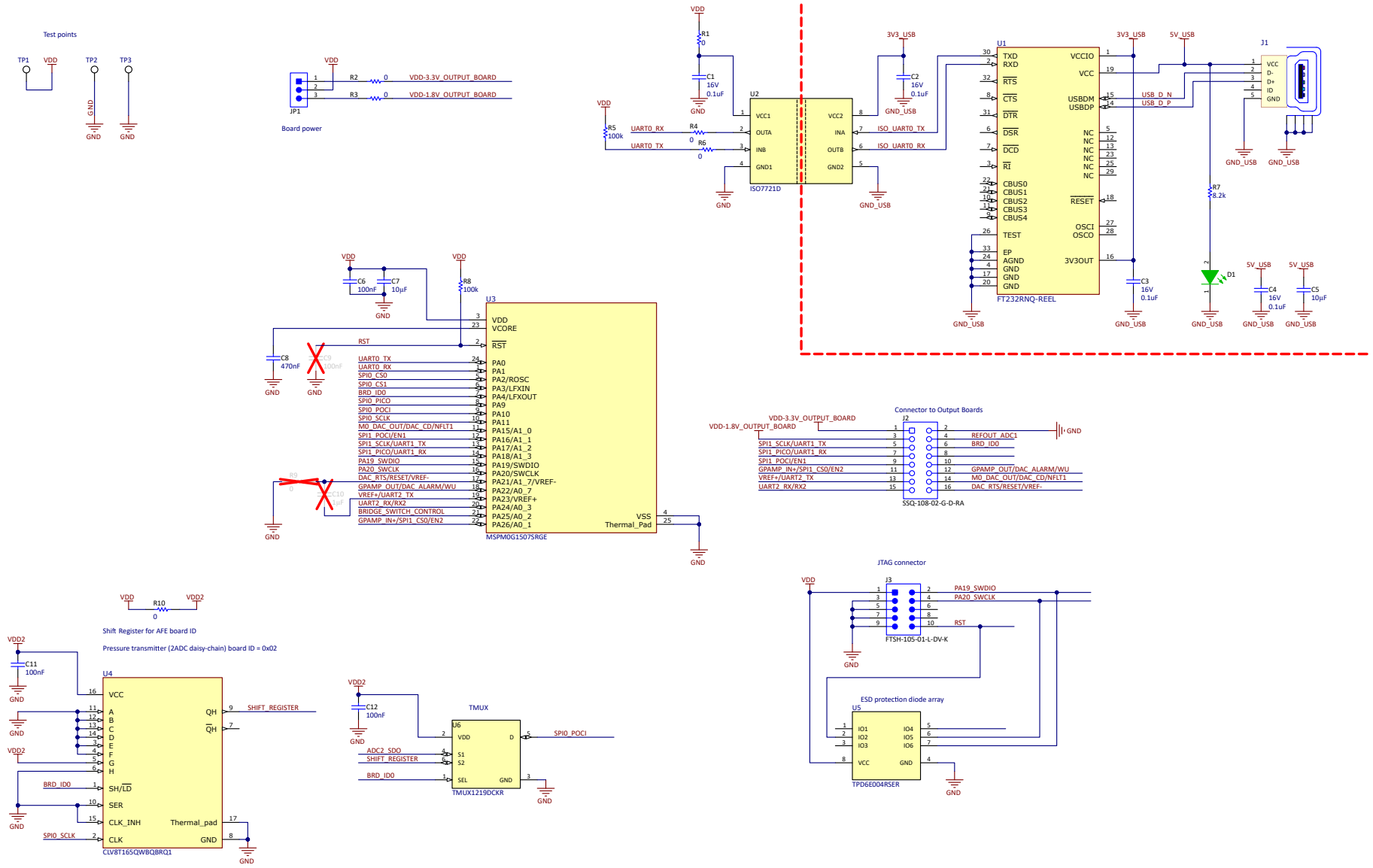

Figure 7-2. SNSR-DUAL-ADC-EVM Digital Schematic

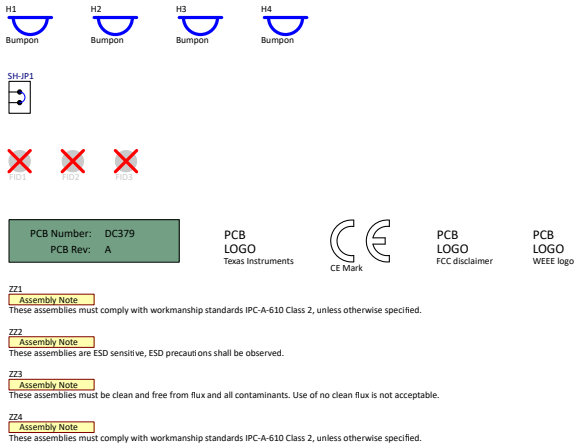

Figure 7-3. SNSR-DUAL-ADC-EVM Hardware

7.2 PCB Layout

Figure 7-4 to Figure 7-7 depict the SNSR-DUAL-ADC-EVM PCB layout. Board layouts are not to scale. These figures are intended to show how the board is laid out. The figures are not intended to be used for manufacturing EVM PCBs.

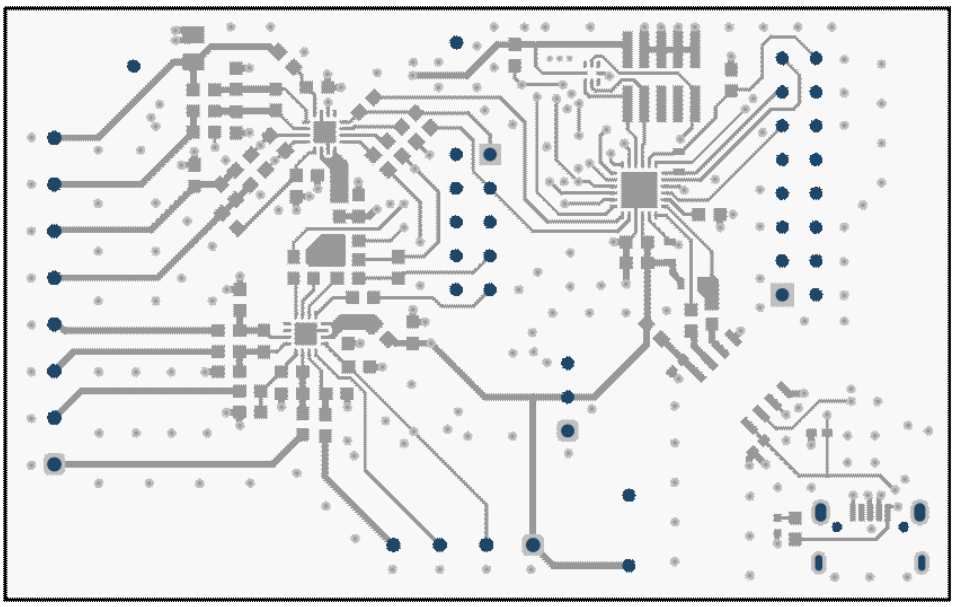

Figure 7-4. SNSR-DUAL-ADC-EVM PCB Layout - Top Layer

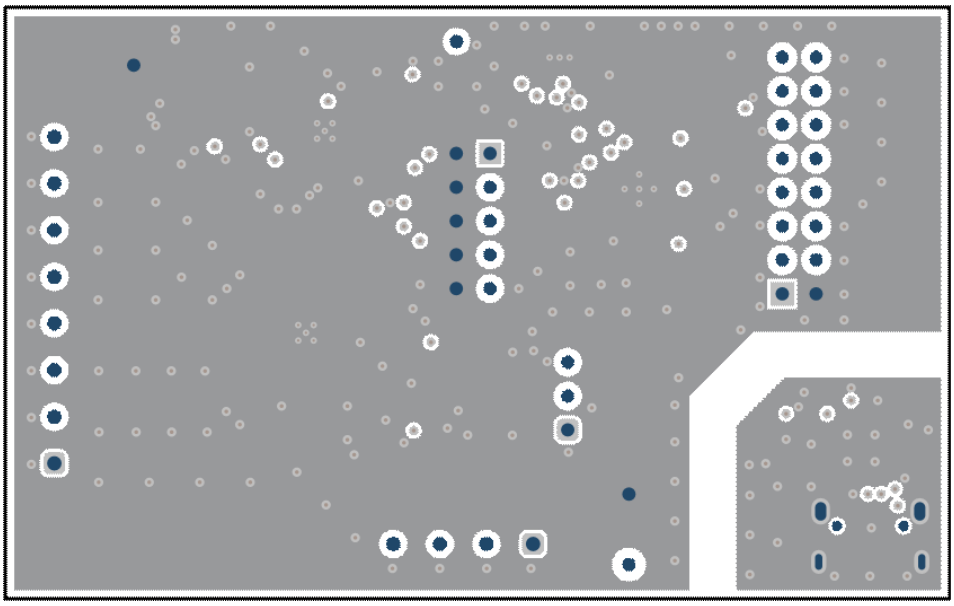

Figure 7-5. SNSR-DUAL-ADC-EVM PCB Layout - Ground Layer 1

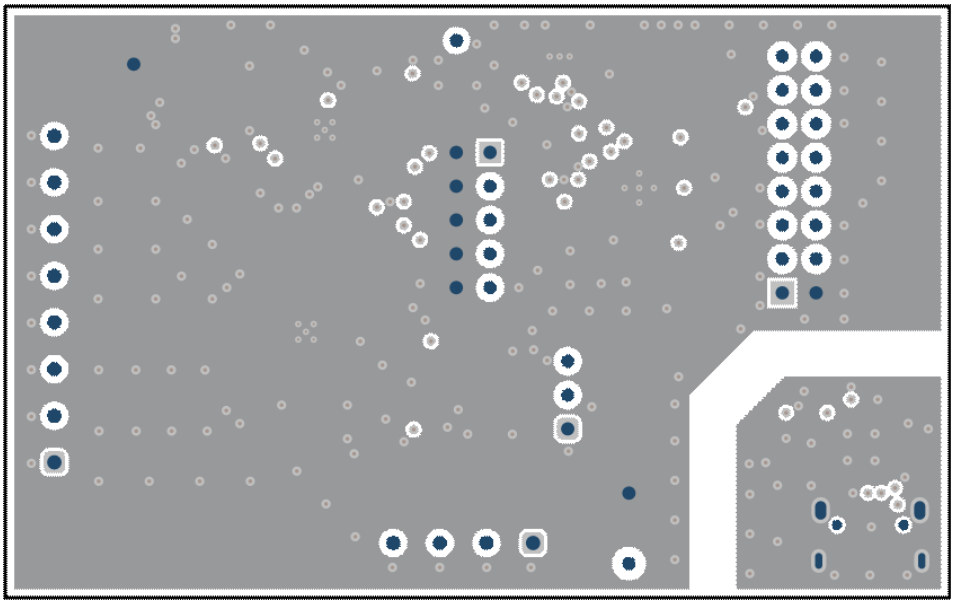

Figure 7-6. SNSR-DUAL-ADC-EVM PCB Layout - Ground Layer 2

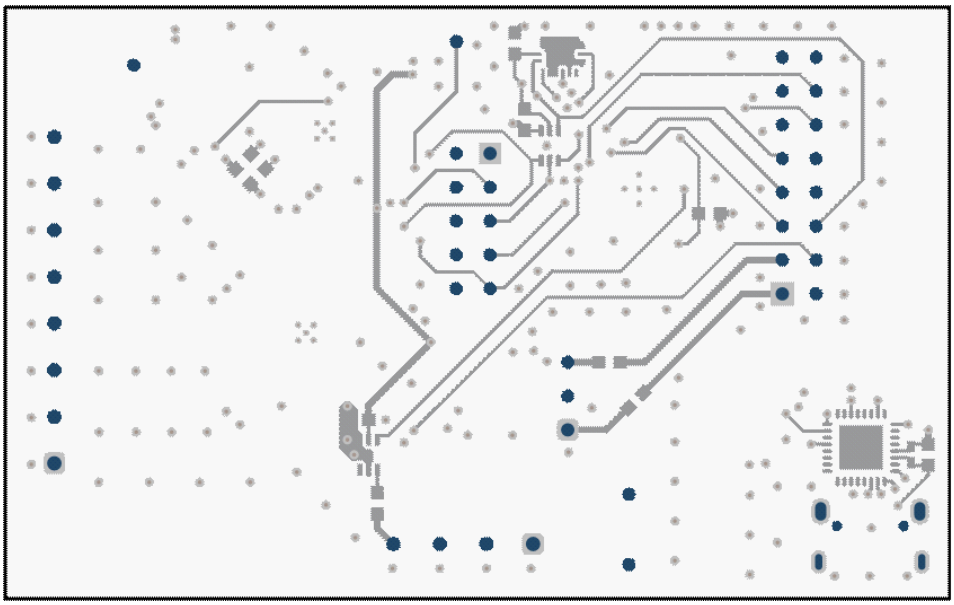

Figure 7-7. SNSR-DUAL-ADC-EVM PCB Layout - Bottom Layer

7.3 Bill of Materials

Table 7-1 lists the bill of materials (BOM) for the SNSR-DUAL-ADC-EVM.

Table 7-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		DC379	Any
C1, C2, C3, C4	4	0.1uF	CAP, CERM, 0.1uF, 16V, +/- 20%, X5R, 0402	402	8.85E+11	Wurth Elektronik
C5, C7	2	10uF	CAP, CERM, 10uF, 10V, +/- 20%, X7R, 0603	603	GRM188Z71A106MA73D	MuRata
C6, C11, C12, C14, C20, C22, C23, C27, C28, C29	10	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 10%, X7R, 0603	603	C0603C104K3RACTU	Kemet
C8	1	0.47uF	CAP, CERM, 0.47uF, 25V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	GCM188R71E474KA64D	MuRata
C13, C15, C17, C18, C21, C24, C26, C30, C32	9	1000pF	CAP, CERM, 1000pF, 50V, +/- 5%, C0G/NP0, 0603	603	GRM1885C1H102JA01D	MuRata
C16, C19, C25, C31, C33	5	0.01uF	CAP, CERM, 0.01uF, 50V, +/- 5%, C0G/NP0, 0603	603	GRM1885C1H103JA01D	MuRata
D1	1	Green	LED, Green, SMD	1x0.5mm	150040GS73240	Wurth Elektronik
H1, H2, H3, H4	4		Bumpon, Cylindrical, 0.312X 0.200, Black	Black Bumpon	SJ61A1	3M
J1	1		USB - micro B USB 2.0 Receptacle Connector 5 Position Surface Mount, Right Angle; Through Hole	CONN_USB_8MM0_6MM6	6.29E+11	Wurth Electronics
J2	1		Receptacle, 100mil, 8x2, Gold, R/A, TH	SSQ-108-02G-D-RA	SSQ-108-02G-D-RA	Samtec
J3	1		Header(Shrouded), 1.27mm, 5x2, Gold, SMT	Header(Shrouded), 1.27mm, 5x2, SMT	FTSH-105-01L-DV-K	Samtec
J4	1		Terminal Block, 3.5mm, 4x1, Tin, TH	Terminal Block, 3.5mm, 4x1, TH	3.94E+08	Molex
J5	1		Header, 100mil, 5x2, Gold, TH	5x2 Header	TSW-105-07G-D	Samtec
J6	1		Terminal Block, 3.5mm, 8x1, Tin, TH	Terminal Block, 3.5mm, 8x1, TH	3.94E+08	Molex
JP1	1		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07G-S	Samtec
L1, L2	2	10uH	Inductor, Multilayer, Ferrite, 10 uH, 0.3A, 0.6ohm, SMD	603	MLZ1608N100LT000	TDK
R1, R2, R3, R4, R6, R10, R12, R21, R24	9	0	RES, 0, 5%, 0.1W, 0603	603	RC0603JR-070RL	Yageo
R5, R8	2	100k	RES, 100k, 5%, 0.1W, 0603	603	CRCW0603100KJNEAC	Vishay-Dale
R7	1	8.2k	RES, 8.2k, 5%, 0.1W, AEC-Q200 Grade 0, 0603	603	CRCW06038K20JNEA	Vishay-Dale

Table 7-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R11, R13, R14, R15, R16, R26, R28, R30, R32, R36, R37	11	1.00k	RES, 1.00k, 0.1%, 0.1W, 0603	603	RG1608P-102B-T5	Susumu Co Ltd
R17, R18, R19, R20, R22, R31, R33, R34	8	47	RES, 47, 5%, 0.1W, AEC-Q200 Grade 0, 0603	603	CRCW060347R0JNEA	Vishay-Dale
R29	1	10.0k	RES, 10.0k, 1%, 0.1W, 0603	603	RC0603FR-0710KL	Yageo
R38	1	4.02k	RES, 4.02k, 0.1%, 0.125W, 0805	805	RT0805BRD074K02L	Yageo America
SH-JP1	1	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP1, TP2, TP3	3		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
U1	1		USB Bridge, USB to UART USB 2.0 UART Interface 32-QFN (5x5)	QFN32	FT232RNQ-REEL	FTDI
U2	1		High Speed, Robust EMC Reinforced Dual-Channel Digital Isolator, D0008B (SOIC-8)	D0008B	ISO7021D	Texas Instruments
U3	1		Mixed-Signal Microcontroller, VQFN24	VQFN24	MSPM0G1507SRGE	Texas Instruments
U4	1		Automotive, 1.65V to 5V parallel-load eight-channel shift register with logic level shifter 16-WQFN -40 to 125	WQFN16	CLV8T165QWBQBRQ1	Texas Instruments
U5	1		Low-Capacitance 6-Channel +/-15 kV ESD Protection Array for High-Speed Data Interfaces, RSE0008A (UQFN-8)	RSE0008A	TPD6E004RSER	Texas Instruments
U8, U9	2		Low-power, 24-Bit, 8-Channel, 64-kSPS, Delta-Sigma ADC with SPI, PGA, and Voltage Reference	WQFN16	ADS122S14RTE	Texas Instruments
C9	0	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 10%, X7R, 0603	603	C0603C104K3RACTU	Kemet
C10	0	1uF	CAP, CERM, 1 µF, 25V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	CGA3E1X7R1E105K080AC	TDK
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J7	0		Header, 100mil, 1x1, Gold, TH	Header, 1x1, 2.54mm, TH	HTSW-101-09G-S	Samtec
R9, R23, R25	0	0	RES, 0, 5%, 0.1W, 0603	603	RC0603JR-070RL	Yageo
R27	0	10.0k	RES, 10.0k, 1%, 0.1W, 0603	603	RC0603FR-0710KL	Yageo
R35	0	47	RES, 47, 5%, 0.1W, AEC-Q200 Grade 0, 0603	603	CRCW060347R0JNEA	Vishay-Dale

8 Compliance Information

Compliance and Certifications

REACH, RoHS, CE, ANSI, IEC, UL, ISO, and so on

9 References

Table 9-1 shows the related documentation from Texas Instruments.

Table 9-1. Related Documentation

Document	Literature Number
ADS122S14 product data sheet	SBASAI9
MSPM0G1507 product data sheet	SLASEW9E

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

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   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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