EVM User's Guide: TMUX48XXDSGDDF-EVM

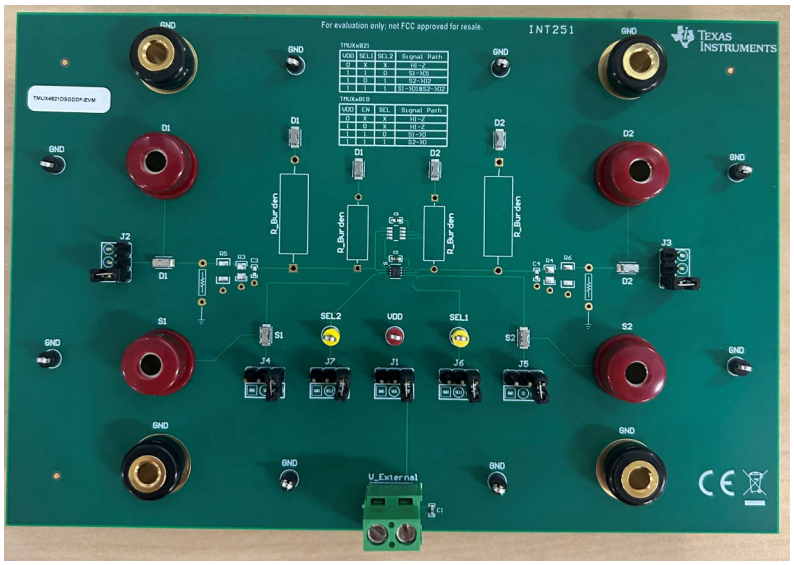
TMUX48XX Evaluation Module

Description

The TMUX48XXDSGDDF-EVM is used to evaluate the performance of the TMUX4821 and TMUX4819. The evaluation module (EVM) comes with a soldered TMUX4821. The EVM allows for an easy way for engineers to evaluate the TMUX4821 and TMUX4819 low Ron and ΔRon capabilities. The EVM has multiple resistor footprints that can be populated to test how the device affects the total resistance on the signal lane. Additionally, the EVM includes multiple test points and banana jack plug-ins to allow high current signals to be applied on the mux.

Features

- External power supply with decoupling capacitor from V_External to ground (1µF 0402)
- One power supply decoupling capacitor from VDD to ground (0.1µF 0402)
- Eight test points on I/Os supporting TMUX4821 and TMUX4819 full current and voltage capabilities
- Eight additional GND test points for ease of probing
- Four banana jack plug-ins on I/Os supporting TMUX4821 and TMUX4819 full current and voltage capabilities
- Four additional GND banana jack plus-ins



TMUX48XXDSGDDF-EVM (Top View)

1 Evaluation Module Overview

1.1 Introduction

This user's guide describes the TMUX48XXDSGDDF-EVM evaluation module (EVM) and the intended use. This board allows for the quick prototyping and characterization of TI's TMUX4821 and TMUX4819 multiplexers in DSG and DDF packages. This EVM allows for evaluation of the device impact on the total resistance on the signal path.

The following is continuation of the features list:

- One 3-pin header for connecting or disconnecting device from external power
- Two 3-pin headers for controlling the logic of the device
- Four 3-pin headers to change signal path state of device
- Multiple unpopulated footprints for potential additional RC loads
- Multiple through holes for mounting resistors

CAUTION

The EVM comes with jumpers populating the headers shorting the pins to ground. Make sure before first usage you are aware about the state of the pins and change them according to your application. Failing to do so risks the reliability of the device and EVM.

1.2 Kit Contents

The EVM kit includes the following :

- (1) TMUX48XXDSGDDF-EVM

1.3 Specification

The TMUX48XXDSGDDF-EVM is used for evaluating TMUX4821 and TMUX4819. The EVM has seven 3-pin headers; four headers for tying the I/Os to the voltage supply level, or to connect them to ground. Two headers for toggling the SEL pins to switch control the signal path routing of the device. The last 3-pin header allows for the VDD supply to be connected to an external source, to the board ground or left floating.

The EVM has test points on each I/O for a total of eight test points that are rated up to 2A to support testing the TMUX4821 and TMUX4819 at the fullest current carrying capabilities. Four of these test points are directly routed to the I/Os. The other four are routed to the unpopulated burden resistance that can be implemented for resistance testing. These are located above the burden resistor and routed to the upper lead. Make sure you connect these test point to ground to test the voltage across the burden resistors. Eight extra ground test points are provided to allow for more connection flexibility on the board.

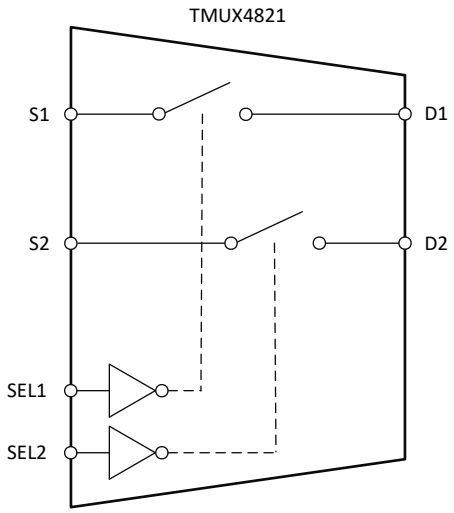


Figure 1-1. TMUX4821 Simplified Circuit

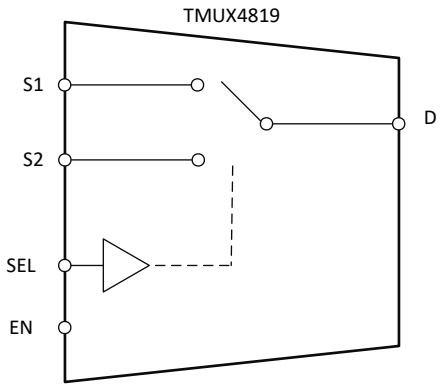


Figure 1-2. TMUX4819 Simplified Circuit

1.4 Device Information

The TMUX4821 and TMUX4819 are complementary metal-oxide semiconductor (CMOS) multiplexers. The TMUX4821 has two independently selectable, single-pole, single-throw (SPST) switch channels. The TMUX4819 has one single-pole, double-throw (SPDT) channel. The devices work with a single supply (1.8V to 5.5V), but can pass bidirectional analog and digital signals beyond the supply from -15V to 15V.

The devices also features powered off protection up to ±15V, which isolates the Dx from a voltage on the Sx even when there is no supply voltage present (VDD = 0V). Without this protection feature, any voltage on the switch can back-power the supply rail through an internal ESD diode and cause potential damage to the rest of the system.

With 1mΩ RON-flatness, the TMUX4821 and TMUX4819 are excellent choices for passing signals without adding distortion.

2 Hardware

2.1 Power Requirements

TMUX48XXDSGDDF-EVM requires a 1.8V to 5.5V supply provided either through the J1 terminal from the V-External, or directly hooked to the red VDD test point to provide a passive signal pathway between the Sx and Dx pins in according to the logic selected. Note, facing up and straight the V-External connections are GND is the left terminal VDD is the right one.

2.2 Header and Jumper Information

The TMUX48XXDSGDDF-EVM has seven 3-pin headers to control the power supply connection, the control inputs, the sources and drains. The following is a description of each header.

1. **Supply Header J1**

   Header J1 connects the VDD pin to either the external power or to ground via a jumper. If Header J1 is not connected, then the devices supply is left floating. Figure 2-1 shows header J1.

   a. To connect to the external supply, short the J1-2 location on the header to J1-3. The V_EXT terminal is now supplying the device power.
   b. To connect to ground, short the J1-2 location on the header to J1-1. The device supply pin is now grounded.
   c. To leave the device supply pin floating, leave J1-2 unconnected and floating.

2. **Control Header J6**

   Header J6 connects the SEL1 pin to either VDD or ground by a jumper. If Header J6 is not connected, then the devices SEL1 pin is left floating.

   a. To connect to VDD, short the J6-2 location on the header to J6-3. VDD is now connected to the devices SEL1 pin.
   b. To connect to ground, GND, short the J6-2 location on the header to J6-1. The device SEL1 pin is now grounded.
   c. Leaving J6-2 unconnected leaves the SEL1 pin floating. Doing this is not recommended as the device is in an unknown state.

3. **Control Header J7**

   Header J7 connects the SEL2 pin to either VDD or ground via a jumper. If Header J7 is not connected, then the devices SEL2 pin is left floating.

   a. To connect to VDD, short the J7-2 location on the header to J7-3. VDD is now connected to the devices SEL2 pin.
   b. To connect to ground, GND, short the J7-2 location on the header to J7-1. The device SEL2 pin is now grounded.
   c. Leaving J7-2 unconnected leaves the SEL2 pin floating. Doing this is not recommended as the device is in an unknown state.

4. **Drain Header J2**

   Header J2 connects the D1 pin to either VDD or ground by a jumper. If Header J2 is not connected, then the devices D1 pin is left floating.

   a. To connect to VDD, short the J2-2 location on the header to J2-1. VDD is now connected to the devices D1 pin.
   b. To connect to ground, GND, short the J2-2 location on the header to J2-3. The device D1 pin is now grounded.
   c. Leaving J2-2 unconnected leaves the D1 pin floating.

5. **Drain Header J3**

   Header J3 connects the D2 pin to either VDD or ground via a jumper. If Header J3 is not connected, then the devices D2 pin is left floating.

   a. To connect to VDD, short the J3-2 location on the header to J3-1. VDD is now connected to the devices D2 pin.
   b. To connect to ground, GND, short the J3-2 location on the header to J3-3. The device D2 pin is now grounded.
   c. Leaving J3-2 unconnected leaves the D2 pin floating.

6. **Source Header J4**

   Header J4 connects the S1 pin to either VDD or ground by a jumper. If Header J4 is not connected, then the devices S1 pin is left floating.

   a. To connect to VDD, short the J4-2 location on the header to J4-3. VDD is now connected to the devices S1 pin.
   b. To connect to ground, GND, short the J4-2 location on the header to J4-1. The device S1 pin is now grounded.
   c. Leaving J4-2 unconnected leaves the S1 pin floating.

7. **Source Header J5**

   Header J5 connects the S2 pin to either VDD or ground by a jumper. If Header J5 is not connected, then the devices S2 pin is left floating.

   a. To connect to VDD, short the J5-2 location on the header to J5-3. VDD is now connected to the devices S2 pin.
   b. To connect to ground, GND, short the J5-2 location on the header to J5-1. The device S2 pin is now grounded.
   c. Leaving J5-2 unconnected leaves the S2 pin floating.

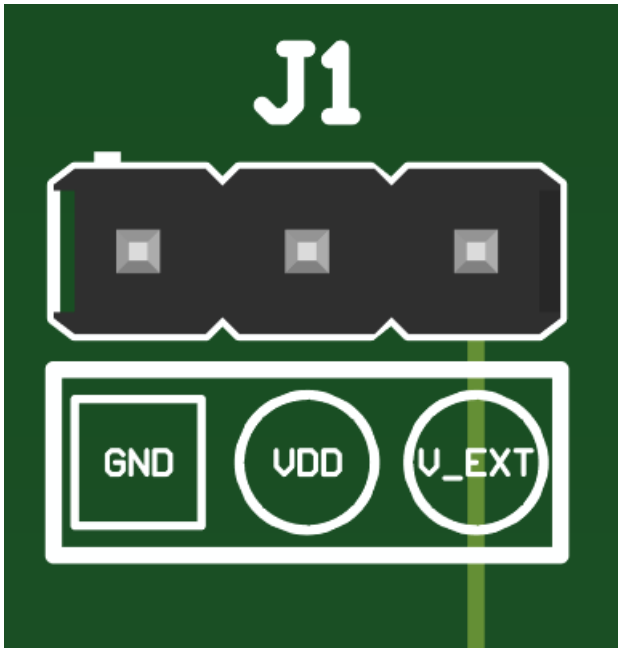


Figure 2-1. Header J1 : J1-1(GND), J1-2(Connection to device VDD), J1-3 (V_EXT)

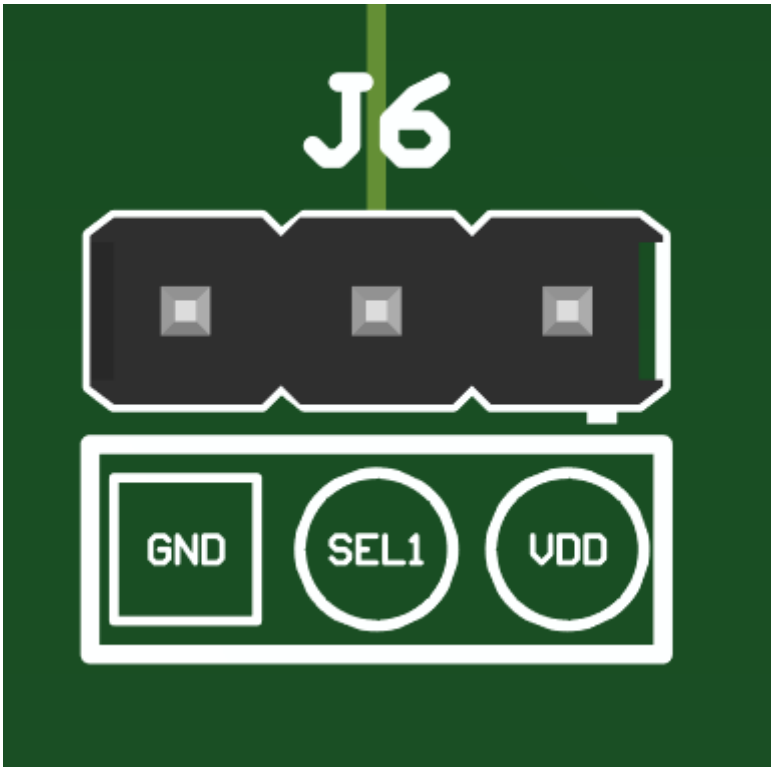


Figure 2-2. Header J6 : J6-1(GND), J6-2(Connection to device SEL1), J6-3 (VDD)

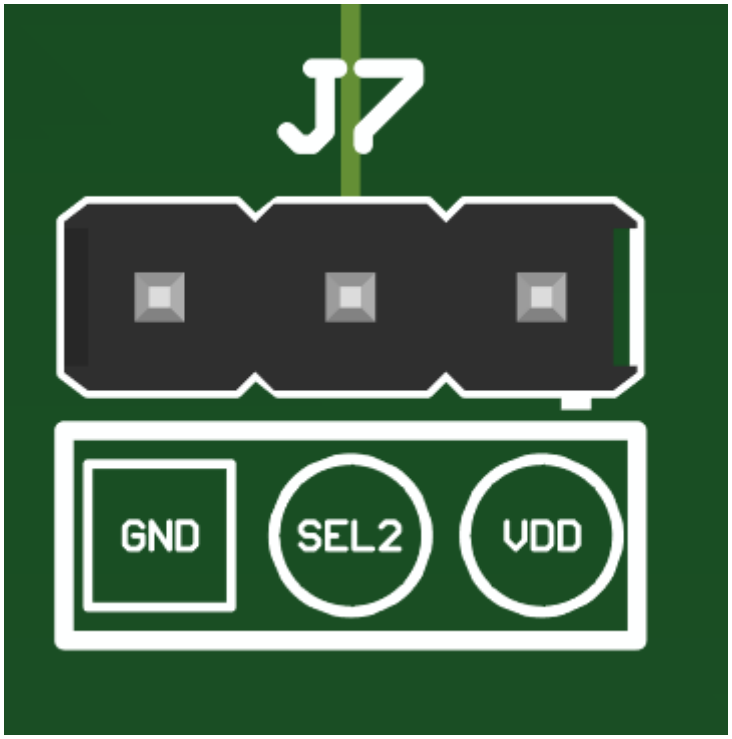


Figure 2-3. Header J7 : J7-1(GND), J7-2(Connection to device SEL2), J7-3 (VDD)

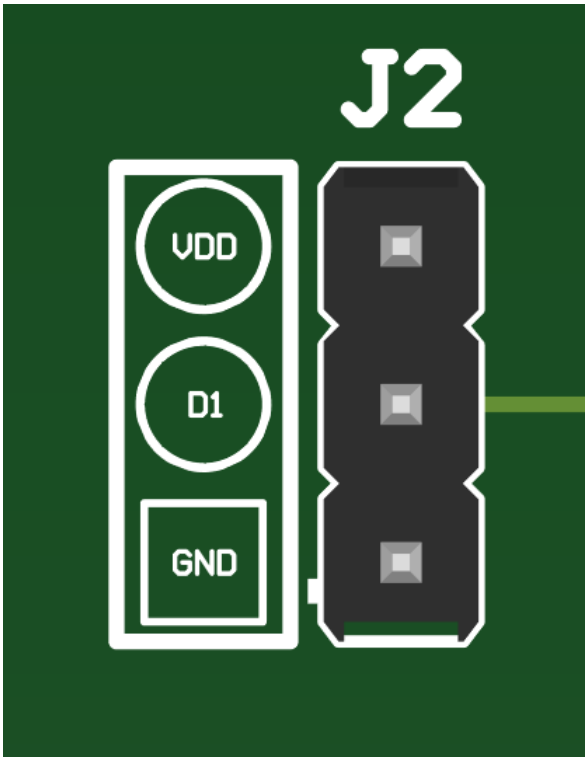


Figure 2-4. Header J2 : J2-1(VDD), J2-2(Connection to device D1), J2-3 (GND)

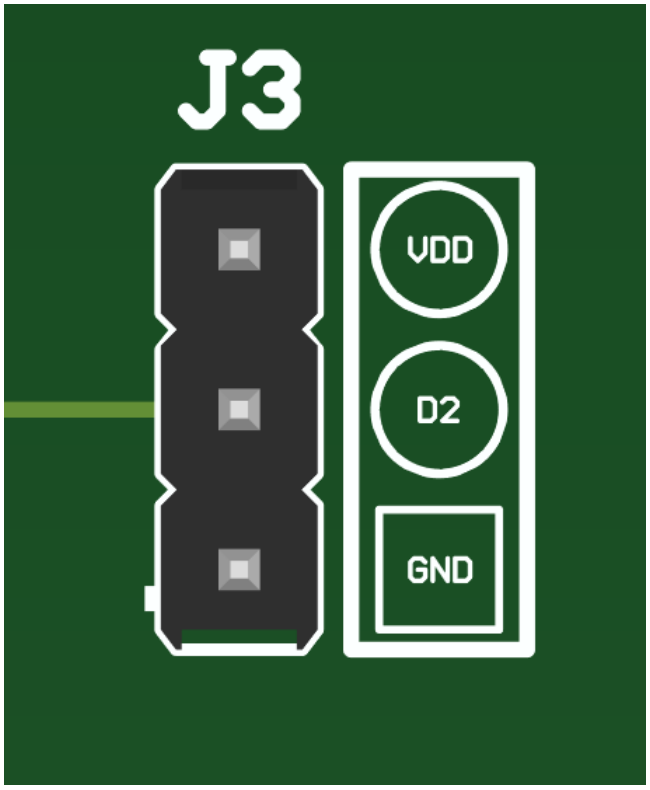


Figure 2-5. Header J3 : J3-1(VDD), J3-2(Connection to device D2), J3-3 (GND)

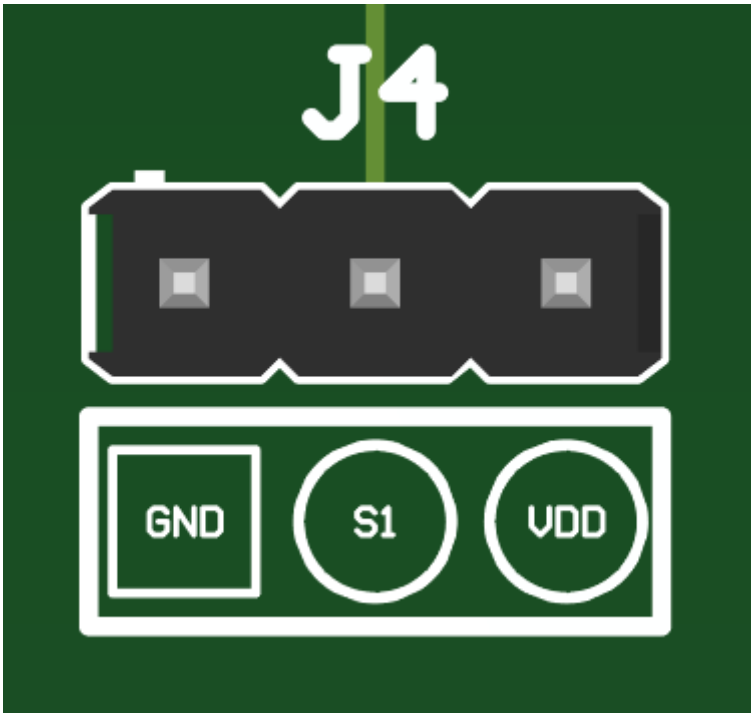


Figure 2-6. Header J4 : J4-1(GND), J4-2(Connection to device S1), J4-3 (VDD)

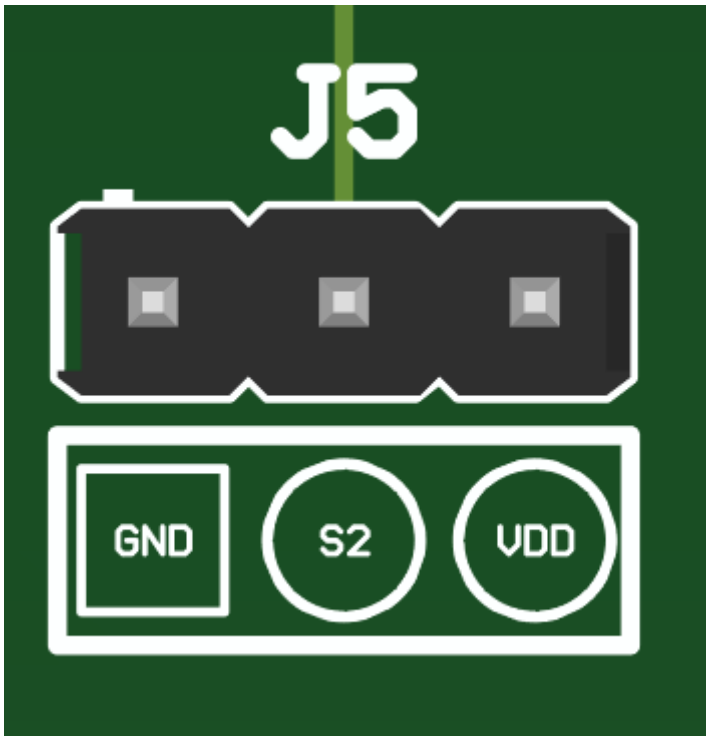


Figure 2-7. Header J5 : J5-1(GND), J5-2(Connection to device S2), J5-3 (VDD)

The logic headers J6(SEL1) and J7(SEL2) can be used to control both the TMUX4821 and TMUX4819. The TMUX4819 has an EN pin which can be controlled by SEL2 and the SEL pin to be controlled by SEL1.

TMUXx821

VDD	SEL1	SEL2	Signal Path
0	X	X	HI-Z
1	1	0	S1->D1
1	0	1	S2->D2
1	1	1	S1->D1&S2->D2

Figure 2-8. TMUX48XXDSGDDF-EVM TMUX4821 Truth Table

TMUXx819

VDD	EN	SEL	Signal Path
0	X	X	HI-Z
1	0	X	HI-Z
1	1	0	S1->D
1	1	1	S2->D

Figure 2-9. TMUX48XXDSGDDF-EVM TMUX4819 Truth Table

2.3 Test Points

The board has a total of 19 test points. 8 GND, 2 SEL, 1 VDD, and 8 I/O.

Test Point ID	Description	Signal
S1	Surface Mount	S1
S2	Surface Mount	S2
D1	Surface Mount	D1
D1	Surface Mount	D1
D1	Surface Mount	D1
D2	Surface Mount	D2
D2	Surface Mount	D2
D2	Surface Mount	D2
VDD	Red	VDD
SEL1	Yellow	SEL1/SEL
SEL2	Yellow	SEL2/EN
GND	Black	GND
GND	Black	GND
GND	Black	GND
GND	Black	GND
GND	Black	GND
GND	Black	GND
GND	Black	GND
GND	Black	GND

3 Hardware Design Files

The following section includes hardware design files for TMUX48XXDSGDDF-EVM . This section includes the board level schematic, PCB layout and Bill of materials (BOM).

3.1 Schematics

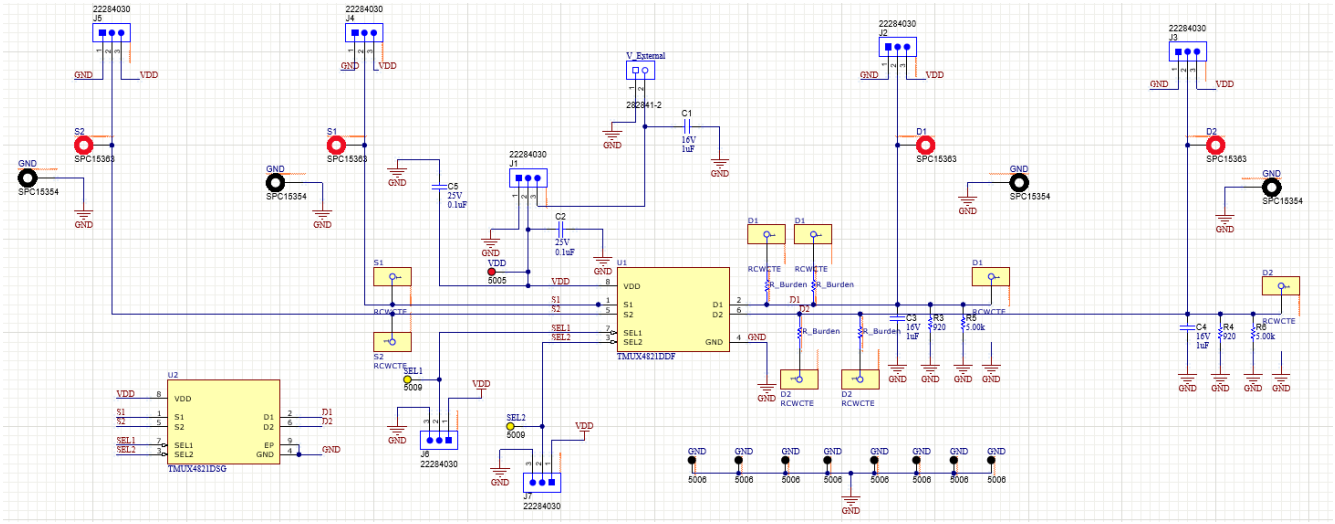


Figure 3-1. TMUX48XXDSGDDF-EVM Schematic

3.2 PCB Layouts

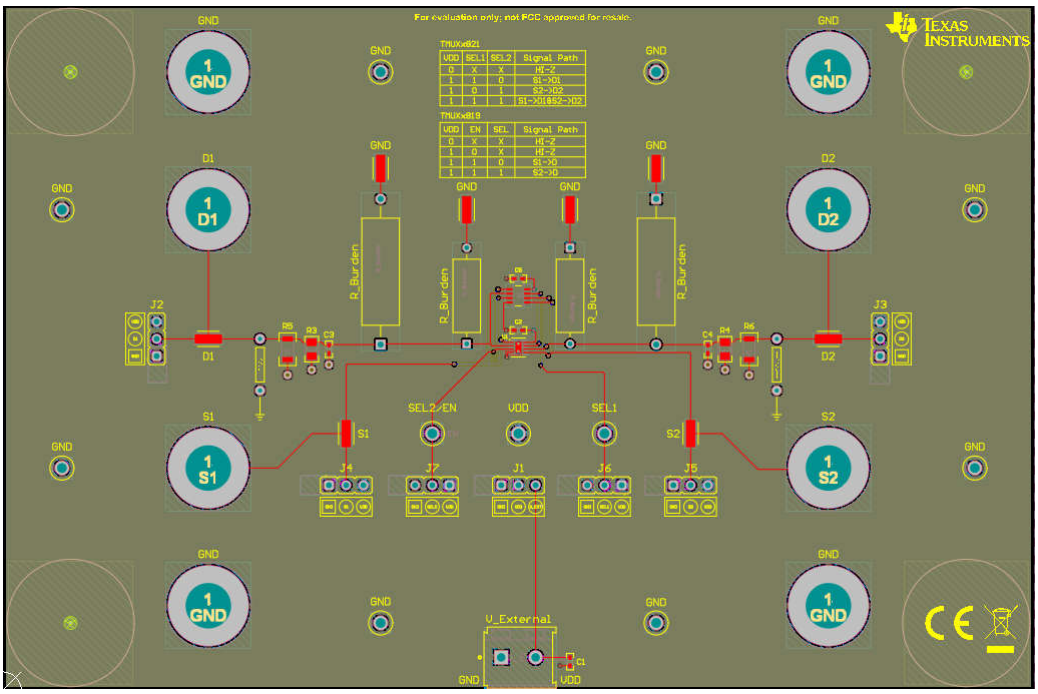


Figure 3-2. TMUX48XXDSGDDF-EVM Top Layer Layout

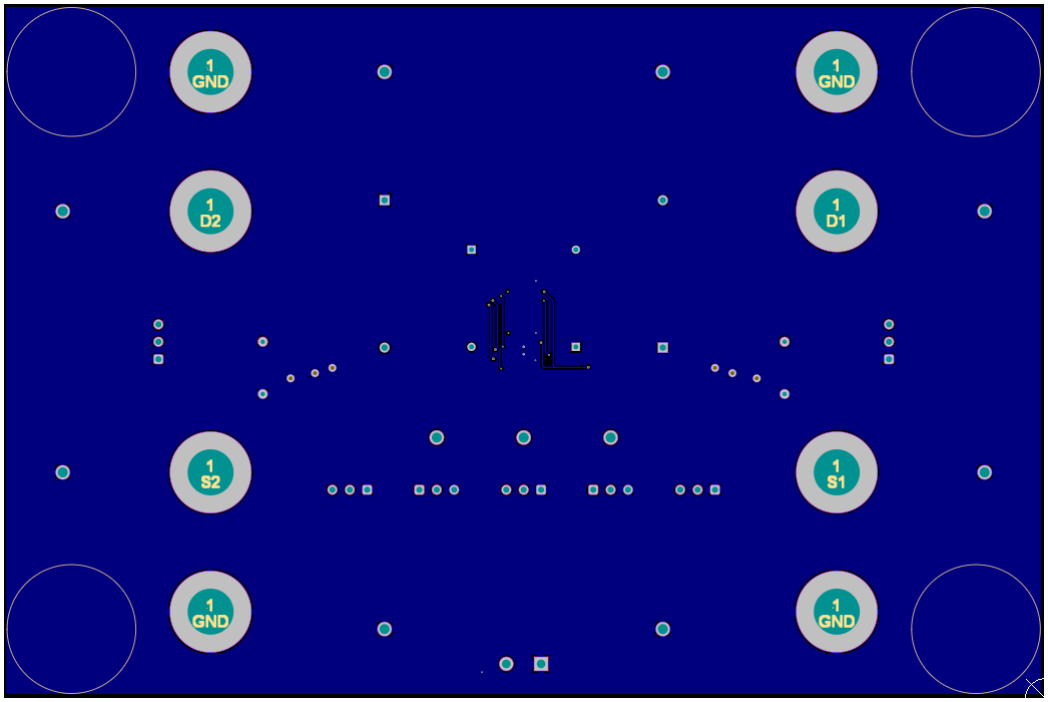


Figure 3-3. TMUX48XXDSGDDF-EVM Bottom Layer Layout

3.3 Bill of Materials (BOM)

Table 3-1. Bill of Materials

Designator	Qty	Value	Description	Manufacturer	Part Number
C1	1	1uF	CAP, CERM, 1uF, 16V, +/- 10%, X5R, 0402	Taiyo Yuden	EMK105BJ105KVHF
C2	1	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 10%, X5R, 0402	MuRata	GRM155R61E104KA87D
S1, S2, D1, D2	4		BANANA JACK, SOLDER LUG, RED, TH	Tenma	GSPC15363
S1, S2, D1, D2	8		PC Test Point Plating Surface Mount Mounting Type	KOA Speer	RCWCTE
GND	4		BANANA JACK, SOLDER LUG, BLACK, TH	Tenma	SPC15354
GND	8		Test Point, Compact, Black, TH	Keystone	5006
J1, J2, J3, J4, J5, J6, J7	7		CONN JUMPER S2 (1 x 2) Position Shunt Connector Black Open Top 0.100" (2.54mm) GoldHORTING .100" GOLD	Sullins	QPC02SXGN-RC
J1, J2, J3, J4, J5, J6, J7	7		Header, 2.54mm, 3x1, Tin, TH	Molex	22284030
P1, P2, P3, P4	4		Bumper Cylindrical, Dome 0.720" Dia (18.30mm) Polyurethane Black	Essentra Components	RBS-37BK
SEL1, SEL2	2		Test Point, Compact, Yellow, TH	Keystone Electronics	5009
TMUX48XX-DSG-DDF-EVM	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10
U2	1		TMUX4821	Texas Instruments	TMUX4821DSG
V_External	1		Terminal Block, 2x1, 5.08mm, TH	TE Connectivity	282841-2
VDD	1		Test Point, Compact, Red, TH	Keystone Electronics	5005
C3, C4	0	1uF	CAP, CERM, 1uF, 16V, +/- 10%, X5R, 0402	Taiyo Yuden	EMK105BJ105KVHF
C5	0	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 10%, X5R, 0402	MuRata	GRM155R61E104KA87D
R3, R4	0	920Ω	RES, 920, 0.1%, 0.125 W, 0805	Yageo America	RT0805BRD07920RL
R5, R6	0	5kΩ	RES, 5.00 k, 0.1%, 0.25 W, 1206	State of the Art	D55342E07B05B0TTR
R_Burden	0	250Ω	250 Ohms ±0.1% 1W Through Hole Resistor Axial Flame Retardant Coating, Moisture Resistant, Safety Metal Film	Vishay	CMF60250R00BHEB
R_Burden	0	45Ω	Res Wirewound 45 Ohm 1% 3W ±20ppm/°C Ceramic Hi Temp Sil AXL Thru-Hole Bulk	Vishay	RS02B45R00FE12
U1	0		TMUX4821	Texas Instruments	TMUX4821DDF

4 Additional Information

4.1 Trademarks

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