

Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
A	N/A	6/4/2026	SD	Revision A

A

B

C

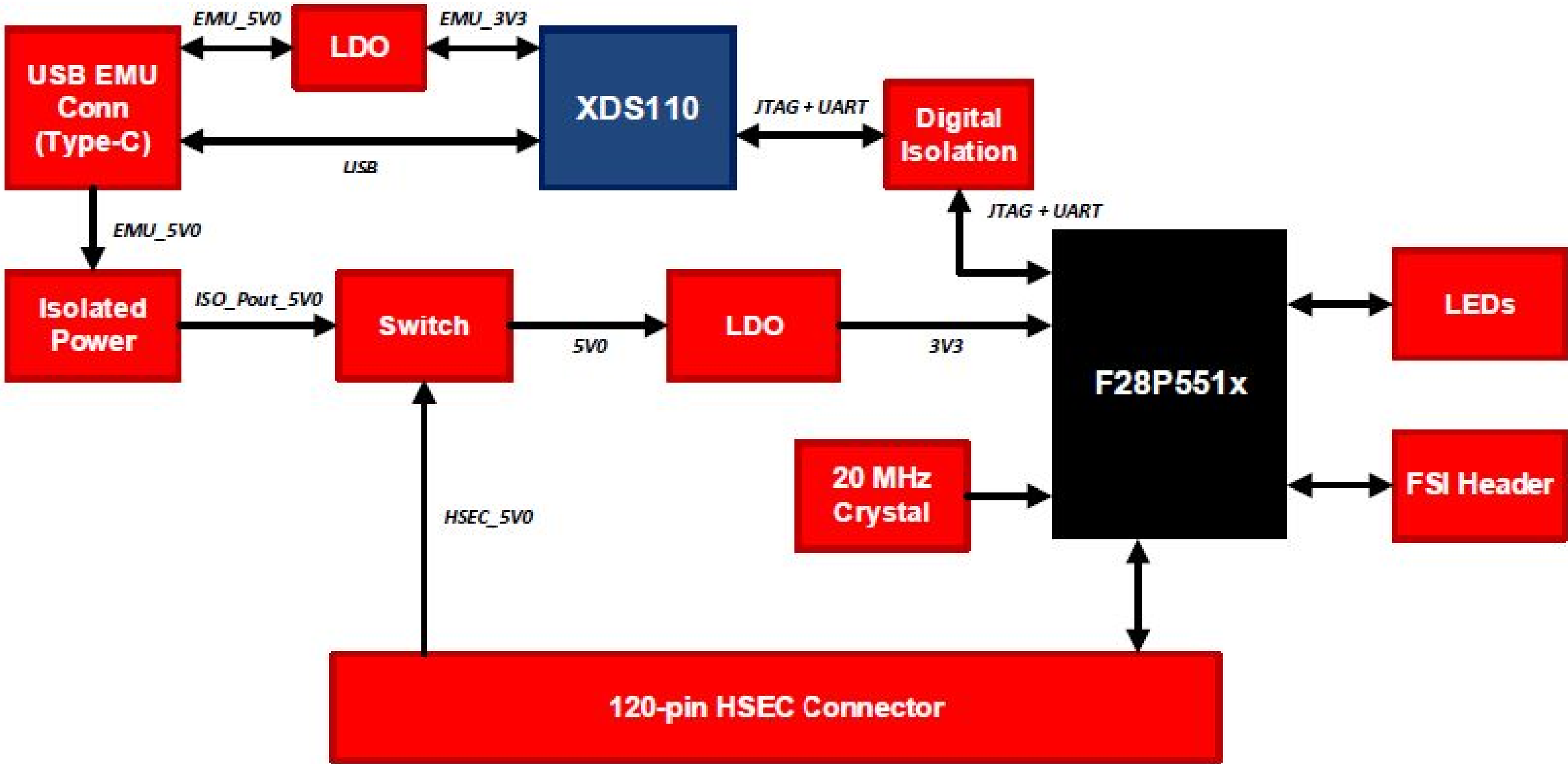
D

A

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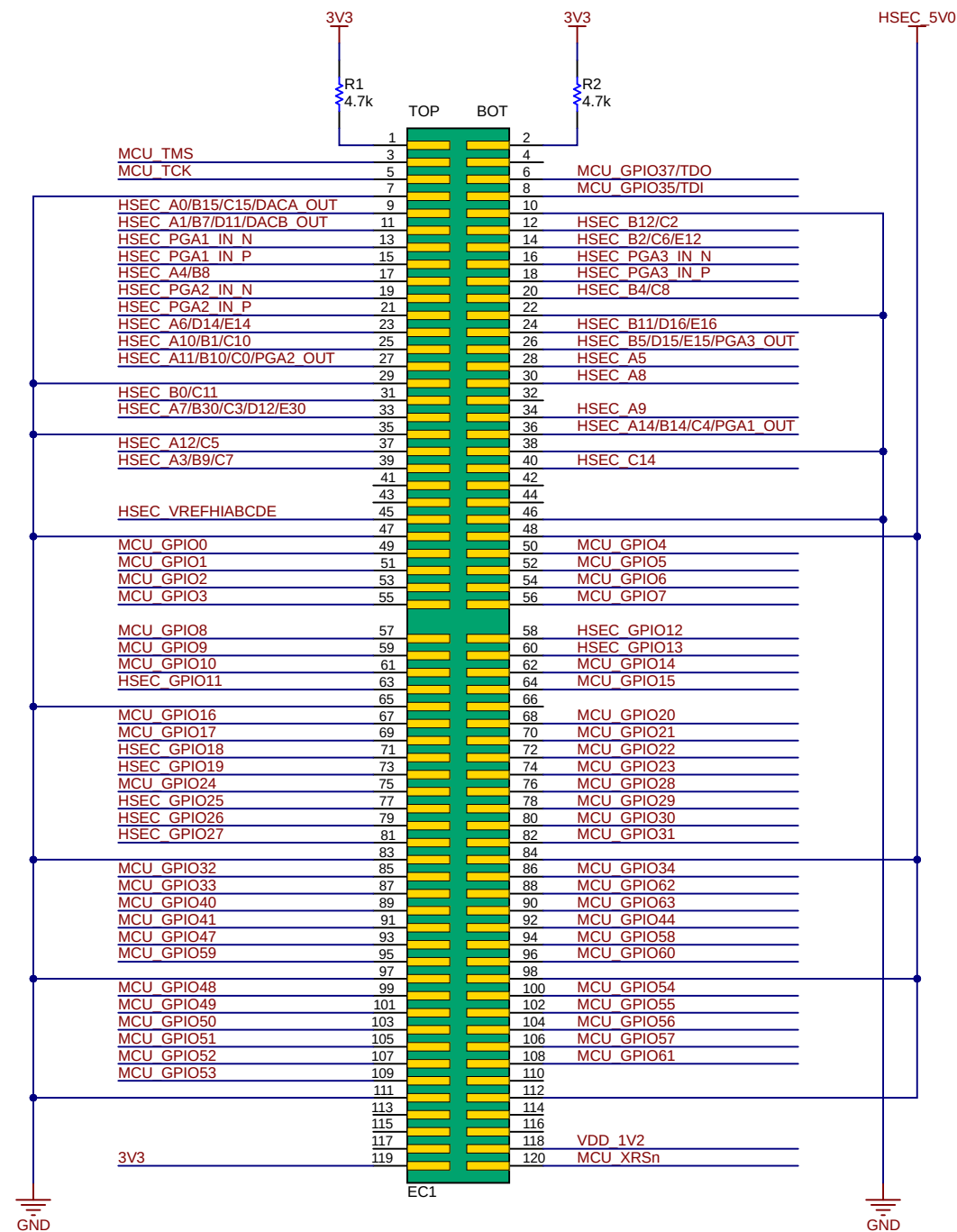
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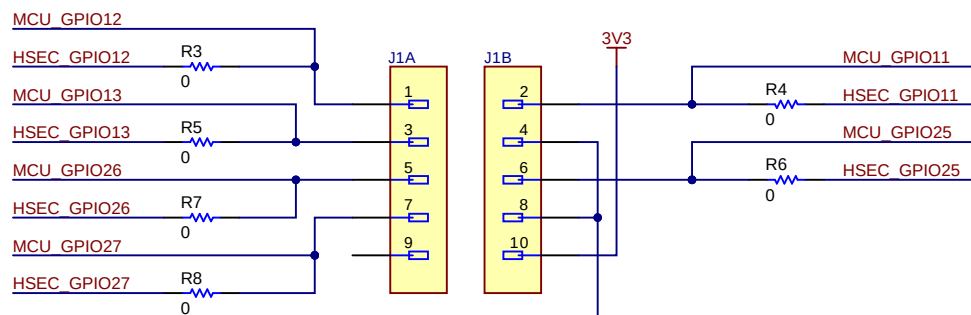


Power to the MCU is either supported by the USB-C on the left or through the HSEC

J1 has been updated over previous designs. Pins 9 and 10 were added enabling power to the connector. Additionally Pins 2 and 6, previously GND, have been repurposed to enable the full 3 pin FSI communication. The user can shunt HSEC GPIO11 and HSEC GPIO25 to ground if backwards compatibility is required.

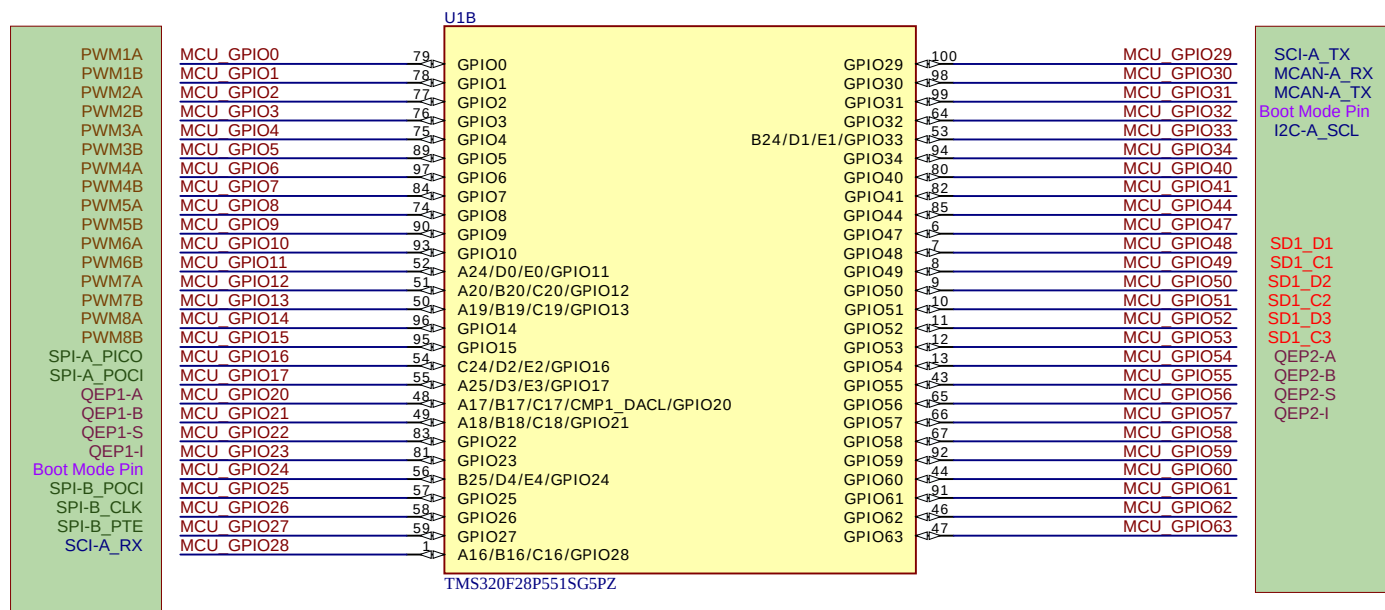


10-pin FSI Connector



1	FSI-RX0	2	FSI-RX1/GND
3	FSI-RXCLK	4	GND
5	FSI-TX0	6	FSI-TX1/GND
7	FSI-TXCLK	8	GND
9	KEY	10	3V3

Pin 9 of J1 is cutoff to key the connector

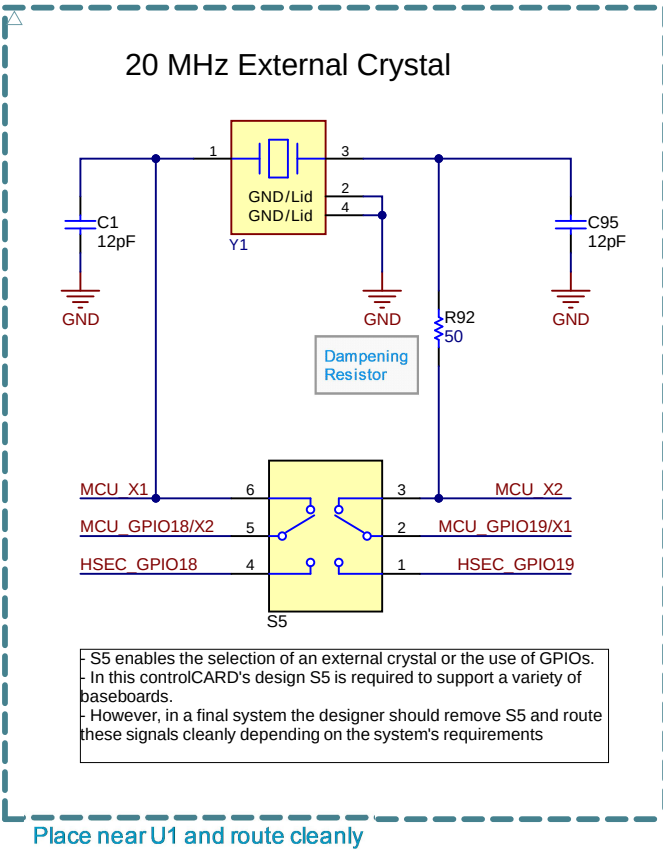
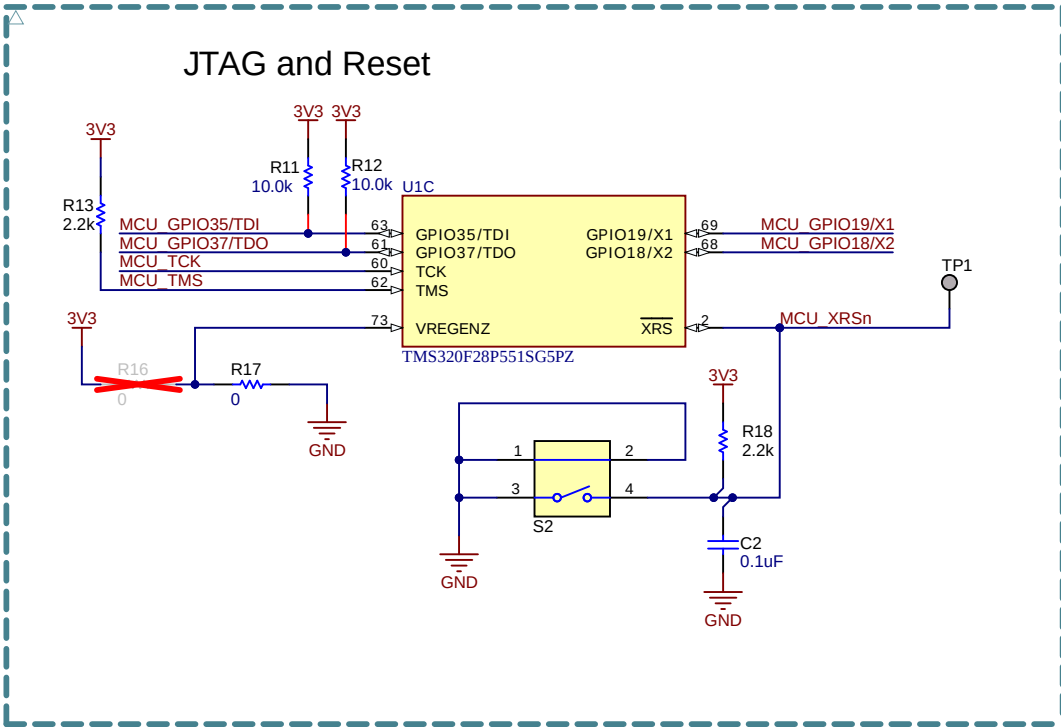


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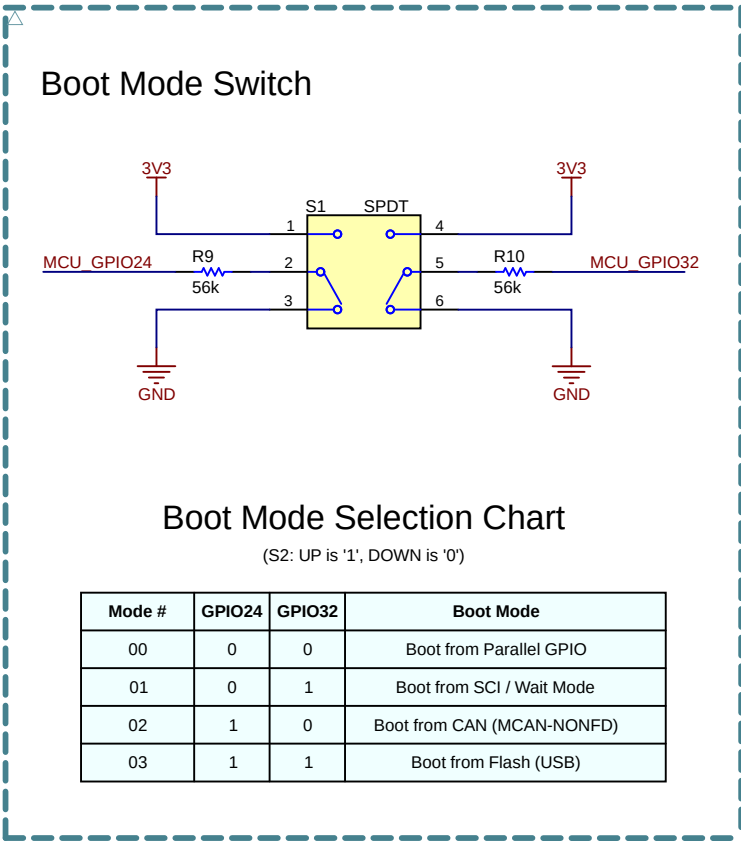
B

A

B



Place near U1 and route cleanly

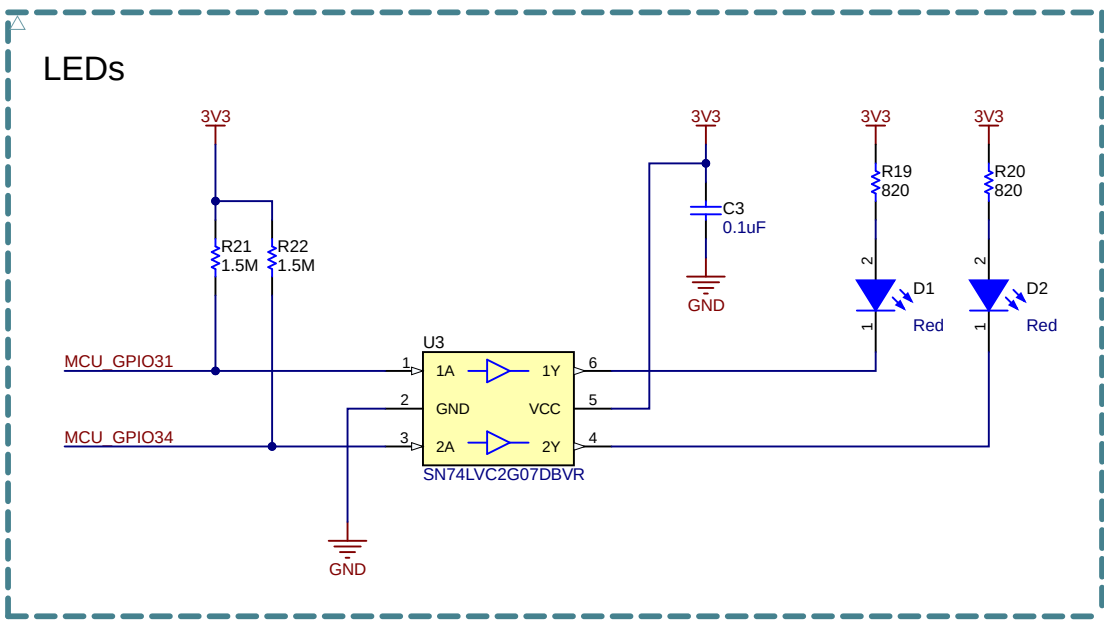
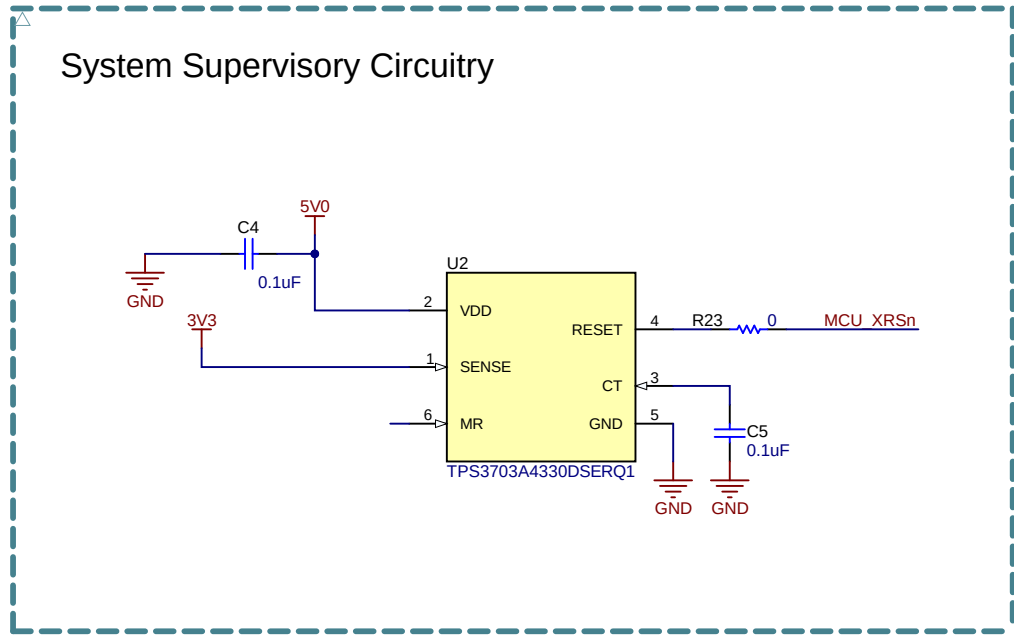


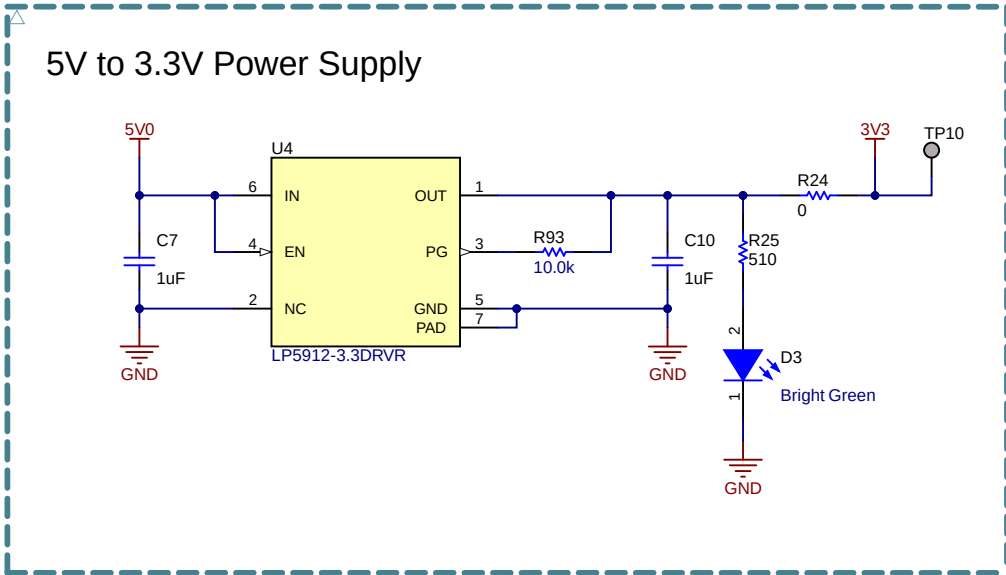
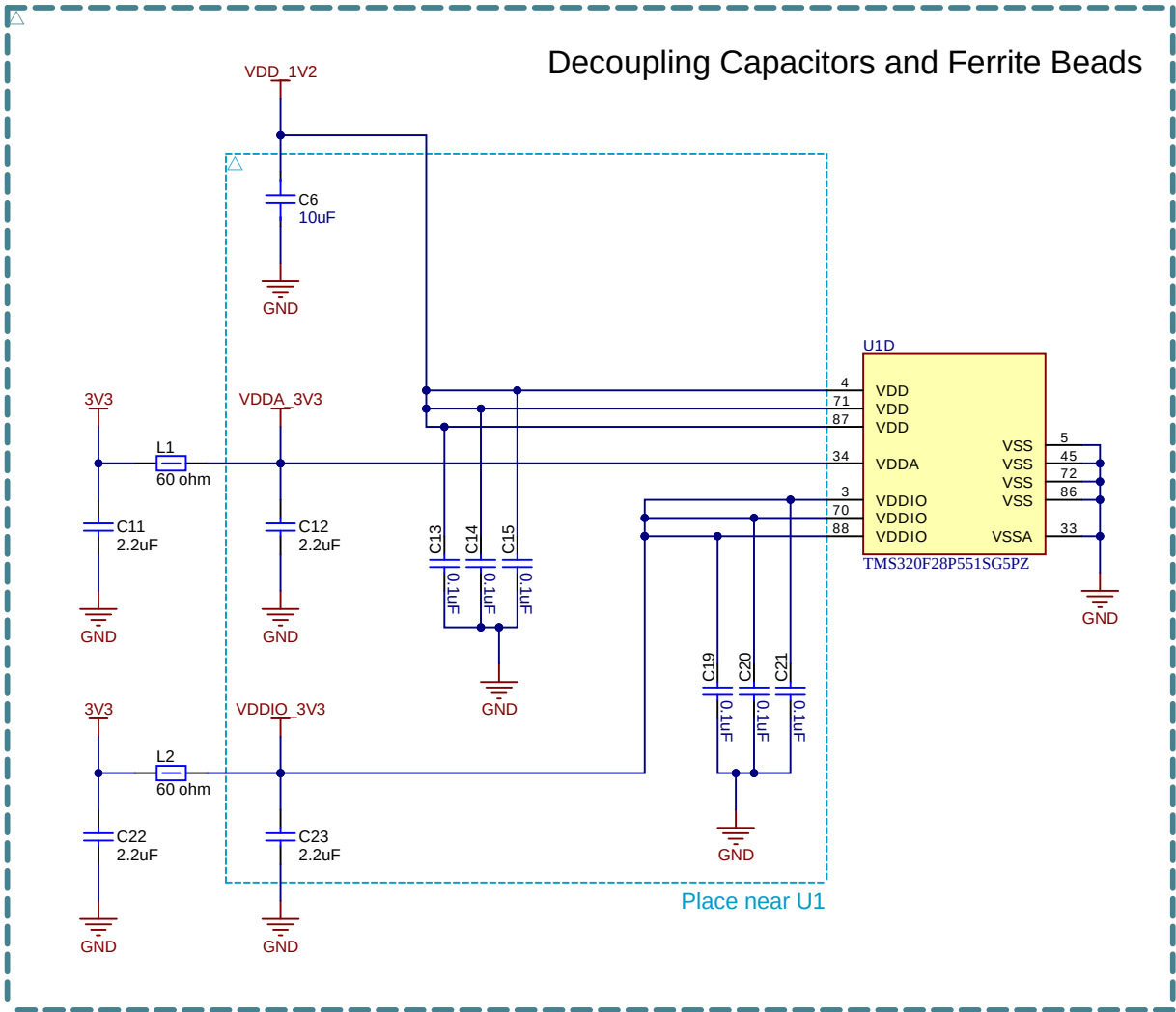
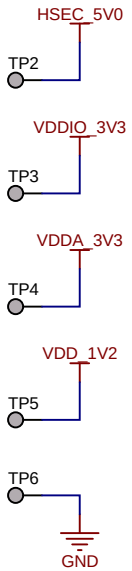
C

C

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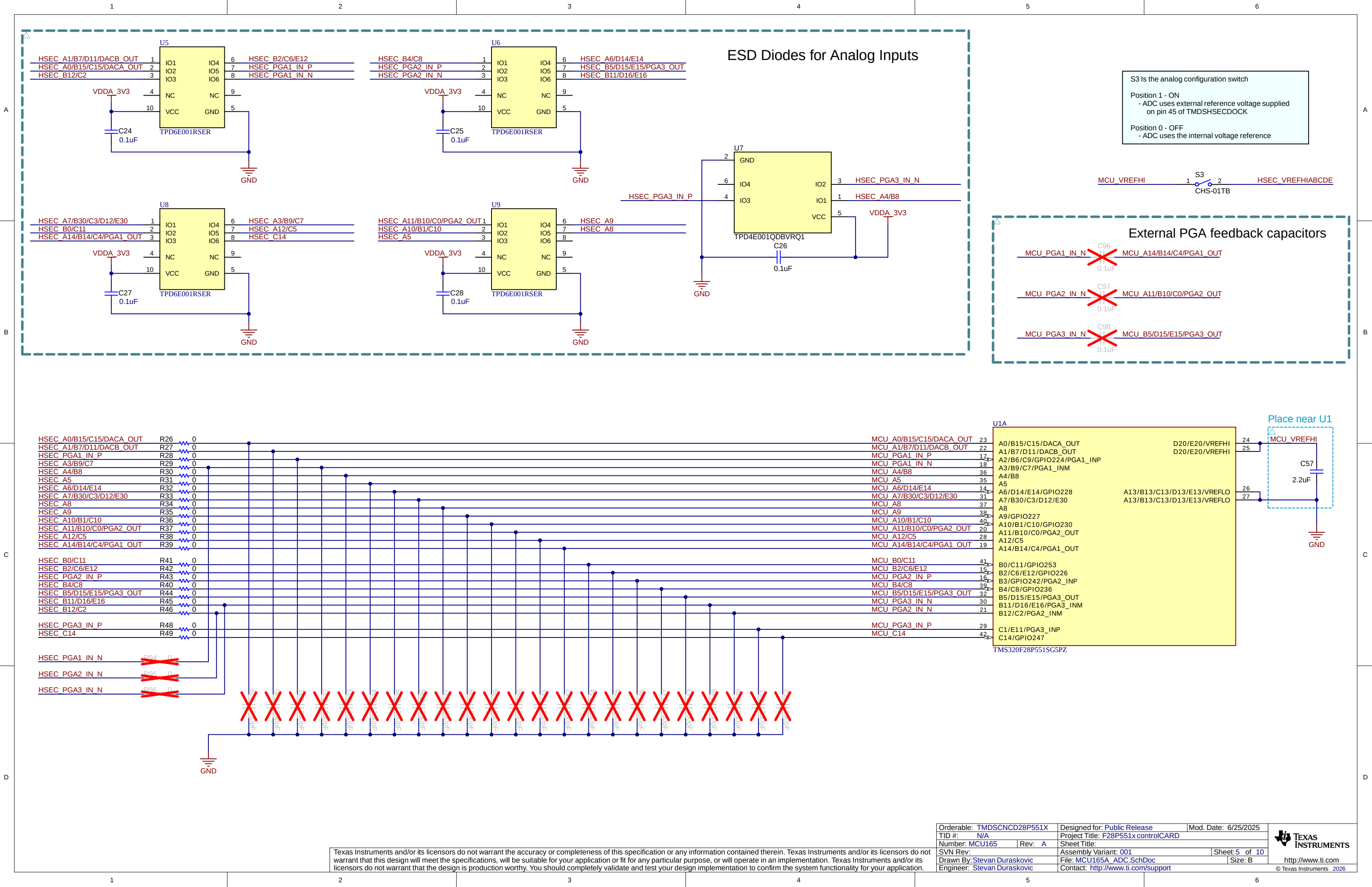
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The F28P551x controlCARD uses the internal VREG to generate the 1.25V voltage rail for VDD.

For custom boards using external VREG mode, recommend to use LDO (e.g., TPS745-Q1) to generate both 3.3V and 1.25V supplies.



ESD Diodes for Analog Inputs

S3 is the analog configuration switch

Position 1 - ON
- ADC uses external reference voltage supplied on pin 45 of TMDSHSECDCK

Position 0 - OFF
- ADC uses the internal voltage reference

External PGA feedback capacitors

Place near U1

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Orderable: TMDSCNCD28P551X	Designed for: Public Release	Mod. Date: 6/25/2025
TID #: N/A	Project Title: F28P551x controlCARD	
Number: MCU165	Rev: A	Sheet Title:
SVN Rev:	Assembly Variant: 001	Sheet: 5 of 10
Drawn By: Stevan Duraskovic	File: MCU165A_ADC.SchDoc	Size: B
Engineer: Stevan Duraskovic	Contact: http://www.ti.com/support	

USB Type-C Connector - XDS110 side

USB Type-C Connector - XDS110 side

EMU_5V0

J3

A4 VBUS B4 VBUS

A9 VBUS B9 VBUS

A7 DN1 B7 XDS_D N

A6 DP1 B6 XDS_D P

A3 SSTXN1 B3

A2 SSTXP1 B2

A10 SSRXN2 B10

A11 SSRXP2 B11

A5 CC1 B5 XDS_CC2

A8 SBU1 B8

A1 GND B1

A12 GND B12

M1 GND M2

S1 Shield S4

S2 Shield S3

632723300011

R65 5.1k

EMU_GND

R62 1.00M

C62 3.3nF

EMU_GND

R64 5.1k

EMU_GND

U13

1 D1+ 10 XDS_D P

2 D1- 9 XDS_D N

3 GND GND 8

4 XDS_CC1 7 XDS_CC1

5 XDS_CC2 6 XDS_CC2

TPD4E05U06DQAR

The schematic diagram, titled "USB Isolated Power", illustrates the power supply for a USB device. It features a USB Type-A connector (U1) on the left, which provides 5V and GND pins. The 5V pin is connected to a 0.1µF capacitor (C64) and a 0Ω resistor (R63). The GND pin is connected to the EMU_GND. The 5V line passes through a 10µF capacitor (C63) and a transformer (T1, 750315371) before reaching the VCC pin (pin 2) of the SN6505BDBVR (U12). The EN pin (pin 5) is connected to the 5V line, and the CLK pin (pin 6) is connected to GND. The transformer's secondary winding (pins 1, 2, 3, 4) is connected to the D1 and D2 pins of U12. The D1 pin (pin 1) is connected to the 5V line, and the D2 pin (pin 3) is connected to GND. The output of the transformer (pins 5, 6) is connected to the ISO_Pout_5V0 pin. The output line includes a 0.1µF capacitor (C65), a 10µF capacitor (C66), and a 0.1µF capacitor (C67) connected to GND. The output is labeled ISO_Pout_5V0.

Power Selection Switch

The diagram illustrates a Power Selection Switch circuit using the TPS2113ADRBR IC. The circuit selects between two 5V0 power sources: HSEC_5V0 and ISO_Pout_5V0. The selection is based on the voltage levels of these sources. The circuit includes various components such as resistors (R66, R67, R68, R69, R70, R71, R72, R73, R74), capacitors (C69, C70, C71, C68), and a red LED (D6) for status indication. The output of the switch is labeled POWER_SWITCH_OUT.

HSEC_5V0 > 4V	ISO_Pout_5V0 > HSEC_5V0	POWER_SWITCH_OUT
Yes	X	HSEC_5V0
No	No	HSEC_5V0
No	Yes	ISO_Pout_5V0

HSEC_5V0 > 4V	ISO_Pout_5V0 > HSEC_5V0	POWER_SWITCH_OUT
Yes	X	HSEC_5V0
No	No	HSEC_5V0
No	Yes	ISO_Pout_5V0

A

B

C

D

A

B

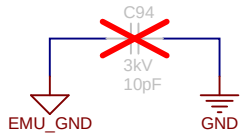
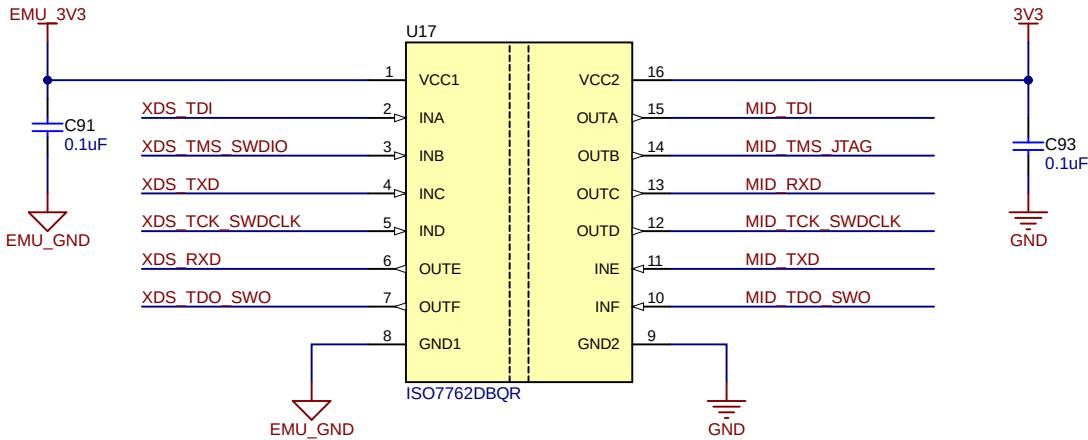
C

D

NOTE: Because the JTAG signals are isolated, cJTAG is not supported on this controlCARD.

(Cold Side)

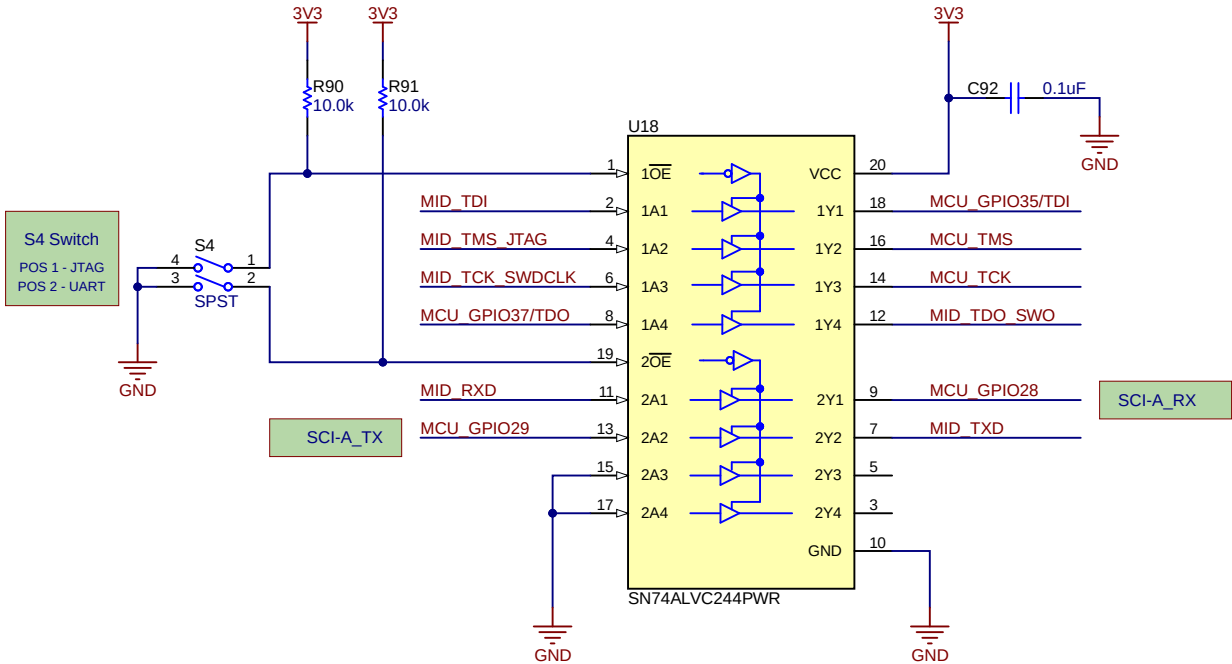
(Hot Side)



WARNING: To avoid potential shock hazard in high-voltage settings, leave the Y cap (C94) unpopulated from the EVM.

S4 - JTAG Emulation & UART Switch

POS 1 ON: Use XDS110 emulator that is on the cCARD
POS 1 OFF: Boot from FLASH/peripheral (see boot mode switch) OR use emulator on baseboard
POS 2 ON: GPIOs 28 & 29 will be connected to the USB-to-UART adapter on the XDS110 emulator
POS 2 OFF: GPIOs 28 & 29 are disconnected from the USB-to-UART adapter on the XDS110 emulator and connected to the HSEC connector pins



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