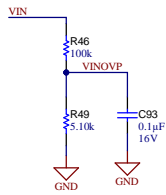
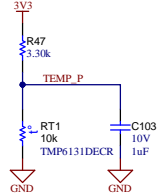


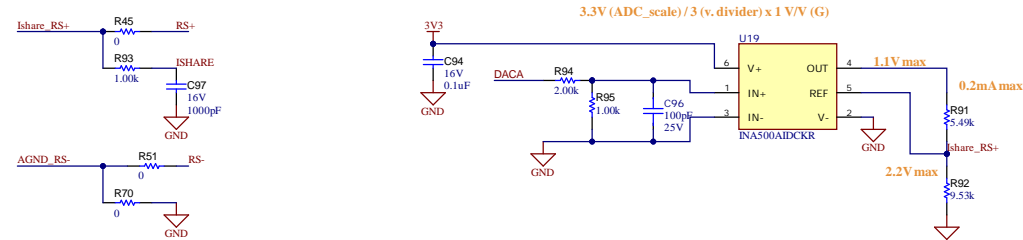
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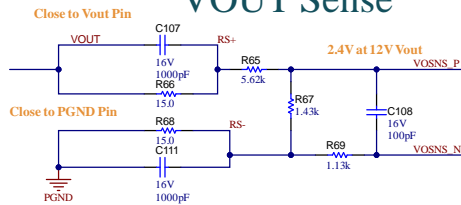
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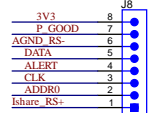
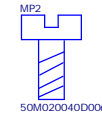
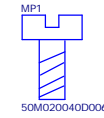
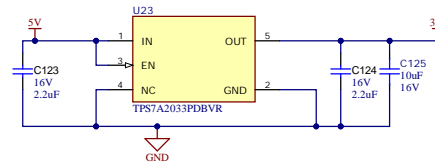
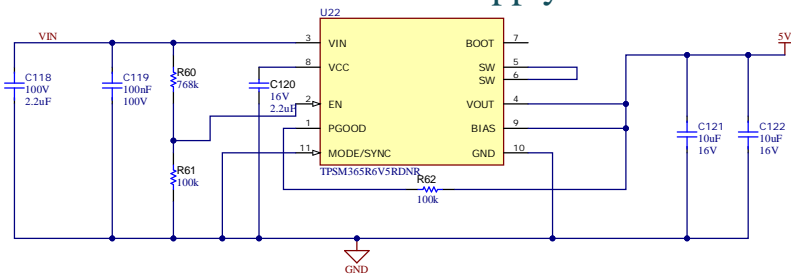
ACS



VOUT Sense

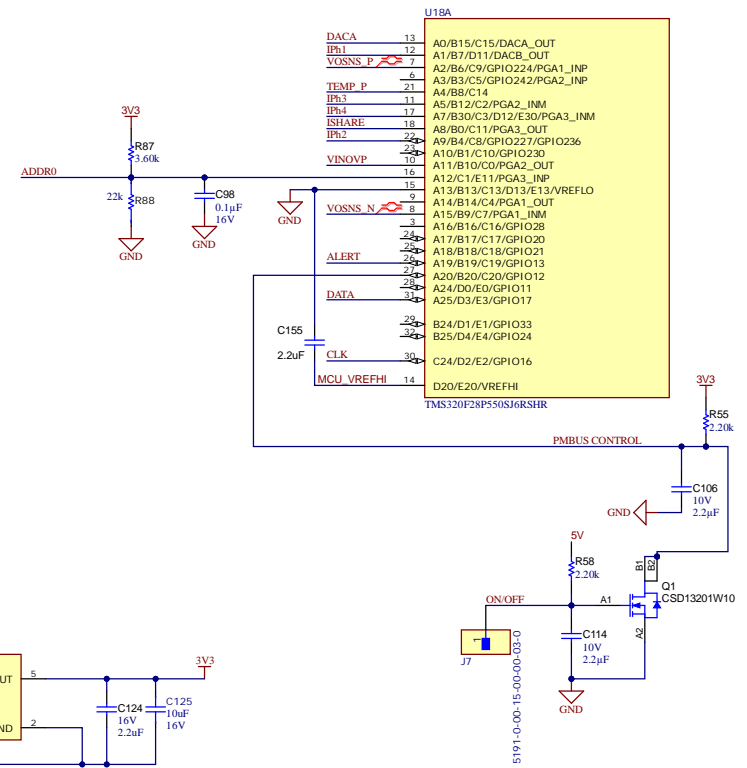


Bias Supply



62000811121

Controller



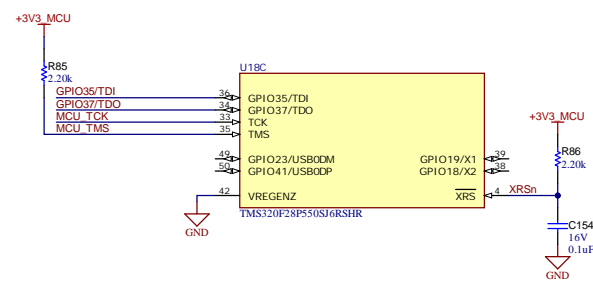
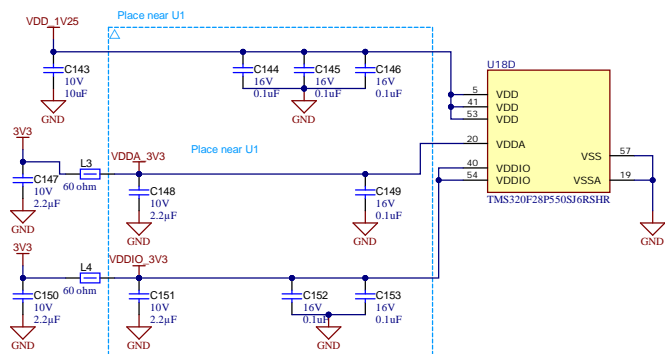
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Orderable:	Designed for: Public Release	Mod. Date: 7/26/2025
TID #: 060095	Project Title: TIDM-02022	
Number: TIDM-02022 Rev: E1	Sheet Title:	
SVN Rev.: Not in version control	Assembly Variant: LMG3100	Sheet: 1 of 4
Drawn By:	File: Control_SchDoc	Size: B
Engineer: Stevan	Contact: http://www.ti.com/support	http://www.ti.com

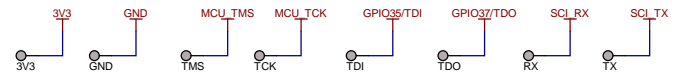
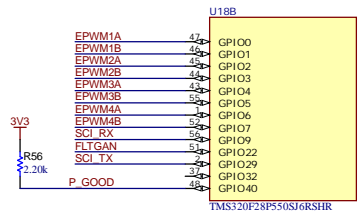


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F28P55x Device



- EPWM1A
- EPWM1B
- EPWM2A
- EPWM2B
- EPWM3A
- EPWM3B
- EPWM3A
- EPWM4A
- EPWM4B
- SCI_RX
- FLTGAN
- SCI_TX
- P_GOOD

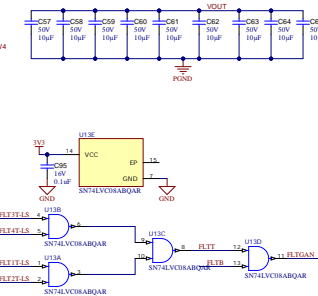
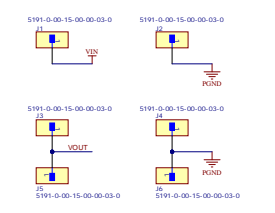
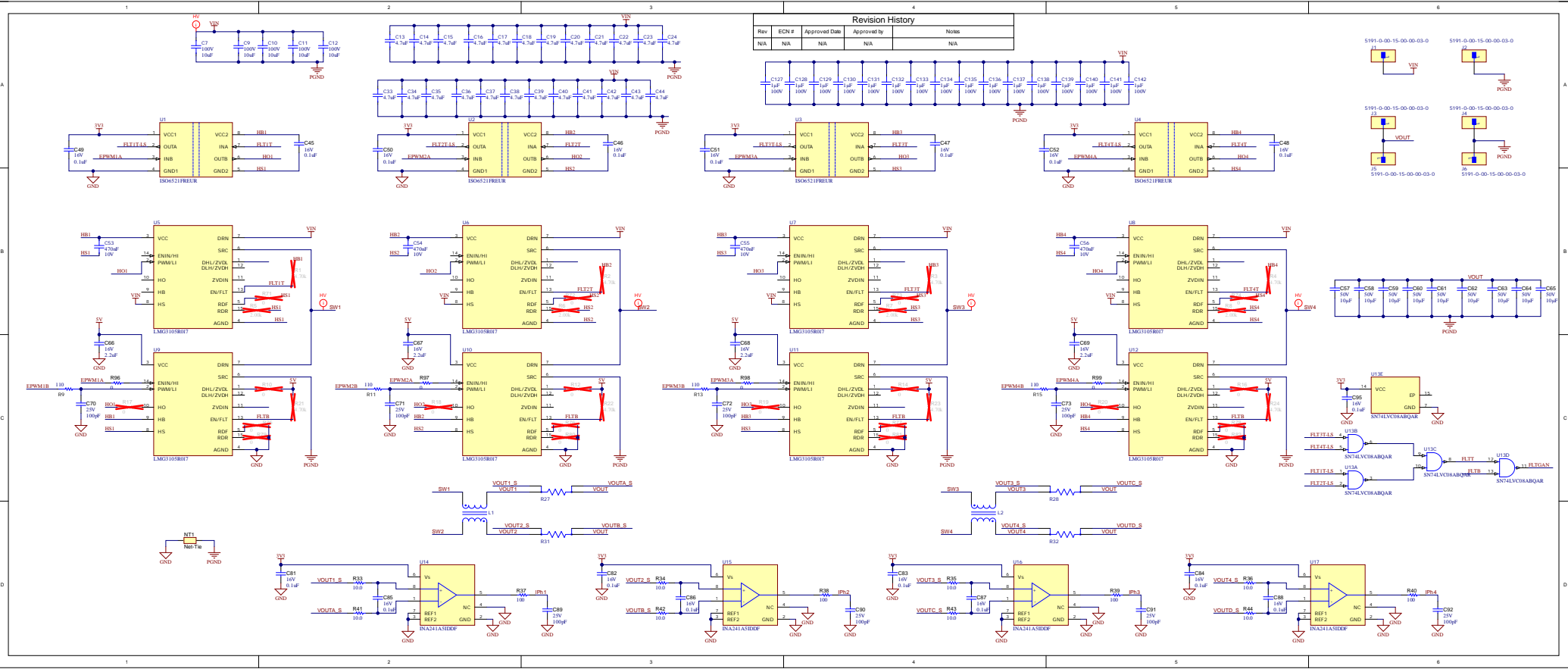


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Orderable:	Designed for: Public Release	Mod. Date: 7/25/2025
TID #: 050095	Project Title: TIDM-02022	
Number: TIDM-02022 Rev: E1	Sheet Title:	
SVN Rev.: Not in version control	Assembly Variant: LMG3100	Sheet: 2 of 4
Drawn By:	File: MCU_Support_SchDoc	Size: B
Engineer: Stevan	Contact: http://www.ti.com/support	http://www.ti.com



Rev	ECN #	Approved Date	Approved By	Notes
N/A	N/A	N/A	N/A	N/A



1 2 3 4 5 6

A

A

PCB Number: TIDM-02022
PCB Rev: E1

PCB
LOGO
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PCB
LOGO
FCC disclaimer

PCB
LOGO
WEEE logo

B

B

C

C

D

D

Orderable:	Designed for: Public Release	Mod. Date: 7/23/2025
TID #:	050095	Project Title: TIDM-02022
Number: TIDM-02022	Rev: E1	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: LMG3100	Sheet: 4 of 4
Drawn By:	File: TIDA-05x_Hardware.SchDoc	Size: B
Engineer: Stevan	Contact: http://www.ti.com/support	http://www.ti.com



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1 2 3 4 5 6

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STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer	COPPER	2.76mil		
	Dielectric 1	FR-4 High Tg	2.80mil	4.1	
2	GND1	COPPER	4.13mil		
	Dielectric 2	FR-4 High Tg	2.80mil	4.1	
3	PWR1	COPPER	4.13mil		
	Dielectric 3	FR-4 High Tg	2.80mil	4.1	
4	PWR2	COPPER	4.13mil		
	Dielectric 4	FR-4 High Tg	2.80mil	4.1	
5	PWR3	COPPER	4.13mil		
	Dielectric 5	FR-4 High Tg	2.80mil	4.1	
6	GND2	COPPER	4.13mil		
	Dielectric 6	FR-4 High Tg	2.80mil	4.1	
7	GND3/SIG1	COPPER	4.13mil		
	Dielectric 7	FR-4 High Tg	2.80mil	4.1	
8	SIG2	COPPER	4.13mil		
	Dielectric8	FR-4 High Tg	46.22mil	4.8	
9	SIG3	COPPER	4.13mil		
	Dielectric 9	FR-4 High Tg	2.80mil	4.1	
10	GND3/SIG4	COPPER	4.13mil		
	Dielectric 10	FR-4 High Tg	2.80mil	4.1	
11	GND5	COPPER	4.13mil		
	Dielectric 11	FR-4 High Tg	2.80mil	4.1	
12	PWR4	COPPER	4.13mil		
	Dielectric 12	FR-4 High Tg	2.80mil	4.1	
13	PWR5	COPPER	4.13mil		
	Dielectric 13	FR-4 High Tg	2.80mil	4.1	
14	GND6	COPPER	4.13mil		
	Dielectric 14	FR-4 High Tg	2.80mil	4.1	
15	GND7	COPPER	4.13mil		
	Dielectric 15	FR-4 High Tg	2.80mil	4.1	
16	Bottom Layer	COPPER	2.76mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Total board thickness: 149.61mil +/-10mils

DESIGN INFORMATION

MIN. TRACK WIDTH: 6 MIL
 MIN. CLEARANCE: 4.92 MIL
 MIN. VIA PAD SIZE: 20 MIL
 MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-4 FR-4 High Tg OTHER _____
 THICKNESS: 149.61mil +/-10mils OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

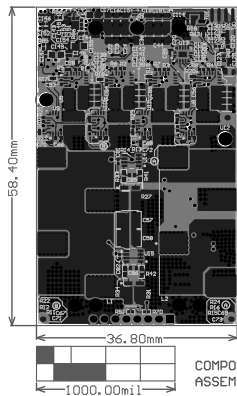
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs
 TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

FAB NOTES

- ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
- UNENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1: 1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED VIA TENTING / COVERING REQUIREMENTS.
- ALL DIMENSIONS ARE IN MM.
- ALL VIAS NEED TO BE FILLED WITH CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001 . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.
- THIS IS NOT AN IMPEDANCE CONTROLLED BOARD



COMPONENTS MARKED 'DNP' SHOULD NOT BE ASSUMED TO BE PRESENT ON THIS BOARD.
 ASSEMBLY VARIANT: [No Variations]

REV: 001	DATE: 12/12/2020	BY: [Name]	DESCRIPTION: [Description]
LAYER: Assembly	TID #: N/A	AN: # DIT	DATE: 12/12/2020 4:32:13 PM
2121MUR211 8AXET	M9 E1:SE:H	GENERATED.SI :: 12/12/2020	TEXAS INSTRUMENTS

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ENGINEER: Stevan	LAYOUT BY: Stevan
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.1.1.15

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