*Application Note*

# *How to Resolve the Issue of PMICs Failing to Resume Operation During Slow Voltage Ramp Tests?*

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**ABSTRACT**

*This document was translated from a simplified Chinese source.* (ZHCAG79)

The Slow Decrease and Increase of Supply Voltage test specified in ISO 16750-2 simulates the gradual discharging and charging processes of a vehicle battery. The test requires applying a ramp rate of (0.5±0.1)V/min (or step size under 25mV) to active inputs, decreasing the supply voltage from the minimum operating voltage to 0V, and then increasing it from 0V back to the minimum operating voltage. The device must not be damaged under this condition and must resume normal operation when power supply returns to normal. Taking TPS650362-Q1 and TPS65224-Q1 as examples, this article introduces the potential causes and solutions for PMICs failing to resume operation during slow supply voltage ramp tests.

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# 1 Introduction

The Slow Decrease and Increase of Supply Voltage test specified in ISO 16750-2 simulates the gradual discharging and charging processes of a vehicle battery. The test requires applying a ramp rate of (0.5±0.1)V/min (or step size under 25mV) to active inputs, decreasing the supply voltage from the minimum operating voltage to 0V, and then increasing it from 0V back to the minimum operating voltage. The device must not be damaged under this condition and must resume normal operation when power supply returns to normal.

TPS650362-Q1 is an automotive-grade PMIC designed by TI for applications such as automotive camera modules, automotive millimeter-wave radars, and safety MCU power supplies. Its core advantage is high integration, consolidating topologies such as 3 Buck converters and 1 LDO into a single chip. BUCK2/3 support output currents up to 2.7A, with the input voltage supporting up to 35V. Equipped with an I2C interface and various monitoring registers, it satisfies system-level functional safety requirements up to ASIL-D. The input of TPS650362-Q1 is typically connected to battery power, making it a direct test subject in slow voltage ramp tests.

TPS65224-Q1 is an integrated power solution introduced by TI for DMS/OMS and safety SOC systems, offering up to 4 BUCK and 3 LDO power rails, where the 4 BUCKs support flexible combinations to accommodate SOC core power demands up to 10A. Its rich set of monitoring and control registers helps customers easily achieve system-level ASIL-D design requirements. TPS65224-Q1 usually serves as a secondary power rail in the system and does not directly connect to the input power supply. However, in slow supply voltage ramp tests, inadequate design of the pre-stage power supply can also cause anomalies on the PMIC input voltage.

Since PMICs typically integrate various power monitoring functions and protection mechanisms to help systems meet functional safety requirements, input voltage anomalies during slow voltage ramp tests can trigger protection mechanisms, preventing customers from passing the test. Therefore, taking TPS650362-Q1 and TPS65224-Q1 as examples, this article focuses on how high-voltage and low-voltage input PMICs address common abnormal states caused by slow supply voltage ramp tests.

# 2 Causes of PMICs Failing to Resume Operation Due to Slow Voltage Ramp Tests

## 2.1 Two Input Undervoltage Lockout (UVLO) Mechanisms of PMICs

Taking TPS650362-Q1 as an example, the PMIC voltage input pin features PVIN_B1_UVLO, an undervoltage lockout distinct from VSYS_UVLO. The main difference is that PVIN_B1_UVLO has a programmable undervoltage threshold, whereas VSYS_UVLO typically has a fixed threshold that is lower than or equal to the minimum programmable threshold of PVIN_B1_UVLO. PVIN_B1_UVLO holds outputs in the OFF state until input voltage exceeds the set threshold while keeping registers and error mechanisms active; VSYS_UVLO places the entire PMIC in a complete shutdown state.

During slow voltage ramp tests, the input voltage remains near the VSYS_UVLO and PVIN_B1_UVLO thresholds for an extended period. If a fault occurs in the PMIC during this time and is not cleared via registers, the error will remain logged and impede normal PMIC output.

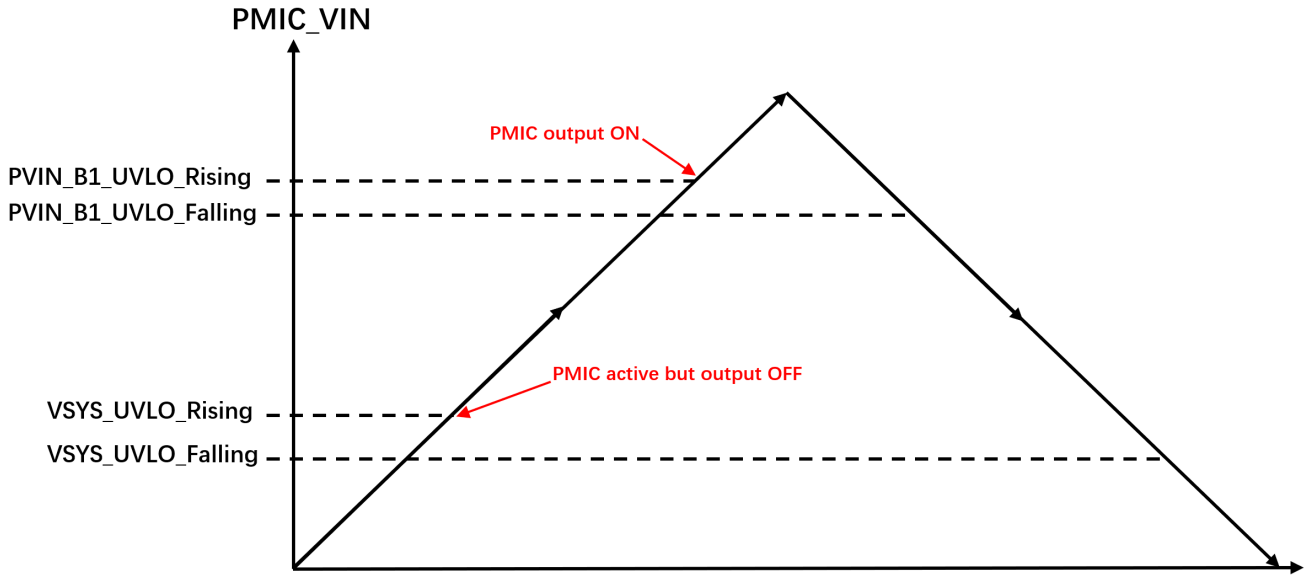


**Figure 2-1. VSYS_UVLO and PVIN_B1_UVLO**

## 2.2 Repeated PVIN_B1_UVLO Triggers Force the PMIC into WT_PWR_REC State

PVIN_B1_UVLO features programmable Falling and Rising thresholds; as input voltage rises, it must reach PVIN_B1_UVLO Rising to enable output, and as input voltage drops, reaching PVIN_B1_UVLO Falling turns output off.

When the input voltage of TPS650362-Q1 drops below PVIN_B1_UVLO Falling, outputs turn off, the PMIC enters SAFE state, and an error interrupt is generated. In the SAFE state, if input voltage exceeds PVIN_B1 UVLO Rising and no other error interrupts exist, the PMIC re-enters Active state. Each time the PMIC enters SAFE state and recovers, the RECOV_CNT counter increments by +1. When the count reaches RECOV_CNT_THR, the PMIC enters WT_PWR_REC state, requiring a power cycle on VSYS to restart the PMIC. The RECOV_CNT_THR threshold defaults to 15 times; the RECOV_CNT counter can be cleared by register operation or power-cycling to trigger VSYS_UVLO restart.

The input protection mechanism of TPS65224-Q1 is similar to that of TPS650362-Q1, where triggering $VCCA_{0V\_TH}$ leads to a PMIC Warm Reset and transitions to To SAFE state. When input voltage exceeds $VCCA_{0V\_TH}$, the PMIC re-enters Active state. Each transition to To SAFE increments RECOV_CNT by +1; once the count exceeds RECOV_CNT_THR, TPS65224-Q1 remains in SAFE_RECOVER state, requiring a power-cycle to restart the PMIC.

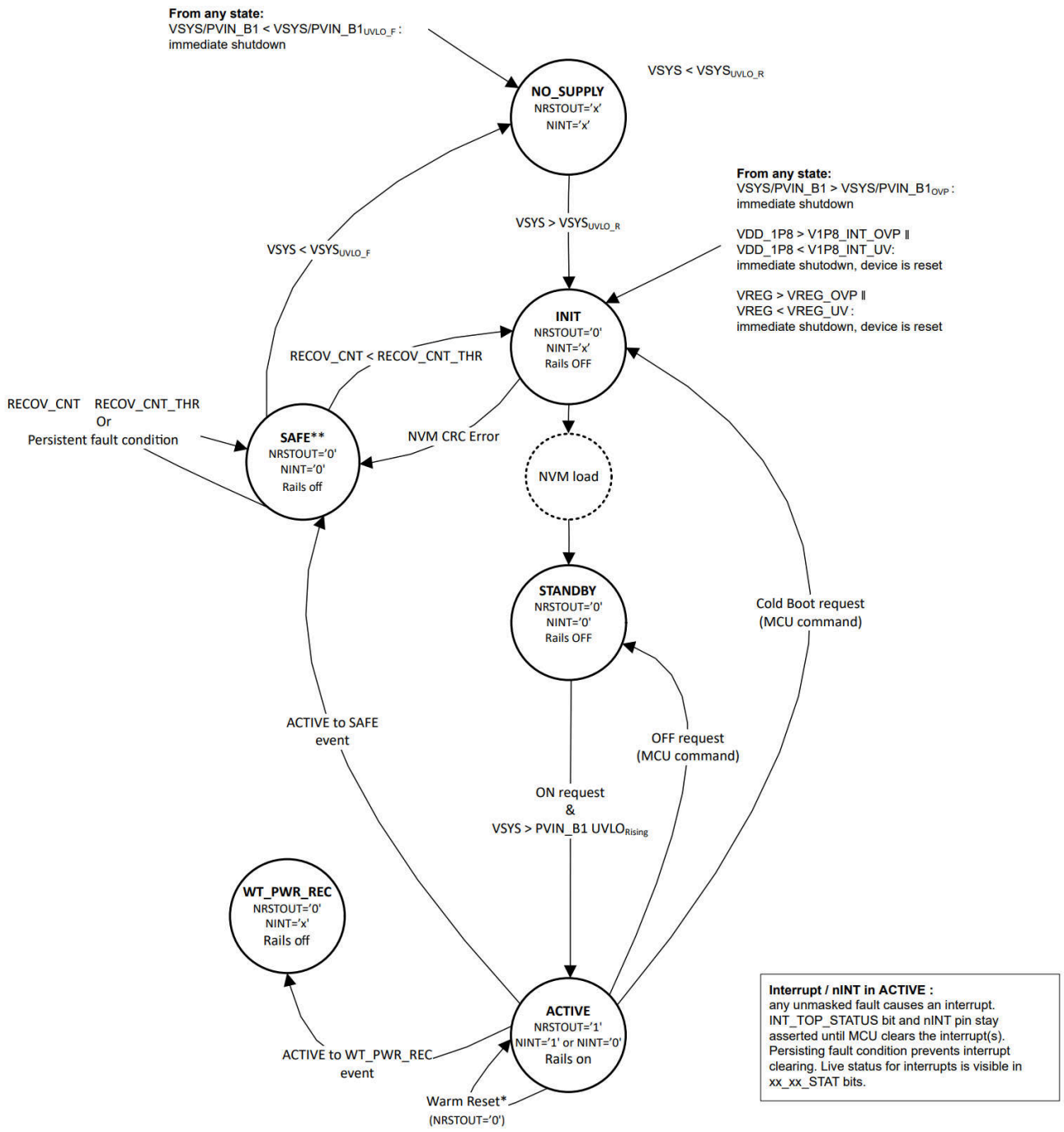


**Figure 2-2. TPS650362-Q1 state machine**

## 2.3 Reasons Why Slow Voltage Ramp Causes the PMIC to Enter WT_PWR_REC State

PVIN_B1_UVLO is a common undervoltage protection mechanism; however, in slow voltage ramp tests, input voltage stays near the PVIN_B1_UVLO threshold for long periods, easily causing repeated UVLO triggers that push the PMIC into WT_PWR_REC state. The reason is that each trigger of PVIN_B1_UVLO Rising/Falling turns PMIC outputs ON/OFF, causing load current changes on the input power supply, effectively dumping or applying load and inducing severe voltage overshoots/undershoots.

During slow voltage ramp testing, the input voltage lingers between PVIN_B1_UVLO Rising and Falling thresholds; excessive overshoot/undershoot triggers PVIN_B1 UVLO Falling/Rising, causing repeated transitions

in/out of SAFE state. When the RECOVERY count reaches RECOV_CNT_THR, the PMIC enters WT_PWR_REC state, leaving the PMIC unable to operate even after power recovers, requiring a VSYS power cycle to clear the RECOVERY count and restart the PMIC.

Figure 2-3 Taking TPS650362-Q1 as an example in a slow decrease test with PVIN_B1_UVLO Falling = 4.5V, PVIN_B1_UVLO Rising = 5.2V, and RECOV_CNT_THR = 15. PVIN_B1_VIN repeatedly triggers PVIN_B1_UVLO due to overshoot/undershoot; after exceeding 15 times, the PMIC yields no output even when PVIN_B1 voltage exceeds PVIN_B1_UVLO Rising =5.2V.

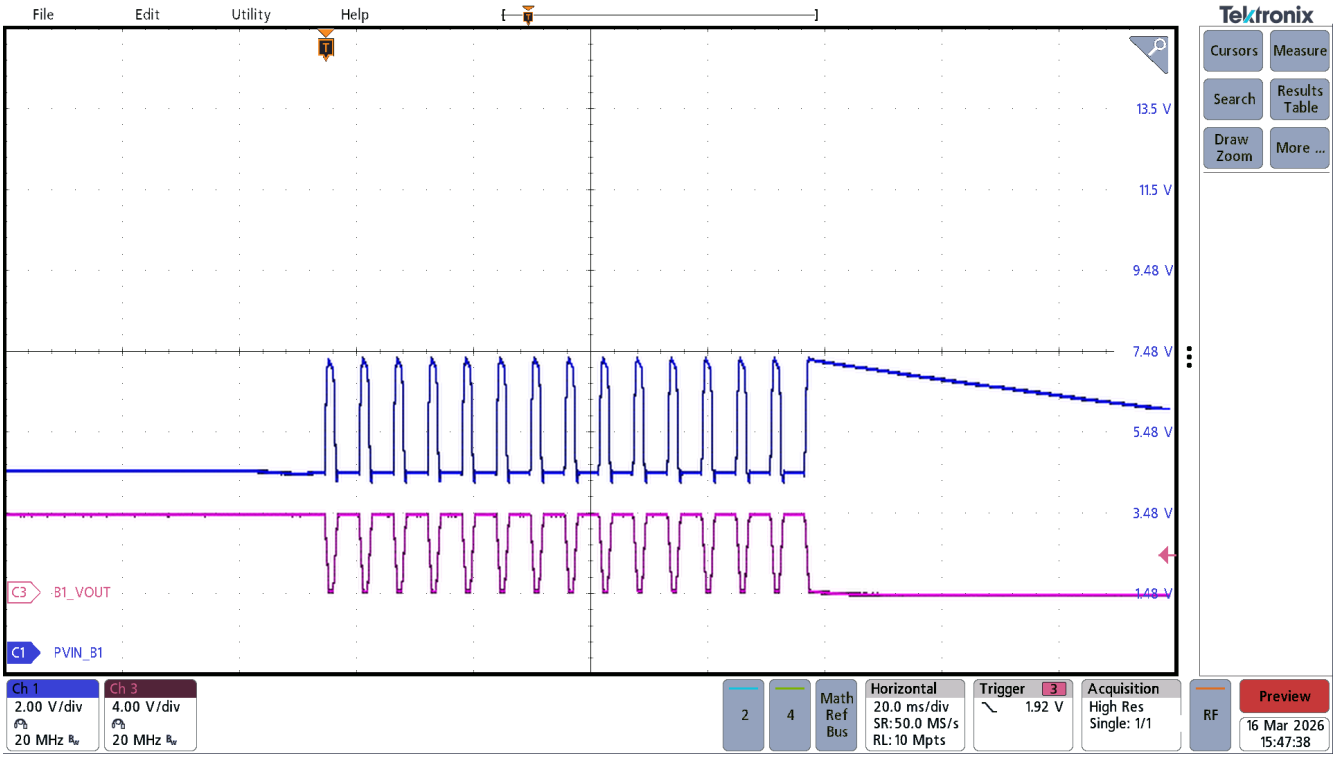


**Figure 2-3. TPS650362-Q1 yields no output after repeated PVIN_B1_UVLO triggers during slow decrease test**

# 3 Common Solutions for Wide-Input PMICs

Wide-input PMICs typically draw input power directly from battery power. Battery lines often carry heavy loads and long wire harnesses, making them more prone to voltage fluctuations than regulated power supplies, thereby triggering PVIN_B1 UVLO Falling/Rising thresholds and increasing RECOVERY count. Once RECOVERY count reaches RECOV_CNT_THR, the PMIC enters WT_PWR_REC state. Taking TPS650362-Q1 as an example, several common solutions are introduced below.

## 3.1 Increase the Gap Between PVIN_B1_UVLO Rising and Falling

In slow voltage ramp tests, overshoot/undershoot caused by PMIC output turning ON/OFF is the key factor triggering repeated UVLOs. Therefore, increasing the gap between PVIN_B1_UVLO Rising and Falling prevents UVLO triggers caused by overshoot/undershoot.

Taking TPS650362-Q1 as an example, the BUCK1_UVLO register (0x1B) can be configured to widen the gap between PVIN_B1_UVLO Rising /Falling thresholds. Figure 3-1 Setting PVIN_B1 UVLO Falling = 4.5V and PVIN_B1 UVLO Rising = 8.32V prevents PVIN_B1_UVLO Rising from triggering even when an overshoot exceeding 3V occurs on the input.

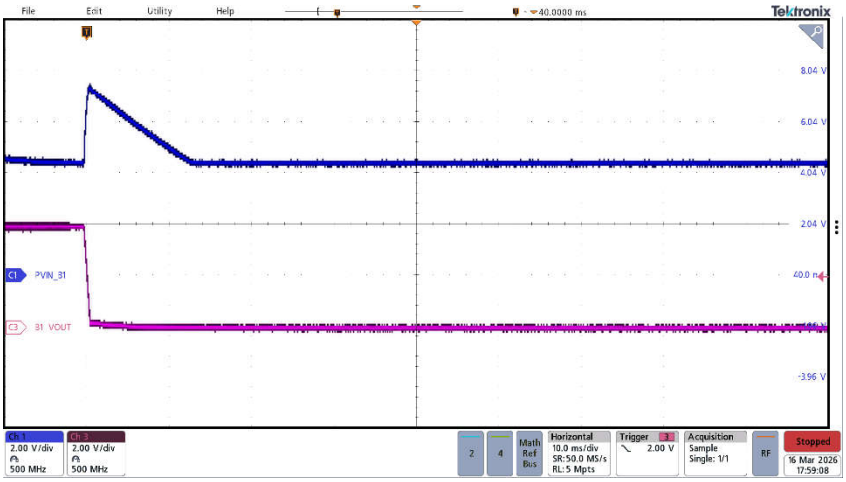


**Figure 3-1. Overshoot on TPS650362-Q1 does not trigger PVIN_B1 UVLO Rising =8.32V**

## 3.2 Replace Reverse-Polarity Protection Diode with an Ideal Diode

TPS650362-Q1 is frequently used in primary power supplies directly powered by battery inputs. In practical applications, a reverse-polarity protection diode is connected between battery and PMIC input to prevent reverse battery connections. However, this often leaves no discharge path between the reverse-polarity protection diode and PMIC input pin during shutdown, amplifying input voltage overshoot and triggering PVIN_B1_UVLO Rising during slow decrease tests.

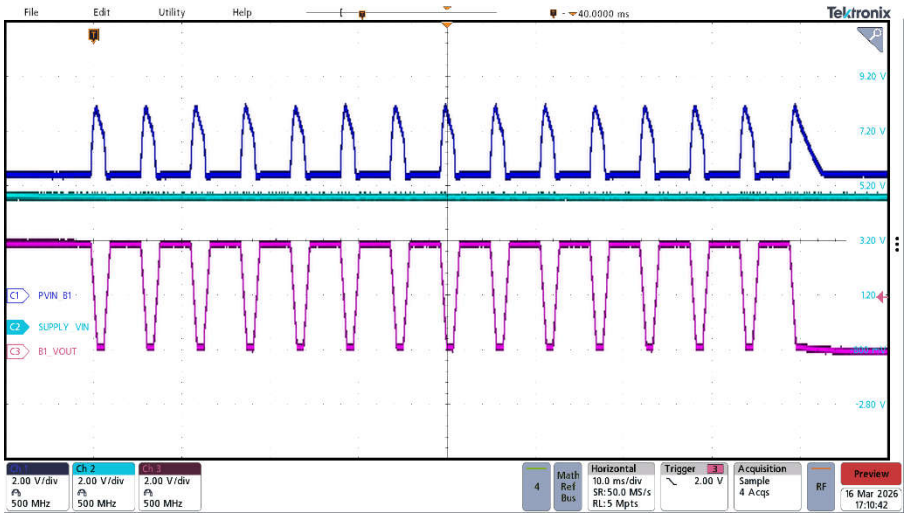


**Figure 3-2. Reverse-polarity protection diodes tend to cause overshoot at PMIC input**

An ideal diode controller is recommended to avoid missing discharge paths caused by the unidirectional conduction of traditional diodes, eliminating overshoot. Figure 3-3 Replacing the diode with LM74501-Q1 eliminates overshoot during slow decrease tests.

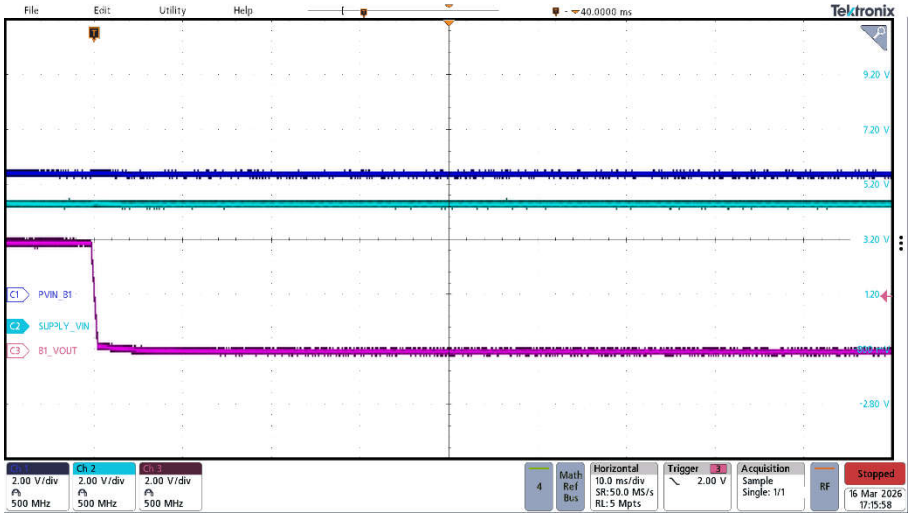


**Figure 3-3. Overshoot disappears after adopting an ideal diode controller**

## 3.3 TPS650362-Q1 Can Use Resistive Discharge Instead of Active Discharge

BUCK1 output of TPS650362-Q1 provides two discharge modes: Resistive discharge or Active discharge, selected via BUCK1_CTRL Register (0x18). When using Active discharge, BUCK1 controls discharge slew rate by switching the internal low-side MOSFET. At this point, the output inductor and internal power MOSFET of BUCK1 form a reverse boost topology feeding back to PVIN_B1_VIN.

If PVIN_B1_VIN lacks a discharge path, VIN experiences an unexpected voltage rise during slow ramp tests, pushing the PMIC into a state of repeated UVLO triggers.

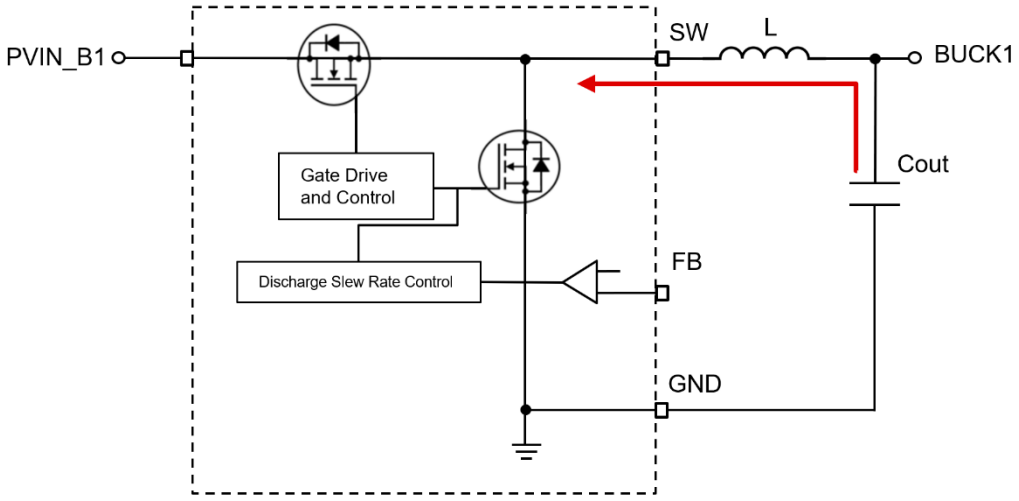


**Figure 3-4. Reverse boost topology**

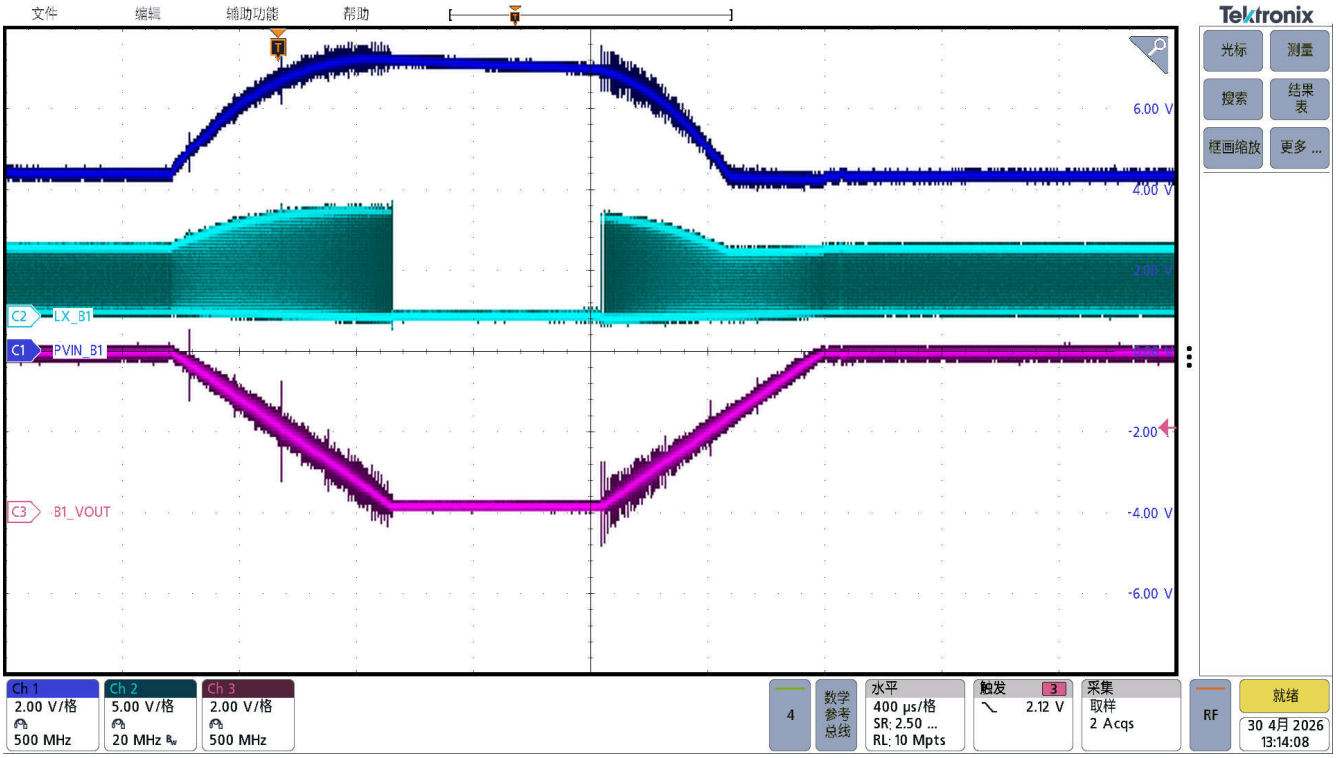


**Figure 3-5. Active discharge causes input voltage rise**

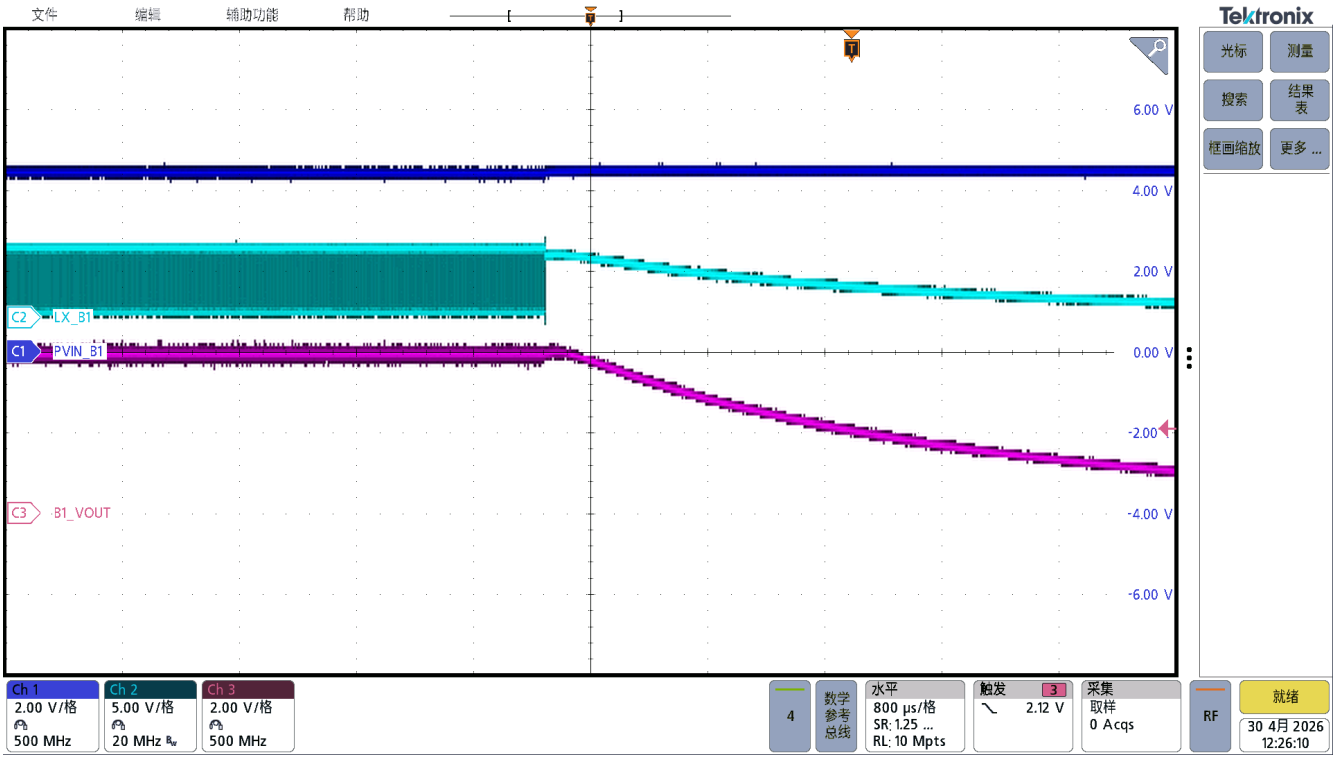


**Figure 3-6. Input voltage no longer rises with Resistive discharge**

# 4 Common Solutions for Low-Input PMICs

Low-input PMICs such as TPS65224-Q1/TPS6594-Q1 do not directly connect to system input power in automotive slow ramp tests; a primary BUCK converter is typically placed between input power and PMIC for step-down regulation. However, if the primary BUCK loop is unstable or the BUCK operates in dropout mode (input voltage lower than output voltage), unstable BUCK output will cause input overshoots/undershoots at the PMIC, triggering UVLO repeatedly.

## 4.1 Adjusting Primary BUCK Loop Stability

PMIC output ON/OFF transitions alter load current on the primary BUCK output rail; an unstable primary BUCK loop induces overshoots or undershoots on PMIC input voltage, triggering PMIC UVLO. Exceeding RECOV_CNT_THR forces the PMIC into SAFE state, preventing continued operation. For details on tuning BUCK loop stability, please refer to *how to test the high-precision loop performance*, omitted here.

## 4.2 Prevent Primary BUCK from Entering Dropout Mode During Slow Ramp Testing

When primary BUCK input voltage exceeds VIN_UVLO threshold but falls below set output voltage, or when headroom between input and output is less than minimum requirement, the BUCK enters dropout state. Particularly during slow ramp testing, the primary BUCK stays in dropout mode for prolonged periods. In this state, loop regulation becomes extremely unstable; once output voltage reaches PVIN_B1_UVLO Rising, the PMIC enables output, causing load fluctuation on the BUCK output rail, inducing undershoot, and triggering PMIC UVLO. Exceeding RECOV_CNT_THR forces the PMIC into SAFE state, preventing continued operation.

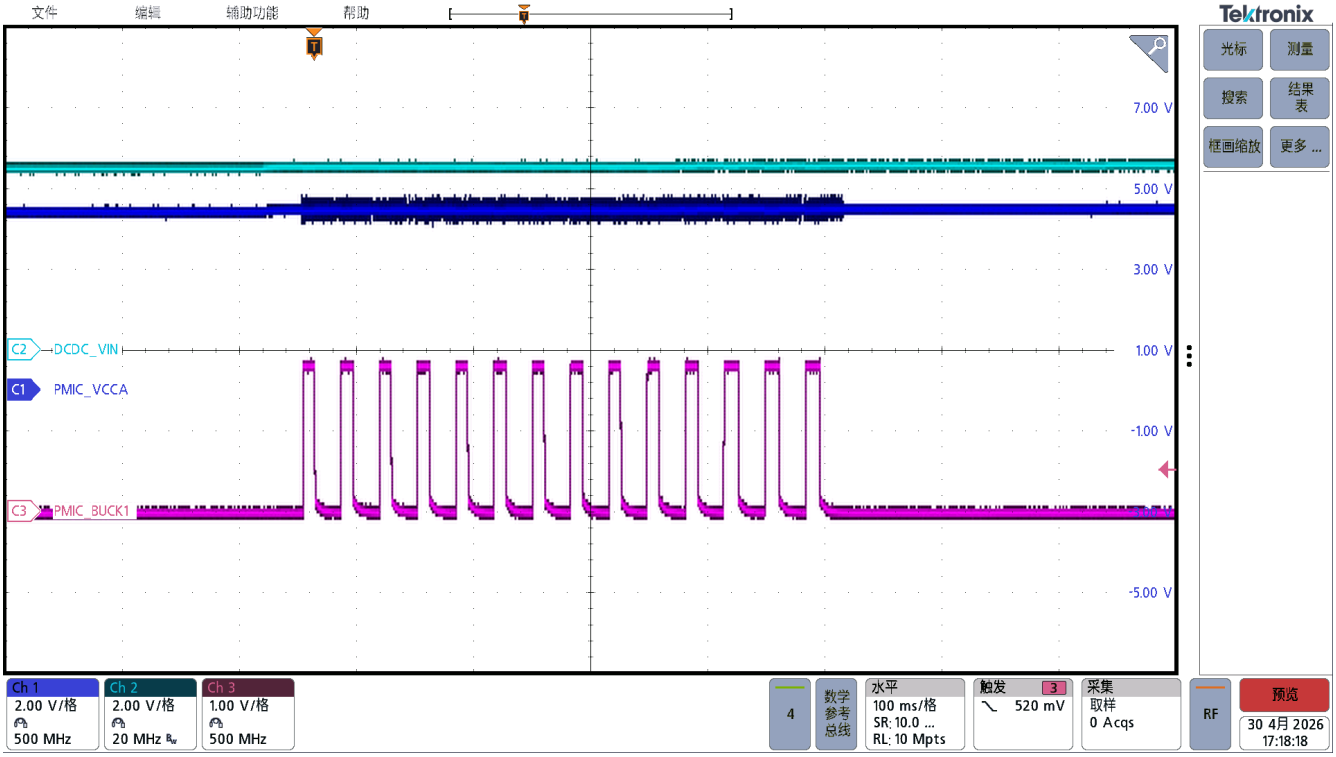


**Figure 4-1. Unstable primary BUCK output in dropout state triggers PMIC UVLO**

To prevent PMIC startup in BUCK dropout state, an additional turn-on threshold can be set via the primary BUCK EN pin. As shown in Figure 3-3 circuit, designating $V_{ON}$ as BUCK turn-on voltage and $V_{OFF}$ as turn-off voltage, $V_{ON}$ and $V_{OFF}$ are calculated using Equation 1 and Equation 2.

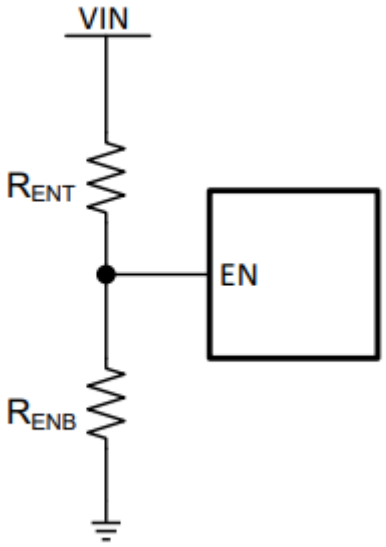


**Figure 4-2. Setting primary BUCK UVLO via EN pin**

$$V_{ON} = \left(1 + \frac{R_{ENT}}{R_{ENB}}\right) \times V_{EN-H} \quad (1)$$

$$V_{OFF} = \left(\frac{V_{ON}}{V_{EN-H}}\right) \times V_{EN-L} \quad (2)$$

Wherein:

$V_{EN-H}$ is the logic high level of BUCK EN pin

$V_{EN-L}$ is the logic low level of BUCK EN pin

# 5 Non-Functional Safety Systems Can Disable/Mask RECOV_CNT_THR to Avoid Entering SAFE/OFF States

For systems without functional safety requirements, PMIC restart limits can be removed by disabling RECOV_CNT_THR. Taking TPS65219-Q1 as an example, setting 0x24[7] = 1 in NVM masks RETRY_COUNT, allowing the PMIC to continue operating after repeated UVLO triggers during slow ramp tests without entering SAFE state.

### 6.7.37 INT_MASK_UV Register (Offset = 24h) [Reset = X]

INT_MASK_UV is shown in Figure 6-54 and described in Table 6-45.

Return to the Summary Table.

**Figure 6-54. INT_MASK_UV Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MASK_RETRY_COUNT | BUCK3_UV_MASK | BUCK2_UV_MASK | BUCK1_UV_MASK | LDO4_UV_MASK | LDO3_UV_MASK | LDO2_UV_MASK | LDO1_UV_MASK |
| R/W-X | R/W-X | R/W-X | R/W-X | R/W-X | R/W-X | R/W-X | R/W-X |

**Table 6-45. INT_MASK_UV Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | MASK_RETRY_COUNT | R/W | X | When set, device can power up even after two retries. (Default from NVM memory)<br>0h = Device does retry up to 2 times, then stay off<br>1h = Device does retry infinitely |

**Figure 5-1. TPS65219-Q1 MASK_RETRY_COUNT register**

# 6 References

1. *TPS65036x-Q1 Automotive Camera, Radar and MCU PMIC datasheet (Rev. A)*
2. *LM636x5-Q1 3.5V to 36V, 1.5A and 2.5A, Automotive, Step-Down Voltage Converter datasheet (Rev. I)*
3. *TPS65224-Q1 Power Management IC (PMIC) with 4 BUCKs and 3 LDOs for Safety-Relevant Applications datasheet (Rev. A)*
4. *TPS65219-Q1 Integrated Power Management IC for ARM Cortex—A53 Processors datasheet (Rev. B)*
5. *LM74501-Q1 TVS Less Automotive Reverse Battery Protection Controller datasheet (Rev. A)*

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