Application Report
SLVA709A–June 2015–Revised May 2019

AEC-Q100-012 Short-Circuit Reliability Test Results for Smart Power Switches

ABSTRACT

Smart power switches are widely used as short-circuit protection devices in automotive systems. Therefore, the robustness of the device under repetitive short-circuit stress is crucial to providing protection for the entire system. In order to guarantee protection, the AEC Q100-012 provides a industry standard qualification certificate which specifies the reliability of this type of device.

This application report describes the AEC Q100-012 specification and provides the test method and results for TI's Smart Power Switch devices.

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1 AEC Q100-012 Introduction

1.1 Introduction

The Automotive Electronics Council (AEC) provides the AEC Q100-012 documentation which specifies standards for short-circuit reliability testing. The main purpose of this test is to determine the reliability of smart-power switches when operating in a continuous short-circuit condition. The AEC Q100-012 specification includes an equivalent test circuit, detailed test conditions, different reliability grade definitions, and other information.

1.2 Equivalent Test Circuit

Figure 1 shows the basic equivalent test circuit for a smart high-side switch (HSS). The HSS is the device under test (DUT) that performs the repetitive short-circuit tests while the R_{supply} and L_{supply} are the input impedance from the voltage source side (VBB), and the R_{short} and L_{short} are the output impedance from the module board and the cables. These input and output impedances simulate input and output cables or interconnects that impact the performance under short-circuit events.

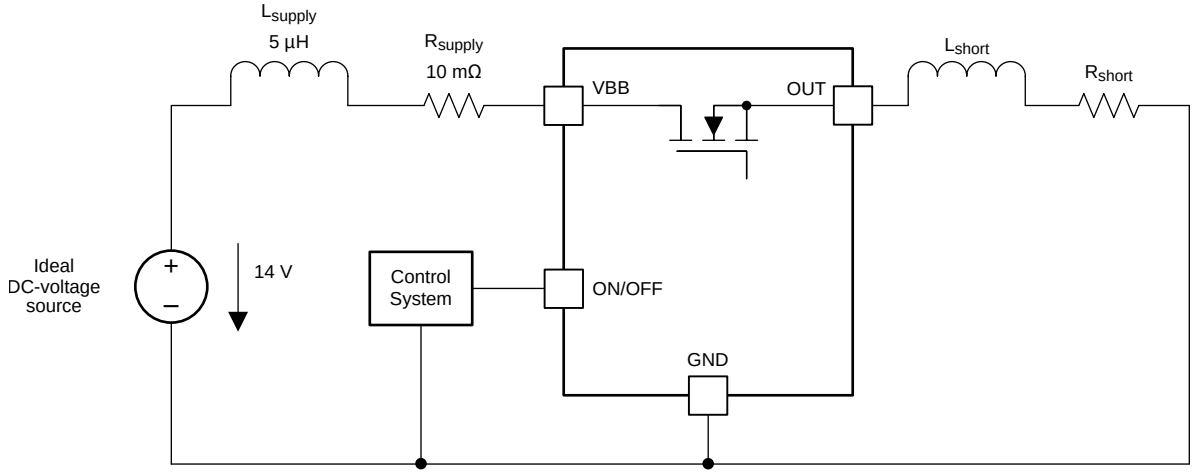

Figure 1. Smart HSS Short-Circuit Model

1.3 Test Conditions

1.3.1 Supply Voltage

The supply is modeled by an ideal voltage source, V_{BAT}, which generally is set at 14 V ± 2%.

1.3.2 Input Impedance

A total resistance of R_{supply} = 10 mΩ ± 20% and an inductance of L_{supply} = 5 µH ± 20% are specified to simulate the cable and interconnects from the automotive battery to the HSS.

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1.3.3 Output Impedance

The short circuit can occur anywhere between the device output and the load, so the output cable must be considered. Therefore, the output impedance may vary according to the cable length and diameter. Two types of short-circuit conditions are specified in the AEC Q100-012: the short circuit directly at the terminal and the long short circuit through a cable. During the terminal short circuit, AEC Q100-012 specifies that the module terminal, R_{short}, is 20 mΩ, and the parasitic inductance is smaller than 1 µH.

For the load short circuit, the specification assumes that the harness inductance is 1 µH/m, and specifies that the harness length is shorter than five meters. Table 1 lists the output impedance parameters of the two the short-circuit types. The short-circuit current is specified by the internal current-limit value of the device. Based on the different current range, different impedance values are provided.

Table 1. Output Impedance

SHORT CIRCUIT TYPE	DESCRIPTION	R_{short} (mΩ) ±20%	L_{short} (µH) ±20%
Terminal short circuit	Short at module	20	< 1
Load short circuit	Short at load, $I_{short} \leq 20$ A	110 – R_{supply}	5
	Short at load, 20 A < $I_{short} \leq 100$ A	100	5
	Short at load, $I_{short} > 100$ A	50	5

The short-circuit current of most TI HSS's is below 100 A, therefore, R_{short} is 100 mΩ and L_{short} is 5 µH. For any devices with a short-circuit level about 100 A, R_{SHORT} is decreased to 50 mΩ.

1.4 Passing Conditions

Different grade levels are specified according to the number of successfully passed cycles in the AEC Q100-012 specification. Samples for short-circuit testing must be drawn from three independent lots. The sample size must be large enough to ensure the statistical validity of the data. At least 10 samples per lot per test are recommended. Table 2 lists the number of cycles and fails and lots for these grade levels.

Table 2. Grade Level Table

GRADE	NUMBER OF CYCLES	LOTS/SAMPLES PER LOT	NUMBER OF FAILS
A	>1 000 000	3/10	0
B	>300 000 – 1 000 000	3/10	0
C	>100 000 – 300 000	3/10	0
D	>30 000 – 100 000	3/10	0
E	>10 000 – 30 000	3/10	0
F	>3000 – 10 000	3/10	0
G	>1000 – 3000	3/10	0
H	300 – 1000	3/10	0
O	<300	3/10	0

2 Types of Short Circuit

In addition to the different component selections, three test modes are defined in the AEC Q100-012 specification to verify the reliability of the device. In an application, the most relevant test mode is the situation that most accurately represents the conditions of the end system.

Cold Repetitive Short-Circuit Test (Short Pulse)— Simulates a case where there is a micro-controller monitoring the HSS that can react to a short-circuit and shut the device off in less than 10 ms.

Cold Repetitive Short-Circuit Test (Long Pulse)— Simulates a case where there is a micro-controller monitoring the HSS that can react to a short-circuit and shut the device off, however the sampling period is longer than 10 ms or unknown. In this case the micro-controller response time is assumed to be 300 ms.

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Hot Repetitive Short-Circuit Test— Simulates a case where there is no micro-controller monitoring the HSS, so the HSS indefinitely stays enabled into the short-circuit.

Table 3 lists the detailed ambient temperature, pulse duration, and cycle numbers.

Table 3. Test Requirements Summary

TEST ITEMS		TEST CONDITION	RECCOMENDED TEST CYCLES
Cold repetitive short-circuit test	Short pulse	–40°C, 10-ms pulse, cool down	1 Million
	Long pulse	–40°C, 300-ms pulse, cool down	1 Million
Hot repetitive short-circuit test		25°C, keeping short	1 Million

2.1 Cold Repetitive Short Circuit—Short Pulse

The cold repetitive short-circuit test is intended to simulate an event where the device is monitored by an MCU that can react to a short-circuit event within 10 ms. For TI's smart high-side switches, a short-circuit fault can be reported on the current sense pin (CS) or the status output pin (ST). In general, the microcontroller turns off the channels when it receives this fault indication, however the microcontroller sampling period introduces some delay. During this 10 ms delay, the device passes in and out of thermal swing shutdown until the microcontroller recognizes the fault. After the fault is recognized, the microcontroller shuts the device off and the device remains off while it cools down. This short-circuit pattern is considered one cycle of repetitive short-circuit.

Due to the relatively short 10 ms pulse, during the thermal cycling, the device always shuts down due to the thermal swing detection, and the temperature never hits the absolute thermal temperature shutdown. Given the high power dissipated in a short-circuit event, the stress of the rapid temperature variation must be considered, especially for the repetitive stress under extremely low temperature.

Figure 2 shows the test sequence. The test sequence is as follows:

1. At point A, the device enables into a short circuit.
2. From point B to point E (10-ms, as specified in AEC-Q100-012), the device remains enabled while the internal thermal swing protection works to minimize the temperature variation.
3. At point C the device has cooled down and turns back on until point D when it turns off again due to thermal cycling.
4. From point E to point F, the device EN goes low for enough time to ensure the device temperature goes back to –40°C. External sensors are required to monitor the device temperature.
5. At point F, the cycle counter increments by 1 and the next cycle occurs. Steps 1 through 4 repeat.

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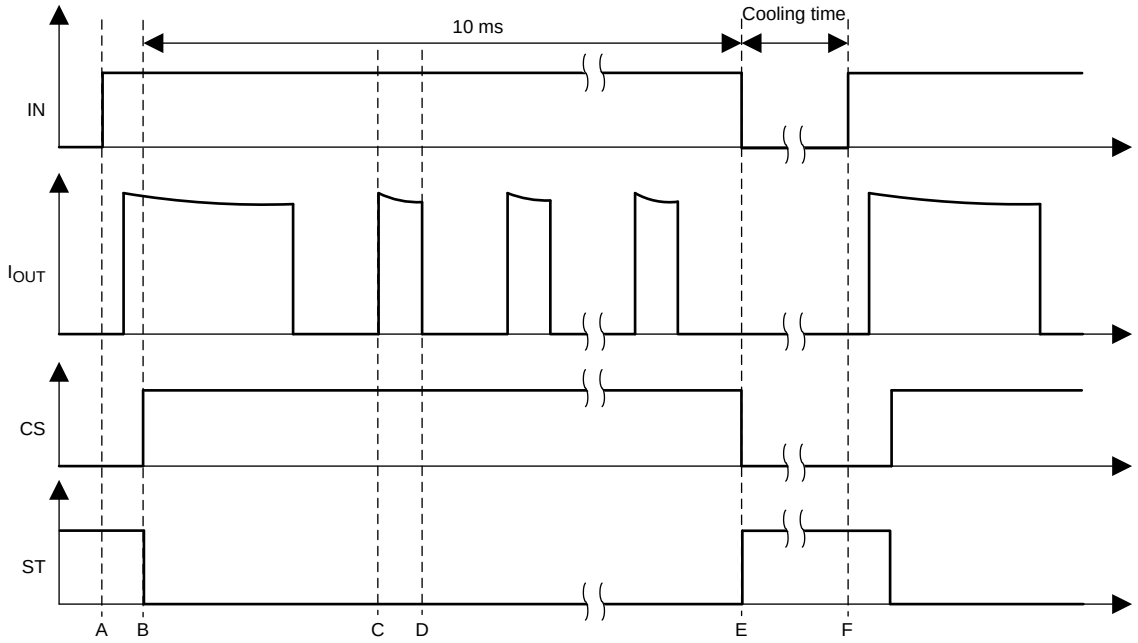

Figure 2. Timing Diagram of Cold Repetitive Short Circuit—Short Pulse

2.2 Cold Repetitive Short Circuit—Long Pulse

The short pulse described in Section 2.1 is intended to simulate the 10-ms scenario in which the microcontroller reacts. However, in some cases, the response time of the microcontroller is longer or difficult to estimate (for example, the RC filtering delay or the conflict with higher priority interrupt). When the short-circuit cycle time increases, the device enters the absolute temperature protection region after a few cycles of repetitive cycling of thermal shutdown. This condition can be harsher for the device than the thermal swing shutdown as the absolute device temperature is higher.

To verify the device reliability under this condition, the cold repetitive short-circuit long-pulse test is required. Similar to the short pulse, the start point of –40°C is the worst case.

Figure 3 shows the test sequence. The test sequence is as follows:

1. At point A, the device enables into a short-circuit.
2. From point B to point G (300-ms pulse, as specified in AEC-Q100-012), thermal swing protection is active and then after multiple cycles absolute thermal shutdown occurs.
3. From point E to point F the device is retrying but since the device has hit absolute shutdown the current limit value is half of the standard value.
4. From point G to point H, the device EN goes low for enough time to ensure that the device temperature goes back to –40°C. External sensors are required to monitor the device temperature.
5. At point H, the cycle counter increments by one and the next cycle occurs. Steps 1 through 4 repeat.

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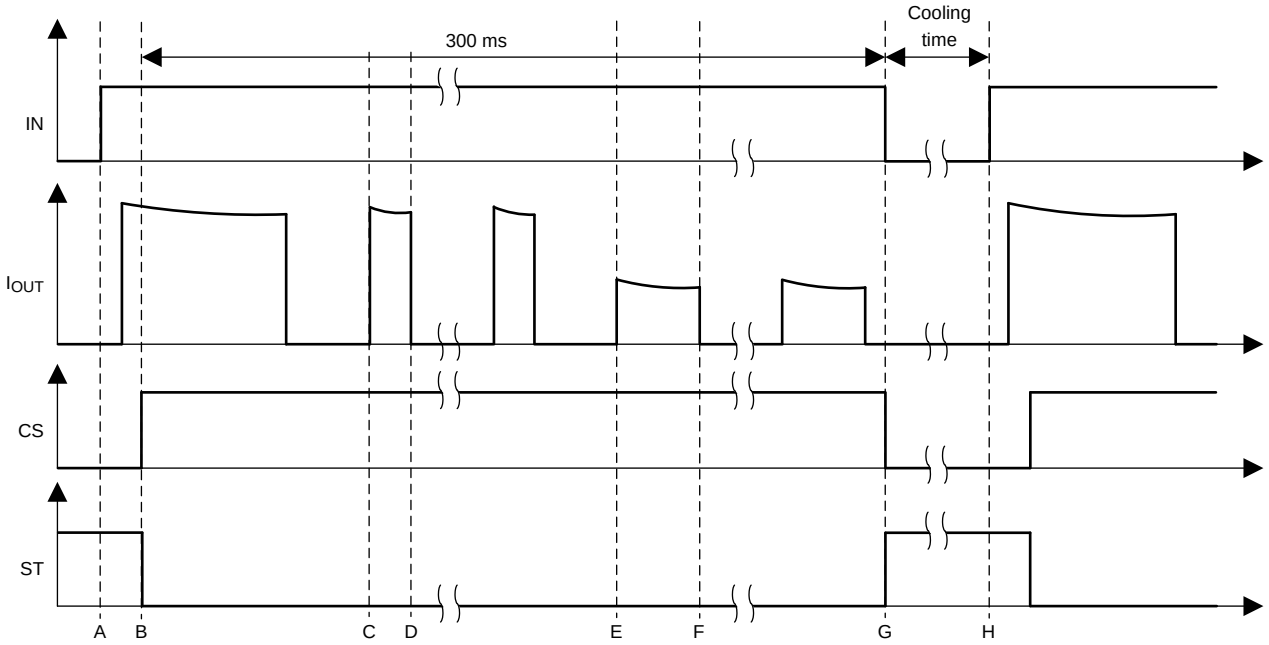

Figure 3. Timing Diagram of Cold Repetitive Short Circuit—Long Pulse

2.3 Hot Repetitive Short Circuit

The cold repetitive short-circuit scenarios are the target for fault cases in applications that are monitored by a microcontroller, however some applications do not have any micro-controller monitoring the HSS so nothing shuts down the EN pin after a short circuit event is recognized. The enable signal remains active during a hot repetitive short-circuit. In this case, the hot repetitive short-circuit test is required. After the short-circuit occurs, the device quickly enters absolute thermal shutdown cycling then remains indefinitely in repetitive thermal cycling mode. A cool-down period for the device is not required. The test begins at room temperature since the temperature variation occurs only at the first cycle and therefore the device is at hot for the entirety of the test.

Figure 4 shows the test sequence. The test sequence is as follows:

1. At point A, the device enables into a short-circuit.
2. From point B to point F, thermal swing protection is active first then thermal shutdown occurs.
3. The short-circuit condition continues indefinitely.

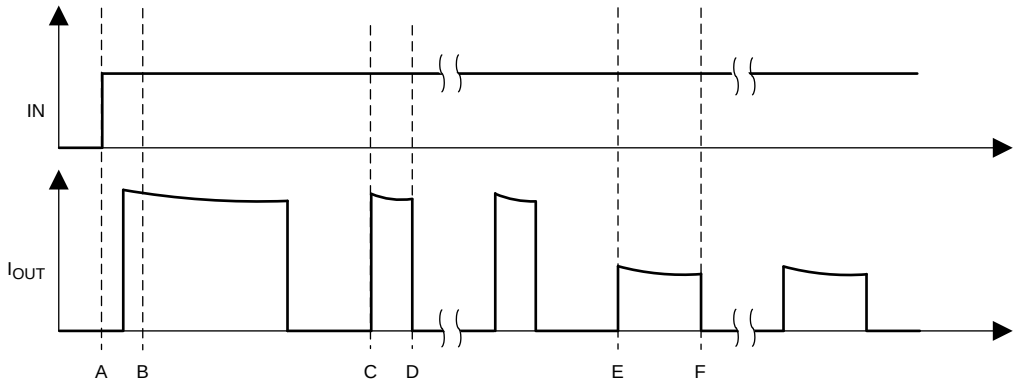

Figure 4. Timing Diagram of Hot Repetitive Short Circuit

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3 Short-Circuit Test Setup

3.1 Test Setup Introduction

The AEC-Q100-012 standard requires at least 30 devices originating from three separate silicon lots for a sufficient sample size. System control relies on a central PC host which is linked to a PXI bus system with PXI-6509 and PXI-6224 cards. The PXI-6509 and PXI-6224 cards generate the control signals and process the feedback signals of the test. All DUTs are processed individually and independently. The PWR_IN_Sx signal enables the current-monitor device. The SC_EN_Sx signal turns on the short-circuit resistor, R_{short}. The PWR_CS_Sx signal is the short-circuit current feedback signal. The IN_Sx signal enables the HSS and triggers the short circuit.

Some power sequences are required to ensure that the test functions correctly. Follow these power sequences:

1. Power on the monitor device with the PWR_IN_Sx signal.
2. Turn on the N-MOS R_{short} with the SC_EN_Sx signal.
3. Turn on the IN_Sx signal to force the device into short-circuit mode.
4. Read back the PWR_CS_Sx signal and process it with a software algorithm.

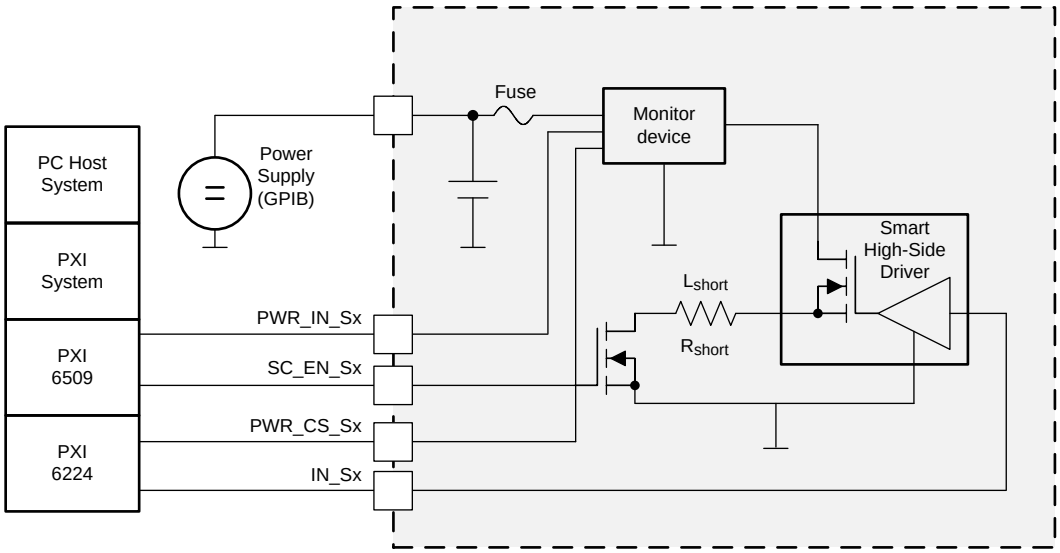

Figure 5. System Block Diagram

3.2 Test Set Up

The three main sections of the test control system are the power and driver boards, the oven and the oven board, and the PC host system.

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Figure 6. Instruments

Figure 7 shows the layout of one cell on the driver board and includes the monitor device and the connectors with the oven boards.

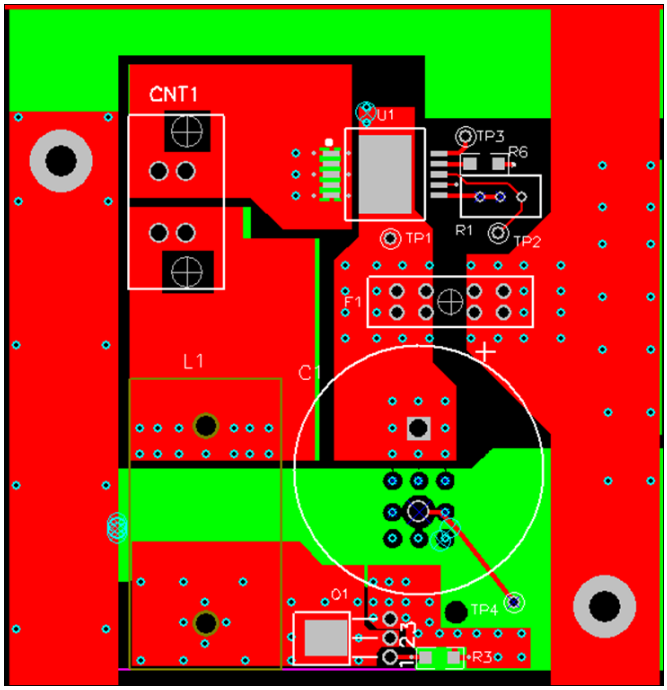

Figure 7. Layout of Driver Board

Figure 8 shows the layout of the oven board. The DUTs are placed on this board, which consists of 20 individual cells. This oven board is placed inside the oven for different temperature tests.

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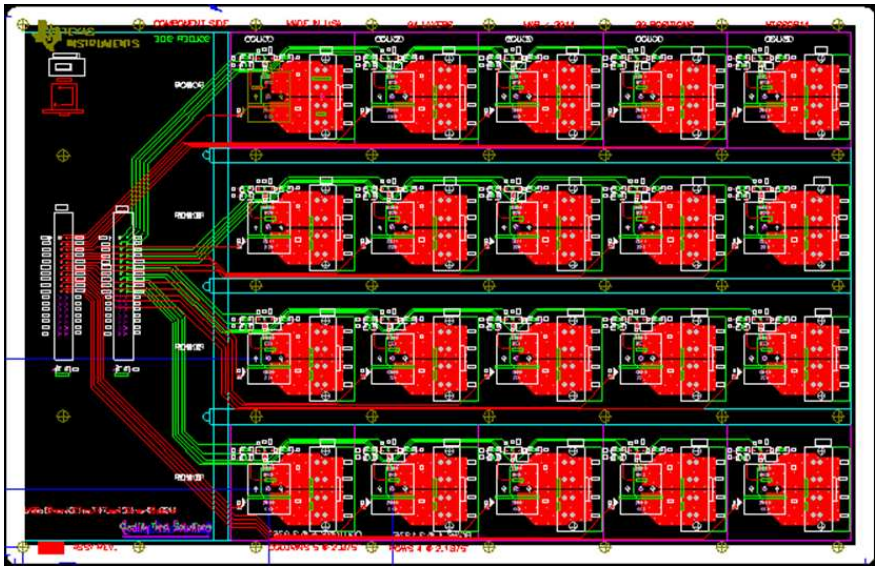

Figure 8. Layout of Oven Board

Figure 9 shows the graphical user interface (GUI) in the PC host system and how different test modes and conditions can be configured easily by the end user. The DUT status, test cycles, and waveforms can be monitored from this interface.

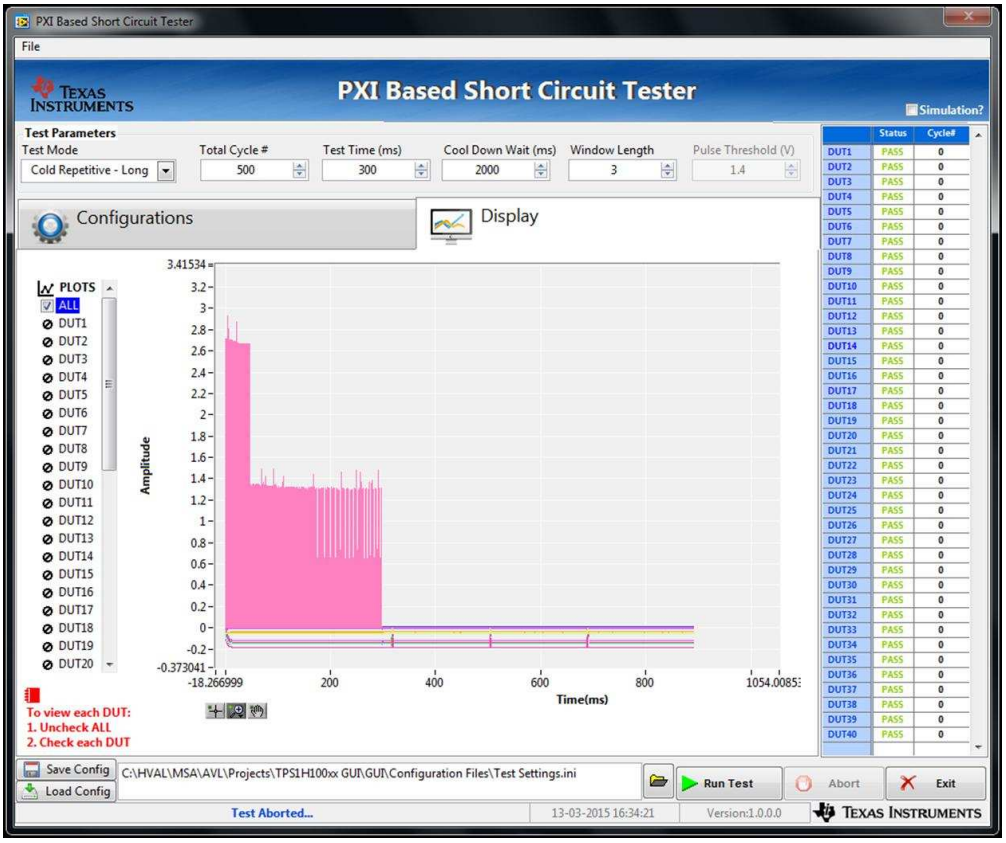

Figure 9. User Interface

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3.3 Failure Check

Two types of failure checks are conducted for each device: the real-time monitor and the pre-test data and post-test data check.

3.3.1 Real-Time Monitor

Any DUT failures, including open loads or device internal shorts, can by caught by real-time monitoring. If either failure mechanism is detected, the number of cycles undergone by the DUT is recorded as a device failure. The two failures are defined as:

Short-circuit failure — If the PWR_CS_Sx signal reaches the maximum set value, the short-circuit failure of the DUT is detected. The controller shuts down the corresponding site and records the number of cycles that have been performed on that site.

Open-load failure — If the PWR_CS_Sx signal reaches zero for the set time, it is recognized as an open-load failure DUT. The controller shuts down the corresponding site and records the number of cycles that have been performed on that site.

3.3.2 The Pre-Test and Post-Test Data Check

Pre-test and post-test data are only checked for each device on the automatic test equipment (ATE). Any value outside of the device specification listed in the data sheet is regarded as a test failure.

4 Results and Conclusion

TI HSS devices are all tested based on the described test conditions and setup. The testing results determine a device grade as defined in the Section 1.4 section which is shown in Table 4.

Table 4. High Side Switch Test Results

DEVICE NAME	R_{ON}	CHANNEL COUNT	GRADE
TPS1H100-Q1	100 mΩ	1	A
TPS2H160-Q1	160 mΩ	2	A
TPS4H160-Q1	160 mΩ	4	B
TPS1H200-Q1	200 mΩ	1	A
TPS1H000-Q1	1000 mΩ	1	A
TPS2H000-Q1	1000 mΩ	2	A
TPS4H000-Q1	1000 mΩ	4	A

The tables below give the specific test results and conditions for each device.

Table 5. TPS1H100-Q1 Test Result Summary

TEST PROCEDURE	LOTS/SAMPLES PER LOT	INITIAL TEMPERATURE	CYCLES	FAILED UNITS	POST TEST
Cold Repetitive Short Pulse	3/10	–40℃	1 000 000	0	Pass
Cold Repetitive Long Pulse	3/10	–40℃	1 000 000	0	Pass
Hot Repetitive Pulse	3/10	25℃	1 000 000	0	Pass

Table 6. TPS2H160-Q1 Test Result Summary

TEST PROCEDURE	LOTS/SAMPLES PER LOT	INITIAL TEMPERATURE	CYCLES	FAILED UNITS	POST TEST
Cold Repetitive Short Pulse	3/10	–40℃	1 000 000	0	Pass

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Table 6. TPS2H160-Q1 Test Result Summary (continued)

TEST PROCEDURE	LOTS/SAMPLES PER LOT	INITIAL TEMPERATURE	CYCLES	FAILED UNITS	POST TEST
Cold Repetitive Long Pulse	3/10	–40℃	1 000 000	0	Pass
Hot Repetitive Pulse	3/10	25℃	1 000 000	0	Pass

Table 7. TPS4H160-Q1 Test Result Summary

TEST PROCEDURE	LOTS/SAMPLES PER LOT	INITIAL TEMPERATURE	CYCLES	FAILED UNITS	POST TEST
Cold Repetitive Short Pulse	3/10	–40℃	1 000 000	0	Pass
Cold Repetitive Long Pulse	3/10	–40℃	300 000	0	Pass
Hot Repetitive Pulse	3/10	25℃	1 000 000	0	Pass

Table 8. TPS1H200-Q1 Test Result Summary

TEST PROCEDURE	LOTS/SAMPLES PER LOT	INITIAL TEMPERATURE	CYCLES	FAILED UNITS	POST TEST
Cold Repetitive Short Pulse	3/10	–40℃	1 000 000	0	Pass
Cold Repetitive Long Pulse	3/10	–40℃	1 000 000	0	Pass
Hot Repetitive Pulse	3/10	25℃	1 000 000	0	Pass

Table 9. TPS1H000-Q1 Test Result Summary

TEST PROCEDURE	LOTS/SAMPLES PER LOT	INITIAL TEMPERATURE	CYCLES	FAILED UNITS	POST TEST
Cold Repetitive Short Pulse	3/10	–40℃	1 000 000	0	Pass
Cold Repetitive Long Pulse	3/10	–40℃	1 000 000	0	Pass
Hot Repetitive Pulse	3/10	25℃	1 000 000	0	Pass

Table 10. TPS2H000-Q1 Test Result Summary

TEST PROCEDURE	LOTS/SAMPLES PER LOT	INITIAL TEMPERATURE	CYCLES	FAILED UNITS	POST TEST
Cold Repetitive Short Pulse	3/10	–40℃	1 000 000	0	Pass
Cold Repetitive Long Pulse	3/10	–40℃	1 000 000	0	Pass
Hot Repetitive Pulse	3/10	25℃	1 000 000	0	Pass

Table 11. TPS4H000-Q1 Test Result Summary

TEST PROCEDURE	LOTS/SAMPLES PER LOT	INITIAL TEMPERATURE	CYCLES	FAILED UNITS	POST TEST
Cold Repetitive Short Pulse	3/10	–40℃	1 000 000	0	Pass
Cold Repetitive Long Pulse	3/10	–40℃	1 000 000	0	Pass
Hot Repetitive Pulse	3/10	25℃	1 000 000	0	Pass

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The results of the AEC Q100-12 testing show that nearly all of the TI HSS devices fulfill 1 million repetitive short-circuits without a failure regardless of test qualification. Therefore, the devices are primarily qualified as Grade A, the highest short-circuit reliability certificate in the industry.

5 References

- *AEC - Q100-012 - REVSHORT CIRCUIT RELIABILITY CHARACTERIZATION OF SMART POWER DEVICES FOR 12V SYSTEMS* (Automotive Electronics Council, 2006)
- *TPS1H100-Q1 40-V, 100-mΩ Single-Channel Smart High-Side Power Switch Data Sheet*

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2015) to A Revision **Page**

- Changed title from Short-Circuit Reliability Test for Smart Power Switch AEC-Q100-012 Test of TPS1H100-Q1 to AEC-Q100-012 Short Circuit Reliability Test Results for Smart Power Switches. 1
- Updated abstract. 1
- Updated wording in Introduction. 2
- Updated wording in Equivalent Test Circuit section. 2
- Moved Test Conditions, Supply voltage, Input Impedance, Output Impedance, and Passing Conditions sections to section 1. 2
- Added Types of Short Circuit section to section 2. 3
- Added Cold Repetitive Short Circuit—Short Pulse, Cold Repetitive Short Circuit—Long Pulse, and Hot Repetitive Short Circuit sections to section 2. 4
- Added Test Setup Introduction, Test Setup, Failure Check, Real-time Monitor, and The Pre-Test and Post-Test Data Check sections to section 3. 7
- Added Results and Conclusion as section 4. 10
- Added table 8-15. 10

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