User's Guide

MC121-Q1, MC121, and MC111 Programming Guide

Abstract

This document outlines the procedures for utilizing the **Test Programming Mode** and **OTP (One-Time Programmable) Programming Mode** through an I2C interface on the MC121-Q1, MC121, and MC111 devices. By leveraging the PWM/DC and FG/RD pins for I2C communication, users can configure device registers to set specific motor performance parameters. These devices features two OTP pages, allowing the configuration to be programmed **up to two times**. The document provides a logic framework for determining page availability by evaluating status register values. A comprehensive register map is provided, covering CRC validation, page selection, unlocking sequences, and I2C mode status. This guide serves as a technical reference for engineers to facilitate successful device testing, configuration, and permanent programming of motor control parameters.

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1 Introduction

The MC121-Q1 is a highly integrated motor driver designed for 5V and 12V automotive single-phase BLDC applications. The device integrates N-channel full-bridge MOSFETs, charge pumps, hall sensor, commutation control logic, and comprehensive protection features. The integrated protections and fault reporting capabilities for the MC121-Q1, MC121, and MC111 devices enable reliable motor drive system designs while reducing the need for external components.

To support seamless integration into diverse system designs, these devices offers highly configurable programming modes:

- **Test Programming Mode:** Allows for temporary register configuration. These settings are volatile and are lost upon a power cycle, at which point the device reverts to the default or previously programmed OTP configuration.
- **OTP (One-Time Programmable) Programming Mode:** Enables permanent configuration storage. To achieve reliable programming, a supply voltage (VM) above 8V must be maintained. This mode requires a specific multi-step sequence, including an unlock key (02h, 01h, 04h), to write to the OTP register pages.

Figure 1-1 shows the basic hardware configuration for configuring and programming the MC121-Q1, MC121, and MC111.

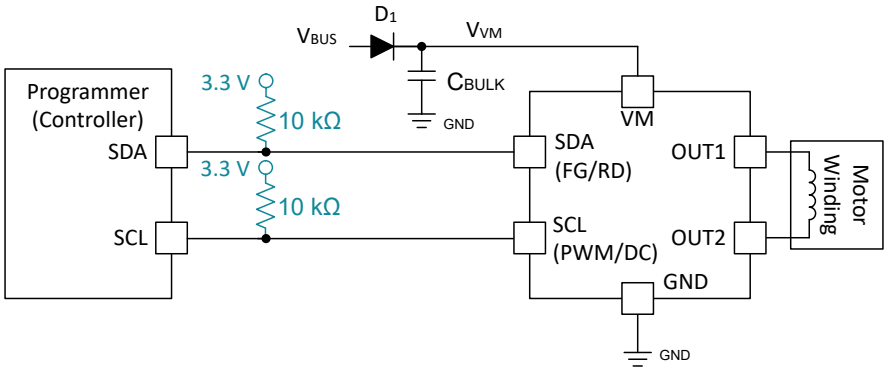


Figure 1-1. I2C Interface for Programming Mode

Figure 1-2 shows the block diagram for the I2C interface, OTP pages and User OTP (USR_OTP) and User Test-mode (USR_TM) registers of the MC121-Q1, MC121, and MC111. At every power-up, the device follows the below sequence to load the device configuration to the USR_OTP registers. and enters active mode of operation.

1. If OTP Page 2 is programmed, the USER_OTP registers are loaded with OTP Page 2 configuration.
2. If OTP Page 2 is blank and OTP Page 1 is programmed, the USER_OTP registers are loaded with OTP Page 1 configuration.
3. If OTP Page 1 is blank, the USER_OTP registers are loaded with default configuration.

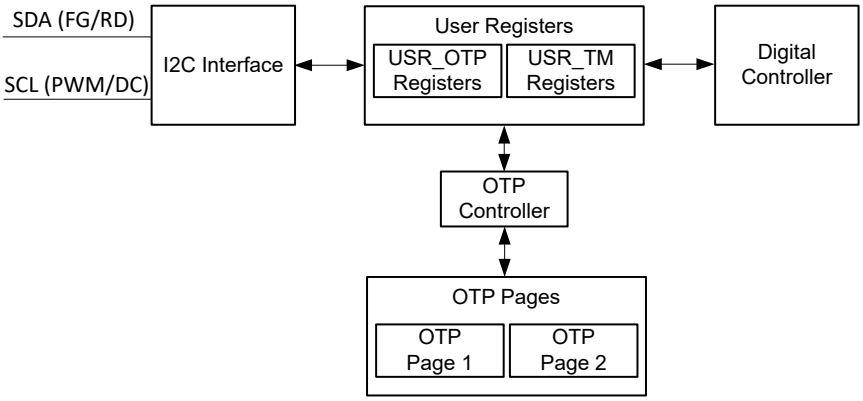


Figure 1-2. User Registers and OTP Programming

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Table 1-1 lists the relevant register addresses and bit fields that can be used for performing the OTP programming operation.

Table 1-1. Register Descriptions for OTP Programming

Register Name	Address	Bit	Bit Field Name	Description	Comments
USR_OTP_CRC	1Bh	7-0	USR_OTP_CRC	CRC Value	CRC value calculated over USR_OTP registers
USR_OTP_CFG	25h	7	USR_OTP_CRC_ERR	Check CRC error	Status of user OTP CRC check 0h = No CRC error 1h = CRC error
USR_OTP_CFG	25h	4-3	USR_OTP_PAGE_USED	OTP Page used	Indicates the OTP on which the latest load operation is performed. These bits need to be used in combination with information from CRC and CRC error flags to arrive at which OTP is programmed. 0h = Invalid combination since device attempts to read at least one OTP at power up. 1h = Latest load attempt is from OTP page 1. Use CRC value in combination to determine whether OTP page 1 is programmed. 2h = Latest load is from USR_OTP page 2. 3h = Invalid combination which is not expected.
USR_OTP_CFG	25h	2	USR_OTP_PAGE_SEL	Select OTP page	This bit indicates whether OTP page 1 is targeted for commanded operation, or OTP page 2 is targeted. 0h = OTP page 1 1h = OTP page 2
USR_OTP_CFG	25h	1	USR_OTP_PROG_VERIFY	Load Selected OTP	Reload selected OTP page and check and update CRC.
USR_OTP_CFG	25h	0	USR_OTP_PROG_ALL	Program selected OTP	Write 1h to this bit to program the OTP page according to USR_OTP_PAGE_SEL
USR_OTP_PRG_UNLOCK	26h	2-0	USR_OTP_PROG_UNLOCK	Unlock OTP	Write a sequence of 2h,1h,4h to these bits in successive write-frames, to unlock access to OTP programming mode
Internal	F1h	7-0	I2C_MODE	I2C mode	Read this register to check the status of I2C mode AAh = I2C mode active Write BBh to this register to exit I2C mode, relinquishing control of PWM and FG/RD pins to functional purposes
Internal	B4h	1	USR_OTP_PG1	Page 1 Programmed	Read this bit after a power recycle to check if OTP page 1 is programmed 0h = OTP Page 1 empty 1h = OTP Page 1 programmed

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Table 1-1. Register Descriptions for OTP Programming (continued)

Register Name	Address	Bit	Bit Field Name	Description	Comments
Internal	B4h	0	USR_OTP_PG2	Page 2 Programmed	Read this bit after a power recycle to check if OTP page 2 is programmed 0h = OTP Page 2 empty 1h = OTP Page 2 programmed

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2 Test Programming Mode Entry and Exit:

The MC121-Q1, MC121, and MC111 enters test programming mode with the following procedure.

1. Pull the FG/RD pin low and apply a high frequency signal in the range of (416-833) kHz at any duty between (20-80) % for 16 to 50 cycles to the PWM/DC pin to enter the test mode. The I2C interface is active in test mode.
2. Optional: To confirm if I2C interface is active, read address F1h. The value should be AAh
3. Communicate with the MC121-Q1, MC121, or MC111 over I2C to read and write to the USR_OTP configuration registers to set the desired motor performance or check the USR_TM test mode registers for the device status.
4. To exit the test programming mode write value BBh at address F1h or power cycle the device.
5. In test programming mode, the configured settings are lost after power cycle the device reverts to the default or previously programmed OTP configuration.

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3 OTP Programming Mode Entry and Exit

1. To achieve reliable OTP memory programming through I2C communication, maintain the MC121-Q1 power supply pin voltage (VM) above 8V throughout the entire duration of the communication
2. Pull the FG/RD pin low and apply a high frequency signal in the range of (416-833) kHz at any duty between (20-80) % for 16 to 50 cycles to the PWM/DC pin to enter the test programming mode. The I2C interface is active in test mode.
3. Optional: To confirm if I2C is active, read address F1h. The value should be AAh.
4. Communicate with the MC121-Q1, MC121, or MC111 over I2C to read and write to the USR_OTP registers to set the configuration to be programmed into the OTP page for desired motor performance and check the USR_TM test mode registers for the device status. Program all the reserved bit fields to 0h.
5. Determine which OTP Page is available to program following the steps mentioned in Section 4. OTP Page 1 must be programmed first if OTP Page 2 is planned to be used in future.
6. Select the OTP Page to be programmed with USR_OTP_PAGE_SEL bit in USR_OTP_CFG register.
7. Write the OTP programming mode entry key 2h, 1h, 4h to the USR_OTP_PROG_UNLOCK bits in USR_OTP_PRG_UNLOCK register in successive write-frames to unlock OTP programming mode.
8. Optional: Read the USR_OTP_PROG_UNLOCK bit to confirm if OTP program mode is active. The value should be 4h.
9. To burn the OTP memory on selected page, write 1h to the USR_OTP_PROG_ALL bit in USR_OTP_CFG Register. The contents of the USR_OTP register will be programmed to the selected OTP page.
10. Verify the OTP program burn by writing 1h to the USR_OTP_PROG_VERIFY bit in USR_OTP_CFG Register.
11. Check the status at USR_OTP_CRC_ERR for no errors. Check the values at USR_OTP_PAGE_USED and USR_OTP_CRC is updated.
12. To exit the OTP mode write key 2h, 1h, 4h to the USR_OTP_PROG_UNLOCK bits in USR_OTP_PRG_UNLOCK register in successive write-frames or power cycle the device.
13. To exit I2C mode write value BBh at address F1h or power cycle the device.
14. The configured settings are loaded from the programmed OTP page after power cycle.

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4 How to Determine which OTP Page is Available to Program

1. After power cycle pull the FG/RD pin low and apply a high frequency signal in the range of (416-833) kHz at any duty between (20-80) % for 16 to 50 cycles to the PWM/DC pin to enter the test mode. The I2C interface is active in test mode.
2. Optional : To confirm if I2C is active, read address F1h. the value should be AAh
3. Read the registers bits listed in Table 4-1

Table 4-1. Register Bits to Determine OTP Page is Availability

Bit Field Name	Address	Bit
USR_OTP_CRC	1Bh	7-0
USR_OTP_CRC_ERR	25h	7
USR_OTP_PAGE_USED	25h	4-3
USR_OTP_PG1	B4h	1
USR_OTP_PG2	B4h	0

The values in Table 4-2 indicates both OTP Page 1 and Page2 are available to be programmed. OTP Page 1 must be programmed first if OTP Page 2 is planned to be used in future.

Table 4-2. Register Bits Values for Both OTP Page 1 and Page 2 Availability

Bit Field Name	Value
USR_OTP_CRC	0h
USR_OTP_CRC_ERR	0h
USR_OTP_PAGE_USED	1h
USR_OTP_PG1	0h
USR_OTP_PG2	0h

The values in Table 4-3 indicates programmed OTP Page 2 is available to be programmed. OTP Page1 is either the active configuration or is having a CRC error

Table 4-3. Register Bits Values for only Page 2 Availability

Bit Field Name	Value
USR_OTP_CRC	N/A
USR_OTP_CRC_ERR	0h or 1h
USR_OTP_PAGE_USED	1h
USR_OTP_PG1	1h
USR_OTP_PG2	0h

The values in Table 4-4 indicates both OTP Page 1 and OTP Page 2 are already programmed. OTP Page2 is either the active configuration or is having a CRC error. No further programming is recommended.

Table 4-4. Register Bits Values for no OTP Page Availability

Bit Field Name	Value
USR_OTP_CRC	N/A
USR_OTP_CRC_ERR	0h or 1h
USR_OTP_PAGE_USED	2h
USR_OTP_PG1	0h
USR_OTP_PG2	1h

All other combination of values indicates the status of OTP pages is undefined and no further programming is recommended.

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5 Summary

This user's guide has detailed the procedures for accessing and using the I2C interface on the MC121-Q1, MC121, and MC111 devices for both Test Programming and OTP (One-Time Programmable) Programming modes. Test Programming Mode provides a volatile method for configuring motor performance parameters through I2C, where settings are temporary and revert to default or programmed OTP values upon a power cycle. In contrast, OTP Programming Mode enables permanent configuration storage, requiring a stable supply voltage (V_{VM}) above 8V and a specific unlocking sequence of 2h, 1h, and 4h. To operate these modes, users must follow specific signal requirements on the PWM/DC and FG/RD pins to enter I2C mode. Successful programming requires careful management of the two available OTP pages, using the provided register map to verify CRC integrity, page selection, and programming status. Continuous validation through the status registers is essential so that the correct configuration is loaded and that no errors occurred during the burn process. By following these technical guidelines, engineers can reliably customize device behavior for specific single ohase BLDC applications and provide permanent, stable motor control settings.

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