User's Guide

TPS562212 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS562212 as well as support documentation for the TPS562212EVM evaluation module. This user's guide includes the following information for the TPS562212EVM:

- Performance specifications
- Board layout
- Schematic
- List of materials

Table of Contents

1 Introduction

The TPS562212 is a single, advanced emulated current mode (AECM) control, synchronous buck converter that is able to deliver 2-A continuous output current and provides selectable Eco-mode operation or FCCM operation and a selectable power-good indicator or external soft start by the configuring the MODE pin. Power sequencing is possible by correctly configuring the Enable pin, power-good indicator, or external soft start. The device implements an AECM control, which can get fast transient response with fixed frequency. The fast transient response results in low voltage drop and fixed frequency brings a better jitter permanence and predictable frequency for EMI design. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design over a wide voltage output range. Rated input voltage and output current ranges for the evaluation module are given in Table 1-1.

The TPS562212EVM is a single, synchronous buck converter providing 3.3 V at 2 A from 4.2-V to 18-V input. This user's guide describes the TPS562212EVM performance.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS562212EVM	V_{IN} = 4.2 V to 18 V	0 A to 2 A

2 Performance Specification Summary

A summary of the TPS562212EVM performance specifications is provided in Table 2-1. Test specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 3.3 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. Performance Specifications Summary

SPECIFICATIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		4.2	12	18	V
Output voltage set point			3.3		V
Operating frequency	V_{IN} = 12 V, I_O = 2 A		1200		kHz
Output current range		0		2	A
Output ripple voltage	V_{IN} = 12 V, I_O = 2 A		20		mV_{PP}

3 Modifications

This evaluation module is designed to provide access to the features of the TPS562212. Some modifications can be made to this module.

3.1 MODE Pin Configuration

The TPS562212 has a MODE pin that can offer two different states of operation under light load conditions, and offer two options for the function of Pin 1.

Table 3-1. MODE Pin Settings

MODE RESISTOR RANGE	RECOMMENDED MODE RESISTOR VALUE	OPERATION MODE in LIGHT LOAD	FUNCTION of PG/SS PIN
[0, 12] kΩ	0	Eco-mode	Power Good(1)
[30, 50] kΩ	47 kΩ	Eco-mode	Soft Start
[83, 120] kΩ	100 kΩ	FCCM	Soft Start
[180, ∞] kΩ	Float	FCCM	Power Good

(1) Connect pin 1 to GND to get a better thermal performance if the PG was not used when PG function was selected.

3.2 Output Voltage Setpoint

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using 1% tolerance or better divider resistors. Referring to the application schematic of Figure 6-1, start with 10 kΩ or 20 kΩ for R9 and use Equation 1 to calculate R8. To improve efficiency at light loads, consider using larger value

resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

$$R_8 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \cdot R_9 \quad (1)$$

Table 3-2 lists the R8 and R9 values for some common output voltages. Note that the values given in Table 3-2 are standard values and not the exact value calculated using above equation.

Table 3-2. Recommended Component Values

OUTPUT VOLTAGE(1) (V)	R8(2) (kΩ)	R9 (kΩ)	L1(3) (µH)	C_{OUT} (4) (µF)	RANGE of $L1 \cdot C_{OUT\_E}$ (5) (µH × µF)	C7(6) (pF)
0.76	5.36	20.0	0.68	2 × 22	17 to 130	—
1.05	15.0	20.0	1.0	2 × 22	17 to 130	10 to 100
1.8	40.0	20.0	1.5	1 × 22	15 to 160	10 to 100
2.5	31.6	10.0	1.8	1 × 22	15 to 160	10 to 100
3.3	45.3	10.0	2.2	1 × 22	15 to 160	10 to 100
5	73.2	10.0	3.3	1 × 22	15 to 160	10 to 100

(1) Use the recommended L1 and C_{OUT} combination of the higher and closest output rail for the unlisted output rails.
(2) R8 = 10 kΩ and R9 = Float for V_{OUT} = 0.6 V
(3) Inductance values are calculated based on V_{IN}=18 V, but they can also be used for other input voltages. Users can calculate their preferred inductance value per the *TPS562212 4.2-V-18-V Input, 2-A Synchronous Buck Converter in a SOT-5X3 Package Data Sheet*.
(4) The C_{OUT} is the sum of nominal output capacitance. 22-µF, 0805, 10-V or higher specification capacitors are recommended .
(5) The C_{OUT_E} is the effective value after derating. The value of $L1 \cdot C_{OUT\_E}$ should be within in the range.
(6) R6 and C7 can be used to improve the load transient response and improve the loop-phase margin.

4 Test Setup

This section describes how to properly connect, set up, and use the TPS562212EVM.

4.1 Input/Output Connections

The TPS562212EVM is provided with input/output connectors and test points as shown in Table 4-1. Figure 4-1 shows connectors and jumpers placement on TPS562212EVM board.

A power supply capable of supplying 2 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 2 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP4 as the ground reference.

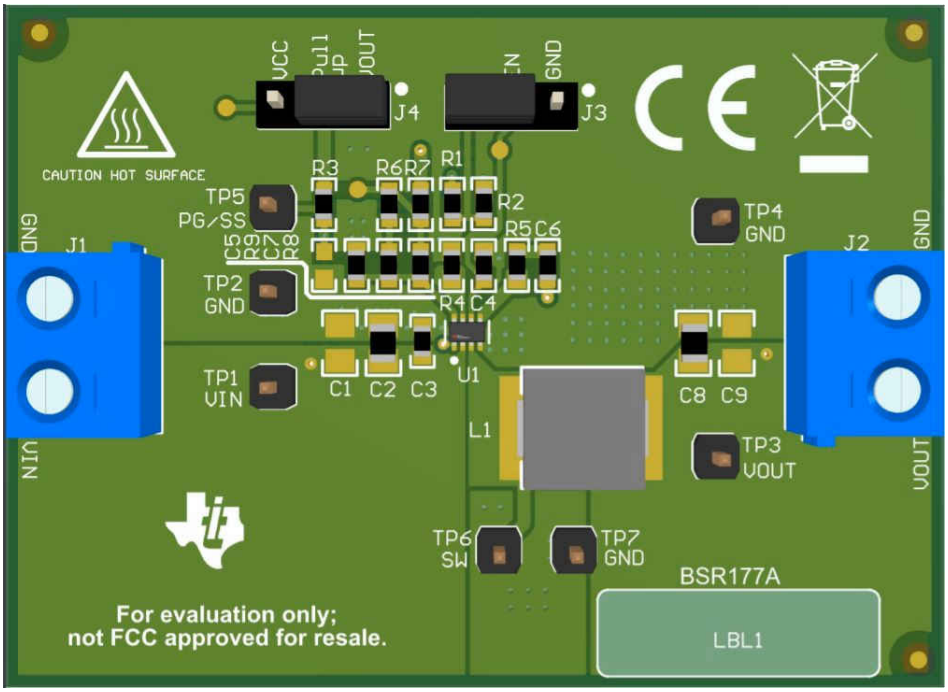

Figure 4-1. Connectors and Jumpers Placement

Table 4-1. Connection and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	V_{IN} (see Table 1-1 for V_{IN} range)
J2	V_{OUT}, 3.3 V at 2 A maximum
J3	EN control. Shunt EN to GND to disable.
J4	Source selection for PGOOD
TP1	V_{IN} positive power point
TP3	V_{OUT} positive monitor point
TP2, TP4, TP7	GND monitor point
TP5	Test point for PG/SS measurment
TP6	Switch node test point

4.2 Start-Up Procedure

1. Ensure that the jumper at J3 (Enable control) pin 1 and 2 are covered to shunt EN to GND, disabling the output.
2. Apply appropriate V_{IN} voltage to VI (J1-2) and GND (J1-1).
3. Move the jumper at J3 (Enable control) pin 1 and 2 (EN and GND) to enable the output.

5 Board Layout

This section provides a description of the TPS562212EVM, board layout, and layer illustrations.

5.1 Layout

The board layout for the TPS562212EVM is shown in Figure 5-1, Figure 5-2, and Figure 5-3. The top layer contains the main power traces for VIN, VOUT, and ground. Also on the top layer are connections for the pins of the TPS562212 and a large area filled with ground. Most of the signal traces are also located on the top side. The input decoupling capacitors, C1, C2, and C3, are located as close to the IC as possible. The input and output connectors, test points, and all of the components are located on the top side. The bottom layer is a ground plane along with the switching node copper fill, signal ground copper fill and the feedback trace from the point of regulation to the top of the resistor divider network. Both the top layer and bottom layer use 2-oz copper thickness.

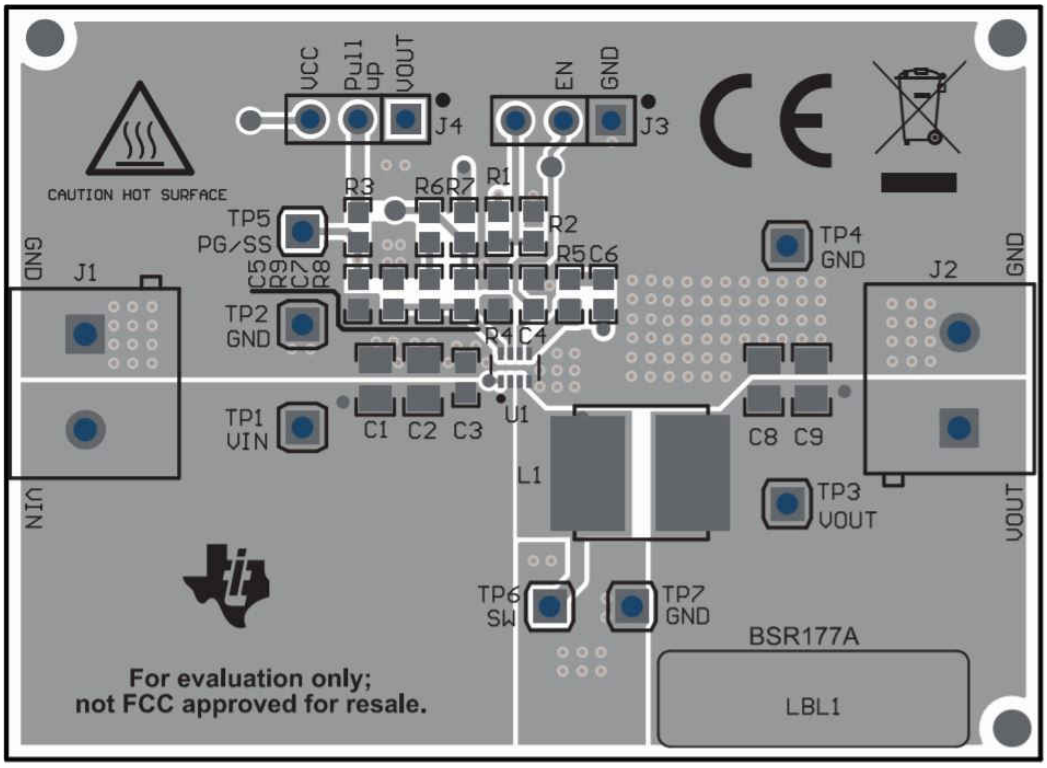

Figure 5-1. TPS562212EVM Top Assembly

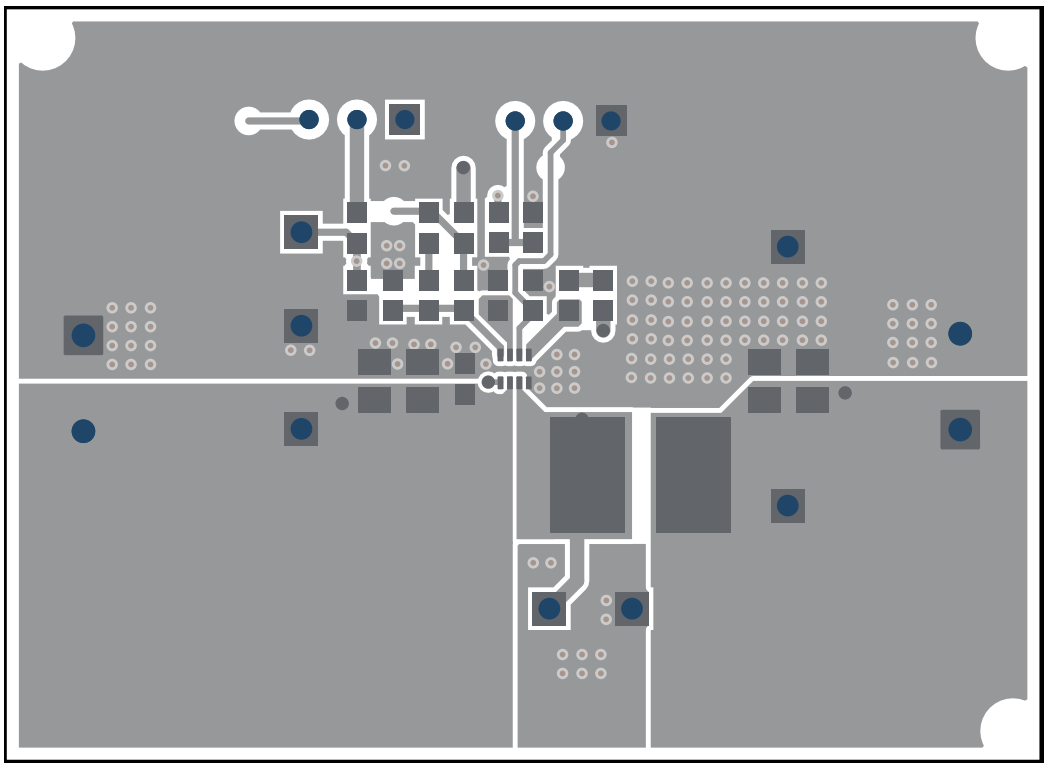

Figure 5-2. TPS562212EVM Top Layer

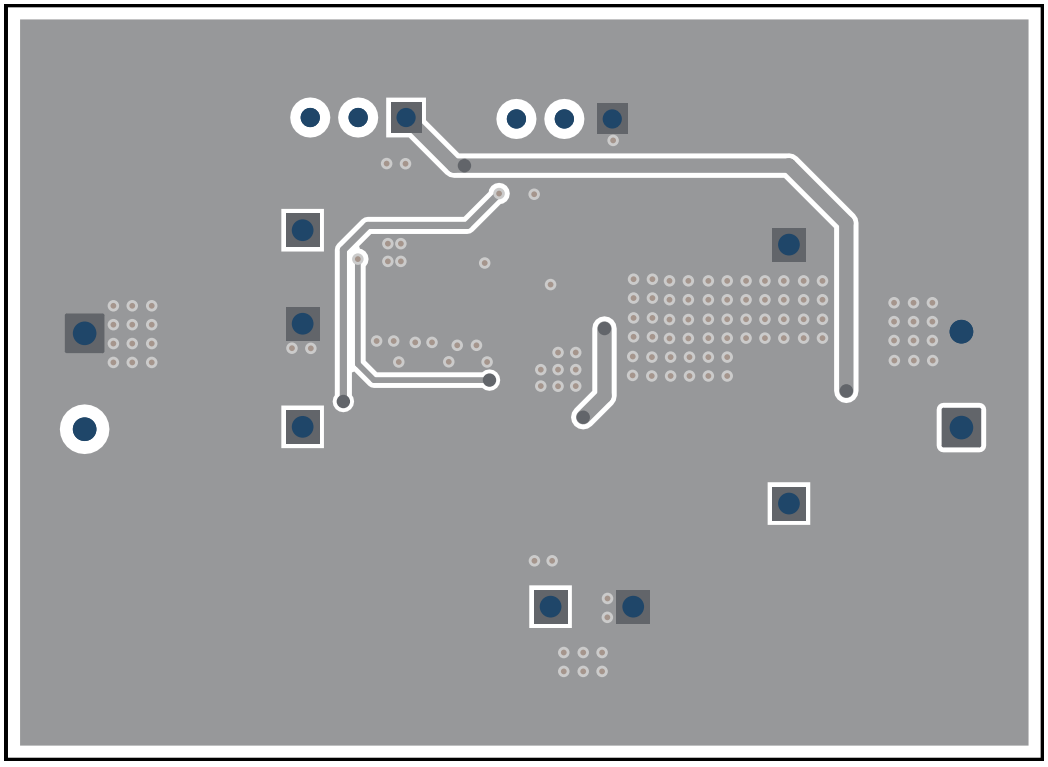

Figure 5-3. TPS562212EVM Bottom Layer

5.2 EVM Picture

Figure 5-4 and Figure 5-5 are the TPS562212EVM board top view and bottom view, respectively.

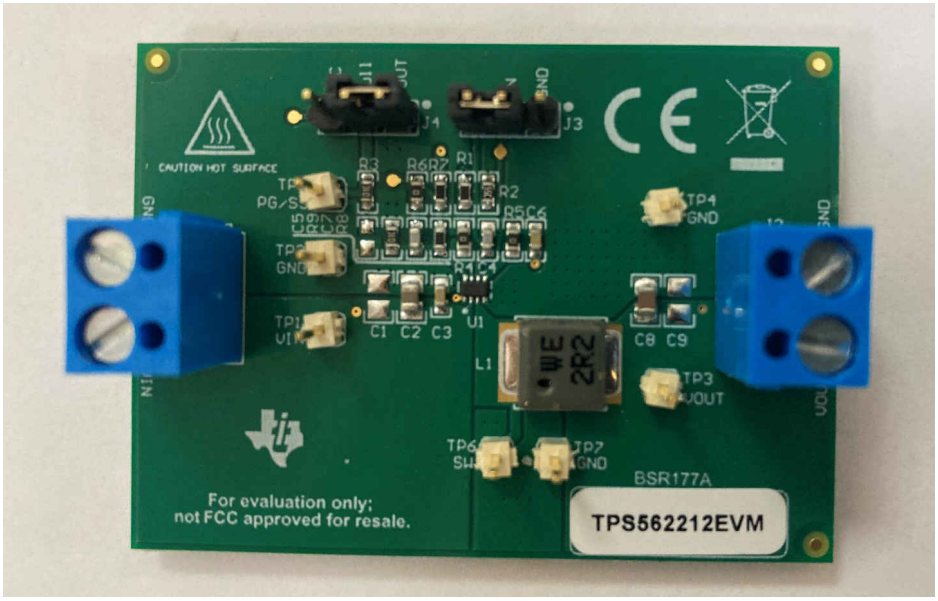

Figure 5-4. TPS562212EVM Board (Top View)

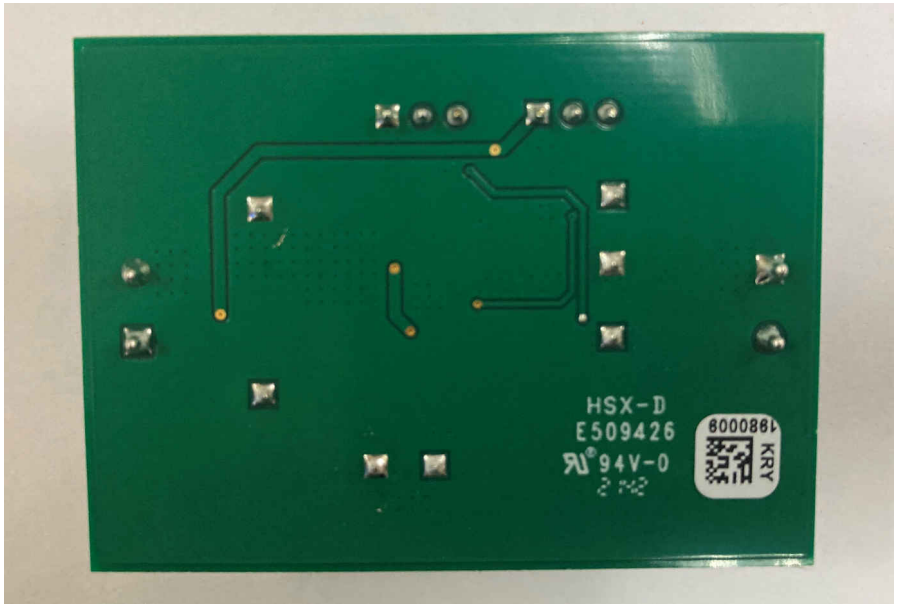

Figure 5-5. TPS562212EVM Board (Bottom View)

6 Schematic, List of Materials, and Reference

6.1 Schematic

Figure 6-1 is the schematic for the TPS562212EVM.

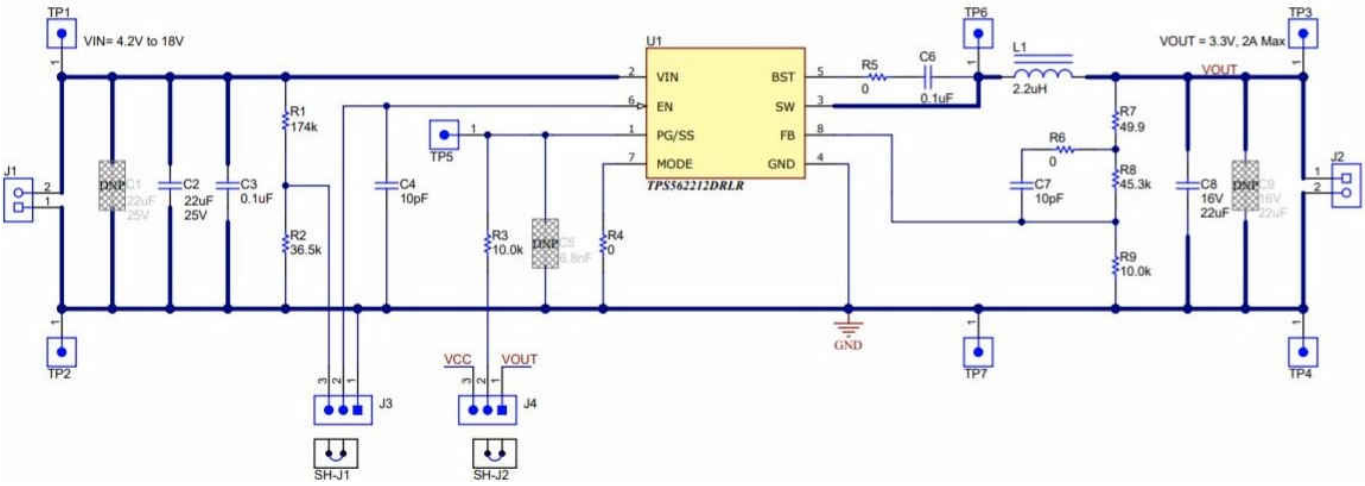

Figure 6-1. TPS562212EVM Schematic Diagram

6.2 List of Materials

Table 6-1 details the EVM list of materials.

Table 6-1. List of Materials

DES	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
!PCB1	1	Printed Circuit Board	BSR177	Any
C2	1	CAP, CERM, 22 µF, 25 V, ±20%, X5R, 0805	GRM21BR61E226ME44L	MuRata
C3, C6	2	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	885012206095	Wurth Elektronik
C4	1	CAP, CERM, 10 pF, 100 V, ±5%, C0G/NP0, 0603	GCM1885C2A100JA16D	MuRata
C7	1	CAP, CERM, 10 pF, 100 V, ±5%, C0G/NP0, 0603	GCM1885C2A100JA16J	MuRata
C8	1	CAP, CERM, 22 µF, 16 V, ±20%, X5R, 0805	GRM21BR61C226ME44L	MuRata
J1, J2	2	Terminal Block, 5.08 mm, 2 × 1, Brass, TH	ED120/2DS	On-Shore Technology
J3, J4	2	Header, 100 mil, 3 × 1, Tin, TH	PEC03SAAN	Sullins Connector Solutions
L1	1	Inductor, Shielded Wirewound, 2.2 µH, 8 A, 0.0105 Ω, SMD	74439344022	Wurth Elektronik
LBL1	1		THT-14-423-10	Brady
R1	1	RES, 174 k, 1%, 0.1 W, 0603	RC0603FR-07174KL	Yageo
R2	1	RES, 36.5 k, 1%, 0.1 W, 0603	RC0603FR-0736K5L	Yageo
R3, R9	2	RES, 10.0 k, 1%, 0.1 W, 0603	RC0603FR-0710KL	Yageo
R4, R5, R6	3	RES, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo
R7	1	RES, 49.9, 1%, 0.1 W, 0603	RC0603FR-0749R9L	Yageo
R8	1	RES, 45.3 k, 1%, 0.1 W, 0603	RC0603FR-0745K3L	Yageo
SH-J1, SH-J2	2	Shunt, 100 mil, Flash Gold, Black	SPC02SYAN	Sullins Connector Solutions
TP1, TP2, TP3, TP4, TP5, TP6, TP7	7	Header, 2.54 mm, 1 × 1, Gold, TH	61300111121	Wurth Elektronik
U1	1	4.2-V to 18-V input, 3-A synchronous buck converter in a SOT583 package	TPS563212DRLR	Texas Instruments
C1	0	CAP, CERM, 22 µF, 25 V, ±20%, X5R, 0805	GRM21BR61E226ME44L	MuRata
C5	0	CAP, CERM, 6800 pF, 50 V, 10%, X7R, 0603	GRM188R71H682KA01D	MuRata
C9	0	CAP, CERM, 22 µF, 16 V, ±20%, X5R, 0805	GRM21BR61C226ME44L	MuRata
FID1, FID2, FID3	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A

7 Reference

Texas Instruments, *TPS562212 4.2-V to 18-V Input, 2-A Synchronous Buck Converter in SOT583 Package Data Sheet*

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