EVM User's Guide: LMG210XEVM-143

LMG210XR022 Evaluation Module

Description

The LMG210XR022 evaluation module (EVM) is a compact, easy-to-use power stage with an external PWM signal. The board can be configured as a buck converter, boost converter, or another converter topology using a half-bridge. The EVM can be used to evaluate the performance of the LMG210XR022 as a hard-switched converter to sample measurements such as efficiency, switching speed and dv/dt (slew rate). The EVM features a LMG210XR022 half-bridge power module with two 100V, 2.2mΩ GaN FETs driven by 80V GaN FET half-bridge gate driver. Do not use to evaluate transient response because this is an open-loop board with an external PWM signal. The EVM is mounted with LMG2104R022 device.

Features

- Input voltage operates up to 80V DC
- Integrated 100V, 2.2mΩ GaN FETs with driver - LMG210XR022
- Open loop control with single or dual PWM signals
- Single-input, onboard for PWM signal with adjustable dead time
- Configurable onboard dead-time adjustment by simple potentiometer change
- Onboard LDO for generating 5V VCC supply from an unregulated supply between 5.5V and 10V
- Kelvin sense capability for efficiency measurements for input and output voltage

Applications

- High-speed synchronous buck and boost converters
- Solar power optimizer, micro inverter
- Class-D amplifiers for audio
- 48V point-of-load converters for industrial
- Motor drives
- Power tools
- Rack and server power

1 Evaluation Module Overview

1.1 Introduction

The LMG210XR022 device is an 100V Gallium Nitride (GaN) half-bridge power module with an integrated driver. The device provides an integrated power stage using enhancement-mode GaN FETs. The LMG210XR022 device consists of two GaN FETs driven by one high-frequency GaN FET driver in a half-bridge configuration. The document shows a circuit and the list of materials describing how to power the board up and how to set the board up for a certain regulation voltage. The EVM board is designed to accelerate the evaluation of the LMG210XR022. This board is not intended to be used as a standalone product, but is intended to evaluate the switching performance of LMG210XR022. The module can deliver up to 45A of current if the application includes adequate thermal management (monitor case temperature and verify adequate airflow is present if required). The thermal management considerations include forced air, heat sink, and lower operating frequency to minimize the power dissipation in the module.

This evaluation module can be configured to either buck or boost mode by providing external gate signals. External heat sink is used to test this module up to 1500W. External supply voltage (5.5V to 10V) is required to power the LMG210XR022 and dead time generation circuit.

1.2 Kit Contents

The kit contains the following:

- Safety instructions
- LMG210XEVM-143 circuit board

1.3 Specification

Parameter	Specifications
V_{in}: input voltage	0V to 80V
V_{out}: output voltage	0V to 80V
V_{cc}: input supply voltage	5.5V to 10V
Maximum power	1500W
Switching frequency	100kHz to 1MHz
Board dimensions	95mm × 71mm × 78mm

1.4 Device Information

The LMG210X device is a family of 100V half bridge power stages, with integrated gate-driver and enhancement-mode Gallium Nitride (GaN) FETs. The devices consist of two 100V GaN FETs driven by one high-frequency GaN FET driver in a half-bridge configuration. GaN FETs provide significant advantages for power conversion as these have zero reverse recovery and very small input capacitance C_{ISS} and output capacitance C_{OSS}. All the devices are mounted on a completely bond-wire free package platform with minimized package parasitic elements. The LMG210x is available in 7.0mm × 4.5mm × 0.89mm lead-free packages and can be easily mounted on PCBs.

The TTL logic compatible inputs can support 3.3V and 5V logic levels regardless of the VCC voltage. A proprietary bootstrap voltage regulation technique makes sure the gate voltages of the enhancement mode GaN FETs are within a safe operating range. The device supports turn-on and turn-off slew-rate control for both FETs, single PWM mode for use with IO-limited controllers, short-circuit protection (SCP), Over-Temperature Detection (OTD) and zero-voltage detection (ZVD) reporting or ideal diode mode to minimize third quadrant conduction time. The device extends advantages of discrete GaN FETs by offering a more user-friendly interface. This is an excellent choice for applications requiring high frequency, high-efficiency operation in a small form factor.

General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's set-up and application instructions, including use of all interface components within the recommended electrical rated voltage and power limits. Always use electrical safety precautions to verify that your personal safety and those working around you. For further information, contact TI's Product Information Center http://ti.com/customer support.

Save all warnings and instructions for future reference.

WARNING
Failure to follow warnings and instructions can result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitably qualified, then immediately stop from further use of the HV EVM.

1. Work Area Safety:
   a. Keep work area clean and orderly.
   b. Qualified observers must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and the interface electronics are energized, indicating operation of accessible high voltages can be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and non-conductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety:
   a. As a precautionary measure, a good engineering practice is to assume that the entire EVM can have fully accessible and active high voltages.
   b. De-energize the TI HV EVM and all the inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   c. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   d. Once EVM readiness is complete, energize the EVM as intended.

   WARNING
   While the EVM is energized, never touch the EVM or the electrical circuits, as the EVM or the electrical circuits can be at high voltages capable of causing electrical shock hazard.
3. Personal Safety
   a. Wear personal protective equipment, for example, latex gloves or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

2 Hardware

2.1 Test Points

Table 2-1. Test Point Functional Description

TEST POINT	DESCRIPTION
TP1	Sense connection for the input supply
TP2	Sense connection for output voltage
TP3	Sense connection for output ground
TP4	Analog Ground sense connection
TP5	Sense connection for switching node, designed for use with oscilloscope probe and spring-type ground connection (TP11) for better measurements
TP6	5V sense connection for LDO output
TP7	Sense connection for the input supply ground
TP8	Sense connection for ZVDL
TP9	Sense connection for ZVDH
TP10	Sense connection for AGND
TP11	Sense connection for PGND of the device
J1	VIN power connector (80V DC maximum)
J2	VOUT power connector (80V DC maximum)
J3	EXT. VCC connection (5.5V - 10V)
J4	MMCX connection for HB-HS measurement
J5	EXT. HB-HS Connector (Optional)
J6	Direct PWM input to HI/LI pins
J7	Connector for PWM IN – Single PWM mode (Uses on-board deadtime generator)
J9	200 mil Jumper

2.1.1 Key Connections

The following test procedure is recommended primarily for powering up and shutting down the evaluation module. Never leave a powered EVM unattended for any length of time. Also, the unit must never be handled while power is applied.

WARNING

There are high voltages present on the EVM. Some components reach temperatures above 50°C. Precautions must be taken when handling the board.

2.1.1.1 Connect a Supply to J3 Connector

There is the bias supply EXTVCC (between 5.5V and 10V) for the LMG210XR022driver. This driver supply is regulated to 5V by the series LDO U2 (LP3869). This regulation verifies that the bias supply for the LMG210XR022 is accurate and is not exceeded beyond the gate voltage specifications. This user's guide refers to this supply as the driver bias supply.

2.1.1.2 PWM Input

There are three ways in which you can provide PWM pulse to the device.

2.1.1.2.1 IIM Mode Using Onboard Dead-Time Generation Circuit (Single PWM Input)-Default Mode

Provide the PWM input using a function generator that is capable of providing the desired switching frequency and duty cycle. This function generator output (0-5V signal) must be connected to the J7 connector as shown in the Figure 2-1. The Pin 1 of J7 is the input of the PWM supply and the Pin 2 is connected to GND. Also make sure Jumper J9 is used to short Pin 3 and Pin 4 of J7 to enable the on-board dead time generation circuit. The potentiometers R2 and R13 generates 5ns to 100ns of dead time.

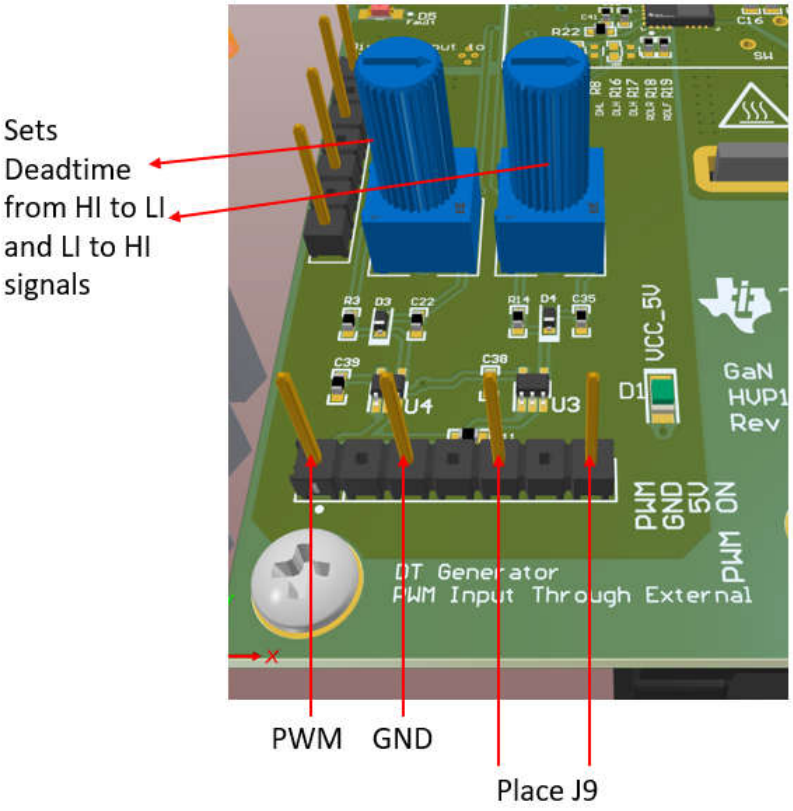

Figure 2-1. IIM Mode Single PWM

2.1.1.2.2 IIM Mode Using Two Separate PWM Inputs (Dual PWM Input)

Two separate PWM inputs can be applied to control HI and LI independently. First, remove jumper J9 placed on pin 3 and pin 4 of J7. Then, apply two separate PWM pulses to J6. HI signal is applied to Pin 2 of J6 and LI signal is applied to Pin 3 of J6. Note, that the EVM no longer generates dead time separating HI and LI transitions. Therefore, careful consideration must be applied to the control signals in this mode of operation to prevent a shoot-through condition. TI recommends to provide at least 5ns of dead time through the external PWM signals.

Make sure that the shunt on pin 3 and pin 4 of J7 is removed to enable this mode.

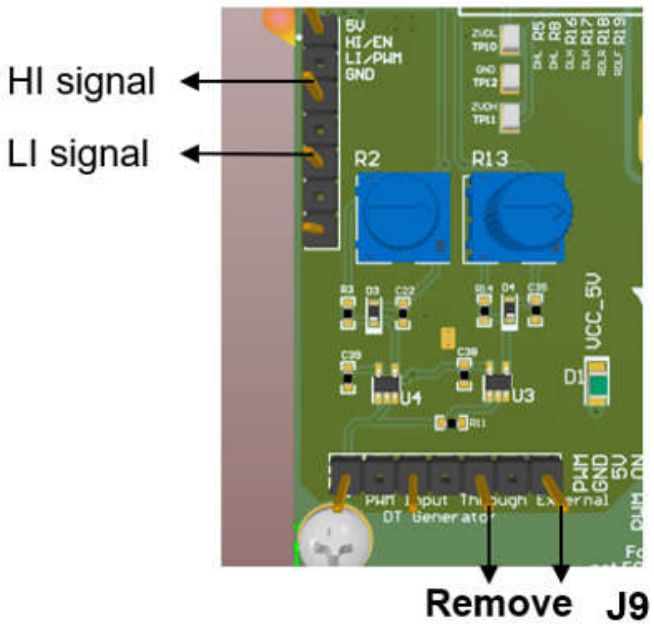

Figure 2-2. IIM Mode Dual PWM

2.1.1.2.3 PWM Input Mode (Single PWM Input)

When used in PWM mode, the LMG210x operates from a single PWM input, with the deadtimes between low-to-high and high-to-low transitions set by external resistors on DLH and DHL pins, respectively. Float RDLF (R19) to enable the PWM mode. Short pin 1 and pin 2 of J6 with jumper J9 to enable the gate drive for both high-side and low-side FET. Single PWM input from the function generator is applied to pin 3 of J6.

Resistors R8 and R17 sets the deadtime for high-to-low transition and low-to-high transition respectively.

Table 2-2. PWM Mode Truth Table

ENIN	PWM	High-side GaN FET	Low-side GaN FET	SW
L	L	OFF	OFF	Hi-Z
L	H	OFF	OFF	Hi-Z
H	L	ON	OFF	VIN
H	H	OFF	ON	PGND

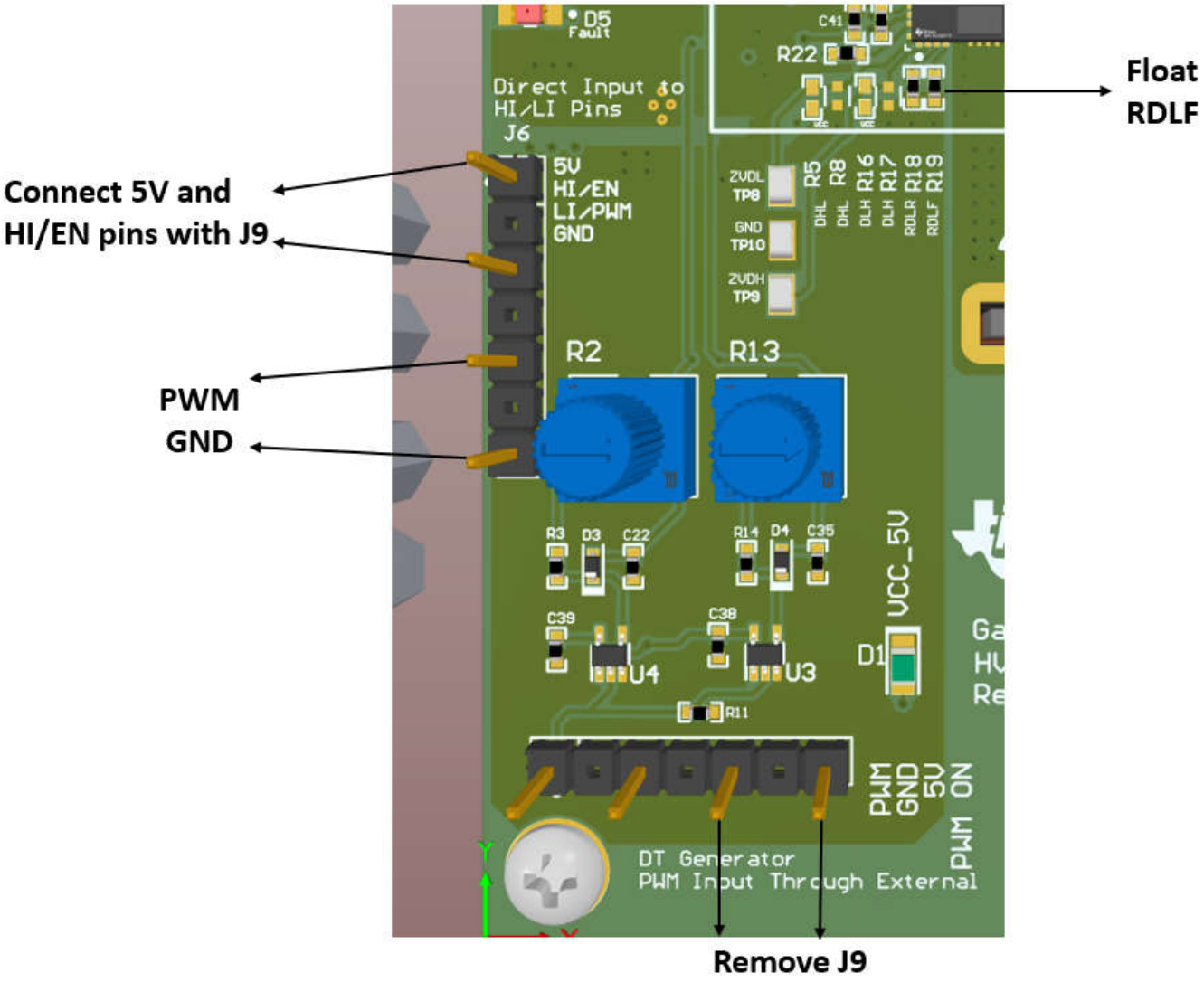

Figure 2-3. PWM Mode Single PWM

2.1.1.3 Resistor controls

2.1.1.3.1 Slew-Rate Control Resistors

The LMG210XEVM-143 offers turn-on and turn-off slew-rate control for both FETs.

R15 (RDHR): Sets the slew-rate control for HS FET turn-on

R20 (RDHF): Sets the slew-rate control for HS FET turn-off

R18 (RDLR): Sets the slew-rate control for LS FET turn-on

R19 (RDLF): Sets the slew-rate control for LS FET turn-off

2.1.1.3.2 Dead-time Control Resistors

Only applicable in PWM mode.

R8 (DHL): sets the dead time for high-to-low transition.

R17 (DLH): sets the dead time for low-to-high transition.

2.1.1.4 Power Supply

Connect the input voltage to the J1 connector and verify that the positive and negative supply is connected appropriately. The positive and negative terminals are marked on the board. The sense connection for the input supply is through the TP1 and TP7 test points, respectively. This is useful when doing efficiency calculations as this verifies that the resistive losses to the board are considered and the losses calculated are related to the board and the LMG210XR022 half bridge.

NOTE

Please remove the TVS Diode (D6) connected to the Input Connector if the Input Voltage applied exceeds 75V.

The output load is connected to the J2 connector. The positive and negative sense signals are TP2 and TP3, respectively.

2.2 Power-Up Procedure

2.2.1 Step 1: Driver Bias Supply

Power up the driver bias supply (5.5V to 10V) first. The D1 diode lights up after the driver bias supply comes up. After this step, apply PWM pulses using one of the three methods in section 2.1.1.2 and observe the PWM signals on Pin 2 and Pin 3 of J6. Verify that the PWM signal for the high and low side are of the desired frequency (100kHz to 1MHz) depending on the input voltage and load). Also observe the default dead time between the high-to-low and low-to-high PWM transitions.

2.2.2 Step 2: Input Supply

Power up the input supply (0V to 80V). The D2 diode lights up after the input supply is powered up. Observe the output voltage on the sense signals (TP2, TP3). Adjust the PWM duty cycle such that the output is of the desired voltage. Load the output with an appropriate electronic load.

Note

The PWM duty cycle must be adjusted to compensate for the losses when the supply is loaded.

2.2.3 Step 3: Measure SW Voltage

To observe the SW node, connect a tip and barrel probe to SW node and PGND as shown in Figure 2-4. This verifies that the measurement loop is small and, hence, accurately reflects the behavior of the SW node. If a large loop is used, due to the high dv/dt on the SW node and the parasitic impedance (inductance) of the loop, then a large amount of ringing is observed on the SW node measurements. This ringing is not representative of the device performance, but is rather a measurement artifact. The probe connection must be made prior to the board being powered up and one must verify that appropriate safety precautions are taken. Pads for TP5 and TP11 are provided on the bottom side to make the measurement convenient, if the heat sink is used.

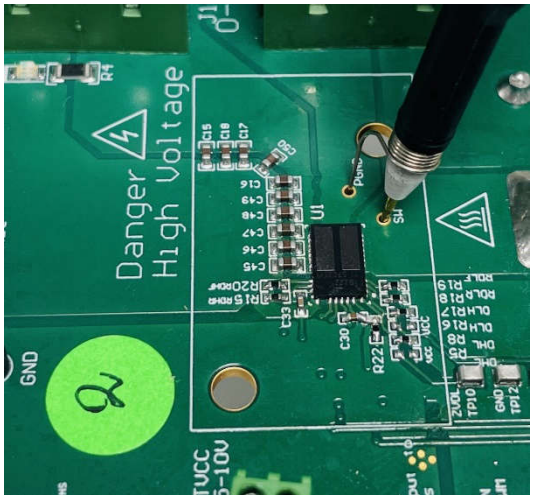

Figure 2-4. Measuring SW Node

2.2.4 Setting Dead-Time

Dead times are set by the RC delays between the inverted and non-inverted PWM input connected to jumper J7. The dead time typically does not require to be changed, however to evaluate impact of dead time on efficiency, the user can vary the RC delay. Changing the potentiometer R2 and R13 to get the appropriate dead time does not take much time. The Minimum deadtime when the potentiometers are set to 0 gives a 5ns Deadtime.

2.3 Power-down Procedure

To power down the board, the power-up procedures must be followed in reverse.

- The load must be turned off first.
- Next, turn off the input supply.
- The PWM signal must be turned off next.
- Finally, turn off the driver bias supply.

2.4 Zero Voltage Detection (ZVD) Reporting

The LMG210xEVM-143 supports Zero-Voltage Detection (ZVD) to indicate whether the high-side and low-side FETs transitioned to third-quadrant in any transition. This information is reported on ZVDH (for high-side FET) and ZVDL (for low-side FET) pins. This feature is only available in the IIM mode.

Test points TP8 and TP9 shows the ZVDL and ZVDH signals, respectively.

2.5 Ideal Diode Mode

The LMG210xEVM-143 supports Ideal Diode Mode (IDM) to minimize the third quadrant conduction time for both high-side and low-side FETs for soft-switching applications. The IDM for the high-side FET is enabled by floating the RDHR pin (R15). The IDM for the low-side FET is enabled by connecting ZVDL pin to VCC this can be done by shorting R5 with a 0Ω resistor.

2.6 Fault Detection

The LMG210XR022 indicates three kind of faults on the EN/FLT pin: short-circuit event on the low-side GaN FET, UVLO event on the VCC supply, and over-temperature event on the driver. Once asserted, the active low fault signal remains asserted as long any of the three faults exist, and the Fault LED D5 turns on indicating Fault.

2.7 Assembly Guidelines

Follow the recommended assembly guidelines for the LMG210XR022 samples:

- Use low temperature solder paste (like Sn42-Bi58) of which the melting temperature is around 130℃-140℃.
- Soldering using bottom side heating:
  - Recommended for thinner board (less than or equal to four layers) with no components directly underneath the device.
  - Place the solder paste as per the stencil recommendation given in the data sheet.
  - Board held on a pedestal at around 2-3 cm from the top of the hot air blower and device is aligned to keep on the footprint.
- Soldering using top side heating:
  - This method is recommended for thicker board (more than 4 layers).
  - Use hot air gun (with temperature set to 400℃) and blow the air around the device avoiding directly above the device (temperature can be higher but used for shorter duration).
- Look for proper soldering connection of signal pins. If there are excess solder, then please remove them manually using solder iron.
- Avoid putting excess solder paste especially near the edge of PGND pad (pin number 6).
- If the assembly is done through automatic reflow oven, then set the temperature to less than 180℃.

3 Implementation Results

3.1 Electrical Performance Specifications

The inductor used in this EVM is a 15µH inductor which is rated for 45.3A. There are chances of heating up this inductor if operated at higher switching frequency and higher current level. Please monitor the temperature of the inductor and add external fan cooling if necessary. The switching frequency is set by an external PWM signal (between 0V and 5V). The duty cycle of this PWM signal sets the duty cycle of the half-bridge module.

3.1.1 Evaluation Setup

This section describes the EVM hardware and outlines the procedure to set up for evaluation. The images below show the top and bottom views of the LMG210XEVM-143, respectively.

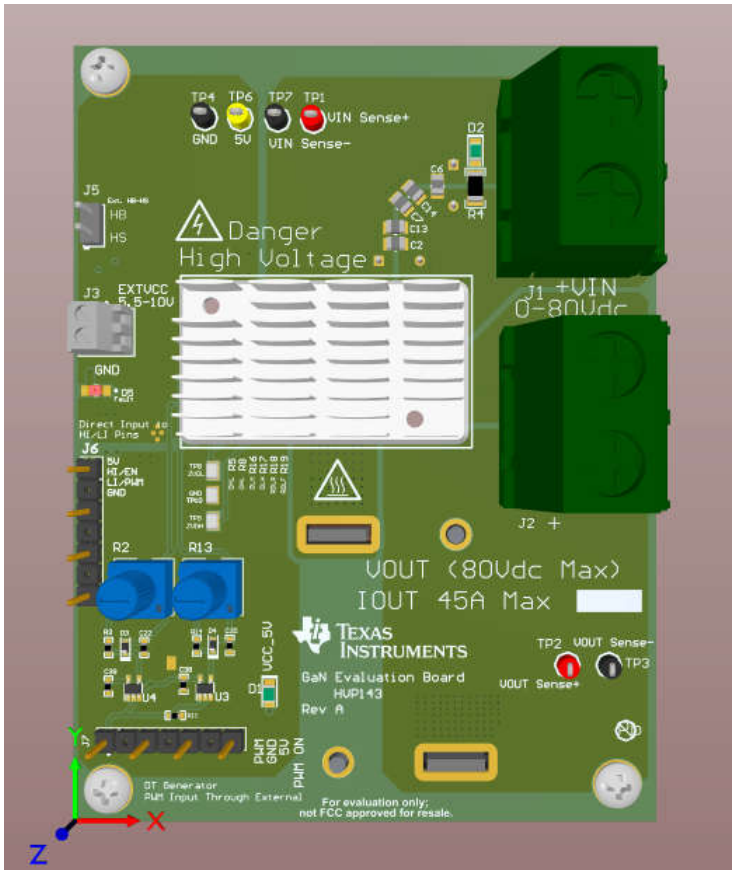

Figure 3-1. LMG210XEVM-143 Board (Top View)

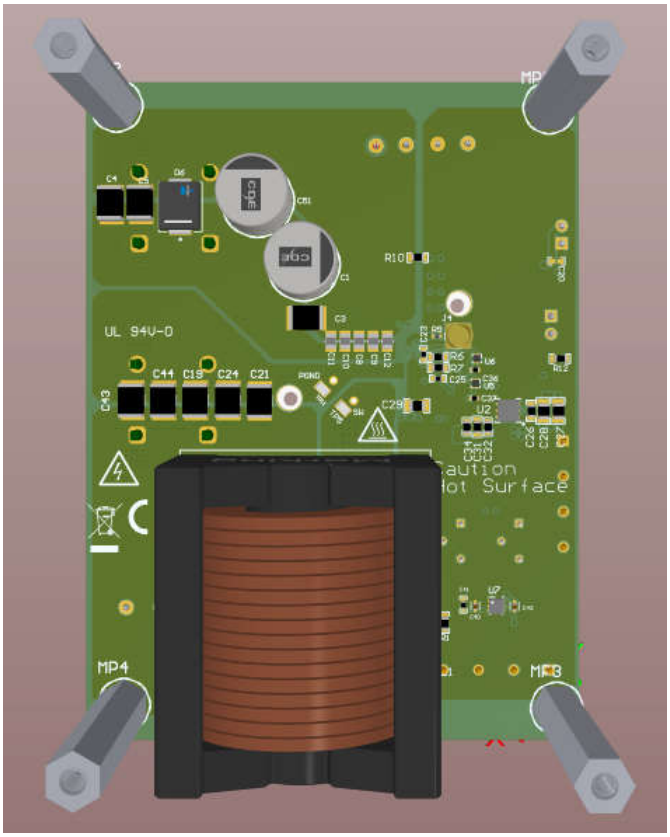

Figure 3-2. LMG210XEVM-143 Board (Bottom View)

The EVM can be mounted with a heat sink (S05MZZ37, 20mm × 35mm × 10mm) to improve the thermal performance. The two exposed thermal pads have a high-voltage potential difference between them, therefore an electrically isolated thermal interface material (TIM) is used. TIM of GR80A-0H-50GY has been placed between the device and the heat sink.

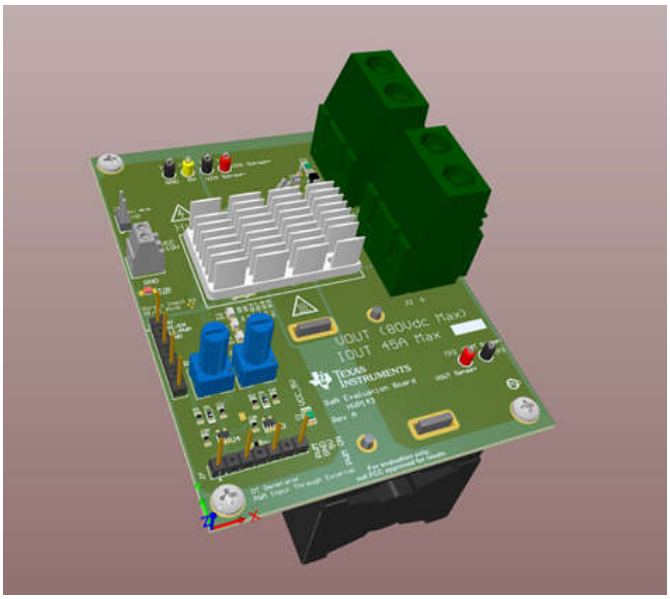

Figure 3-3. Evaluation Module with Heat Sink

3.2 Performance Data and Results

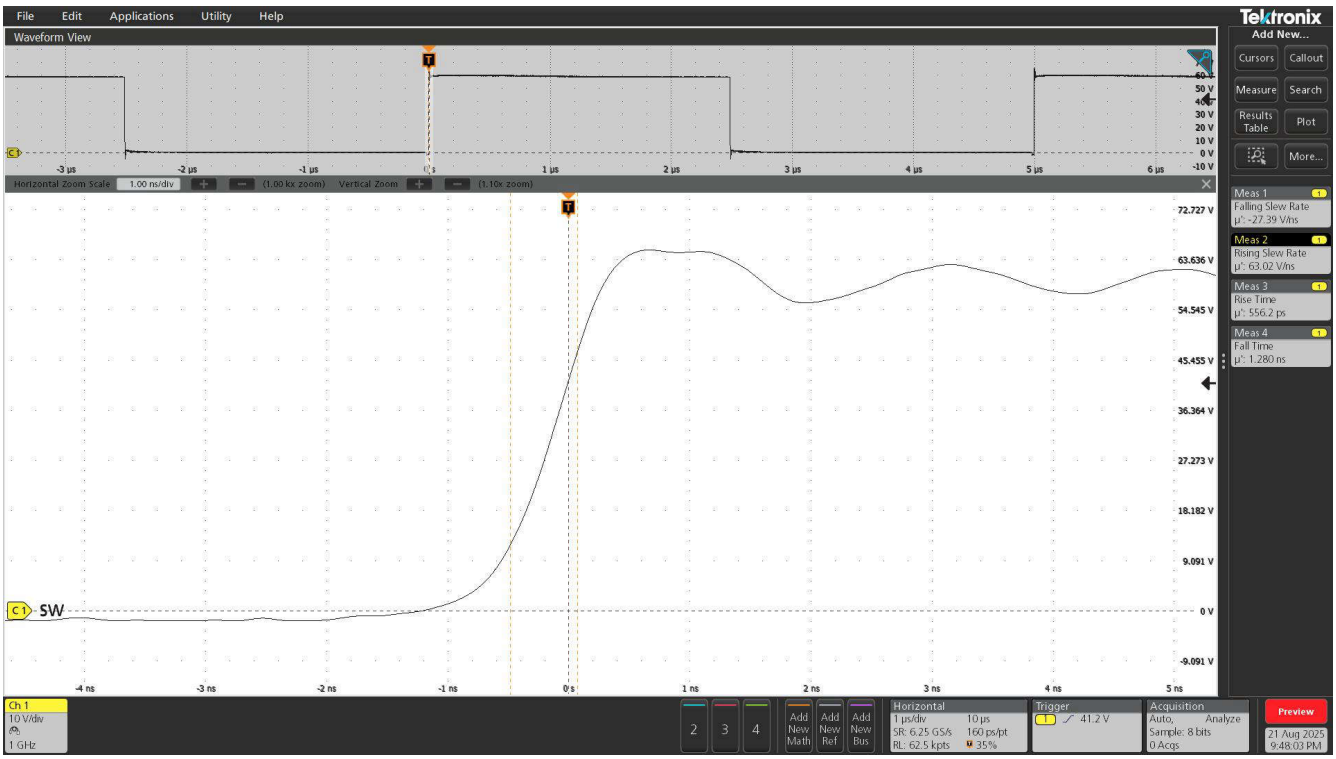

Figure 3-4. SW Voltage Rise with RDHR, RDHF, RDLR, RDLF Set to 0kOhm

Switching node behavior for 60V-30V 20A load buck at 200kHz with RDHR, RDHF, RDLR, RDLF resistors set to 0kOhm. Rising Slew rate- 63V/ns, Falling Slew rate-27.4V/ns.

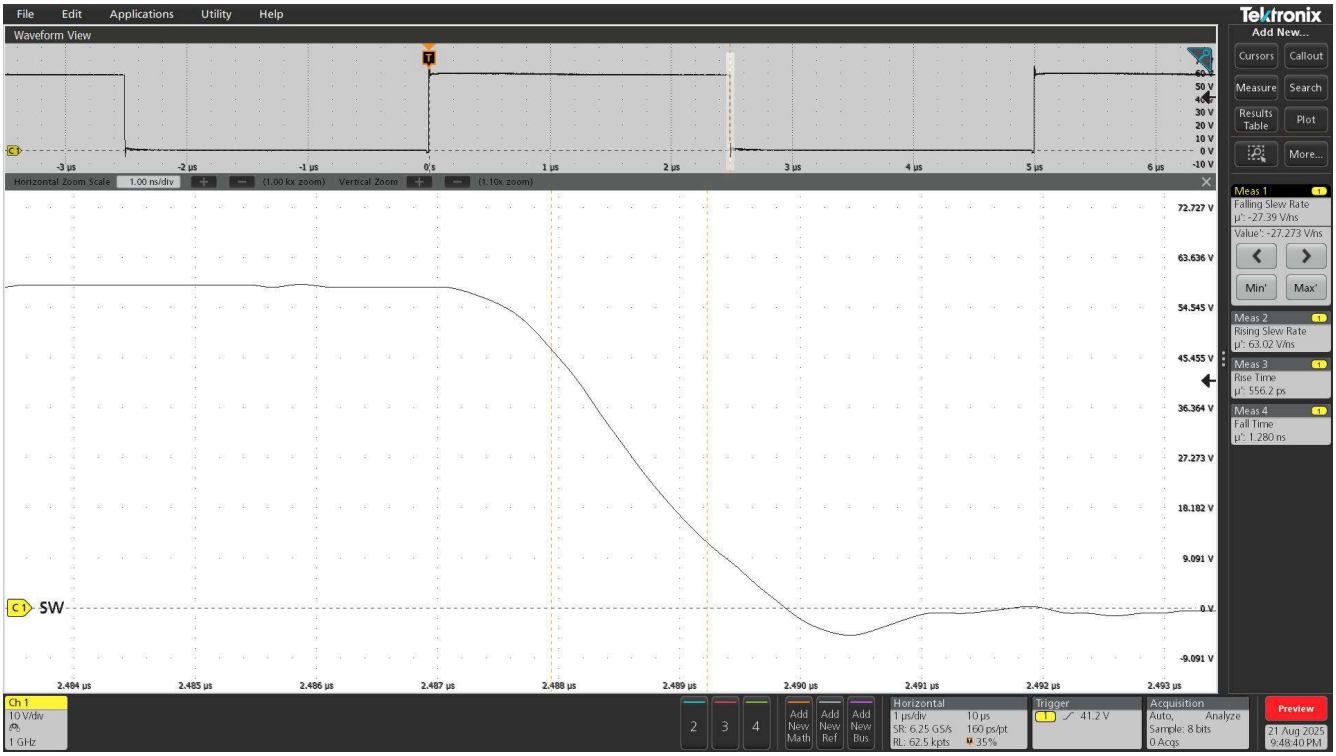

Figure 3-5. SW Voltage Fall with RDHR, RDHF, RDLR, RDLF Set to 0kOhm

Switching node behavior for 60V-30V 20A load buck at 200kHz with RDHR, RDHF, RDLR, RDLF resistors set to 8kOhm. Rising Slew Rate-7.4V/ns, Falling Slew rate - 10V/ns

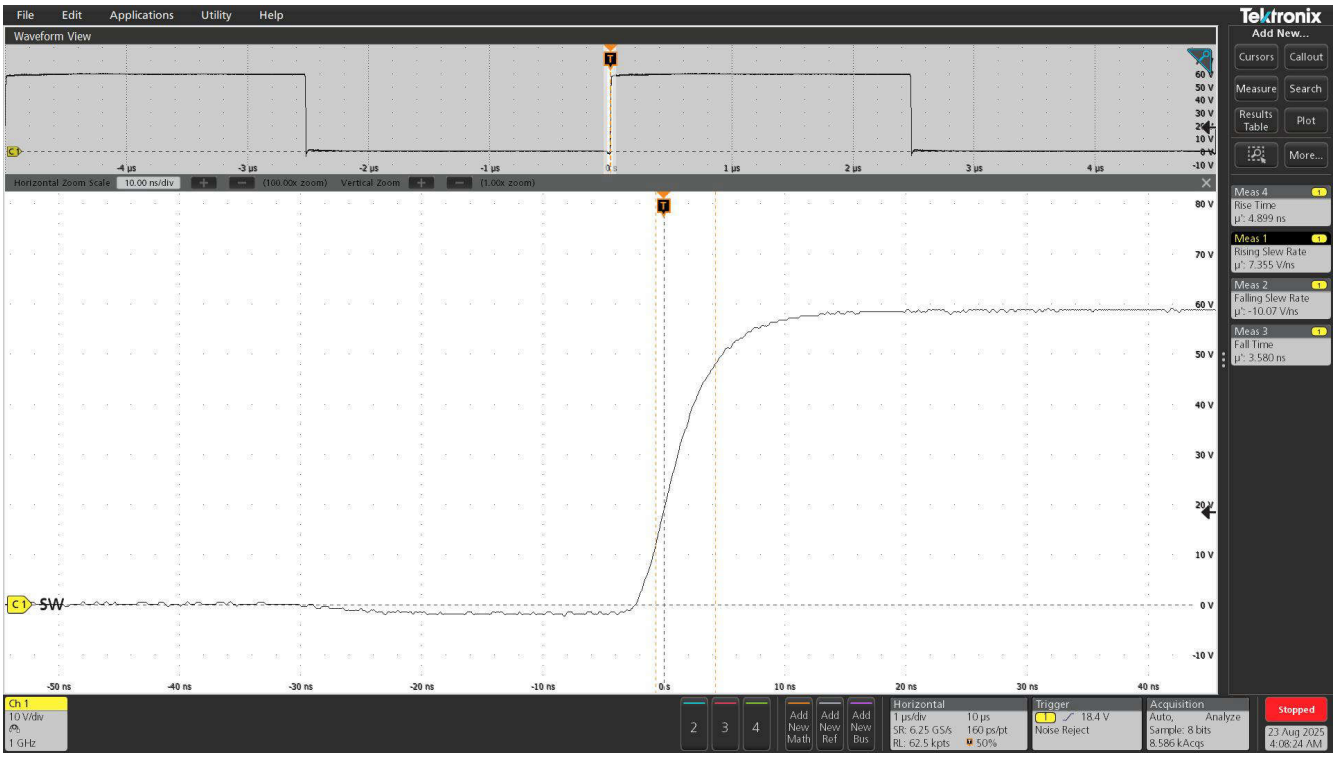

Figure 3-6. SW Voltage Rise with RDHR, RDHF, RDLR, RDLF Set to 8kOhm

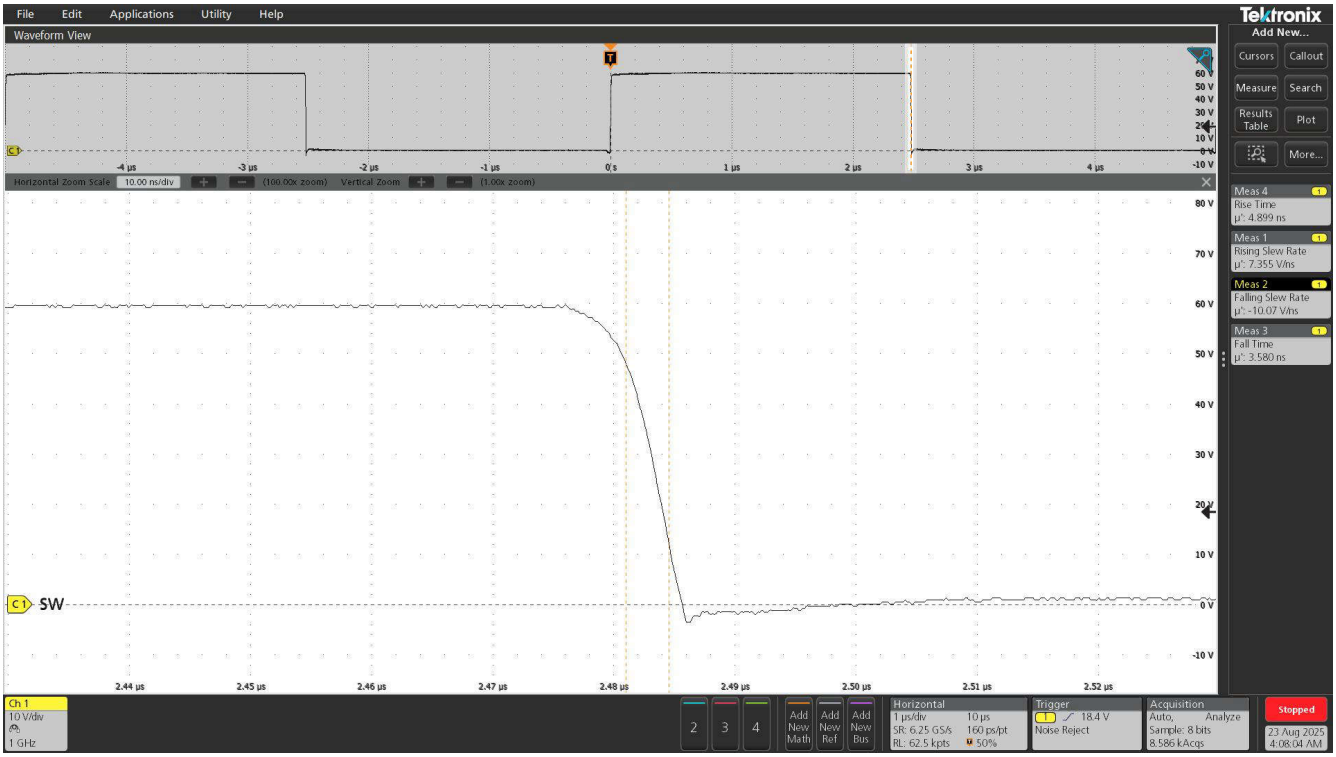

Figure 3-7. SW Voltage Fall with RDHR, RDHF, RDLR, RDLF Set to 8kOhm

Switching node behavior for 60V-30V 20A load buck at 200kHz with RDHR, RDHF, RDLR, RDLF resistors set to 16kOhm. Rising Slew rate-4.7V/ns, Falling Slew rate-6.4V/ns

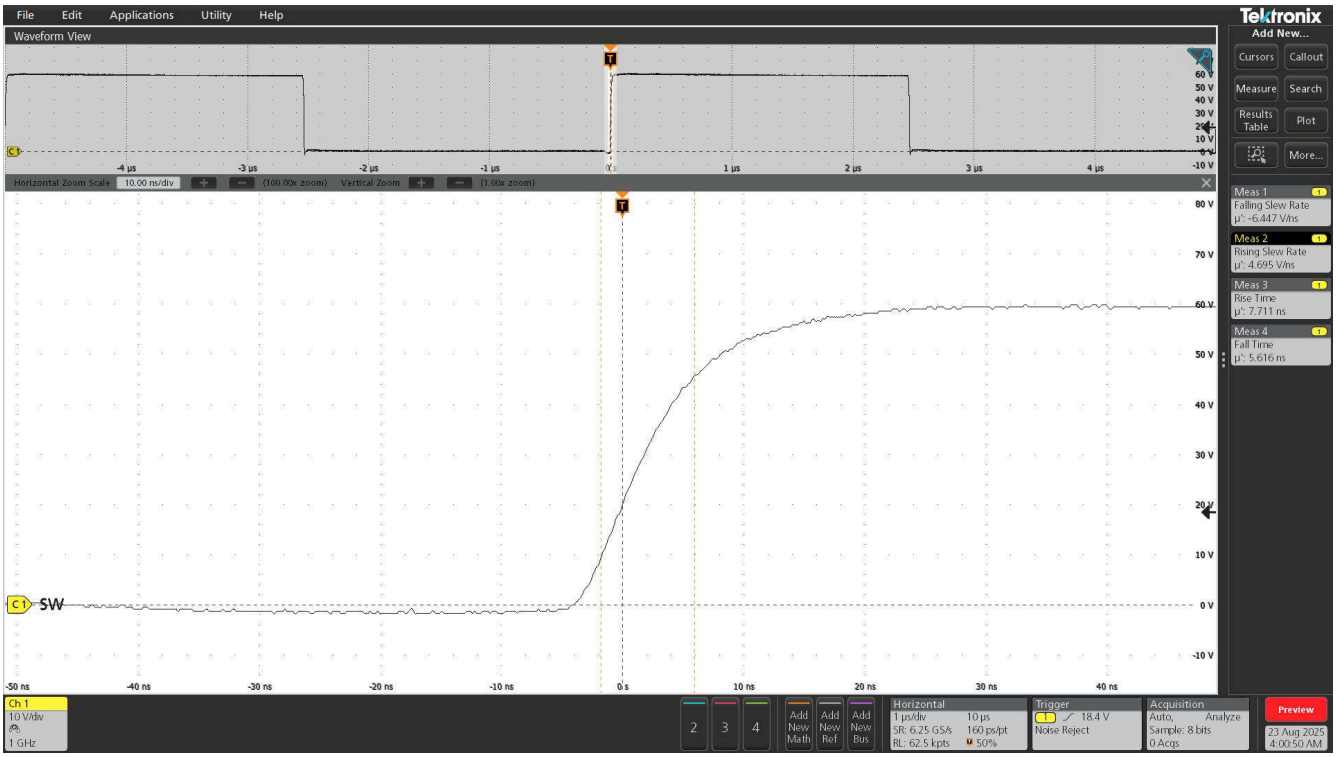

Figure 3-8. SW Voltage Rise with RDHR, RDHF, RDLR, RDLF Set to 16kOhm

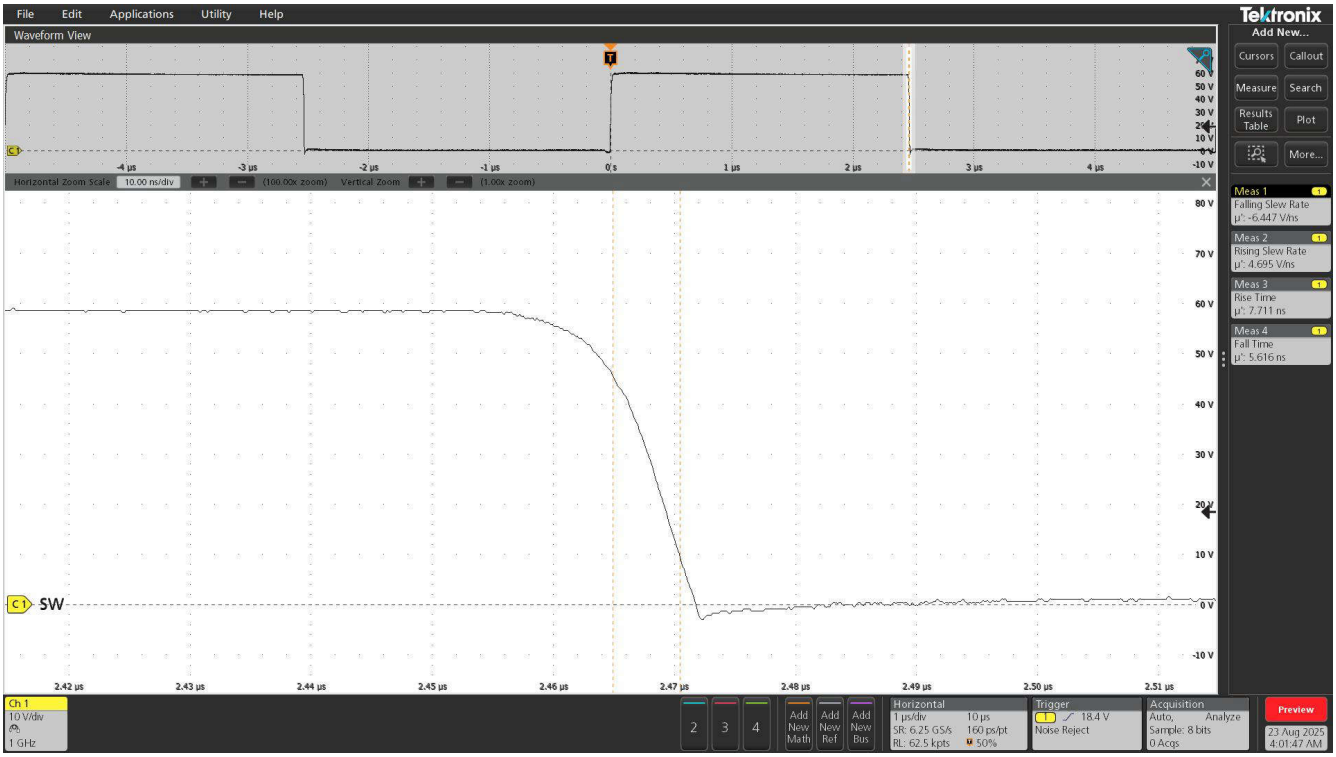

Figure 3-9. SW Voltage Fall with RDHR, RDHF, RDLR, RDLF Set to 16kOhm

Switching at 200kHz, 60V-30V at 20A load.

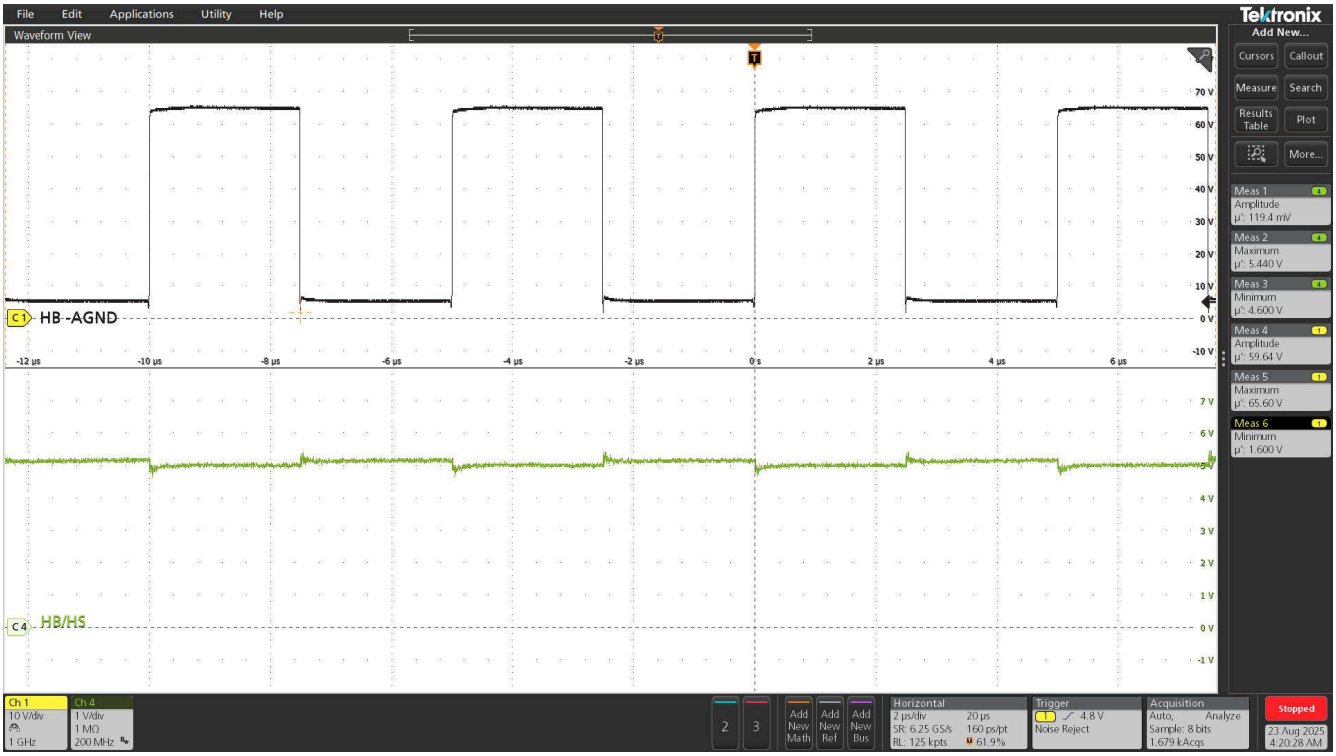

Figure 3-10. HB-AGND and HB-HS Waveform

PWM mode at 200kHz, 60V-30V at 20A load showing dead time between LI fall and HI rise and HI fall and LI rise with DLH and DHL set to 10kOhm.

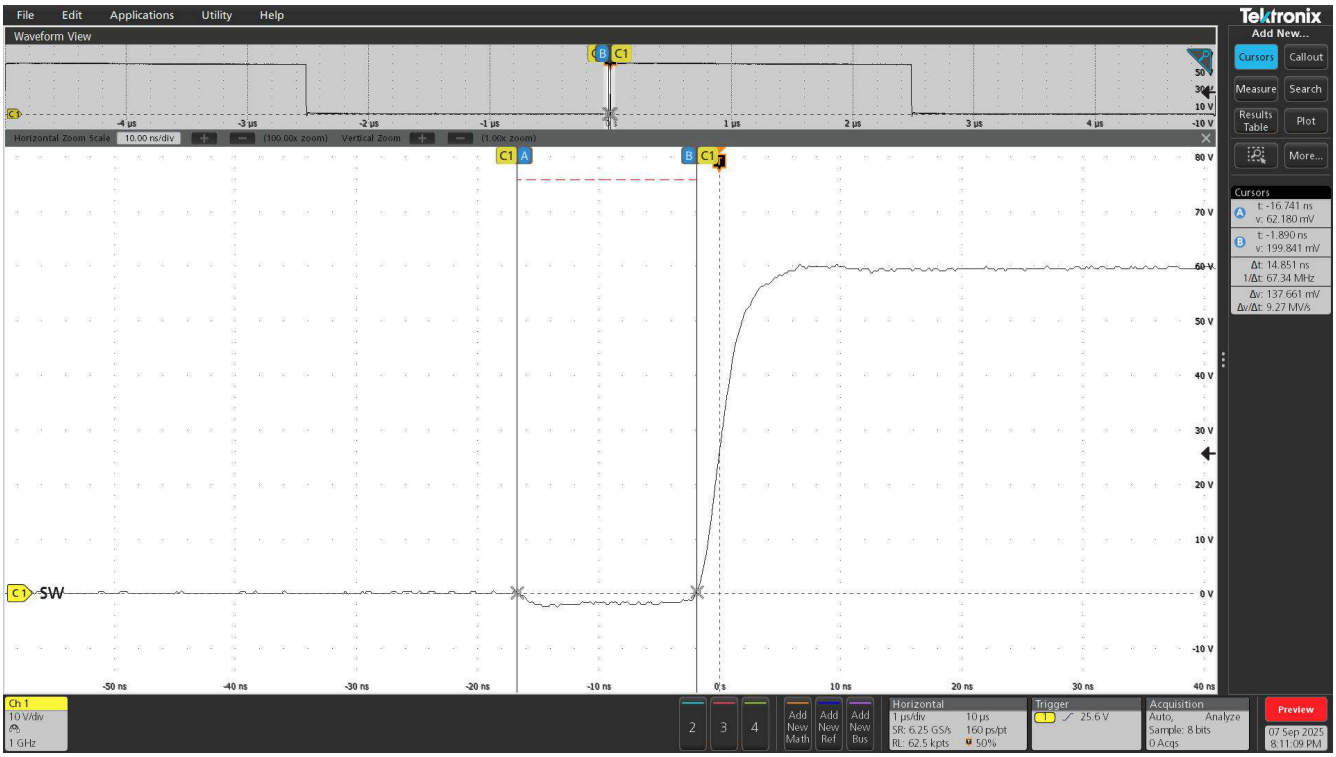

Figure 3-11. PWM Mode Deadtime Between LI Fall to HI Rise

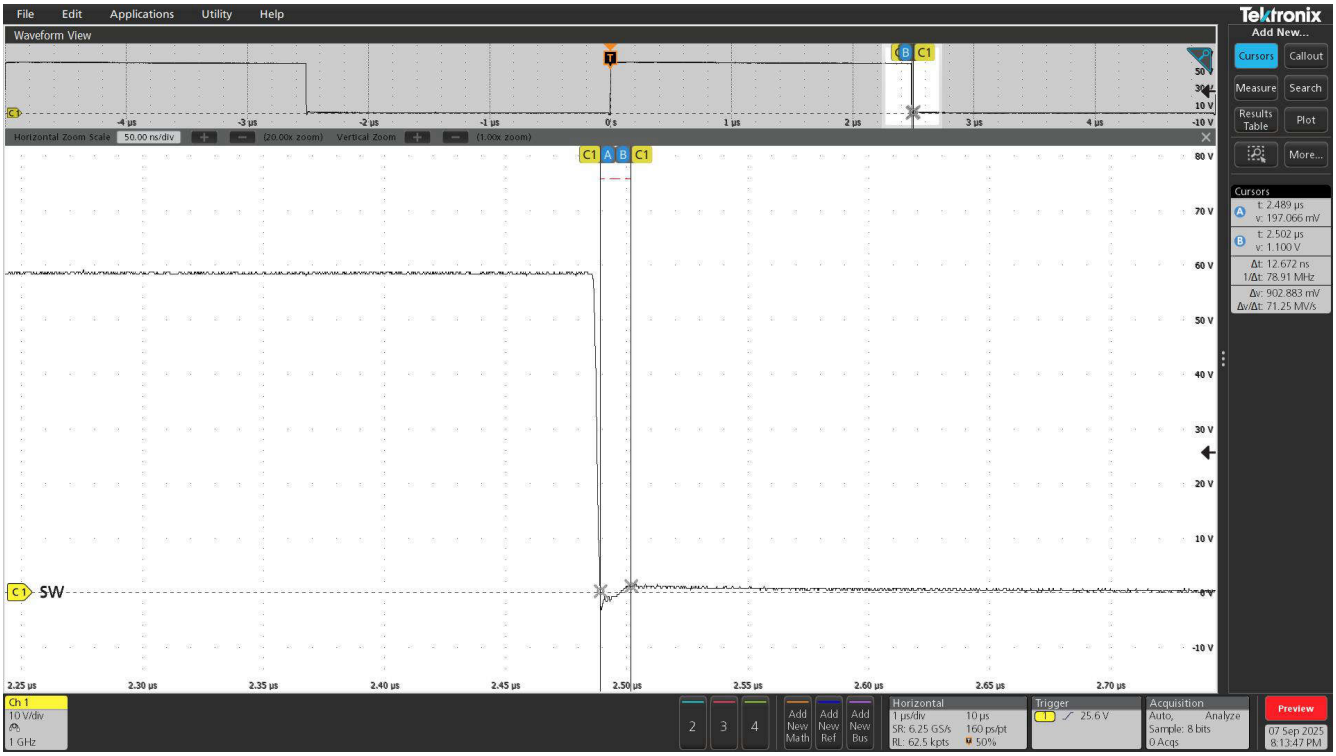

Figure 3-12. PWM Mode Deadtime Between HI Fall to LI Rise

Zero voltage detection for high-side FET and low-side FET at 60V-30V no load.

Figure 3-13. ZVDH and ZVDL Reporting

Here, the ZVDH is reported 1 pulse delayed and ZVDL is reported in the same pulse.

Ideal diode mode for high-side FET and low-side FET.

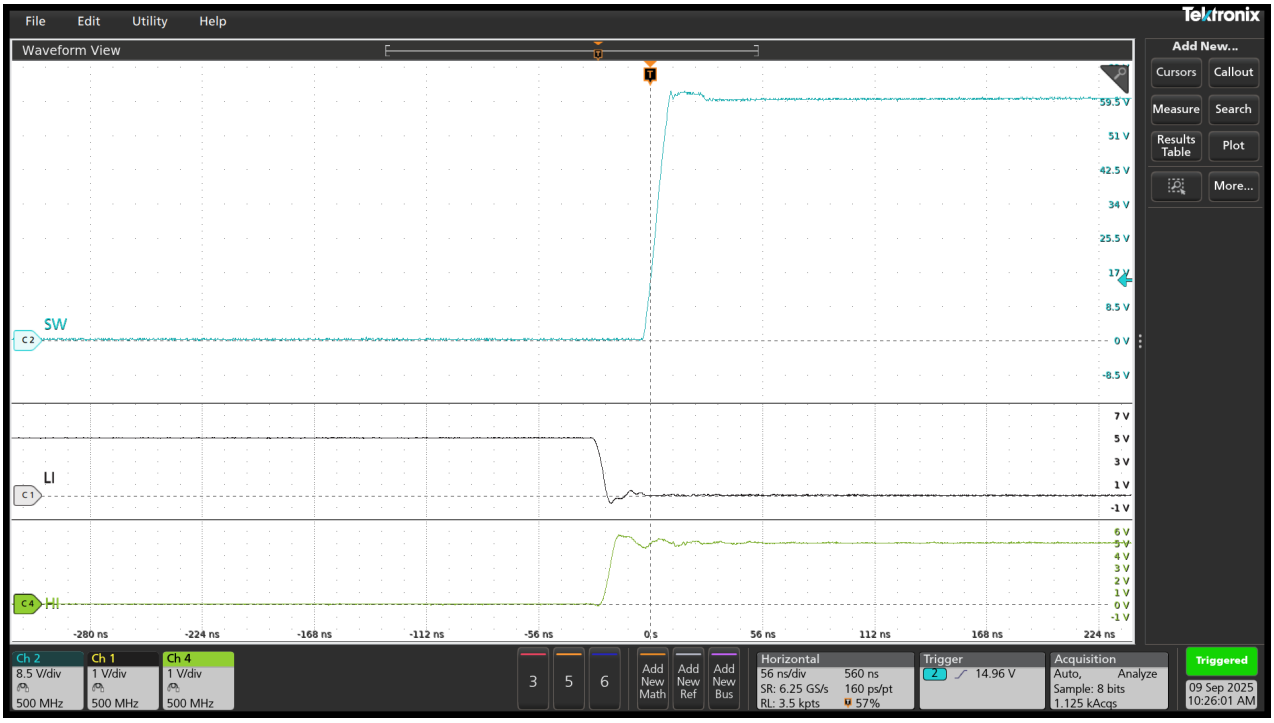

Figure 3-14. IDM for HS FET

IDM for HS FET is enabled and HI=High. The device waits for the switch node (SW) to complete soft-switching and transition VTHRESH_ZVD above VIN. At that point, the high-side device is turned on.

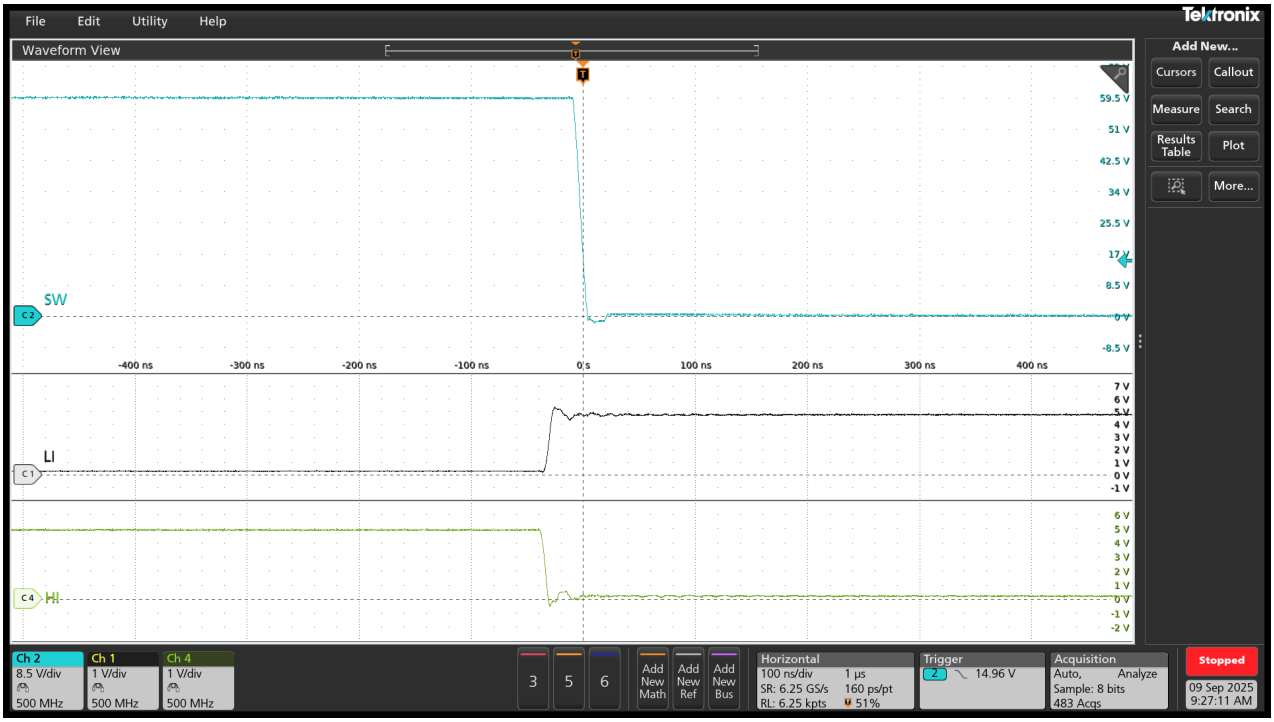

Figure 3-15. IDM for LS FET

IDM is enabled for LS FET, and LI=High. the device waits for the switch node (SW) to complete soft-switching and transition VTHRESH_ZVD below AGND.

3.2.1 Efficiency Results

Efficiency data for Buck and Boost configurations for the EVM Board.

Conditions: 250kHz with 15ns of deadtime between HI and LI pulses.

Table 3-1. Buck Configuration, 60V to 30V with 10A, 20A, and 25A Loads

V_IN(in V)	I_IN(in A)	V_OUT(in V)	I_OUT(in A)	Efficiency
59.92	5.01	29.7	10	98.8
59.81	10	29.43	20	98.37
59.77	12.49	29.26	25	97.93

Table 3-2. Boost Configuration, 30V to 60V with 5A, 7.5A, and 10A Loads

V_IN(in V)	I_IN(in A)	V_OUT(in V)	I_OUT(in A)	Efficiency
29.8	9.8	58	5	99.2
29.56	14.9	57.67	7.5	98.4
29.4	19.76	56.7	10	97.83

4 Hardware Design Files

4.1 Schematics

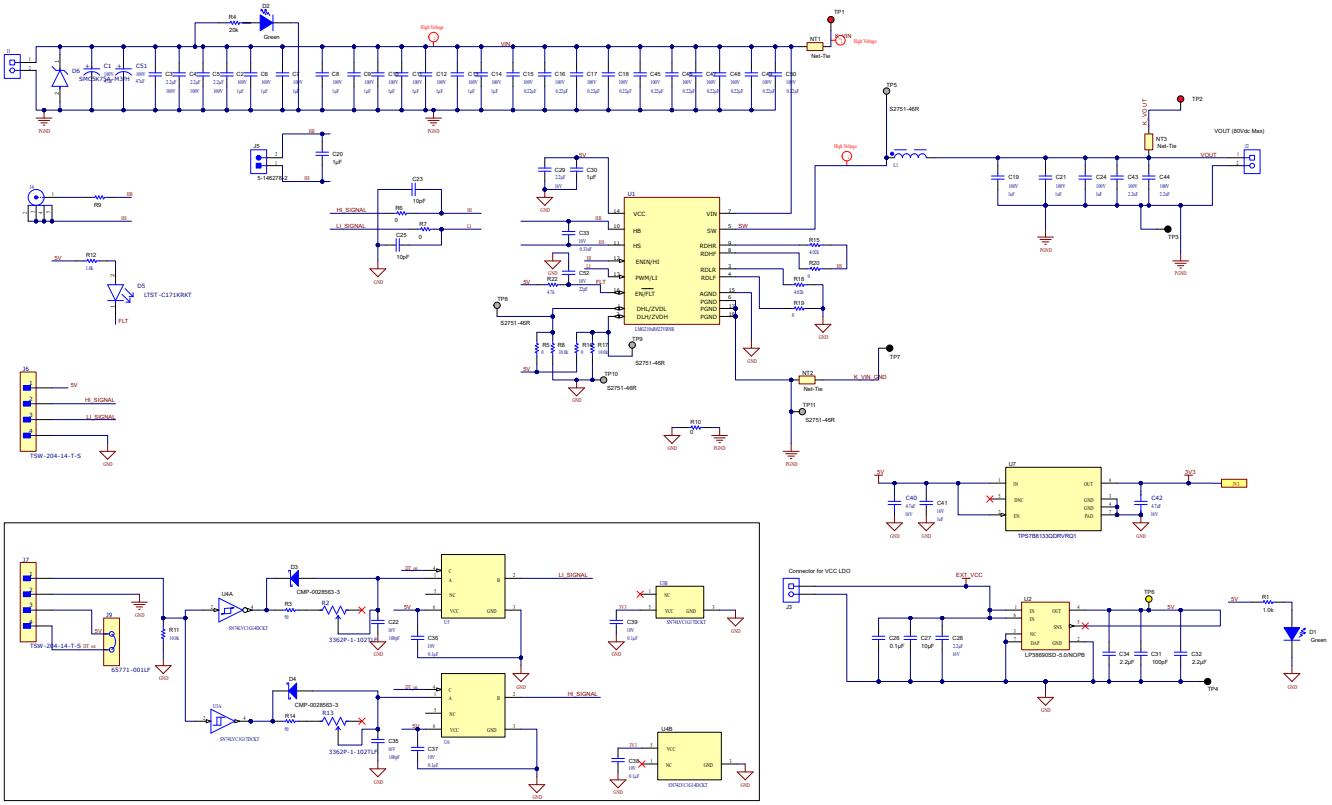

Figure 4-1. LMG210XEVM-143 Schematic

4.2 PCB Layouts

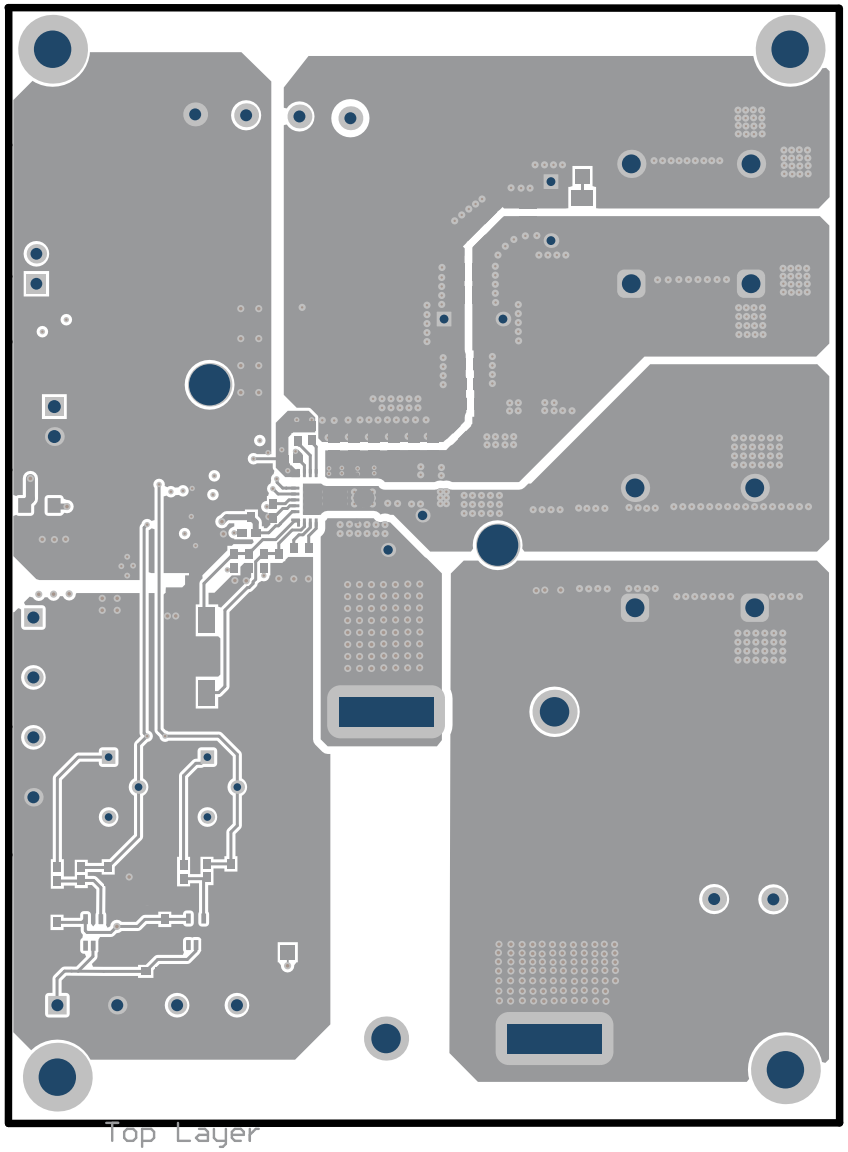

Figure 4-2. Top Layer of PCB

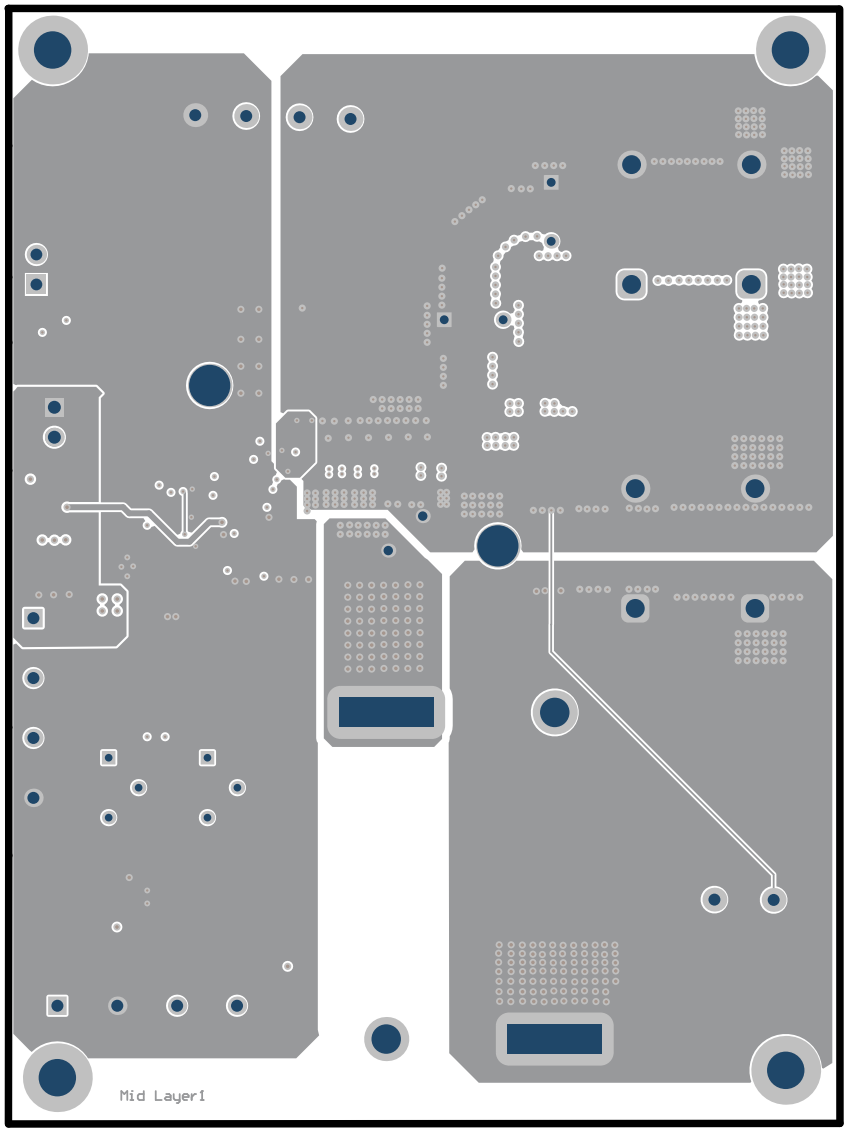

Figure 4-3. Mid Layer -1 Showing Return Path For Power Loop

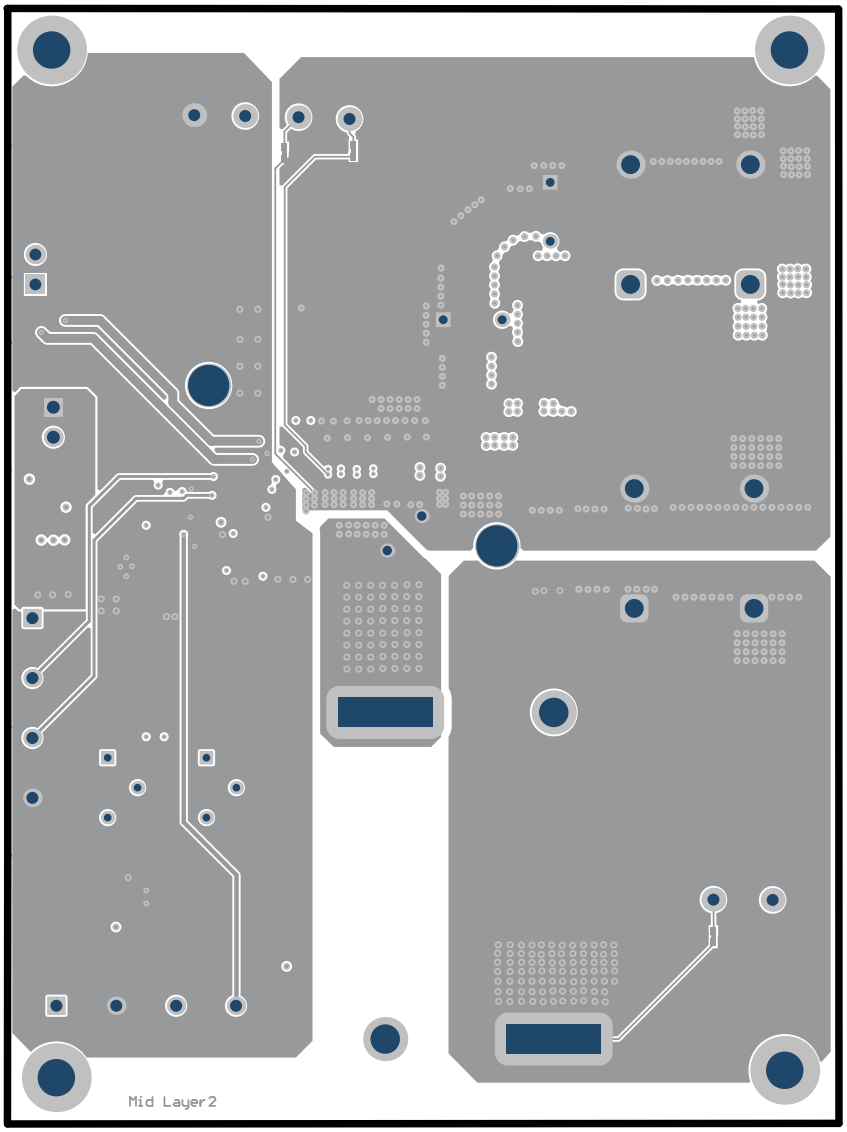

Figure 4-4. Mid Layer-2

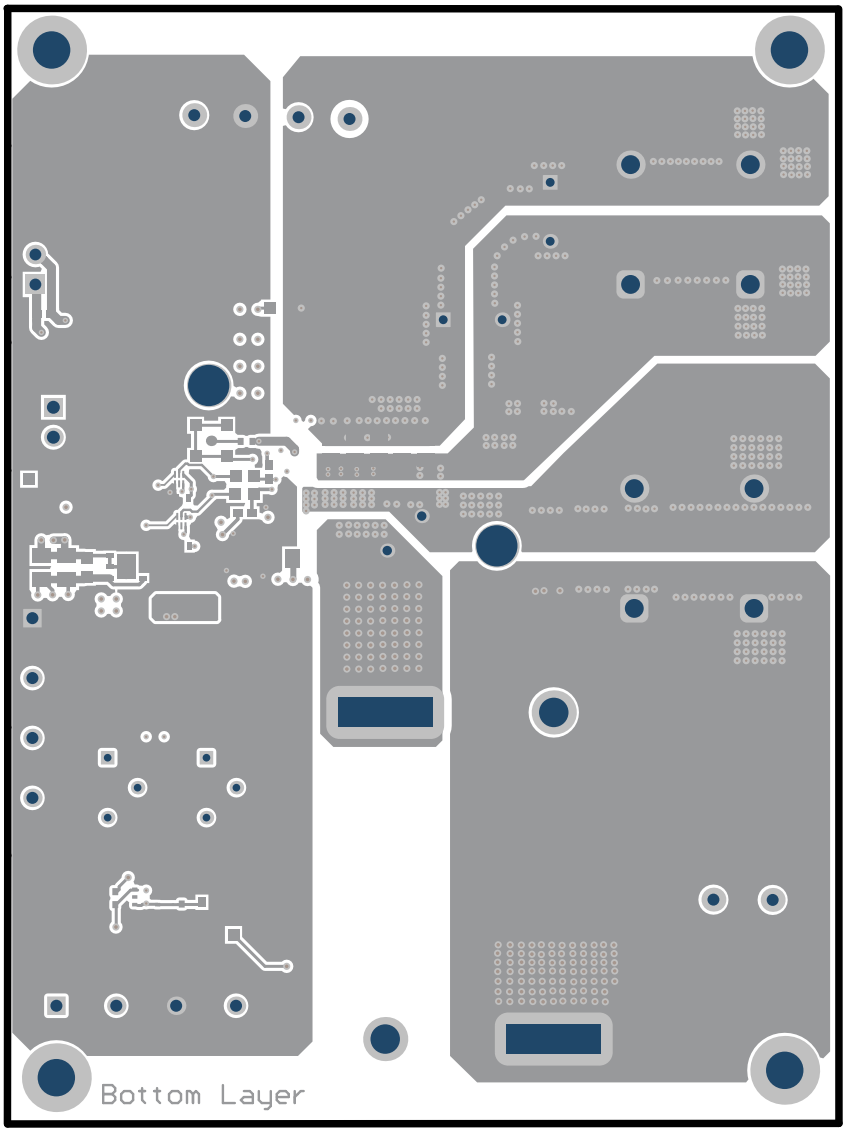

Figure 4-5. Bottom Layer

4.3 Bill of Materials (BOM)

Table 4-1. Bill of Materials

Designator	Qty	Description	Package Reference	Part Number	Manufacturer
!PCB1	1	Printed Circuit Board		HVP143	Any
C1, C51	2	47µF 100V Aluminium - Polymer Capacitors Radial, Can 38mOhm 2000 Hrs at 125°C	RADIAL	476AVG100MGBJ	Cornell Dubilier
C2, C6, C7, C8, C9, C10, C11, C12, C13, C14	10	CAP, CERM, 1µF, 100V,+/- 10%, X7R, AEC-Q200 Grade 1, 0805	0805	KAF21KR72A105KU	AVX
C3, C4, C5	3	CAP, CERM, 2.2µF, 100V,+/- 10%, X7R, 1812	1812	C1812C225K1RACTU	Kemet
C15, C16, C17, C18, C45, C46, C47, C48, C49, C50	10	CAP, CERM, 0.22µF, 100V,+/- 10%, X7S, AEC-Q200 Grade 1, 0603	0603	HMK107C7224KAHTE	Taiyo Yuden
C19, C21, C24	3	CAP, CERM, 1uF, 100V, +/- 10%, X7R, 1812	1812	C4532X7R2A105K230KA	TDK
C22, C35	2	CAP, CERM, 100pF, 16V, +/- 10%, X7R, 0402	0402	0402YC101KAT2A	AVX
C23, C25	2	CAP, CERM, 10pF, 50V, +/-5%, C0G/NP0, 0402	0402	GRM1555C1H100JA01D	MuRata
C26	1	CAP, CERM, 0.1µF, 16V, +/- 5%, X7R, 0603	0603	0603YC104JAT2A	AVX
C27	1	CAP, CERM, 10uF, 25V, +/-10%, X5R, 0805	0805	C2012X5R1E106K125AB	TDK
C28, C29	2	CAP, CERM, 2.2uF, 16V, +/- 10%, X7R, 0805	0805	GRM21BR71C225KA12L	MuRata
C30	1	CAP, CERM, 1uF, 25V, +/-10%, X5R, 0402	0402	C1005X5R1E105K050BC	TDK
C31	1	CAP, CERM, 100pF, 25V, +/-10%, X7R, 0603	0603	06033C101KAT2A	AVX
C32, C34	2	CAP, CERM, 2.2uF, 10V, +/-10%, X7R, 0603	0603	GRM188R71A225KE15D	MuRata
C33	1	CAP, CERM, 0.33uF, 10V, +/- 10%, X5R, 0402	0402	GRM155R61A334KE15D	MuRata
C36, C37, C38, C39	4	CAP, CERM, 0.1µF, 10V,+/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	C0402C104K8RACAUTO	Kemet
C40, C42	2	0402 4.7uF 16V ±20% Tolerance X5R Surface Mount Multilayer Ceramic Capacitor	0402	0402YD475MAT2A	KYOCERA AVX
C41	1	CAP, CERM, 1uF, 16V, +/- 10%, X5R, 0402	0402	EMK105BJ105KVHF	Taiyo Yuden
C43, C44	2	CAP, CERM, 2.2uF, 100V, +/- 10%, X7R, AEC-Q200 Grade 1, 1812	1812	CGA8N2X7R2A225K230 KA	TDK
C52	1	CAP, CERM, 22pF, 10V,+/- 5%, C0G/NP0, 0402	0402	885012005009	Wurth Elektronik
D1, D2	2	LED, Green, SMD	LED_0805	LTST-C170KGKT	Lite-On
D3, D4	2	Diode, Schottky, 40V, 0.03A, SOD-523	SOD-523	SDM03U40-7	Diodes Inc.
D5	1	Red 631nm LED Indication - Discrete 2V 0805 (2012 Metric)	0805	LTST-C171KRKT	Lite-On
D6	1	TVS DIODE 75VWM 121VC DO214AB	SMC	SMC5K75A-M3/H	Vishay General Semiconductor - Diodes Division

Table 4-1. Bill of Materials (continued)

Designator	Qty	Description	Package Reference	Part Number	Manufacturer
H1	1	Heat Sink, Black Anodized, 35x 50mm, 20mm high, with Push Pin and Spring		S05MZZ37	Alpha Novatech
H2	1	Thermal Interface Material		GR80A-0H-50GY	Fuji Polymer Industries
H3, H4, H5, H6	4	MACHINE SCREW PAN PHILLIPS 4-40	Machine Screw, 4-40, 1/4 inch	PMSSS 440 0025PH	B&F Fastener Supply
J1, J2	2	Terminal Block, 2 Pos, 10.16mm, TH	Terminal Block, 2 Pos, 10.16mm, TH	1986660-2	TE Connectivity
J3	1	Terminal Block, 2x1, 2.54mm, TH	Terminal Block, 2x1, 2.54mm, TH	282834-2	TE Connectivity
J4	1	MMCX JACK, 50Ohm, Gold, SMT	MMCX JACK, 1 Pos, Body 3.45x3.45mm, SMT	73415-2063	Molex
J5	1	Header, 100mil, 2x1, Tin, TH	Header, 2x1, 100mil, TH	5-146278-2	TE Connectivity
J6, J7	2	onn Unshrouded Header HDR 4 POS 5.08mm Solder ST Top Entry Thru-Hole Bulk	HDR4	TSW-204-14T-S	Samtec
J9	1	MINI JUMP 2POS 200CC	SHUNT	65771-001LF	Amphenol ICC
L1	1	WE-HCFT THT High Current Inductor, size 3540, 15uH, 45.3A, 2.16mOhm		7443763540150	Wurth Elektronik
MP1, MP2, MP3, MP4	4	Hex Standoff Threaded #4-40 Aluminium 1.563" (39.69mm)	STANDOFF	2121-440-AL	RAF Electronic Hardware
R1	1	RES, 1.0k ohm, 5%, 0.1W, 0603	0603	CRCW06031K00JNEA	Vishay-Dale
R2, R13	2	1 kOhms 0.5W, 1/2W PC Pins Through Hole Trimmer Potentiometer Cermet 1 Turn Top Finger Adjustment	PTH_POT_6MM6_6MM99	3362P-1-102TLF	Bourns
R3, R14	2	RES, 50, 0.1%, 0.5W, 0402	0402	FC0402E50R0BTBST1	Vishay Thin Film
R4	1	RES, 20k ohm, 5%, 0.25W, 1206	1206	CRCW120620K0JNEA	Vishay-Dale
R6, R7, R10	3	RES, 0ohm, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R8, R11, R17	3	RES, 10.0k, 1%, 0.063W, AEC-Q200 Grade 0, 0402	0402	CRCW040210K0FKED	Vishay-Dale
R9	1	RMCF/RMCP Series General Purpose Thick Film Standard Power and High Power Chip Resistor	0402 (1005 metric)	RMCF0402ZT0R00	Stackpole
R12	1	RES, 1.0k, 5%, 0.1W, AEC-Q200 Grade 0, 0603	0603	RCA06031K00JNEA	Vishay-Dale
R15, R18	2	RES, 4.02k, 1%, 0.063W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K02FKED	Vishay-Dale
R19, R20	2	RES, 0, 5%, 0.063W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
R22	1	RES, 4.7k, 5%, 0.063W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K70JNED	Vishay-Dale
TP1, TP2	2	Test Point, Miniature, Red, TH	Red Miniature Test point	5000	Keystone
TP3, TP4, TP7	3	Test Point, Miniature, Black, TH	Black Miniature Test point	5001	Keystone
TP5, TP8, TP9, TP10, TP11	5	Test Point, SMT	Test Point, SMT	S2751-46R	Harwin

Table 4-1. Bill of Materials (continued)

Designator	Qty	Description	Package Reference	Part Number	Manufacturer
TP6	1	Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
U1	1	LMG210xR022VBNR	VQFN-FCRLF18	LMG210xR022VBNR	Texas Instruments
U2	1	1A Low Dropout CMOS Linear Regulators Stable with Ceramic Output Capacitors, 6-pin LLP, Pb-Free	SDE06A	LP38690SD-5.0/NOPB	Texas Instruments
U3	1	Single Schmitt-Trigger Buffer, DCK0005A, SMALL T&R	DCK0005A	SN74LVC1G17DCKT	Texas Instruments
U4	1	Single Schmitt-Trigger Inverter, DCK0005A (SOT-SC70-5)	DCK0005A	SN74LVC1G14DCKT	Texas Instruments
U5, U6	2	Single Analog Switch, DSF0006A, LARGE T&R	DSF0006A	SN74LVC1G66DSFR	Texas Instruments
U7	1	Automotive 150mA high-voltage ultra-low-IQ low-dropout (LDO) linear regulator, DRV0006A (WSON-6)	DRV0006A	TPS7B8133QDRVRQ1	Texas Instruments
C20	0	CAP, CERM, 1uF, 25V, +/-10%, X5R, 0402	0402	C1005X5R1E105K050BC	TDK
R5, R16	0	RES, 0, 5%, 0.063W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale

5 Additional Information

5.1 Trademarks

All trademarks are the property of their respective owners.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2025) to Revision A (December 2025)	Page

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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