

Debugging Guide for Class D Audio Amplifier Overcurrent Protection Issues



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Abstract

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Class D amplifiers are widely used in consumer electronics such as portable speakers, smart home devices, TWS earbuds, and flat-panel TVs due to their high efficiency and low power consumption. In practical applications, however, OCP (overcurrent protection) often becomes one of the most common fault types as a result of improper software configuration or unreasonable hardware circuit parameter settings. Under normal operating conditions, the OCP mechanism plays an indispensable protective role—when abnormal overcurrent occurs in the circuit, it can effectively protect the amplifier chip and speaker from damage. Under certain special conditions, however, false triggering of OCP can lead to unexpected speaker muting and other issues, severely degrading the user experience. In such cases, it is necessary to systematically investigate the root cause of OCP triggering from both software and hardware perspectives and optimize accordingly.

This article focuses on common OCP issues in Class D amplifiers used in consumer audio applications, provides an in-depth analysis of typical triggering scenarios, and offers corresponding troubleshooting approaches and solutions for reference.

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1 Introduction to Class D Amplifier Overcurrent Protection Principles

First, a brief introduction to the overcurrent protection mechanism of Class D amplifiers. In the half-bridge output stage of a Class D amplifier, when the MOSFET (M1) is turned on, its drain-to-source path (V_{ds}) is equivalent to a small resistance, $R_{ds(on)}$, and the inductor current flowing through it produces a voltage drop across its terminals. An internal comparator continuously monitors this voltage drop. Once it exceeds a preset threshold, an overcurrent condition is determined to have occurred, and the PWM drive to M1/M2 is immediately shut off to protect the device. This protection mechanism is similar to that of conventional switching power supplies. The entire scheme requires no external sense resistor and directly reuses the MOSFET itself as the sensing element, offering both low loss and a simple structure. In addition, the sensing of the high-side transistor M1 is typically implemented with the aid of the BST bootstrap capacitor, which provides a floating reference potential. To prevent current spikes at the moment of PWM switching from causing false triggering, the circuit also incorporates a brief blanking time window.

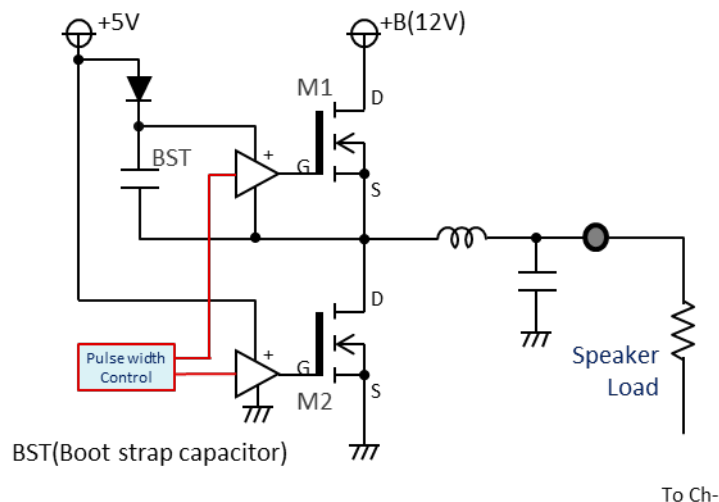


Figure 1-1. Block diagram of the Class D amplifier half-bridge output stage

2 Analysis of Common OC Issues and Solutions

When encountering OCP (overcurrent protection) issues in an application, the first step is to verify whether the test method is accurate. The overcurrent detection mechanism of the amplifier operates by sensing the current flowing through the MOSFETs in the half-bridge output stage. Therefore, it is recommended to preferentially use an oscilloscope current probe to measure the current along the path from the SW pin to the inductor. A common test method is to lift the pin at the end of the inductor closest to the chip and perform the current measurement at that point. This is because the current waveform at this test point most accurately reflects the actual current condition inside the chip, making the measurement results more reliable.

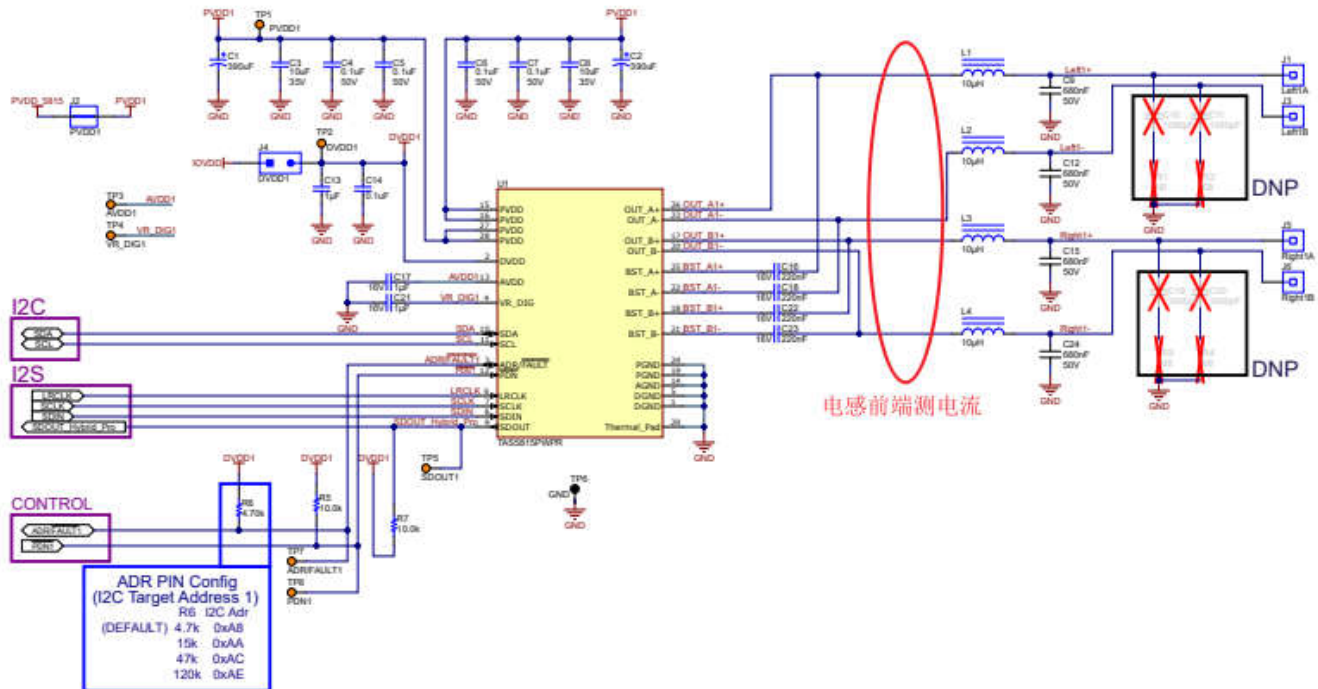


Figure 2-1. Inductor current test point on the TAS5815EVM

For capturing the current at the moment OCP is triggered, there are generally two approaches: one is to use the signal on the chip's FAULT pin as the oscilloscope trigger source; the other is to set the oscilloscope to Roll mode and locate the abnormal moment by capturing the current peak. After completing the correct hardware measurements described above, if it can be confirmed that the cause of the FAULT is indeed OCP triggering and that the hardware behavior is consistent with the register error report, it is then necessary to further investigate the root cause of the excessive current from both the software configuration and hardware design perspectives.

2.1 Software Configuration

In terms of the amplifier's software configuration, in addition to properly configuring the necessary functional registers (such as BTL/BPTL mode, switching frequency, modulation scheme, etc.), the analog gain and digital gain should also be reasonably set at the outset of development based on the output power and PVDD voltage. This ensures that the volume of small- and medium-signal content is not affected while limiting the output amplitude of large signals, thereby avoiding clipping distortion and also protecting the speaker. The core logic for configuring the analog and digital gains is to use the hardware supply voltage (PVDD) and the rated output power as constraints and work backward to derive the gain parameters at each stage. First, the maximum peak voltage that the speaker can withstand is calculated based on the voltage divider principle. Then, the required peak voltage is derived in reverse from the rated power. The larger of the two is taken as the design reference. From this, the Analog Gain (which limits the output voltage to no more than PVDD to prevent clipping) and the Total Gain (corresponding to the rated power point) are calculated. Finally, the two are subtracted to obtain the DRC/AGL threshold, thereby achieving both overvoltage and overpower protection for the speaker while ensuring the system delivers maximum dynamic performance. The following example, using a 12V supply, a 4Ω speaker, and 2 x 8W output, demonstrates the calculation flow for the digital and analog gains. Zdc is the

inductor DC resistance, and $R_{ds(on)}$ is the on-resistance of the high-side transistor. Here, it is assumed that $R_{ds(on)} = 0.18\Omega$ and $Z_{dc} = 0.023\Omega$.

No	Step	Calculation Formula	Result
1	Speaker maximum peak voltage	$PVDD \times R_{spk} \div (R_{spk} + 2 \times (R_{ds(on)} + Z_{dc}))$	10.89V
2	Peak voltage at rated power	$\sqrt{2 \times P_{spk} \times R_{spk}}$	8V
3	Selected clipping-free peak voltage	$MAX(V_{spk_max}, V_{spk_peak})$	10.89V
4	Analog gain	$20 \times \log_{10} [MAX(V_{spk_max}, V_{spk_peak}) \div 29.5]$	-9dB
5	Total gain	$20 \times \log_{10} (V_{spk_peak} \div 29.5)$	-11.34dB
6	AGL/DRC gain	$TotalGain - AnalogGain$	-2.5dB

2.2 Hardware Configuration

The most important aspect of hardware configuration is the selection of the inductor parameters. The inductor saturation current I_{SAT} must be greater than all possible peak currents in the system; otherwise, inductor saturation will cause the circuit to lose control and may even damage the device. In audio amplifier design, the following three scenarios with large instantaneous currents must be considered:

1. At power-up, when the duty cycle rapidly increases from 0 to θ , the LC filter generates an inrush charging current:

$$I_{peak_power_up} \approx PVDD \times \sqrt{(C/L) \times \sin(1/\sqrt{(L \times C)} \times \theta / F_{sw})} \quad (1)$$

2. Peak current during audio clipping:

$$I_{peak_clipping} \approx PVDD \times (1 - \theta) / (F_{sw} \times L) \quad (2)$$

3. During normal playback, the inductor peak current corresponding to the maximum output power:

$$I_{peak_output_power} \approx \sqrt{(2 \times Max_Output_Power / R_{speaker_load})} \quad (3)$$

The inductor saturation current must be greater than or equal to the maximum of these three scenarios to ensure safe operation of the system under all conditions.

$$I_{SAT} \geq MAX(I_{peak_power_up}, I_{peak_clipping}, I_{peak_output_power}) \quad (4)$$

The chip datasheet generally contains detailed requirements for inductor parameter selection. Please strictly follow the datasheet when selecting components, or contact a TI FAE for design assistance.

In addition to abnormal OCP issues caused by improper inductor parameter selection, excessive noise at the SW node can also lead to abnormal current and thus abnormal OCP. [Figure 2-2](#) shows the SW node voltage waveform under normal conditions, where CH1 is the FAULT pin waveform, CH2 is the SW node voltage waveform, and CH4 is the inductor current waveform. It can be seen that under normal operating conditions, the voltage overshoot at the SW pin is very small, and the current detected inside the chip at this time is closer to the actual inductor current.

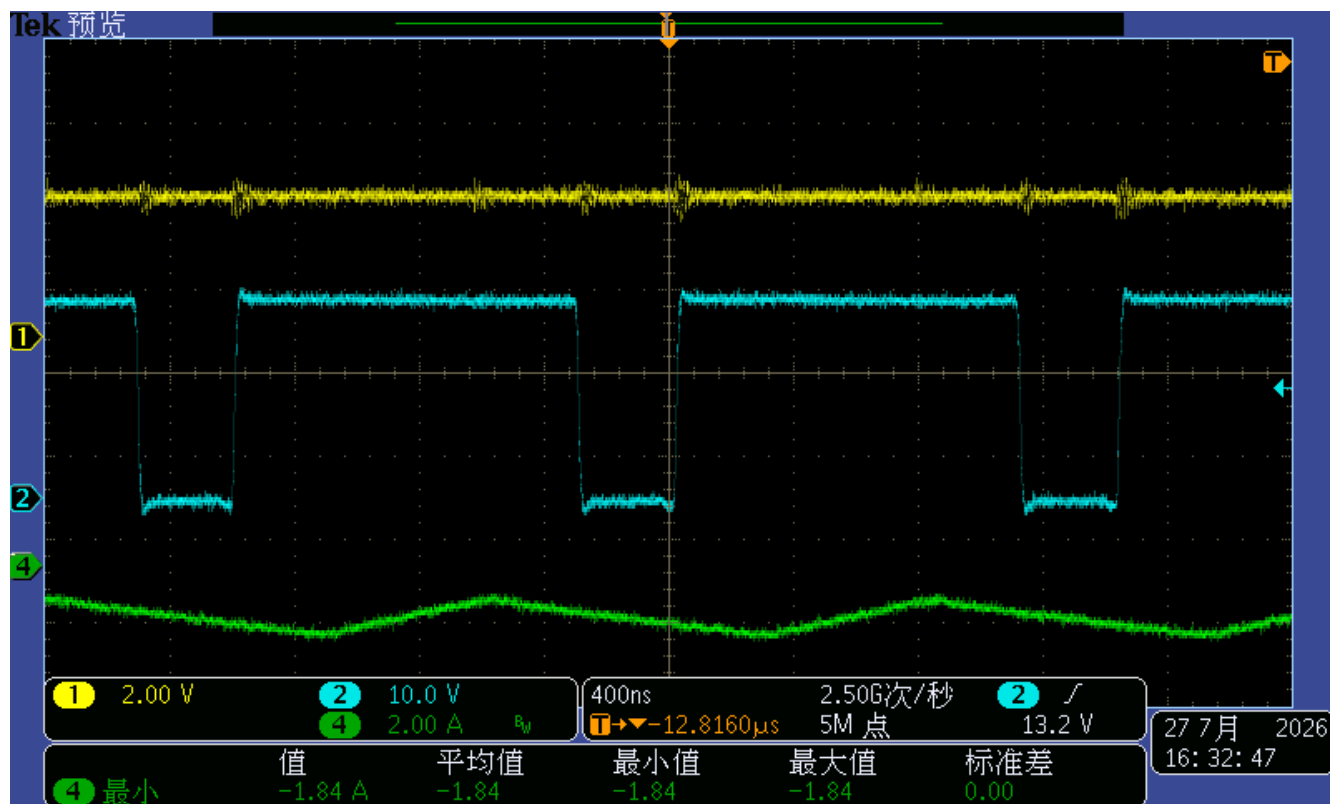


Figure 2-2. SW node voltage waveform under normal conditions

Figure 2-3 shows the SW node voltage waveform when the noise is excessive, where CH2/CH3 are the SW node-to-ground voltage waveforms of the left and right channels. It can be seen that excessive noise causes a large overshoot during the voltage rise period, which in turn causes the instantaneous current detected inside the chip to be excessive, thereby triggering OCP, pulling the FAULT level low, and causing the chip to report an error. A common hardware solution is to reserve an RC snubber network on the board to reduce the voltage overshoot at the SW node and mitigate the OCP issue. In addition, some devices also provide registers for adjusting the slew rate, which allows optimization from the software side as well.

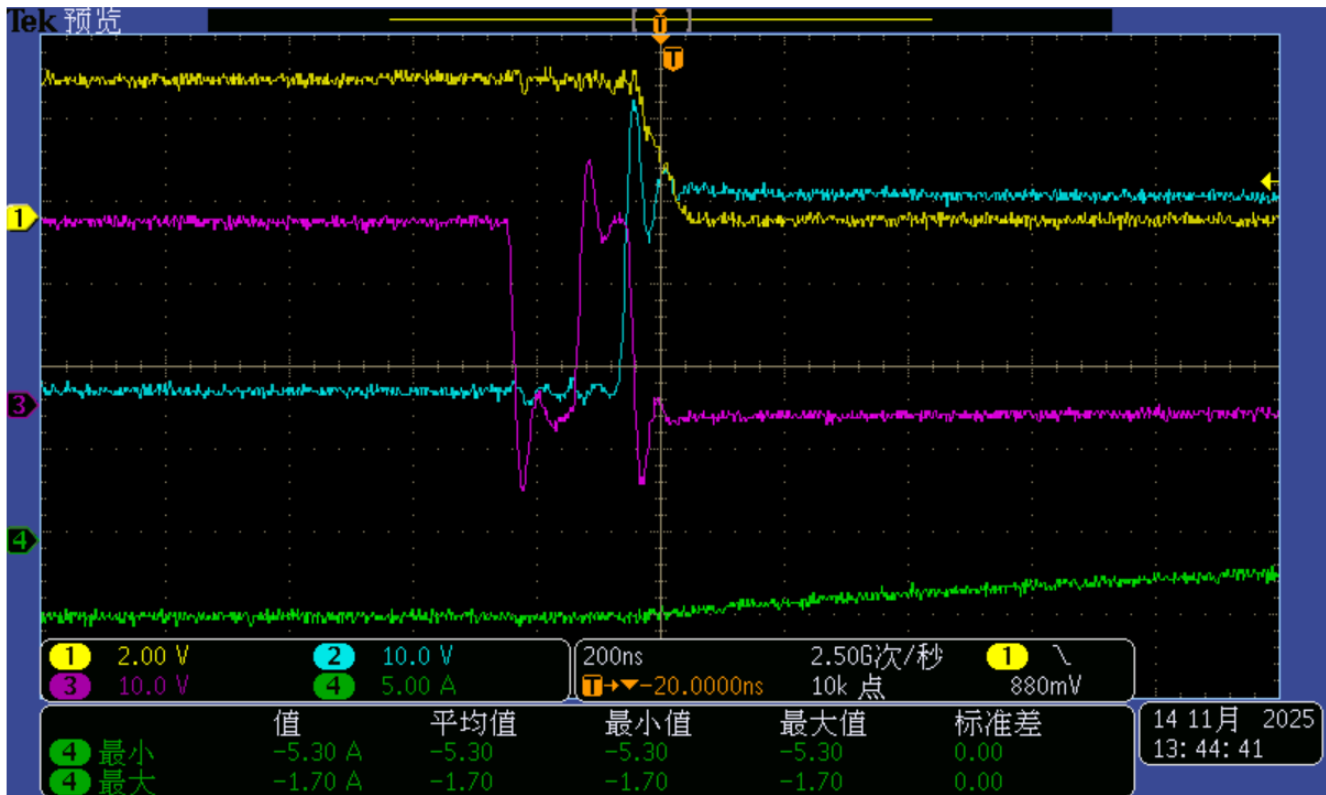


Figure 2-3. Excessive SW node noise causing current overshoot and triggering OCP

3 Analysis and Solutions for Fake OC Issues

In addition to conventional OCP issues, another common category of OCP is Fake OC, or false OCP. As the name implies, the actual inductor current has not reached the overcurrent threshold, but the current detection mechanism produces an abnormally large detection result under certain special scenarios, thereby triggering the internal OC protection.

The core condition for triggering Fake OC is a low-frequency, high-amplitude input signal combined with a relatively large output impedance. The most extreme scenario is an input of a high-amplitude, low-frequency signal with the output open-circuited. In this case, the real load current is zero, yet the system's overcurrent protection is falsely triggered. The root cause of this false triggering is insufficient charging of the BST bootstrap capacitor, which causes the gate drive voltage (BST – OUT) of the high-side transistor M1 to drop abnormally, preventing M1 from fully turning on and causing $R_{ds(on)}$ to rise significantly. Since the OC detection circuit samples current based on $V_{sense} = I_{out} \times R_{ds(on)}$, the abnormal increase in $R_{ds(on)}$ makes the sampled voltage artificially high, ultimately exceeding the OC threshold and triggering false protection.

As shown in Figure 2-1, the basic principle of OC is illustrated from the internal architecture of the Class D amplifier and the MOS switching waveforms. The BST capacitor needs to be charged through the bootstrap diode during the PWM low-level period (when the low-side transistor M2 is on). Under large audio amplitude conditions, the PWM duty cycle approaches 100%, the low-level time is extremely short, and the charging time of the BST capacitor is severely insufficient. Under low audio frequency conditions, the high-duty-cycle state lasts longer, and the BST capacitor continues to discharge over an extended period without being effectively replenished, causing its voltage to keep dropping. Under high load impedance conditions, the RC time constant at the switching node increases, the PWM rising and falling edges become slower, further compressing the effective charging window of the BST capacitor. These three factors compound one another and together cause a severe drop in BST voltage.

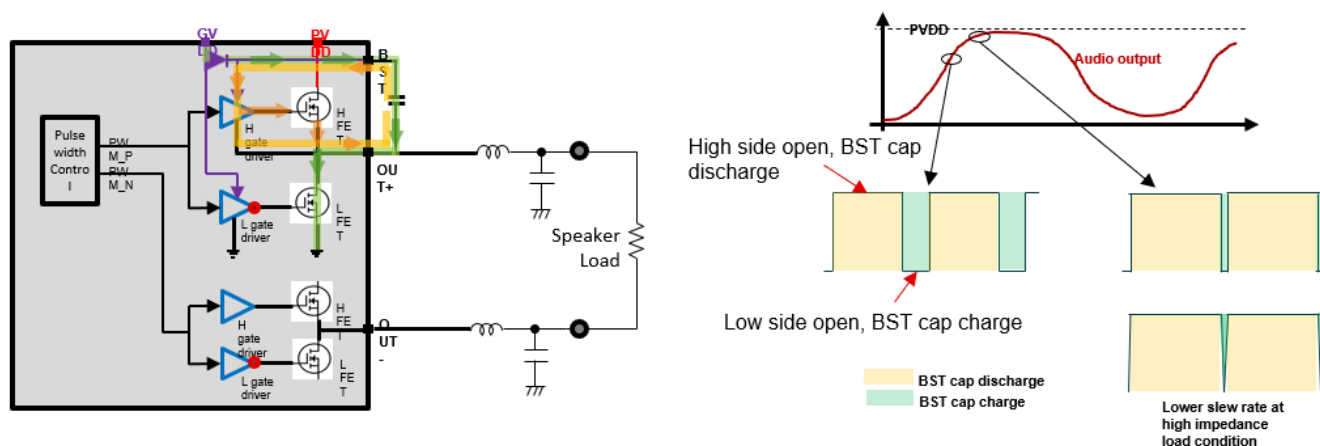


Figure 3-1. Schematic diagram of LM5145 Fake OC triggering principle

For solutions to this type of OC issue, the most direct approach is to increase the BST capacitor value to enhance its energy storage capability and thereby delay the voltage drop. Of course, based on this cause, other approaches can also address this type of false OC issue, such as forcibly inserting a minimum low-level time inside the chip, monitoring the BST voltage in real time, or introducing temperature/voltage compensation into the OC detection to dynamically adjust the OC threshold according to the actual BST voltage.

4 Summary

OC issues are a common category of problems for audio amplifiers in consumer electronics applications. On the one hand, reasonable gains must be configured at the design stage based on the constraints of output voltage and power. On the other hand, at the hardware level, troubleshooting can also be carried out from aspects such as inductor selection and bootstrap capacitor selection. In addition, SW pin noise, thermal considerations, and other factors are also points that cannot be overlooked during troubleshooting. This article has analyzed the principles behind common OC phenomena and provided corresponding solutions. In addition, different amplifier series may have slightly different handling logic, so please strictly follow the datasheet during design. Doing so can help avoid at least half of all OC issues.

5 References

1. [TAS5815 30-W, Closed-loop Class-D Audio Amplifier with 96kHz Enhanced Processing datasheet \(Rev. A\)](#)
2. [TAS5815 and TAS5802 Process Flows](#)
3. [TAS58xx Series General Tuning Guide Application Note](#)
4. [TAS5815PWP Evaluation Module](#)

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