Functional Safety Information

LM704xx-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for LMR70410-Q1 (DDC (SOT-23-THN, 6) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the functional block diagram of LMR70410-Q1 for reference.

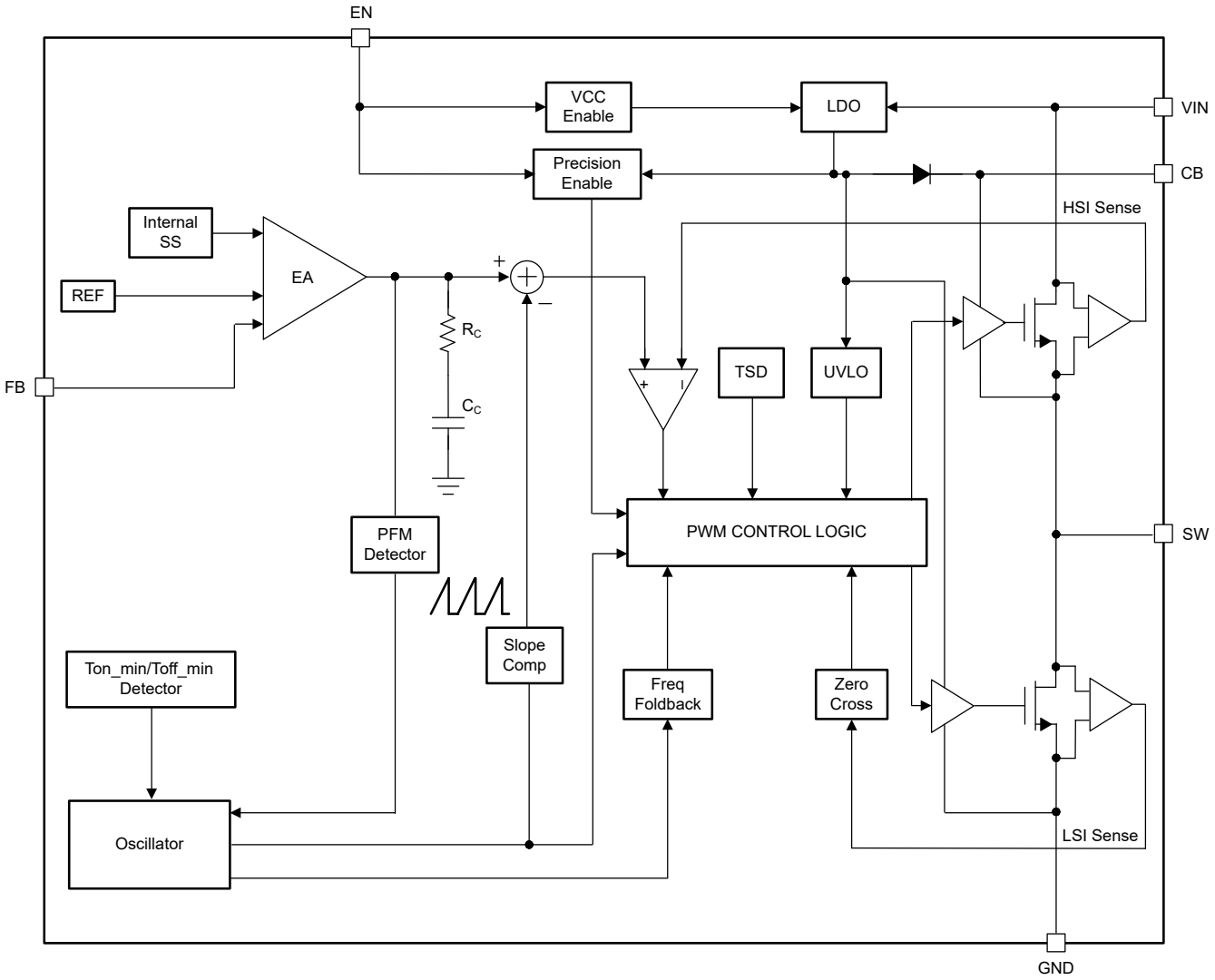


Figure 1-1. LMR70410-Q1 Functional Block Diagram

LMR70410-Q1 were developed using a quality-managed development process, but were not developed in accordance with IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LMR70410-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	7
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 250mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog or mixed	25	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMR70410-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	40%
Output voltage not in specification -- voltage or timing	55%
Power FET suck on	5%

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LMR70410-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Note

When a pin short-to-ground case is discussed, only the primary side ground shorts are considered.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Below is the LMR70410-Q1 pin diagram package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LMR70410-Q1 4V to 40V, 1A Automotive Synchronous Buck Converter datasheets.

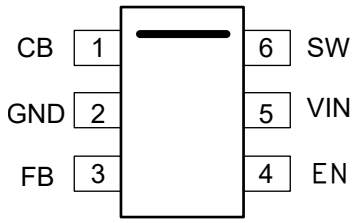


Figure 4-1. LMR70410-Q1 Pin Diagram

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (Primary)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CB	1	No output voltage	B
GND	2	Normal Operation	D
FB	3	The regulator operates at maximum duty cycle. Output voltage rises to nearly the input voltage (VIN) level. Possible damage to customer load or output stage components can occur. There is no effect on the device.	B
EN	4	ENABLE functionality is lost. The device remains in shutdown mode.	B
VIN	5	The device does not operate. No output voltage is generated. The output capacitors discharge through the input short. Large reverse current can damage the device. The EN ESD clamp can run current to destruction.	A
SW	6	Damage to internal FET.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CB	1	There is no output voltage.	B
GND	2	VOUT can be abnormal due to switching noise on analog circuits.	B
FB	3	VOUT is undefined.	B
EN	4	Loss of ENABLE functionality. Erratic operation can occur. Loss of regulation is probable.	B
VIN	5	There is no output voltage.	B
SW	6	There is no output voltage.	B

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
CB	1	GND	No output voltage	B
GND	2	FB	The regulator operates at maximum duty cycle. Output voltage rises to nearly the input voltage (VIN) level. Possible damage to customer load or output stage components can occur. There is no effect on the device.	B
FB	3	GND	The regulator operates at maximum duty cycle. Output voltage rises to nearly the input voltage (VIN) level. Possible damage to customer load or output stage components can occur. There is no effect on the device.	B
EN	4	VIN	There is no damage to the device. ENABLE functionality is lost.	B
VIN	5	SW	Damage to internal FET	A
SW	6	VIN	Damage to internal FET	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CB	1	If VIN exceeds 5.5V, damage occurs. There is no output voltage.	A
GND	2	There is no output voltage. There is damage to other pins referred to GND.	A
FB	3	If VIN exceeds 5.5V, damage occurs. There is no output voltage.	A
EN	4	There is no damage to the device. ENABLE functionality is lost.	B
VIN	5	There is no effect	D
SW	6	There is damage to the internal FET	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2026	*	Initial Release

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