Functional Safety Information

LM654x0 and LM654x0-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LM654x0 and LM654x0-Q1 (WQFN-FCRLF (20) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

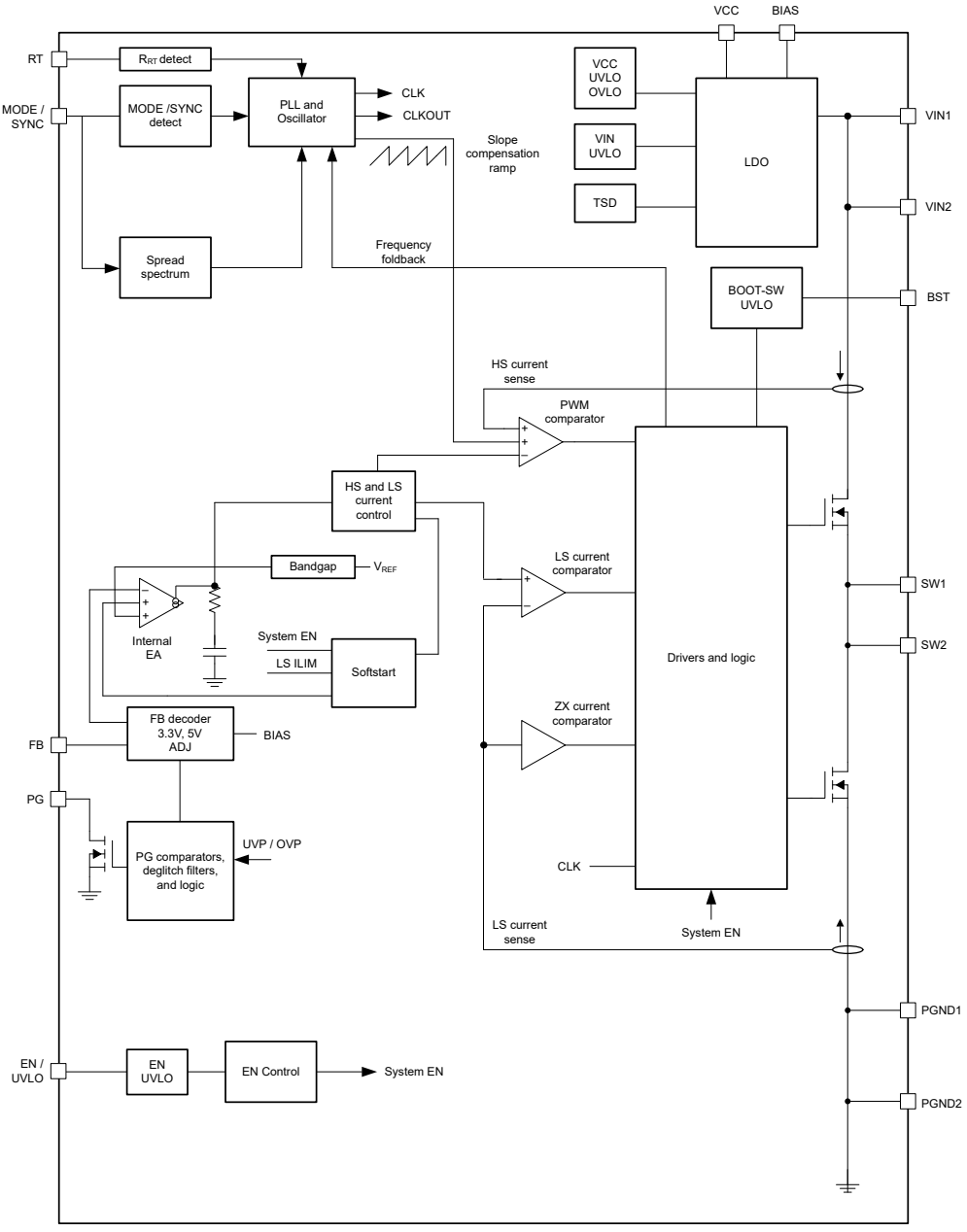

Figure 1-1. Functional Block Diagram

LM654x0 and LM654x0-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for LM654x0 and LM654x0-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	10
Die FIT rate	4
Package FIT rate	6

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 700mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed HV < 50V supply	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM654x0 and LM654x0-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No SW output	50
SW output not in specification – voltage or timing	40
SW power FET stuck on	5
PG false trip, fails to trip	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM654x0 and LM654x0-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM654x0 and LM654x0-Q1 pin diagram. For a detailed description of the device pins refer to the *Pin Configuration and Functions* section in the LM654x0 and LM654x0-Q1 datasheet.

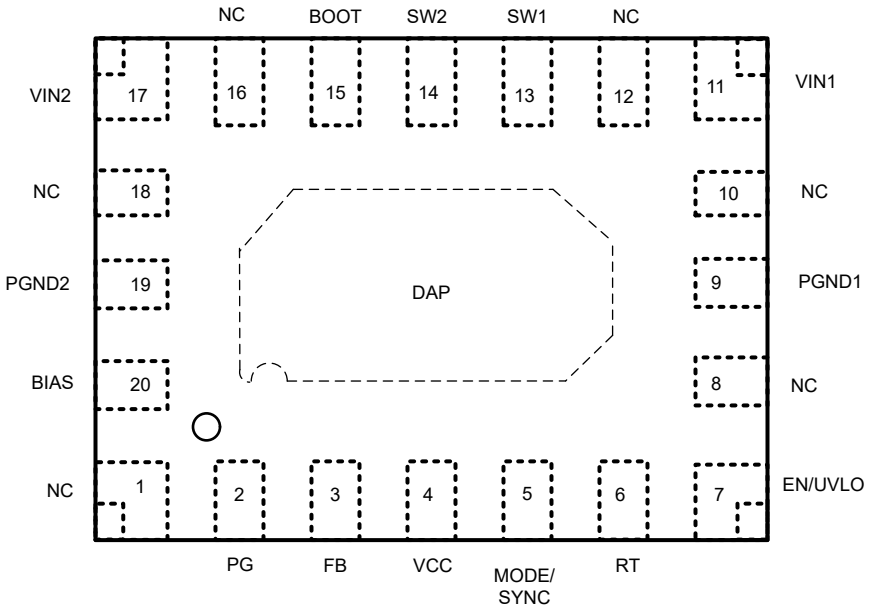

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the LM654x0 and LM654x0-Q1 datasheets

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
NC	1	Normal operation.	D
	8		
	10		
	12		
	16		
	18		
PG	2	Loss of power-good functionality.	B
FB	3	Fixed 3.3Vout. FB shorted to ground by default. Normal operation.	D
		Fixed 5Vout. VCC shorts to ground. Loss of regulation.	B
		Adjustable VOUT. Loss of regulation. VOUT = VIN.	B
		At start-up, fixed 3.3V output.	B
VCC	4	Loss of regulation. VOUT = 0V.	B
MODE/SYNC	5	If configured for PFM safe fault, no flag. Loss of synchronization functionality.	B
		If configured for FPWM, VCC shorts to ground. VOUT = 0V.	B
RT	6	If configured for 400kHz, VCC shorts to ground. VOUT = 0V.	B
		For adjustable frequency, loss of regulation.	B
		2.2MHz. Safe fault. Normal operation.	D
		At start-up, 2.2MHz. Unstable operation can potentially occur.	C
EN/UVLO	7	Device disabled, VOUT = 0V.	B
PGND	9	Normal operation.	D
	19		
VIN	11	VOUT = 0V.	B
	17		
SW1, SW2	13	Device damage.	A
	14		
BOOT	15	Loss of regulation, VOUT = 0V.	B
BIAS	20	If BIAS is tied to VOUT, VOUT = 0V.	B
		If BIAS is at ground, safe fault.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
NC	1	Normal operation.	D
	8		
	10		
	12		
	16		
	18		
PG	2	Loss of power-good functionality.	B
FB	3	For fixed VOUT, next cycle is no switching. PG is low.	C
		At start-up, no regulation. VOUT = 0V.	B
		For adjustable VOUT, VOUT = VIN.	B
VCC	4	Unstable operation. No damage.	B
MODE/SYNC	5	No flag. PFM in next cycle. Loss of external synchronization functionality.	B
RT	6	2.2MHz. PG low in the next turn-on cycle.	C
		In adjustable, loss of regulation. VOUT = 0V.	B
EN/UVLO	7	Device disabled. VOUT = 0V.	B
PGND1	9	Normal operation. Performance degradation.	C
	19		
VIN	11	Normal operation. Performance degradation.	C
	17		
SW1,SW2	13	Normal operation. Performance degradation.	C
	14		
BOOT	15	No device damage. VOUT = 0V.	C
BIAS	20	Normal operation.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No	Shorted to	Description of Potential Failure Effects	Failure Effect Class
NC	1	PG	Normal operation.	D
PG	2	FB	In adjustable VOUT, loss of regulation.	B
			In fixed VOUT, loss of PG functionality.	C
			At start-up for 3.3Vout, loss of PG functionality.	C
			At start-up for 5Vout fixed, shorts VCC to ground.	B
FB	3	VCC	For 5Vout, fixed. Normal operation.	D
			For 3Vout, fixed. Loss of regulation.	B
			For adjustable output. Loss of regulation.	B
VCC	4	MODE/SYNC	When in PFM mode. Loss of regulation.	B
			When in FPWM mode. Normal operation.	D
MODE/SYNC	5	RT	When RT is at ground and MODE is at ground, normal operation.	D
			When RT is at ground and the MODE pin is tied to VCC, loss of regulation.	B
			When RT is populated with a resistor and the MODE pin is at VCC.	C
			When RT is populated with a resistor and the MODE pin is at ground, loss of regulation.	B
			At start-up, if RT is populated with a resistor and the MODE pin is at VCC. 400kHz operation, unstable operation can occur.	C
RT	6	EN/UVLO	When RT is populated with a resistor and enabled at VIN, loss of regulation.	B
			When RT is at ground and enabled at VIN, loss of regulation.	B
			When RT is tied to VCC and enabled at VIN, device damage.	A
EN/UVLO	7	NC	Normal operation.	D
NC	8	PGND1	Normal operation.	D
PGND1	9	NC	Normal operation.	D
NC	10	VIN1	Normal operation.	D
VIN1	11	NC	Normal operation.	D
NC	12	SW1	Normal operation.	D
SW1	13	SW2	Normal operation.	D
SW2	14	BOOT	Loss of regulation.	B
BOOT	15	NC	Normal operation.	D
NC	16	VIN2	Normal operation.	D
VIN2	17	NC	Normal operation.	D
NC	18	PGND2	Normal operation.	D
PGND2	19	BIAS	If BIAS is at ground, normal operation.	D
			If BIAS is at VOUT, hiccup mode.	B
			If BIAS is floating, normal operation.	D
BIAS	20	NC	Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No	Description of Potential Failure Effects	Failure Effect Class
NC	1	Normal operation.	D
	8		
	10		
	12		
	16		
	18		
PG	2	If input supply is greater than PG absolute maximum ratings, device damage is possible.	A
FB	3	Device damage if supply is > 5.5V.	A
VCC	4	Device damage if supply is > 5.5V.	A
MODE/SYNC	5	Device damage if supply is > 5.5V.	A
RT	6	Undefined switching frequency.	C
EN/UVLO	7	Normal operation.	D
PGND1	9	VOUT = 0V.	B
	19		
VIN	11	Normal operation.	D
	17		
SW1,SW2	13	Device damage.	A
	14		
BOOT	15	Device damage.	A
BIAS	20	If input supply is greater than BIAS absolute maximum ratings, device damage is possible.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2026	*	Initial Release

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