Functional Safety Information

TLC69621-Q1 and TLC69631-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TLC69621-Q1 and TLC69631-Q1 (X2QFN (16) and SOT-23-THIN (16) packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

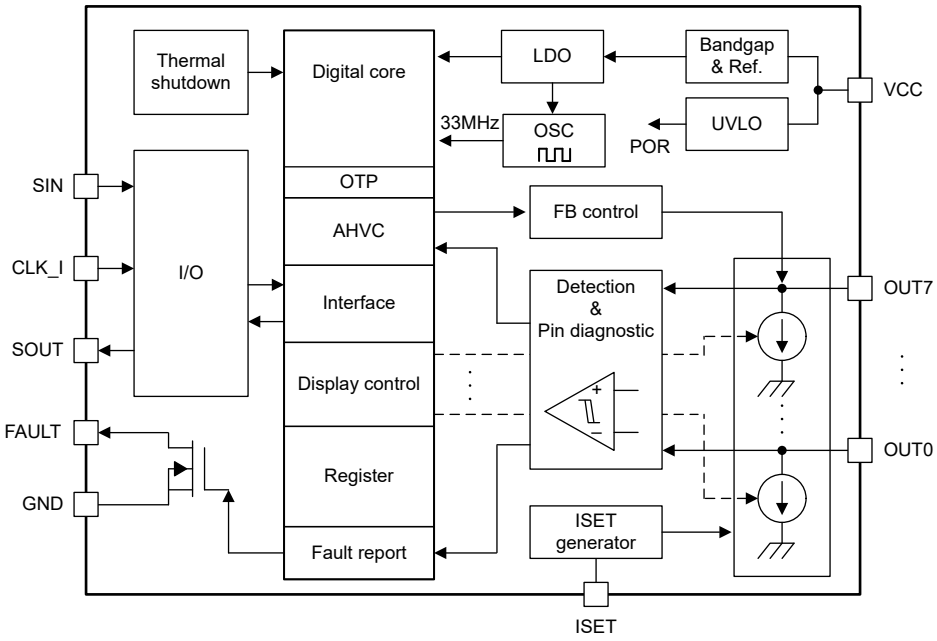

Figure 1-1. Functional Block Diagram

The TLC69621-Q1 and TLC69631-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 X2QFN (16) Package

This section provides functional safety failure in time (FIT) rates for the X2QFN (16) package of the TLC69621-Q1 and TLC69631-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-3 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6.12
Die FIT rate	2.09
Package FIT rate	4.03

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile:
  - 10,000 power-on-hours | 300,000km driving
  - 15 year lifetime

Table 2-2. Temperature and Distribution Assumptions

Temperature [°C]	Distribution [%]
–40	1
–20	5
32	20
60	65
95	8
105	1

- Power dissipation: 0.17W
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-3. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-3 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 SOT-23-THIN (16) Package

This section provides functional safety failure in time (FIT) rates for the SOT-23-THIN (16) package of the TLC69621-Q1 and TLC69631-Q1 based on two different industry-wide used reliability standards:

- Table 2-4 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-4. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	5.84
Die FIT rate	2.07
Package FIT rate	3.77

The failure rate and mission profile information in Table 2-4 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile:
  - 10,000 power-on-hours | 300,000km driving
  - 15 year lifetime

Table 2-5. Temperature and Distribution Assumptions

Temperature [°C]	Distribution [%]
–40	1
–20	5
32	20
60	65
95	8
105	1

- Power dissipation: 0.17W
- Climate type: World-wide table 8 and figure 13
- Package factor (lambda 3): From table 17b and figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLC69621-Q1 and TLC69631-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
All constant-current outputs are out of specification	20.3
All constant-current outputs are stuck high	3.1
All constant-current outputs are stuck low	3.7
One of the constant-current outputs is out of specification	2.6
One of the constant-current outputs is stuck high	0.4
One of the constant-current outputs is stuck low	0.4
Fault fails to trigger	8.9
Fault is falsely triggered	17.2
Communication failure	43.4

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TLC69621-Q1 and TLC69631-Q1 (X2QFN (16) and SOT-23-THIN (16) packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Special considerations on pin level tailoring: The OUT7 pin can be selected as either the constant-current sink channel or the FB function.

4.1 X2QFN (16) Package

Figure 4-1 shows the TLC69621-Q1 and TLC69631-Q1 pin diagram for the X2QFN (16) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLC69621-Q1 and TLC69631-Q1 datasheet.

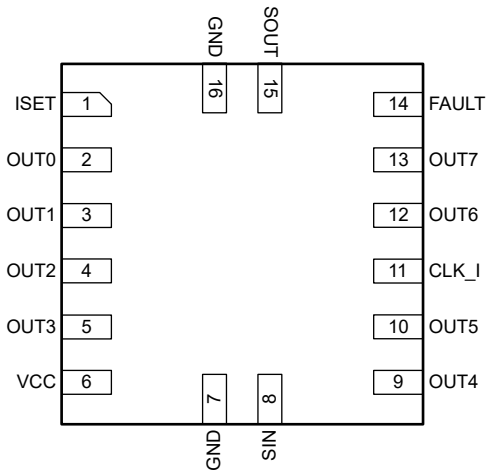

Figure 4-1. Pin Diagram (X2QFN (16)) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ISET	1	No adjacent pin.	D
OUT0–OUT3	2–5	No adjacent pin.	D
VCC	6	No adjacent pin.	D
GND	7, 16	The device operates as normal.	D
SIN	8	There is a communication failure.	B
OUT4–OUT5	9–10	No adjacent pin.	D
CLK_I	11	No adjacent pin.	D
OUT6–OUT7	12–13	No adjacent pin.	D
FAULT	14	No adjacent pin.	D
SOUT	15	There is a communication failure.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ISET	1	The device reports an error on the ISET pin.	B
OUT0–OUT3	2–5	The device reports LED open.	B
VCC	6	The device cannot start up.	B
GND	7, 16	There is no effect on the device. There are multiple GND pins.	D
SIN	8	There is a communication failure.	B
OUT4–OUT5	9–10	The device reports LED open.	B
CLK_I	11	There is a communication failure.	B
OUT6–OUT7	12–13	The device reports LED open.	B
FAULT	14	A fault fails to trigger on the device.	B
SOUT	15	There is a communication failure.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
ISET	1	OUT0	The device reports an error on the ISET pin.	B
OUT0	2	OUT1	The LEDs connected to the OUT0 and OUT1 pin cannot perform the correct brightness.	B
OUT1	3	OUT2	The LEDs connected to the OUT1 and OUT2 pin cannot perform the correct brightness.	B
OUT2	4	OUT3	The LEDs connected to the OUT2 and OUT3 pin cannot perform the correct brightness.	B
OUT3	5	VCC	The device reports LED short.	B
VCC	6	GND	The VCC and GND pin are both corner pins, the adjacent-pin short is not applicable.	D
GND	7	SIN	There is a communication failure.	B
SIN	8	OUT4	The SIN and OUT4 pin are both corner pins, the adjacent-pin short is not applicable.	D
OUT4	9	OUT5	The LEDs connected to the OUT4 and OUT5 pin cannot perform the correct brightness.	B
OUT5	10	CLK_I	There is a communication failure.	B
CLK_I	11	OUT6	There is a communication failure.	B
OUT6	12	OUT7	The LEDs connected to the OUT6 and OUT7 pin cannot perform the correct brightness.	B
OUT7	13	FAULT	The device reports fault falsely.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
FAULT	14	SOUT	The FAULT and SOUT pin are both corner pins, the adjacent-pin short is not applicable.	D
SOUT	15	GND	There is a communication failure.	B
GND	16	ISET	The GND and ISET pin are both corner pins, the adjacent-pin short is not applicable.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ISET	1	No adjacent pin.	D
OUT0–OUT2	2–4	No adjacent pin.	D
OUT3	5	The device reports LED short.	B
VCC	6	The device operates as normal.	D
GND	7, 16	No adjacent pin.	D
SIN	8	No adjacent pin.	D
OUT4–OUT5	9–10	No adjacent pin.	D
CLK_I	11	No adjacent pin.	D
OUT6–OUT7	12–13	No adjacent pin.	D
FAULT	14	No adjacent pin.	D
SOUT	15	No adjacent pin.	D

4.2 SOT-23-THIN (16) Package

Figure 4-2 shows the TLC69621-Q1 and TLC69631-Q1 pin diagram for the SOT-23-THIN (16) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLC69621-Q1 and TLC69631-Q1 datasheet.

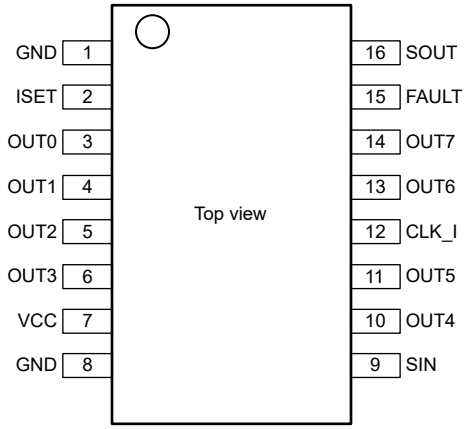

Figure 4-2. Pin Diagram (SOT-23-THIN (16) Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1, 8	The device operates as normal.	D
ISET	2	The device reports LED open.	B
OUT0–OUT3	3–6	No adjacent pin.	D
VCC	7	The device cannot start up.	B
SIN	9	No adjacent pin.	D
OUT4–OUT5	10–11	No adjacent pin.	D
CLK_I	12	No adjacent pin.	D
OUT6–OUT7	13–14	No adjacent pin.	D
FAULT	15	No adjacent pin.	D
SOUT	16	No adjacent pin.	D

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1, 8	There is no effect on the device. There are multiple GND pins.	D
ISET	2	The device reports an error on the ISET pin.	B
OUT0–OUT3	3–6	The device reports LED open.	B
VCC	7	The device operates as normal.	B
SIN	9	There is a communication failure.	B
OUT4–OUT5	10–11	The device reports LED open.	B
CLK_I	12	There is a communication failure.	B
OUT6–OUT7	13–14	The device reports LED open.	B
FAULT	15	A fault fails to trigger on the device.	B
SOUT	16	There is a communication failure.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	ISET	The device reports an error on the ISET pin.	B
ISET	2	OUT0	The device reports an error on the ISET pin.	B
OUT0	3	OUT1	The LEDs connected to the OUT0 and OUT1 pin cannot perform the correct brightness.	B
OUT1	4	OUT2	The LEDs connected to the OUT1 and OUT2 pin cannot perform the correct brightness.	B
OUT2	5	OUT3	The LEDs connected to the OUT2 and OUT3 pin cannot perform the correct brightness.	B
OUT3	6	VCC	The device reports LED short.	B
VCC	7	GND	The device cannot start up.	B
GND	8	SIN	The GND and SIN pin are both corner pins, the adjacent-pin short is not applicable.	D
SIN	9	OUT4	There is a communication failure.	B
OUT4	10	OUT5	The LEDs connected to the OUT4 and OUT5 pin cannot perform the correct brightness.	B
OUT5	11	CLK_I	There is a communication failure.	B
CLK_I	12	OUT6	There is a communication failure.	B
OUT6	13	OUT7	The LEDs connected to the OUT6 and OUT7 pin cannot perform the correct brightness.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT7	14	FAULT	The device reports fault falsely.	B
FAULT	15	SOUT	The device reports fault falsely.	B
SOUT	16	GND	The SOUT and GND pin are both corner pins, the adjacent-pin short is not applicable.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	No adjacent pin.	D
ISET	2	No adjacent pin.	D
OUT0–OUT3	3–6	No adjacent pin.	D
VCC	7	The device operates as normal.	D
GND	8	The device cannot start up.	B
SIN	9	No adjacent pin.	D
OUT4–OUT5	10–11	No adjacent pin.	D
CLK_I	12	No adjacent pin.	D
OUT6–OUT7	13–14	No adjacent pin.	D
FAULT	15	No adjacent pin.	D
SOUT	16	No adjacent pin.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

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