Functional Safety Information

TPS61129-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TPS61129-Q1 (VSON package) to aid in a functional safety system design. Information provided is:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

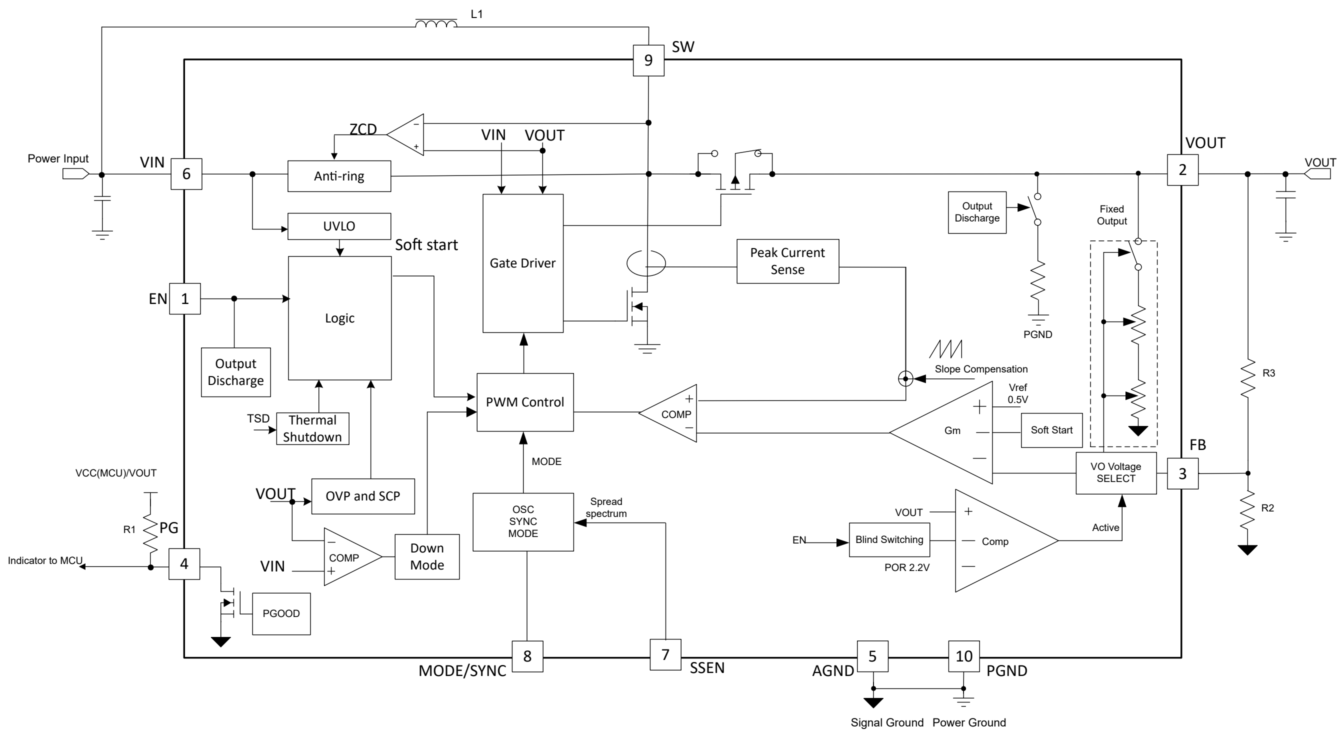

Figure 1-1. Functional Block Diagram

The TPS61129-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS61129-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	8
Package FIT rate	5

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1000mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS61129-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT not in specification voltage or timing	80
VOUT No output GND or HIZ	5
SW FETs stuck on	10
EN enable fails or false enable	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS61129-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 to Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS61129-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS61129-Q1 datasheet.

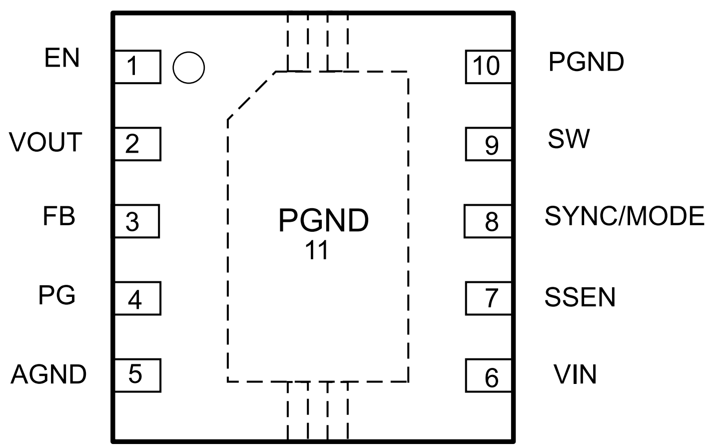

Figure 4-1. Pin Diagram (DRC(VSON,11) Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	There is a loss of ENABLE functionality. The device remains in shutdown mode.	B
VOUT	2	The device remains in short circuit protection.	B
FB	3	Adjustable Vout version. The OVP is triggered.	B
		Fixed Vout version. There is no effect.	D
PG	4	Correct output voltage. PG functionality is lost.	B
AGND	5	There is no effect.	D
VIN	6	The device does not operate. The power supply is short.	B
SSEN	7	Frequency spread function is disabled.	C
SYNC/MODE	8	The device remains in auto PFM mode.	C
SW	9	The device can be damaged.	A
PGND	10,11	There is no effect.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	Loss of ENABLE functionality. The device remains in shutdown mode.	B
VOUT	2	The device can be damaged.	A
FB	3	Adjustable Vout version. The OVP is triggered.	B
		Fixed Vout version. There is no effect.	D
PG	4	Correct output voltage. PG functionality is lost.	B
AGND	5	The device can be damaged.	A
VIN	6	The device does not work and there is no output voltage.	B
SSEN	7	Correct output voltage. Frequency spread function is in an unknown state, enabled or disabled.	C
SYNC/MODE	8	The device remains in auto PFM mode.	C
SW	9	The device can be damaged.	A
PGND	10,11	The device can be damaged.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
EN	1	VOUT	Output voltage is out of regulation.	B
VOUT	2	FB	Adjustable Vout version, output voltage selected to 5V.	C
			Fixed Vout version. There is no effect.	D
FB	3	PG	The output voltage is out of regulation.	B
PG	4	AGND	Correct output voltage. PG functionality is lost.	C
AGND	5	VIN	The device does not operate. VIN is short.	B
VIN	6	SSEN	The frequency spread function is enabled.	C
SSEN	7	SYNC/MODE	Correct output voltage. If these pins are shorted to low, frequency spread function is disabled, and the device operates in auto PFM mode. If these pins are shorted to high, frequency spread function is enabled, and the device operates in forced PWM mode.	C
SYNC/MODE	8	SW	The device can be damaged.	A
SW	9	PGND	The device can be damaged.	A
PGND	10,11	EN	The device does not work. Vout = 0V.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	Loss of disable functionality. The device is always enabled.	B
VOUT	2	VOUT = VIN. The device operates in down mode if EN is high.	B
FB	3	Adjustable Vout version. The output voltage is out of regulation.	B
		Fixed Vout version. There is no effect.	D
PG	4	Correct output voltage. The PG functionality is lost.	C
AGND	5	The device does not operate. Power supply is short.	B
VIN	6	There is no effect.	D
SSEN	7	The frequency spread function is enabled.	C
SYNC/MODE	8	The device operates in forced PWM mode.	C
SW	9	The device can be damaged.	A
PGND	10,11	The device does not operate. Power supply is short.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release