Functional Safety Information

LM72880-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for LM72880-Q1 (QFN-29 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

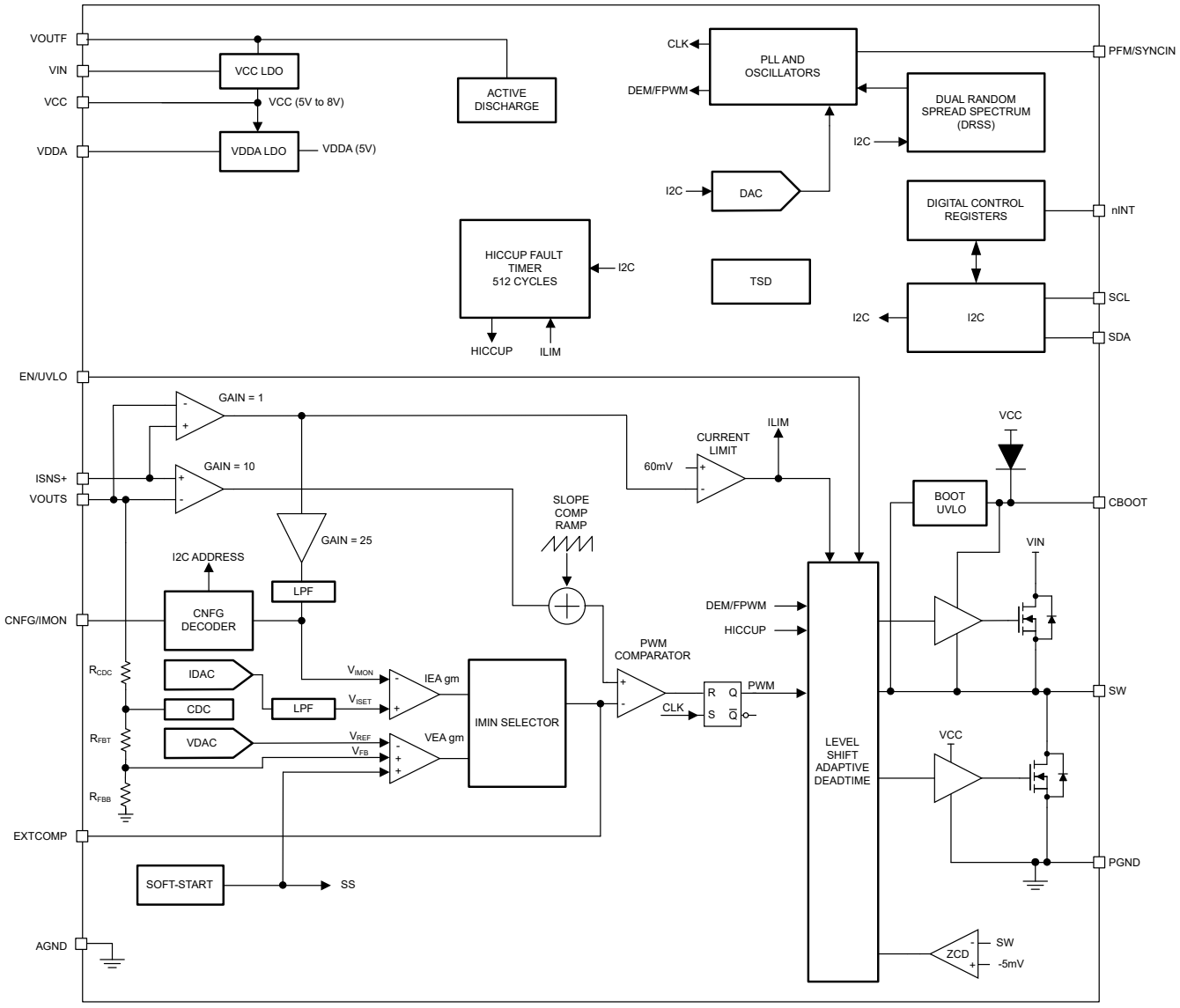


Figure 1-1. Functional Block Diagram

LM72880-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

2.1 LM72880-Q1 FIT Rates

This section provides functional safety failure in time (FIT) rates for LM72880-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	28
Die FIT rate	6
Package FIT rate	22

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1.6W
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM72880-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	50
SW output not in specification – voltage or timing	40
SW power FET stuck on	5
nINT false trip or fails to trip	5

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM72880-Q1 (QFN-29 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM72880-Q1 pin diagram. For a detailed description of the device pins, refer to the *Pin Configuration and Functions* section in the LM72880-Q1 datasheet.

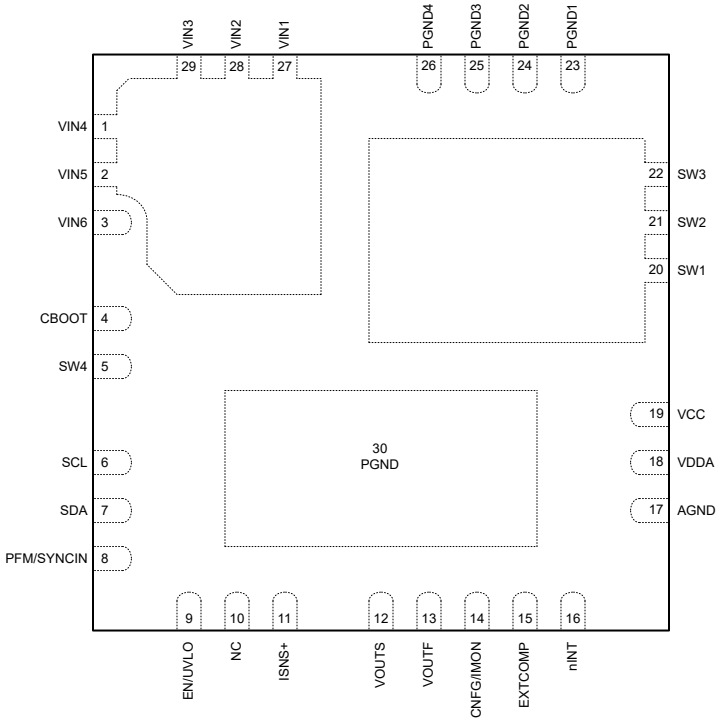


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The application circuit is used according to the LM72880-Q1 datasheet.
- The PG pin is pulled up to the VDDA pin.

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1–3	VOUT = 0V.	B
CBOOT	4	VOUT = 0V; the VCC regulator is loaded to current limit.	B
SW	5	VOUT = 0V; the high-side (HS) FET is shorted from the VIN pin to GND.	A
SCL	6	VOUT = 0V; there is no I2C communication.	B
SCA	7	VOUT = 0V; there is no I2C communication.	B
PFM/SYNC	8	VOUT = VOUT is as expected; synchronization is not possible and the pin is in FPWM mode.	C
EN/UVLO	9	VOUT = 0V; the device enters shutdown mode.	B
NC	10	N/A	D
ISNS+	11	VOUT = 0V; the device damage can occur.	A
VOUTS	12	The device reaches the current limit, VOUT = 0V and enters hiccup mode.	B
VOUTF	13	There is no BIAS function, which leads to lower efficiency and higher quiescent current.	B
CNFG/IMON	14	VOUT = 0V; there is no I2C communication.	B
EXTCOMP	15	VOUT = 0V.	B
nINT	16	VOUT = VOUT is as expected; there is no nINT pin output.	C
AGND	17	AGND is GND; VOUT = VOUT is as expected.	D
VDDA	18	VOUT = 0V; switching is not possible, the VCC output is loaded.	B
VCC	19	VOUT = 0V; switching is not possible, the VCC output is loaded.	B
SW	20–22	VOUT = 0V; the HS FET is shorted from the VIN pin to GND.	A
PGND	23–26	PGND is GND; VOUT = VOUT is as expected.	D
VIN	27–29	VOUT = 0V.	B

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Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1–3	VOUT = VOUT is as expected; the part works through the VIN pins (27–29) with EMI or thermals worsening.	C
CBOOT	4	VOUT = 0V.	A
SW	5	VOUT = VOUT is as expected; the part works through the SW pins (20–22) with EMI or thermals worsening.	C
SCL	6	VOUT = 0V; there is no I2C communication	B
SDA	7	VOUT = 0V; there is no I2C communication	B
PFM/SYNC	8	VOUT = VOUT is as expected; the behavior of CCM/DCM is erratic at light loads.	C
EN/UVLO	9	The OFF/ON state of the device is indeterminate.	B
NC	10	VOUT = VOUT is as expected.	D
ISNS+	11	The OPEN current sense pin blocks current limit and causes VOUT oscillations.	A
VOUTS	12	When there is no output sense, VOUT charges VIN when switching.	B
VOUTF	13	There is no BIAS function or output active discharge function.	B
CNFG/IMON	14	VOUT = 0V; there is no I2C communication.	D
EXTCOMP	15	VOUT oscillates; if VOUT oscillates to VIN, damage can occur if VIN > 60V.	A
nINT	16	VOUT = VOUT is as expected; there is no nINT pin output.	B
AGND	17	VOUT is indeterminate.	B
VDDA	18	Poor noise prevention.	C
VCC	19	VOUT = VOUT is as expected until damage occurs.	A
SW	20–22	VOUT = 0V.	B
PGND	23–26	VOUT is indeterminate.	B
VIN	27–29	VOUT = VOUT is as expected; the part works through the VIN pins (1–3) with EMI or thermals worsening.	C

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VIN4	1	VIN5	There is no impact on the device.	D
VIN5	2	VIN6	There is no impact on the device.	D
VIN6	3	CBOOT	For VIN < 12V, VOUT=0V; switching is erratic due to insufficient voltage to drive the HS gate. For VIN > 12V, voltage on CBOOT exceeds the absolute maximum ratings of the pin and CBOOT is damaged. VOUT = 0V.	A
CBOOT	4	SW4	Switching ceases due to BOOT UVLO. VOUT discharges to 0V.	B
SW4	5	SCL	The SCL pin is damaged.	A
SCL	6	SDA	VOUT = 0V; there is no I2C communication.	B
SDA	7	PFM/SYNCIN	VOUT = 0V; there is no I2C communication.	B
PFM/SYNCIN	8	EN/UVLO	VOUT = VOUT is as expected.	A
EN/UVLO	9	NC	VOUT = VOUT is as expected. If EN/UVLO > 6.5V, the PFM/SYNCIN pin is damaged.	D
NC	10	ISNS+	VOUT = VOUT is as expected.	D
ISNS+	11	VOUTS	Current limit is disabled since the current limit resistor is shorted. VOUT is not regulated (unstable) since current mode feedback is shorted.	A
VOUTS	12	VOUTF	Current limit is less accurate and stability degrades.	B
VOUTF	13	CNFG/IMON	The I2C address and functionality of IMON are configured incorrectly.	B
CNFG/IMON	14	EXTCOMP	There is a loss of voltage regulation.	B
EXTCOMP	15	nINT	High voltage of the EXTCOMP pin drives the part into current limit. There is a loss of voltage regulation.	B
nINT	16	AGND	VOUT = VOUT is as expected; there is no nINT pin functionality.	B
AGND	17	VDDA	VOUT = 0V.	B
VDDA	18	VCC	The VDDA pin is damaged. VOUT = 0V.	A
VCC	19	SW1	The VCC pin is damaged. VOUT = 0V.	A
SW1	20	SW2	There is no impact to the device.	D
SW2	21	SW3	There is no impact to the device.	D
SW3	22	PGND1	There is HS FET damage. VOUT = 0V.	A
PGND1	23	PGND2	There is no impact to the device.	D
PGND2	24	PGND3	There is no impact to the device.	D
PGND3	25	PGND4	There is no impact to the device.	D
PGND4	26	VIN1	The device does not start-up. VOUT = 0V.	A
VIN1	27	VIN2	There is no impact to the device.	D
VIN2	28	VIN3	There is no impact to the device.	D
VIN3	29	VIN4	There is no impact to the device.	D

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Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN4, VIN5, VIN6	1–3	There is no impact to the device.	D
CBOOT	4	If VIN < 6.5V, VOUT = VOUT is as expected; switching is erratic.	C
		If VIN > 6.5V, the CBOOT pin exceeds maximum ratings and the pin is damaged.	A
SW5	5	VOUT=VIN; there is excess current from VIN through the low-side FET.	A
SCL	6	If VIN < 6.5V, there is no I2C communication.	B
		If VIN > 6.5V, the SCL pin exceeds the maximum ratings and the pin is damaged. VOUT = 0V.	A
SDA	7	If VIN < 6.5V, there is no I2C communication.	B
		If VIN > 6.5V, the SCL pin exceeds the maximum ratings and the pin is damaged. VOUT = 0V.	B
PFM/SYNC	8	If VIN < 6.5V, VOUT = VOUT is as expected.	D
		If VIN > 6.5V, the PFM/SYNC pin exceeds the maximum ratings and the pin is damaged. VOUT = VOUT is as expected.	A
EN/UVLO	9	The part is always enabled. VOUT = VOUT is as expected.	C
NC	10	There is no impact to the device.	D
ISNS+	11	If VIN < 6.5V, VOUT = VIN.	B
		If VIN > 60V, the ISNS+ pin exceeds the maximum ratings and the pin is damaged.	A
VOUTS	12	If VIN > 60V, the VOUT pin exceeds the maximum ratings and the pin is damaged.	A
VOUTF	13	If VIN > 60V, the VOUTF pin exceeds the maximum ratings and the pin is damaged.	A
CNFG/IMON	14	If VIN < 6.5V, VOUT = VOUT is as expected.	B
		If VIN > 6.5V, the CNFG/IMON pin exceeds the maximum ratings and the pin is damaged.	A
EXTCOMP	15	This brings VCC up to VIN. VOUT = VIN.	A
nINT	16	The pulldown MOSFET of the nFAULT pin is damaged.	A
AGND	17	VIN shorts to GND. VOUT = 0V.	A
VDDA	18	If VIN < 6.5V, there is no impact to the device.	D
		If VIN > 6.5V, the VDDA pin exceeds the maximum ratings and the pin is damaged.	A
VCC	19	If VIN < 12V, there is no impact to the device.	D
		If VIN > 12V, the VCC pin exceeds the maximum ratings and the pin is damaged.	A
SW1, SW2, SW3	20–22	VOUT = VIN; there is excess current from VIN through the low-side FET.	A
PGND1, PGND2, PGND3, PGND4	23–26	VIN shorts to GND. VOUT = 0V.	A
VIN1, VIN2, VIN3	27–29	There is no impact to the device.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 13, 2025 to November 4, 2026 (from Revision * (November 2025) to Revision A (November 2026)) **Page**

- Removed the *TI Confidential - NDA Restrictions* banner..... 2

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