Functional Safety Information

TPS7A14-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the TPS7A14-Q1 (DRV package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

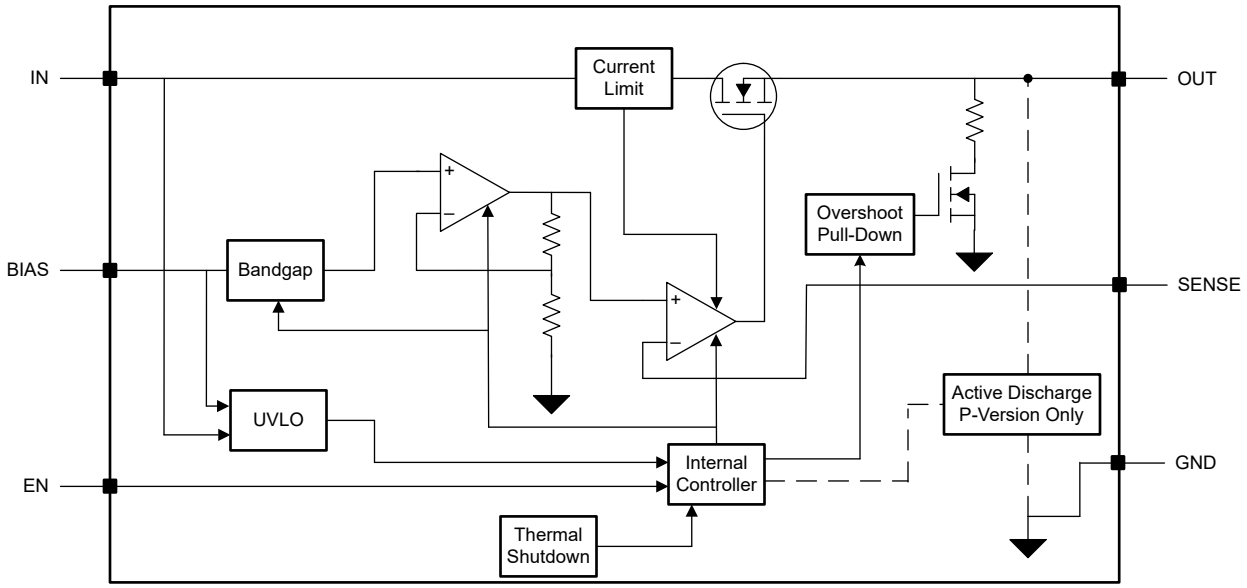

Figure 1-1. Functional Block Diagram

The TPS7A14-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS7A14-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	12
Die FIT rate	9
Package FIT rate	3

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 900mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7A14-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT high (following VIN)	40
VOUT low (no output)	40
Short any two pins	10
VOUT not in specification (voltage or timing)	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7A14-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS7A14-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7A14-Q1 datasheet.

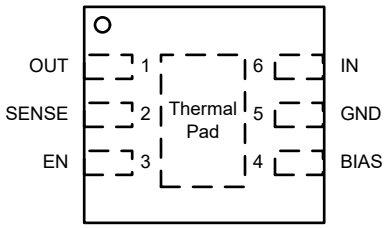

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device operates at free-air temperatures between –40°C and 150°C.
- The device operates at an input voltage of at least 0.7V and no more than 2.2V.
- The device operates according to all recommended operating conditions, and the absolute maximum ratings in the device datasheet are not exceeded.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device hits a current limit state. If the power dissipation is significant, the device hits a thermal shutdown state, and can continue to cycle between the two states. Continuously running the device above the rated current degrades the reliability of the device.	A
SENSE	2	The output voltage is the input voltage minus the dropout voltage because the error amplifier drives the pass transistor gate to the rail.	B
EN	3	The device does not turn on. There is no damage to the device.	B
BIAS	4	An undervoltage lockout (UVLO) of the BIAS pin is asserted, and the device turns off.	B
GND	5	There is no impact to the device. The device operates as normal.	D
IN	6	The device does not turn on. There is no damage to the device.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The output of the device is disconnected from the load.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SENSE	2	The feedback loop loses the regulation point. The output can drift high or become unstable.	A
EN	3	Since the voltage floats to an indeterminate value, the device can disable.	B
BIAS	4	The BIAS supply is lost or floating, which causes a UVLO of the BIAS pin to assert. The device is disabled.	B
GND	5	With the reference pin floating, the voltages at the remaining pins are also floating and the device is not functional. There is a risk of violating the absolute maximum ratings.	A
IN	6	Power is not supplied to the device. The device is not functional	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	SENSE	Regulation of the device remains possible, but the remote sensing capability is lost, and load regulation can degrade due to PCB trace drops.	C
SENSE	2	EN	Depending on the operating conditions, a UVLO of the BIAS pin asserts. Regulation of the device can become unstable or undefined.	B
EN	3	BIAS	The EN pin is forced high whenever the BIAS pin is present, and causes the device to remain enabled whenever the BIAS supply is valid.	B
BIAS	4	GND	A UVLO of the BIAS pin is asserted, and the device is disabled.	B
GND	5	IN	Power is not supplied to the device. The device is not functional.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation of the device is not possible, leading to an undesired output state.	B
SENSE	2	Regulation of the device is not possible, leading to an undesired output state.	B
EN	3	The device remains on, and regulation of the device is possible.	B
BIAS	4	Depending on the operating conditions, the device can trigger a UVLO of the BIAS pin and turn off, or enter a bias voltage (VBIAS) dropout which leads to an undesired output state.	B
GND	5	The device does not turn on. There is no damage to the device.	B
IN	6	There is no impact to the device. The device operates as normal.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

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