

# Extending Ultra-Low-Power Logic Operation Down to 0.63V

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## Abstract

The SN74UVP family is TI's next generation of ultra-low-power logic devices and is capable of drop-in replacement with SN74AUP family. Compared with SN74AUP devices specified down to 0.8V, the extended minimum operating voltage is as low as 0.63V, which enables logic control at lower battery, backup, and energy-harvesting rail voltages. The SN74UVP is drop-in compatible with the SN74AUP family and delivers a typical static supply current of 10nA, as well as loff partial-power-down protection. The operating temperature range of SN74UVP is  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

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## 1 Introduction

Single-gate logic devices are commonly used in wake, reset, enable, interrupt, and power-sequencing paths. These paths can remain powered even when the MCU, RF block, display, or primary system rail are disabled.

For these applications the key design requirements are:

- Very low static supply current ( $I_{CC}$ )
- Reliable operation at the minimum system voltage
- Valid input and output logic levels at low  $V_{CC}$
- Predictable propagation delay at the minimum supply voltage
- Safe behavior during power-up, power-down, and partial-power-down conditions

The SN74UVP family addresses all five requirements. While extending the minimum  $V_{CC}$  from 0.8V to 0.63V, the SN74UVP family maintains a 3.6V maximum.

**Table 1-1. Operating Voltage Range and Key Parameter Comparison**

| Logic Family                        | Min $V_{CC}$ | Max $V_{CC}$ | Max $V_I$ | Typical $I_{CC}$ |
|-------------------------------------|--------------|--------------|-----------|------------------|
| Standard LV-CMOS (for example, LVC) | 1.65V        | 5.5V         | 5.5V      | 1 $\mu$ A        |
| SN74AUP (single channel)            | 0.8V         | 3.6V         | 3.6V      | 500nA            |
| SN74UVP (single channel)            | 0.63V        | 3.6V         | 5.5V      | 10nA             |

## 2 Detailed Description

### 2.1 Applications

The benefit of 0.63V operation is functional continuity at supply voltages where SN74AUP devices are already outside their recommended operating range. This is useful whenever the logic path must remain active after the main system rail is disabled or when the available supply falls below 0.8V.

Typical applications include:

- Always-on wake logic
- PMIC enable and reset control
- Battery end-of-discharge operation
- Backup or retention rails
- Energy-harvesting startup with low open-circuit voltage
- Brownout or power-fail detection

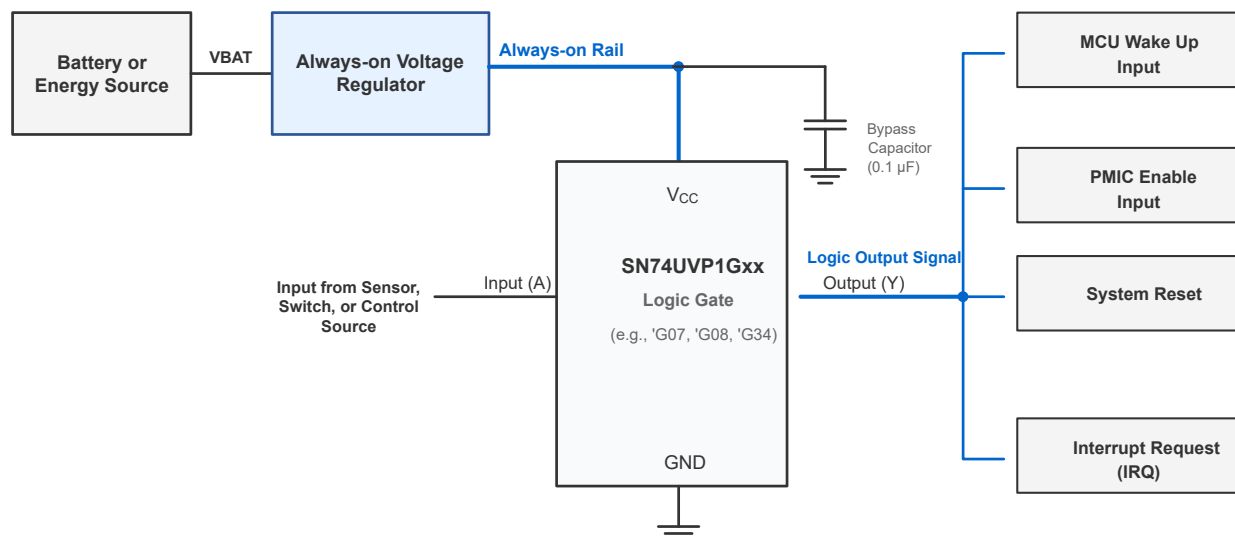


**Figure 2-1. Typical Logic Path Using SN74UVP**

Input threshold margin at 0.63V is a critical design constraint. The SN74UVP uses a  $V_{IH} = 0.65 \times V_{CC}$  and  $V_{IL} = 0.35 \times V_{CC}$  threshold scheme across the  $V_{CC}$  range of 0.63V to 1.98V. At  $V_{CC} = 0.63V$ , this gives:

- $V_{IH} (\text{min}) = 0.41V$
- $V_{IL} (\text{max}) = 0.22V$
- Noise margin = 0.19V on each side

The SN74UVP inputs are 5.5V-tolerant, allowing inputs from higher-voltage domains to drive the device even when  $V_{CC}$  is low. Built-in input hysteresis improves immunity to slow or noisy input transitions, which is particularly useful at low  $V_{CC}$  where signal amplitudes are small.

At 0.63V, the SN74UVP is practical for low-power control signals rather than high-speed data paths. Output drive strength is reduced, and propagation delay increases significantly as  $V_{CC}$  decreases.

## 2.2 Power Consumption

For always-on logic, current consumption is often the most important design parameter. The SN74UVP family achieves a typical  $I_{CC}$  of 10nA across the full  $V_{CC}$  range of 0.63V to 3.6V, with a maximum of 1.4μA over the full operating temperature range.

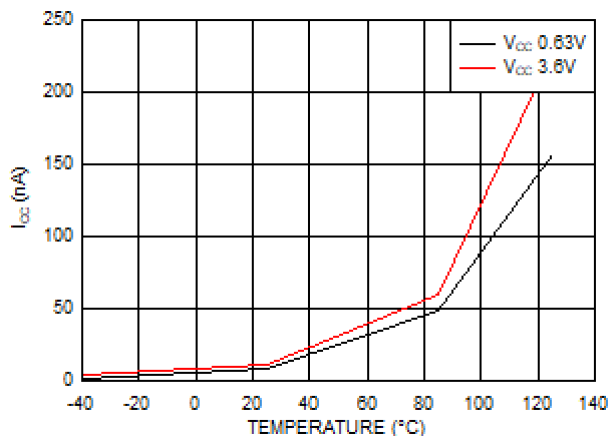
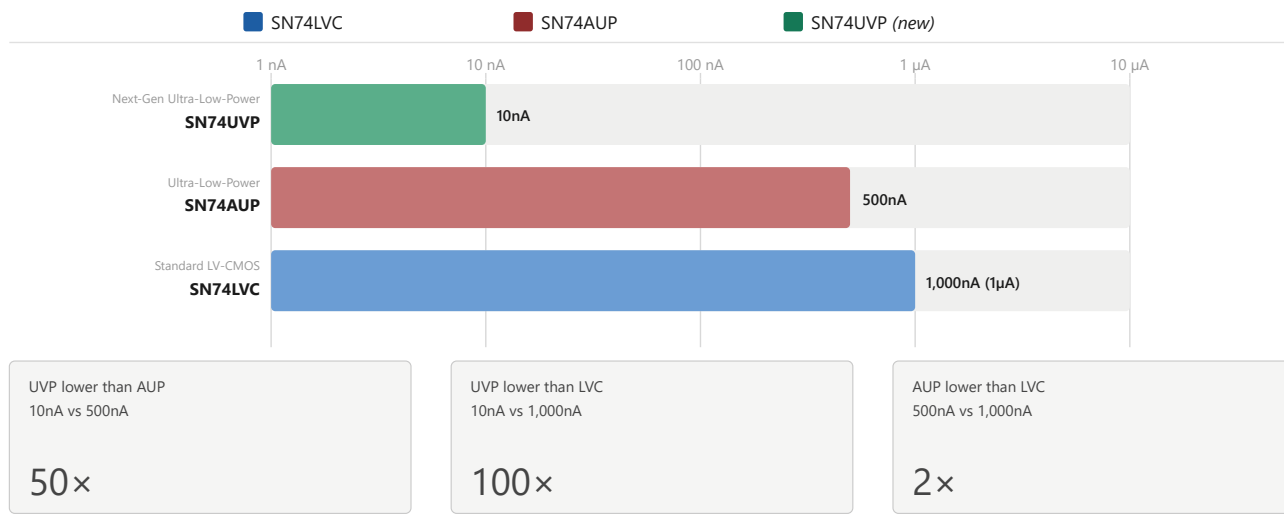


**Figure 2-2. Static Supply Current vs Supply Voltage**

The SN74UVP achieves a typical  $I_{CC}$  of just 10nA — a 50× reduction compared to the SN74AUP family (500nA typical) and a 100× reduction compared to the standard SN74LVC family (1,000nA typical).



SN74UVP vs SN74AUP vs SN74LVC |  $V_I = V_{CC}$  or GND,  $T_A = 25^\circ\text{C}$

**Figure 2-3. Typical  $I_{CC}$  of the SN74UVP, SN74AUP, and SN74LVC at 25°C**

## 2.3 Timing at Low Supply Voltage

Propagation delay increases sharply as  $V_{CC}$  decreases. Timing must always be verified at the minimum system operating voltage and worst-case temperature, not only at 1.8V or 3.3V.

The SN74UVP family shows a large increase in propagation delay below 0.8V. As a reference, at  $V_{CC} = 0.63V$  with  $C_L = 5pF$ ,  $t_{pd}$  maximum is approximately 310ns. At  $V_{CC} = 0.8V$  with  $C_L = 5pF$ ,  $t_{pd}$  maximum is approximately 50ns. At  $V_{CC} = 1.8V$  with  $C_L = 15pF$ ,  $t_{pd}$  maximum is approximately 6ns. Refer to the specific device datasheet for the exact  $t_{pd}$  specifications at each  $V_{CC}$  and load condition.

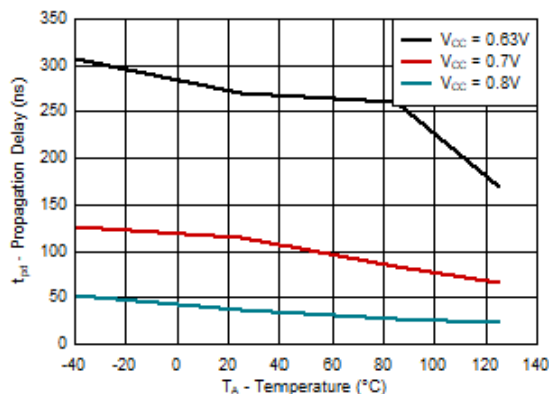


Figure 2-4. Propagation Delay vs Temperature ( $C_L = 5pF$ )

## 2.4 Power-Up, Power-Down, and Ioff Behavior

In multi-rail systems, the SN74UVP can be unpowered ( $V_{CC} = 0V$ ) while another device connected to the input or output of SN74UVP remains active. Without protection, current can flow from the active signal into the  $V_{CC}$  rail of the unpowered device, causing back-powering and unintended circuit behavior.

The SN74UVP family includes Ioff partial-power-down protection. When  $V_{CC} = 0V$ , the Ioff circuitry limits leakage current into the input and output pins to a maximum of  $\pm 1\mu A$ , preventing back-powering of the supply rail. The inputs and outputs of the SN74UVP can tolerate applied voltages up to 5.5V under recommended operating conditions when  $V_{CC} = 0V$ .

### 3 Summary

The SN74UVP family extends ultra-low-power single-gate logic operation down to 0.63V — below the 0.8V lower limit of SN74AUP devices. The extended voltage range enables simple logic control functions to remain active in always-on, backup, battery end-of-discharge, and energy-harvesting applications where the available supply can fall below 0.8V.

The most important design considerations for 0.63V operation are:

- Static current: Verify  $I_{CC}$  meets the always-on standby power budget.
- Input threshold margin: Verify the driving source meets the noise margin level of  $V_{IH}(\min)$  and  $V_{IL}(\max)$ .
- Input transition rate: Do not exceed the  $\Delta t/\Delta V$  limit, this limits the input rise and fall time.
- Propagation delay: Verify timing at worst-case, delay at 0.63V is significantly longer than at 1.8V or 3.3V.
- Partial-power-down:  $I_{off}$  limits leakage to  $\pm 1\mu A$  maximum when  $V_{CC} = 0V$ , with input and output pins tolerating up to 5.5V.
- Output loading: Minimize output capacitance due to reduced drive strength at the lower voltage.

## 4 References

1. Texas Instruments, [SN74UVP1G06 Single, 0.65V-to-3.6V low-power low-voltage inverter with open-drain outputs](#), product page
2. Texas Instruments, [Logic Guide](#), application note

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