Application Note

Managing Receiver Output Transient in RS-485 Half-Duplex Systems With THVD4431A

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Abstract

RS-485 transceivers with fast edge rates and short driver disable times enable high-speed communication but require careful system design to manage transient behavior during direction switching. This application note discusses a system-level consideration when using high-performance RS-485 transceivers, such as the THVD4431(A) in half-duplex mode with ferrite beads on the bus lines. Practical design recommendations are provided to verify robust UART communication.

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Trademarks

1 Introduction

RS-485 is a robust differential physical-layer standard widely used in industrial automation, building automation, and telecommunications for long-distance, multi-point communication. In many applications, a half-duplex RS-485 transceiver shares a single pair of differential bus lines for both transmitting and receiving. The direction of data flow is controlled by a direction (DIR) pin, which enables the driver and disables the receiver during transmission, and vice versa during reception.

THVD4431 is a highly integrated multiprotocol transceiver supporting RS-232, RS-422, and RS-485 physical layers. In RS-485 half-duplex mode, the DIR pin controls the bus direction: when DIR is high, the driver is enabled, and the receiver is disabled. When DIR is low, the driver is disabled, and the receiver is enabled.

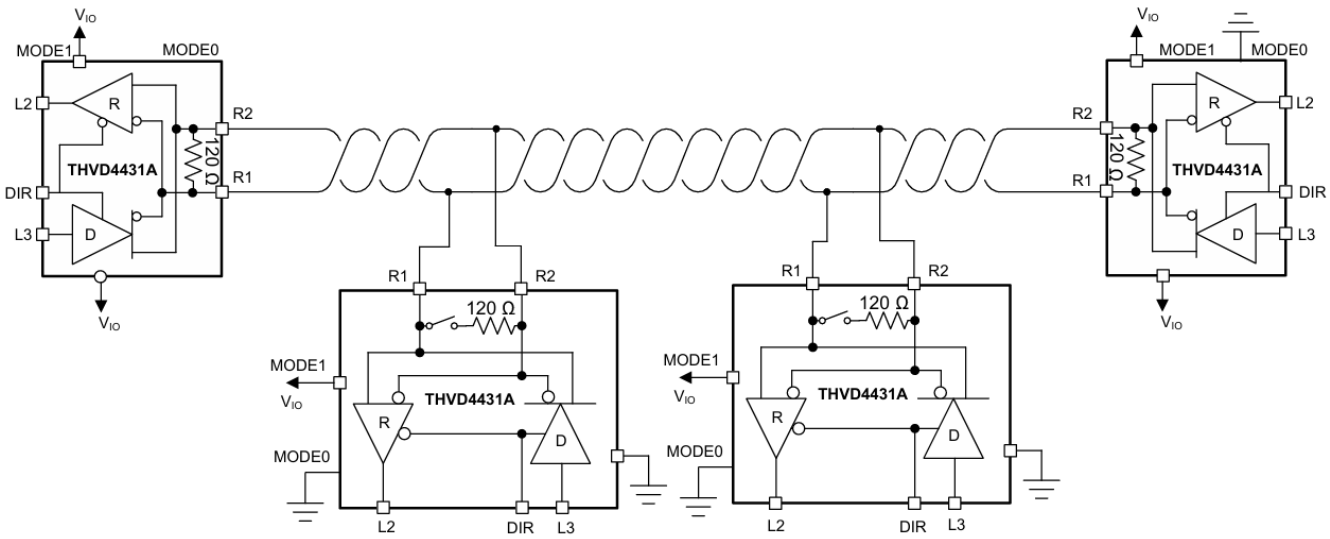

Figure 1-1. Typical RS-485 Network with Half-Duplex Transceivers

In certain system implementations, a glitch can appear on the receiver output pin (L2) during the DIR high-to-low transition. This glitch can be misinterpreted by the UART as a start bit, causing an extra 0x00 byte to be received and leading to system level frame errors. This application note analyzes the root cause of this glitch and provides practical designs.

2 THVD4431A RS-485 Half-Duplex Operation

2.1 Mode Configuration

THVD4431A is configured for RS-485 half-duplex mode through the MODE pins. The device supports multiple protocols including RS-232, RS-422, and RS-485, with pin-selectable mode control. In RS-485 half-duplex mode:

- DIR = High → Driver enabled, receiver disabled (transmit mode)
- DIR = Low → Driver disabled, receiver enabled (receive mode)

2.2 Driver Disable Timing

A key parameter for understanding the glitch is the driver disable time. Ideally, switching from transmit mode to receive mode has no switching time, but that's impossible for actual analog device. For THVD4431A, the typical driver disable time is around 65ns. This switching time results in turn-off of the RS-485 driver, which can generate significant di/dt when inductive elements are present on the bus.

3 System-Level Transient Behavior

3.1 What Is Observed

In systems where ferrite beads are placed on the RS-485 bus lines (R2 and R1), a brief voltage disturbance can appear on the receiver output (R) when the transceiver switches from transmit to receive mode (DIR high-to-low transition).

This transient is of very short duration and is typically below the sampling window of most UARTs. However, in some system configurations, the transient can be interpreted as a start bit, leading to an unexpected 0x00 byte and subsequent checksum or framing errors. Figure 3-1 represents what the spike and glitch look like theoretically, and Figure 3-2 shows the actual waveform captured on board.

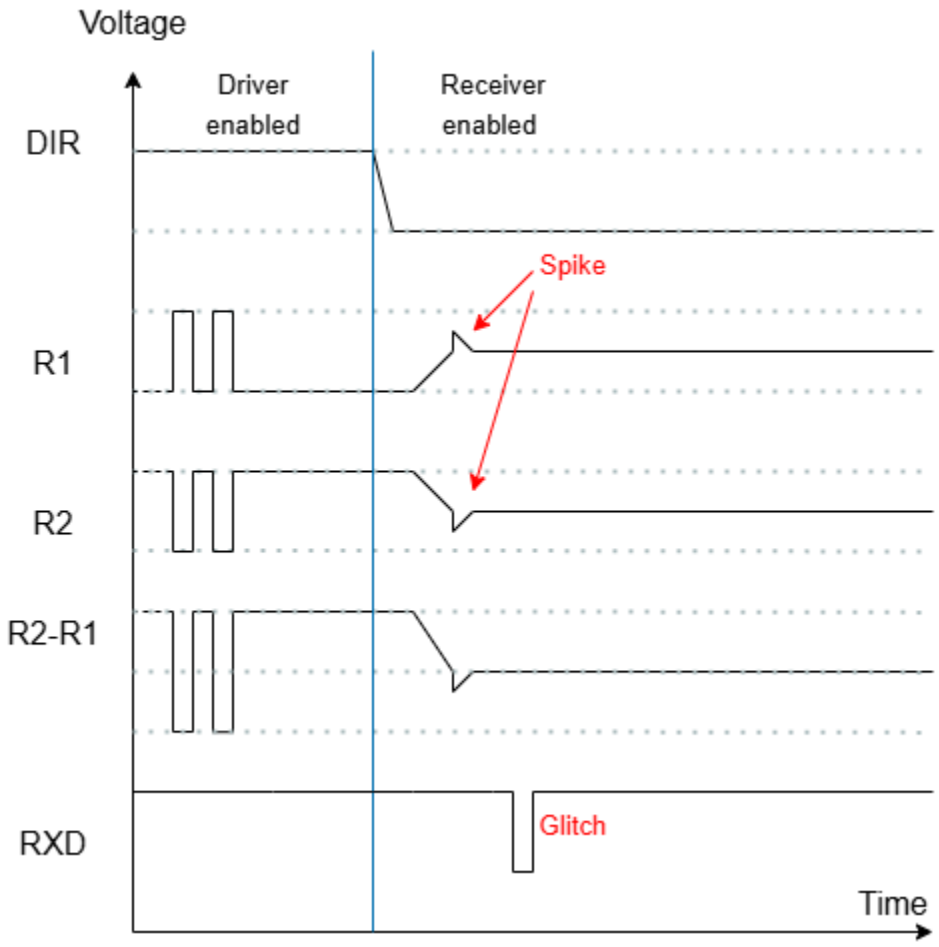

Figure 3-1. Theoretical RXD Glitch State

Figure 3-2. Actual RXD Glitch (Approximately 100ns)

3.2 Why It Occurs

The inductive energy storage in ferrite beads is the root cause for this glitch on RXD. Ferrite beads are common on RS-485 interfaces for EMI suppression. While effective, ferrite beads are inductive components that store energy when current flows through them. If the series bus parasitic inductance is large enough, the same effect can also occur.

During transmission (DIR = High), current flows through the ferrite beads on both bus lines, magnetizing them. During transition (DIR High-to-Low), the driver turns off and current stops flowing. The energy stored in the inductances dissipates through the system's load and parasitic elements. This dissipation produces a brief ringing waveform on the bus of R2 and R1. For a short period, this creates a differential voltage across the bus that can approach the receiver input threshold, and lead to the glitch on RXD.

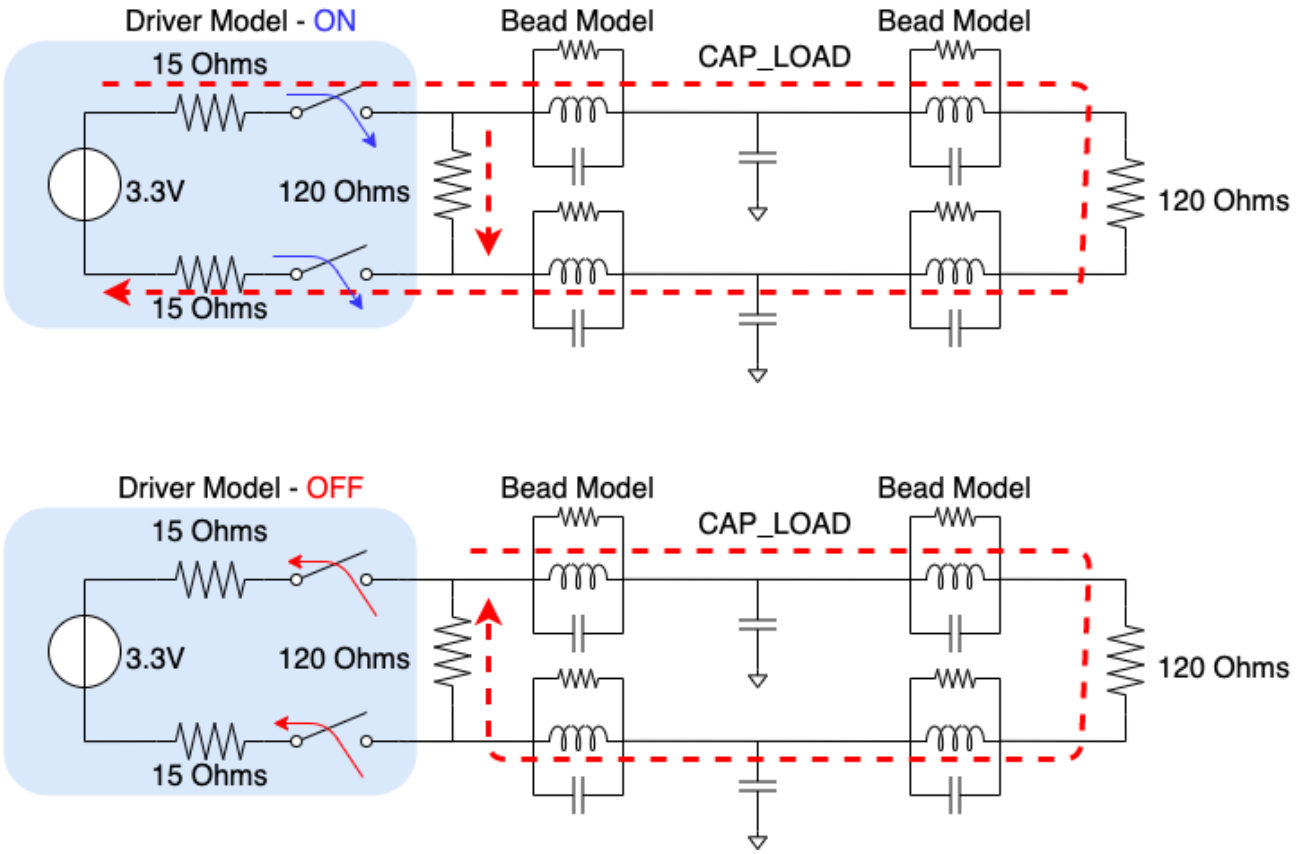

Figure 3-3. Effect of Bead (Series Bus Inductance)

Figure 3-4 shows the simulation circuit, including real bead model, capacitor and far-end terminal resistor. Figure 3-5 shows the simulation results with Glitch on L2, and agrees with the theoretical analysis.

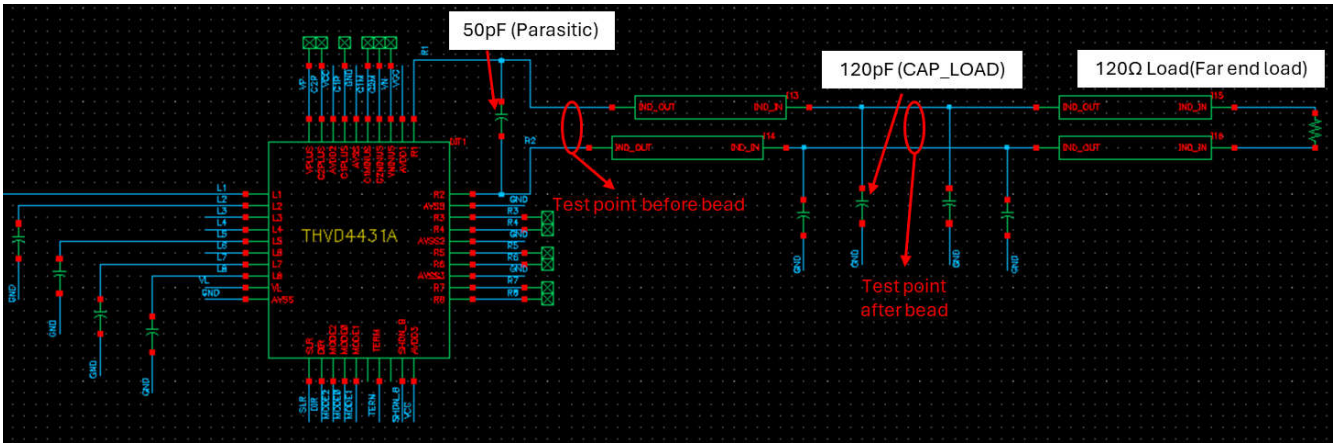

Figure 3-4. Simulation Circuit with Real Bead Model

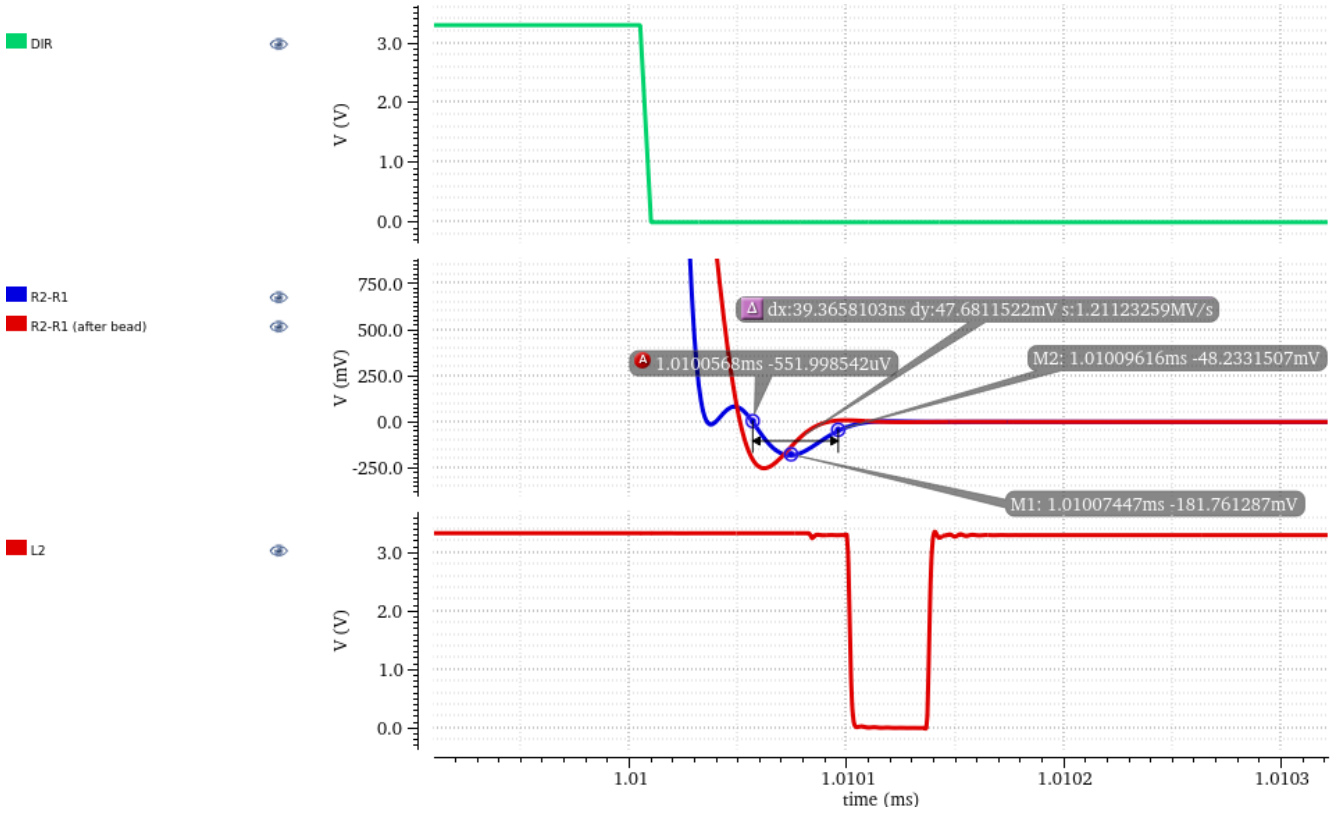

Figure 3-5. Simulated Glitch on RXD (L2)

The driver disable time of THVD4431A is 65ns typical. This fast turn-off is a feature that enables higher data throughput, reduces bus contention time and improves overall system efficiency. However, fast turn-off also produces higher di/dt. When ferrite beads are present, this results in a higher-amplitude transient compared to slower legacy devices. Because this is the natural behavior of any high-speed transceiver operating in the presence of inductive bus components, the same transient can be observed with any fast RS-485 transceiver under similar conditions.

4 Design Recommendations

The following design practices verify robust communication when using THVD4431A or any high-speed RS-485 transceiver.

4.1 Increase Differential Bus Capacitance

Adding capacitance across the bus lines attenuates transients by providing a low-impedance path for high-frequency energy. If adding additional beads to improve the EMI performance, use the following recommendations:

- Add a differential capacitor (R2 to R1) with values larger than 220pF and place as close as possible to the transceiver pins. Figure 4-1 presents simulation results with the bus capacitor (CAP_LOAD) from 20pF to 620pF.
- Add capacitors to ground on each bus line. Figure 4-2 presents the actual waveform after adding the bus capacitor of 390pF to GND each other.

This workaround can have slight impact on signal integrity, so TI recommends users test on boards to verify signal integrity. Figure 4-3 shows the rise and fall time increase from approximately 18ns to approximately 40ns at 620pF total, and 10Mbps of communication remains fully supported.

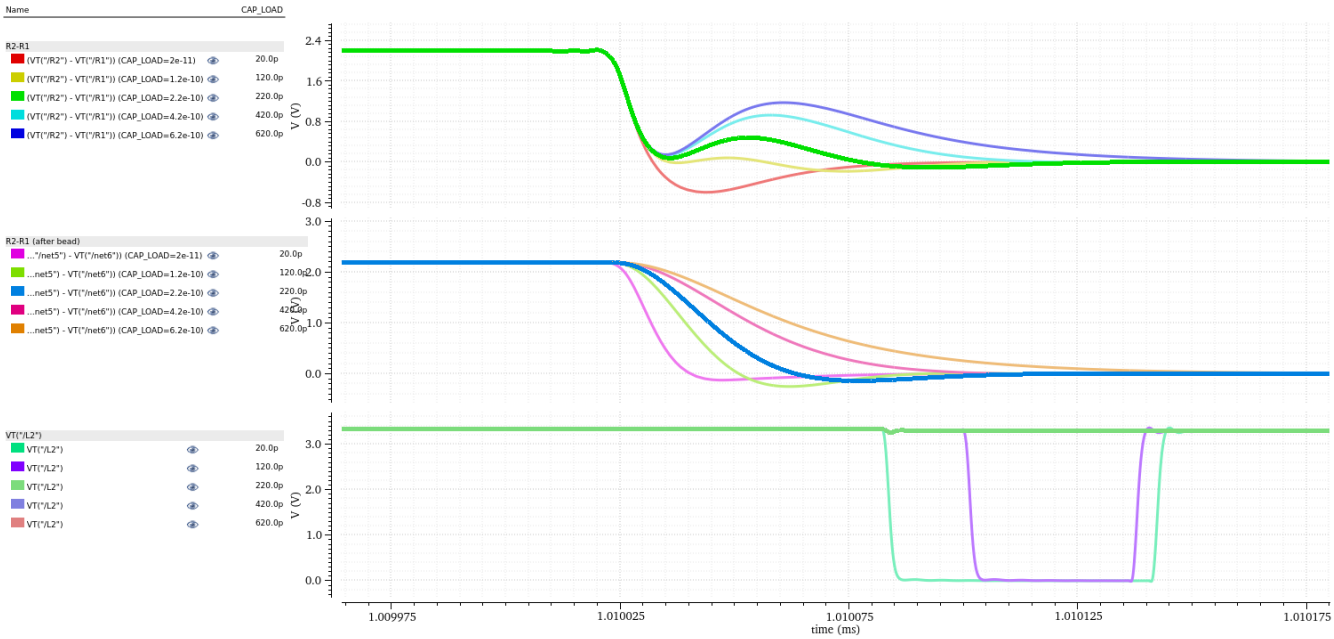

Figure 4-1. Simulation Results: Effect of CAP_LOAD from 20pF to 620pF

Figure 4-2. Test Results: No Glitch After Increasing Bus Capacitor

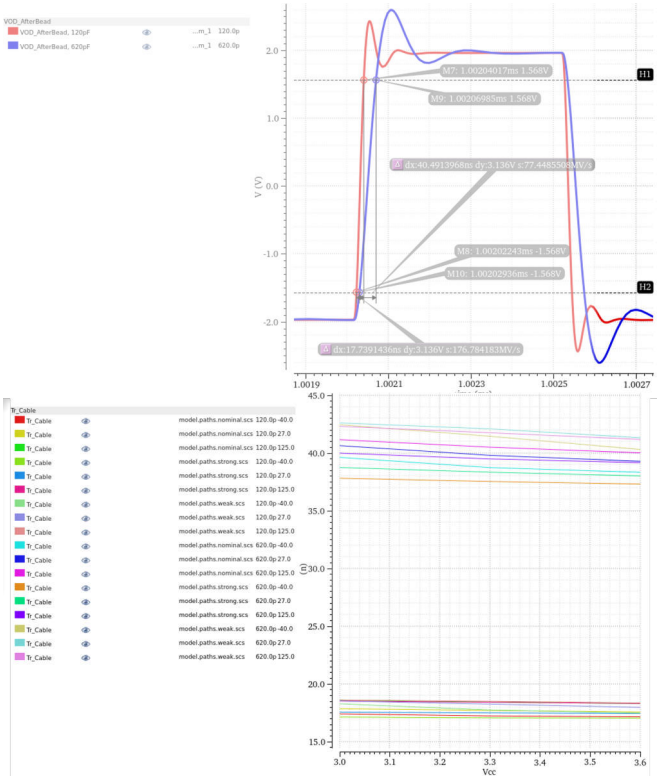

Figure 4-3. Simulation Results: Effect of Increasing CAP_LOAD (120pF and 620pF)

4.2 Add Bus Biasing Resistors

External fail-safe biasing resistors provide a defined bus state during idle periods and help damp transients. Pullup on R2 (to VIO) and pulldown on R1 (to GND) with value range of 750Ω to 10kΩ. Lower values provide stronger biasing but increase quiescent current, so 1kΩ to 10kΩ is preferred for most applications.

4.3 Ferrite Bead Selection

When EMI filtering is required:

- Select ferrite beads with lower inductance and higher DC resistance, which improve damping.
- Consider placing ferrite beads closer to the connector rather than immediately adjacent to the transceiver.
- Evaluate transient behavior during system validation.

4.4 Software Consideration

Because the transient occurs only during the DIR transition period when the receiver is being enabled, the UART of the MCU is typically not actively sampling. If the transient is captured by the UART, firmware can be configured to ignore the RX signal during the direction-change window as a temporary workaround.

5 Summary

Fast transceivers such as THVD4431A offer significant performance advantages but require appropriate attention to system-level design. Ferrite beads on RS-485 bus lines interacted with fast driver disable transitions produce brief transients. Three practical solutions are available:

1. Add ≥220pF differential capacitance across the bus
2. Add external fail-safe bias resistors (750Ω to 10kΩ)
3. Select ferrite beads with appropriate damping characteristics

These recommendations apply broadly to any high-speed RS-485 transceiver and represent good engineering practice for robust industrial communication systems.

6 References

1. Texas Instruments, *THVD4431A Multiprotocol (RS-232, RS-422, RS-485) Transceiver With 120Ω Switchable Termination, Pin-Selectable Diagnostic Loopback, and IEC-ESD*, datasheet.

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