Application Note

Signal Sensing in ATE Systems

JIngquan Zhu

ABSTRACT

This article discusses how to sense signal in ATE system and give TI designs for these applications. For ultra-high voltage sensing, give two designs to resolve accuracy and fast sampling requirements.

Table of Contents

Trademarks

1 Introduction

ATE system is for semiconductor chip testing. Each chip needs to pass testing cases before it is shipped to customer or product manufacturer. So ATE systems play a vital role in semiconductor manufacturing. It requires high speed to complete complex tests in seconds instead of hours because high speed means small testing time and low cost. Another, with advancements in semiconductor technology, chip signal accuracy is becoming increasingly high, ATE testing system needs higher measuring accuracy. Lastly, ATE system needs to be scalable. There are thousands of channels to perform the same testing cases for hundreds of chips in ATE system at the same time, that means these testing channels have same functionality and performance.

2 Detailed Description

2.1 ATE Testing Card and Signal Sensing

In ATE system, there are many functional cards like DPS, PE, PMU, HV PMU, Digitizer and AWG, RF, and so on. Each board has special testing functions. DPS is for supplying power to DUT. PE is integrated Pin driver and PPMU and active load to test many functions like pattern testing and open or short testing, and so on. PMU is testing DUT parameters, such as current or voltage. AWG is for generating arbitrary waveform to measuring like SNR, THD, audio performance, and so on.

There are many current or voltage signals that need to be sampled and measured in every function card. For example, in DPS or PMU, output voltage and current need to be measured. In PE, output voltage needs to be measured for calibration. There are also some general power supply must be monitored in every function board.

2.2 Signal Sensing Requirements

The first is fast measuring. Signal sensing circuit must have preferred bandwidth and slew rate. Typically, signal settling time needs to be less than tens of us, and sometimes, it needs to be less than several us, for example, <6us.

The second is accuracy. In most ATE systems, the measuring accuracy needs to be from 500ppm to 10ppm, so the testing probe circuit has as small a testing impact as possible on the DUT. When testing current, the drawn current of the probe circuit needs to be lower by at least two levels than the current range, for example, if the measured max current is 10uA, the leakage of the current sensing circuit needs to be less than a few pAs. If the max current is 100pA, the current leakage needs to be less than a few fAs.

The last is scalability. The sensing circuits should be able to be copied and reusable. This means the circuit is better off not being much influenced by component tolerance parameters or PCB board parasitic parameters.

2.3 Signal Sensing

In most measuring cases, the typical circuit topology is as shown in Figure 2-1. The buffer converts the signal voltage to the ADC input range. In some cases, an ADC with an integrated AFE buffer can directly sense the signal voltage or current, such as the ADS9308V8I, which has eight voltage channels and eight current channels of ADC.

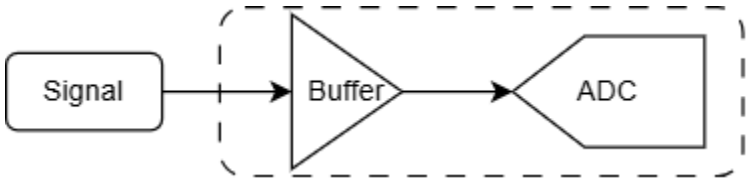

Figure 2-1. Signal Sensing Typical Topology

2.4 General Purpose Sensing

It is very common to monitor power supply voltage or current in ATE systems. In these cases, the buffering voltage circuit can be two resistors divider (as shown in Figure 2-2) to scale down to ADC voltage range. This does not need speed or high accuracy, just pay attention to the maximum divided voltage ratio and resistor power and voltage rating.

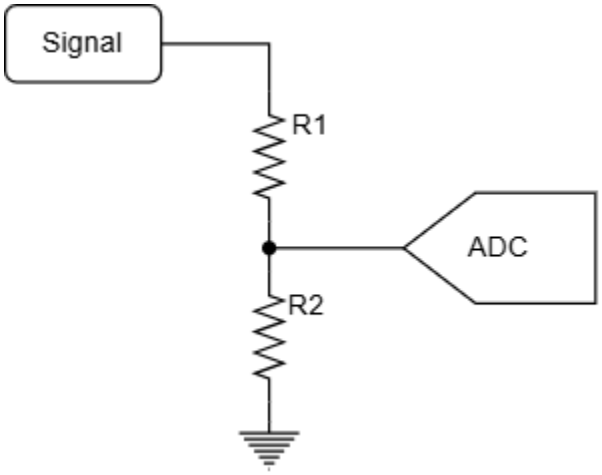

Figure 2-2. General Purpose Sensing Topology

Buffering current circuits may be a current sensing amplifier.

INA187, INA180 and INA214 are difference amplifiers for current sensing. INA751A, INA750A and INA791A are difference amplifiers which are integrated current sensing resistor. INA2227, INA234 or INA237 are integrated ADC and current sensing difference amplifiers. INA745A, INA701 and INA740 are integrated ADC and difference amplifier and current sensing resistor.

Sampling ADC may not be very high resolution and fast. ADS8689W, ADS1015L and ADS1014L are low cost and I2C ADC.

2.5 Precision Signal Sensing

There are many precision signals that need to be measured in an ATE system.Figure 2-3 is a typical precision voltage sensing circuit. A low leakage and fast buffer (Figure 2-3) is placed before the resistor divider. In some cases, the PGA can take low leakage and scale down requirements, such as PGA855 and PGA849.

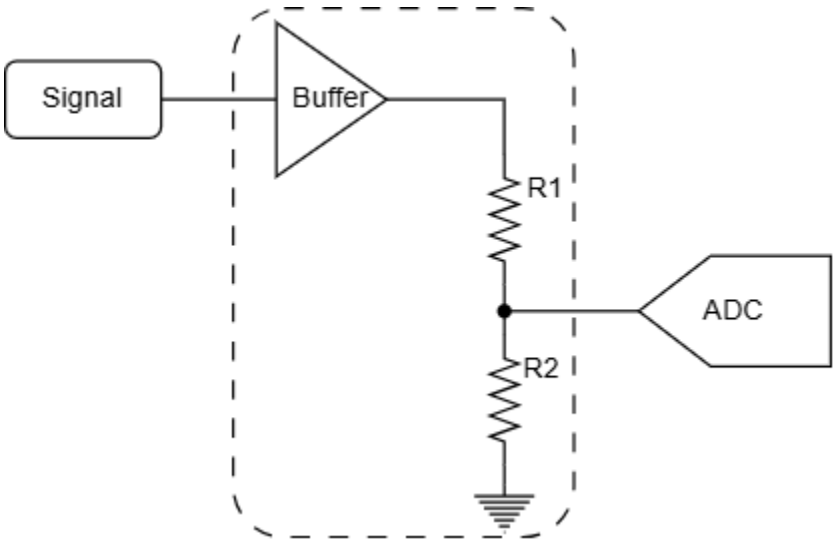

Figure 2-3. Precision Signal Sensing Topology

Next, this document discusses some typical sensing approaches according to different voltage and current leakage and bandwidth requirements.

2.5.1 Middle and High Voltage Signal

Precision middle voltage sensing is most common application in PMU and DPS, For voltage<200V, Table 2-1 OP buffer can be used.

Table 2-1. Middle and High Voltage Buffer Amplifier

PN	Key Feature
OPA182	36V, 5Mhz, 10V/us, Ib=50pA(typ), CMRR=168dB(typ, ±18V), THD+N=0.8ppm, En=0.119uVpp Offset drift=3nV/°C
OPA196	36V, 2.5Mhz, 5.5V/us, Ib=5pA(typ), CMRR=140dB(typ, ±18V), THD+N=12ppm, En=7uVpp Offset drift=0.5uV/°C
OPA192	36V, 10Mhz, 20V/us, Ib=5pA(typ), CMRR=140dB(typ, ±18V), THD+N=0.8ppm, En=4uVpp Offset drift=0.1uV/°C
PGA849	36V, 10Mhz, 35V/us, Ib=500pA(typ), CMRR=100dB(gain=1), THD+N=3.2ppm, En=0.91uVpp(gain=1) Offset drift=0.2uV/°C, gain drift=1ppm/°C(max)
PGA854	36V, 6.2Mhz, 45V/us, Ib=500pA(typ), CMRR=88dB(gain=1), THD+N=11ppm, En=0.76uVpp(gain=1) Offset drift=0.2uV/°C, gain drift=0.2ppm/°C
PGA855	36V, 10Mhz, 35V/us, Ib=500pA(typ), CMRR=88dB(gain=1), THD+N=3.2ppm, En=0.8uVpp(gain=1) Offset drift=0.3uV/°C, gain drift=1ppm/°C(max)
OPA486	48V, 5.6Mhz, 15V/us, Ib=50pA(typ), CMRR=160dB(±24V), THD+N=1.2ppm, En=0.3uVpp Offset drift=5nV/°C
OPAx488	48V, 14Mhz, 40V/us, Ib=55pA(typ), CMRR=150dB(±24V), THD+N=1.2ppm, En=0.3uVpp Offset drift=4nV/°C
OPA596	85V, 3.75Mhz, 100V/us, Ib=5pA(typ), CMRR=140dB, THD+N=8ppm, En=1.4uVpp Offset drift=1uV/°C
OPA591	85V, 3.75Mhz, 100V/us, Ib=5pA(typ), CMRR=140dB, THD+N=8ppm, En=1.4uVpp Offset drift=0.3uV/°C
OPA454	100V, 2.5Mhz, 13V/us, Ib=1.4pA(typ), CMRR=146dB, THD+N=8ppm, En=15uVpp Offset drift=1.6uV/°C
OPA455	150V, 6.5Mhz, 32V/us, Ib=30pA(typ), CMRR=128dB, THD+N=9ppm, En=12uVpp Offset drift=4uV/°C
OPA462	180V, 6.5Mhz, 32V/us, Ib=30pA(typ), CMRR=128dB, THD+N=9ppm, En=12uVpp Offset drift=4uV/°C

2.5.2 Current Signal with Middle and High Common Mode Voltage

Figure 2-4 shows a typical current sensing topology. For a low common-mode-voltage current signal, a PGA or INA may be used directly for sensing the current signal. For an over-36V common-mode-voltage current signal, a discrete buffer and difference op amp (difference op amp, INA, or PGA) are mostly used instead.

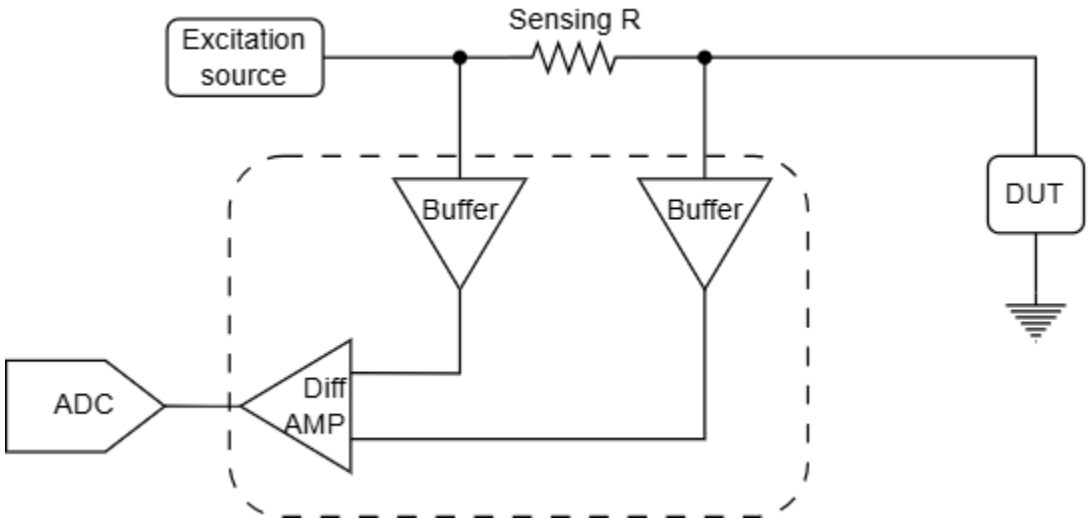

Figure 2-4. Typical Current Sensing Topology

The buffer and PGA are the same as above. The difference op amp and INA (Table 2-2) can be selected as shown in Table 2-2.

Table 2-2. Difference Amplifiers

PN	Key Feature
INA597	Input voltage -54~+54V, 2Mhz, input impedance = 12k ohm, CMRR=94dB, En=6uVpp, THD+N=6.6ppm, offset drift=1.4uV/°C, gain drift=0.25ppm/°C
INA592	Input voltage -54~+54V, 2Mhz, input impedance = 24k ohm, CMRR=94dB, En=6uVpp, THD+N=6.6ppm, offset drift=0.7uV/°C, gain drift=0.2ppm/°C
INA149	Input voltage -275~+275V, 0.5Mhz, input impedance = 200k ohm, CMRR=100dB, En=20uVpp, offset drift=0.7uV/°C, gain drift=0.2ppm/°C
INA851	36V, 22Mhz, 37V/us, Ib=5nA(typ), CMRR=96dB(gain=1), THD+N=3.5ppm, En=12uVpp Input Offset drift=5uV/°C, output offset drift=5uV/°C, gain drift=35ppm/°C (gain>1)
INA823	36V, 1.9Mhz, 32V/us, Ib=1.2nA(typ), CMRR=110dB(gain=1), En=0.4uVpp Input Offset drift=0.2uV/°C, output offset drift=1uV/°C, gain drift=12ppm/°C (gain>1)
INA818	36V, 2Mhz, 0.9V/us, Ib=0.15nA(typ), CMRR=105dB(gain=1), En=2.6uVpp Input Offset drift=0.4uV/°C, output offset drift=5uV/°C, gain drift=35ppm/°C (gain>1)
INA821	36V, 4.7Mhz, 2V/us, Ib=0.15nA(typ), CMRR=105dB(gain=1), En=2.5uVpp Input Offset drift=0.1uV/°C, output offset drift=5uV/°C, gain drift=35ppm/°C (gain>1)

2.5.3 Signal Which Requires Very Low Current Leakage

When the current signal range is at the nA or pA level, the current leakage of the sensing path buffer needs to be at the fA level; otherwise, the measuring accuracy will be greatly affected. For fA-leakage op amps, Table 2-3 can be used:

Table 2-3. fA Current Leakage Buffer Amplifiers

PN	Key Feature
OPA928	36V, 2.5Mhz, 5V/us, Ib=1fA(typ), CMRR=120dB, THD+N=12ppm, En=1.4uVpp Offset drift=0.1uV/°C
LMP7721	5.5V, 17Mhz, 10V/us, Ib=3fA(typ), CMRR=100dB, THD+N=7ppm, Offset drift=1.5uV/°C
LMC608x	15.5V, 1.3Mhz, 1.5V/us, Ib=10fA(typ), CMRR=85dB, THD+N=2000ppm, Offset drift=1uV/°C

2.5.4 Fast Voltage Signal

For signals like RF, C-phy and D-phy signal, these frequencies are up to Ghz.

Table 2-4. High Bandwidth Buffer Amplifiers

PN	Key Feature
OPA892	±18V, 2Ghz, 700V/us, 200mA, Ib=-9uA(typ), CMRR=104dB, THD+N=2ppm(1Khz), Offset drift=1uV/°C
OPA955	5.25V, 11Ghz, 3750V/us, input capacitance = 0.9pF, Ib=-2uA(typ), CMRR=86dB, HD2=-62dBc(100Mhz), HD3=74dBc(100Mhz), Offset drift=1uV/°C
OPA855	5.25V, 8Ghz, 2750V/us, input capacitance = 0.6pF, Ib=-12uA(typ), CMRR=86dB, HD2=-65dBc(100Mhz), HD3=74dBc(100Mhz), Offset drift=1uV/°C
BUF802	Buffer, ±6.5V, 3.1Ghz, 7000V/us, Offset drift=700uV/°C
TRF1218	25Ghz, single to difference, 50ohm in/out, HD2=-62dBc, HD3=-50dBc. OP1dB=13.1dBm(16G)

2.5.5 Ultra-High Voltage Signal

1. Resistor Divider and Capacitor Approach

   For signal voltage over 200V or 400V, it is difficult to find a preferred buffer amplifier with high voltage and low leakage and high bandwidth. Many times, two resistor divider with parallel capacitors are designed for converting high voltage to low voltage to fit ADC input range. it is very effective, has relatively small current leakage, simple circuit and small layout area if divider resistors and capacitors value are not too high and very accurately. Following Figure 2-5 is a simulation which uses resistors and capacitors divider in ultra-high voltage sensing. It is drawed in TINA-TI simulation tool which is downloaded from TI.com.

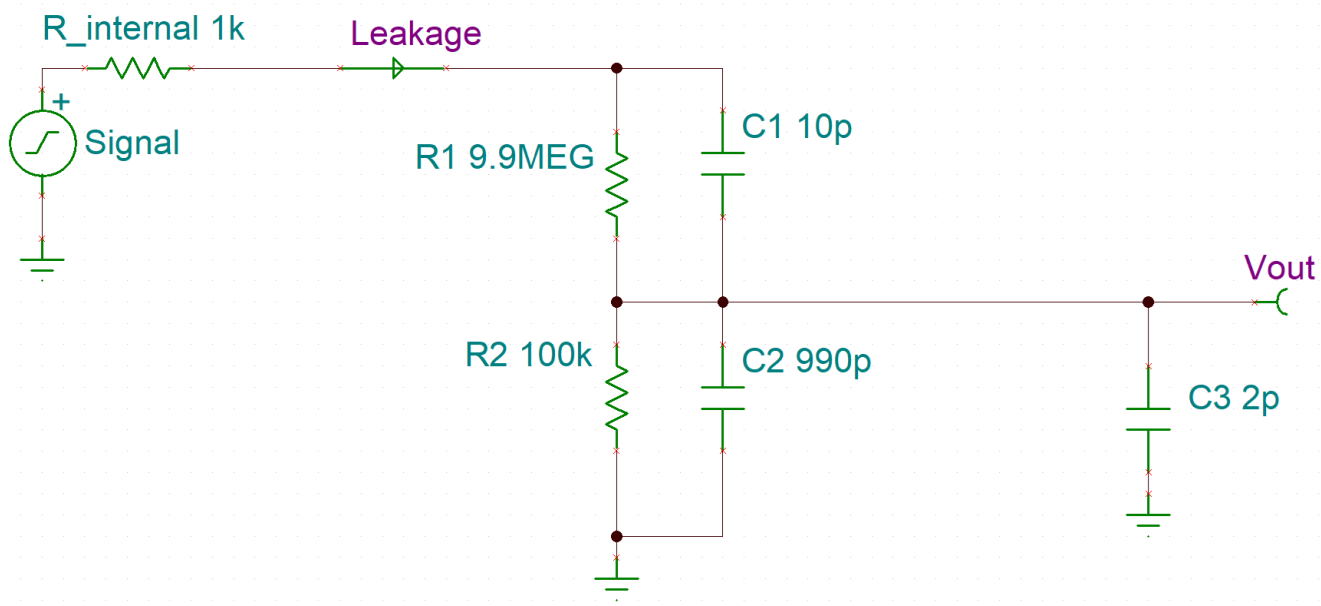

Figure 2-5. RC Divider Sensing Simulation Circuit

Assume input 200V step with max 200mA output capability(R_internal=1K ohm), resistor and capacitor are ideal, and there is not parasitic parameter in layout and trace. From simlation result, everything looks perfect especially for very small settling time (Figure 2-6), but it has 20uA current leakage and converting output accuracy is not good because different signal sources have different internal resistance.

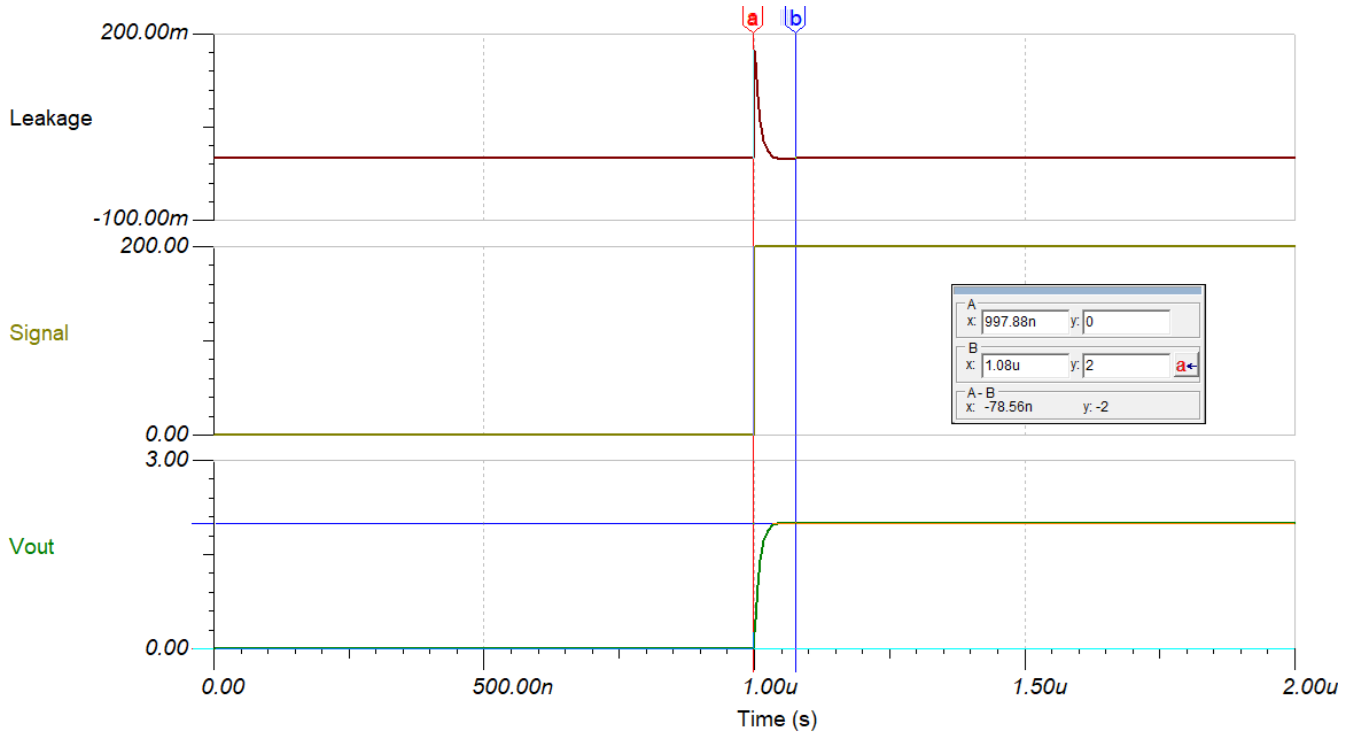

Figure 2-6. RC Divider Simulation Result

If considering capacitor and layout are not ideal, let's say C1 total capacitance vary from 6pF to 14pF, we will see settling time (Figure 2-7) is different and max is near 0.5ms, and sometimes overshoot is very big which means need reserve enough input margin for ADC and lost ADC resolution.

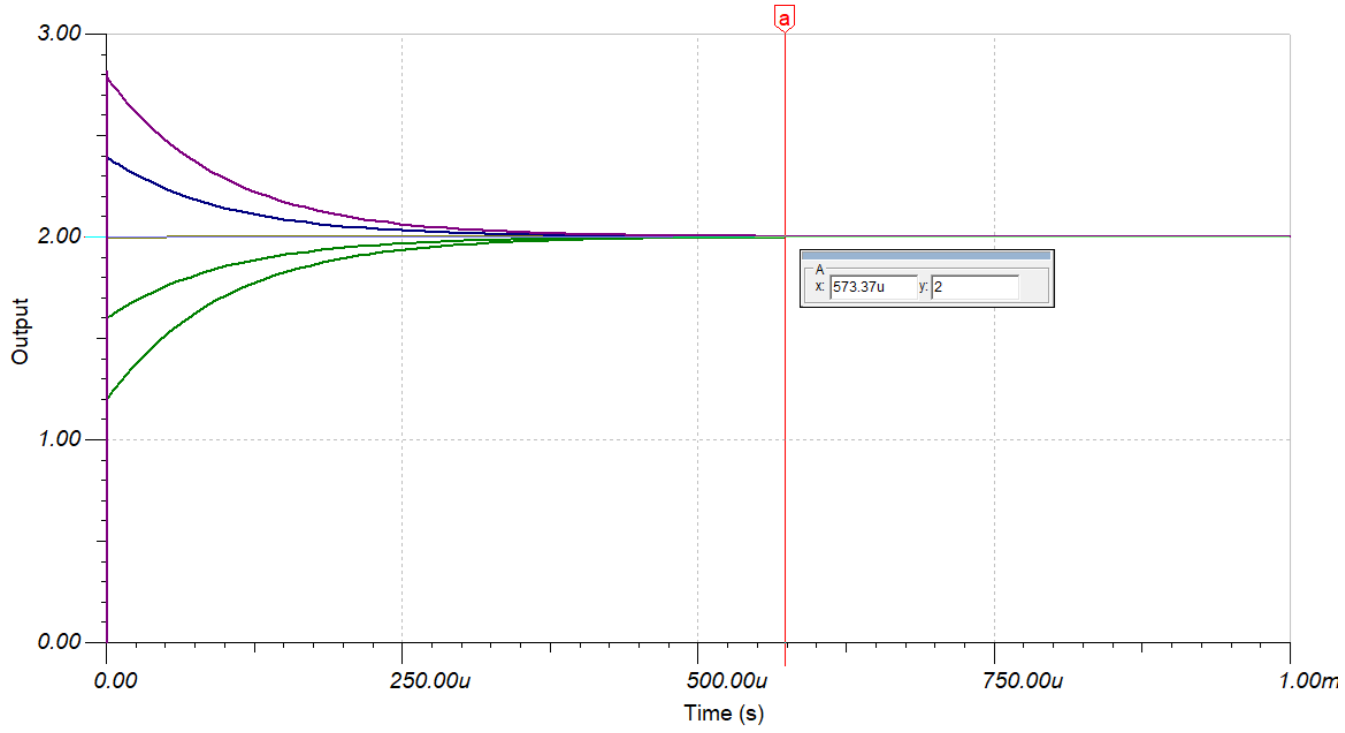

Figure 2-7. Various C1 Simulation

Too small C1 value is much affected by parasitic parameters of components and layout and air. Proportionally increase C1 and C2 value to keep away from these effects. Assume C1=100pF and C2=9.9nF , let's say C1=100pF and C2=9.9nF, both have 5% tolerance which include components tolerance and layout parasitic parameter, vary C1 from 95pF to 105pF, the max settling time is near 5ms shown in Figure 2-8.

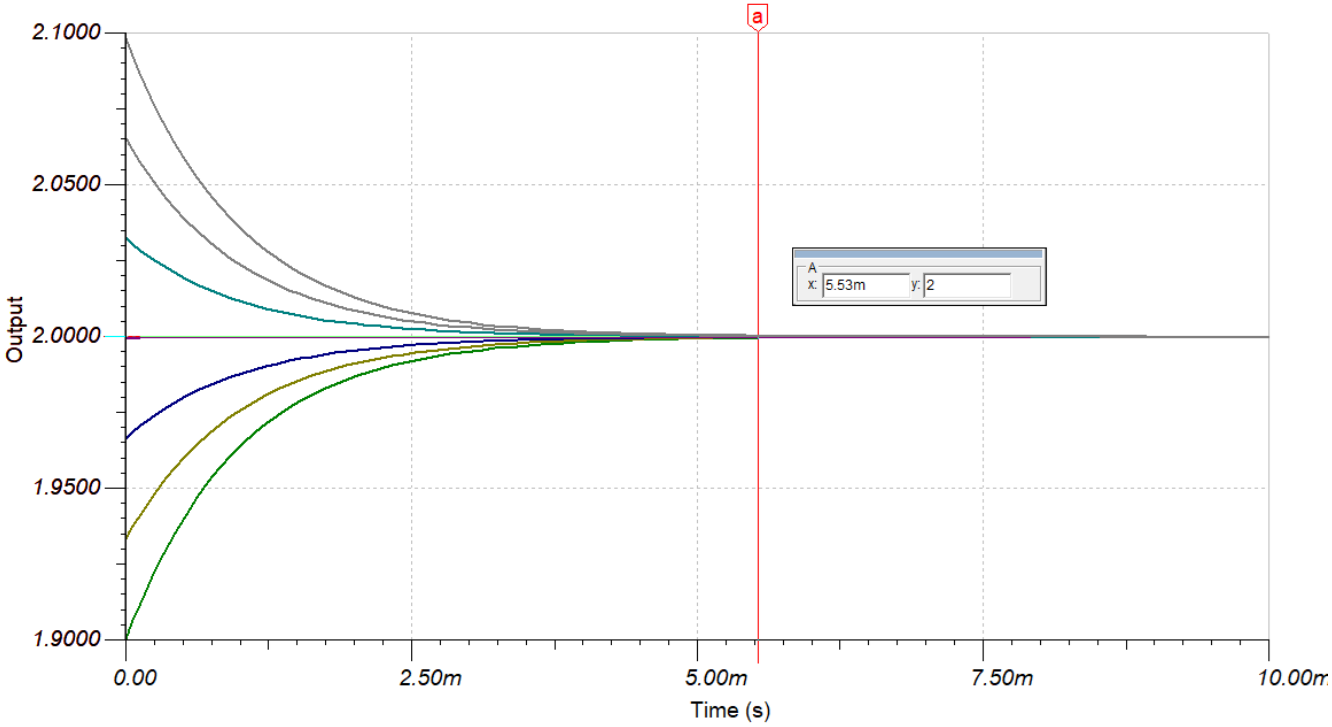

Figure 2-8. Increase C1 C2 and Various C1 Simulation

With these simulations, resistor and capacitor divider sensing approach maybe suitable for precision instruments development, each channel needs fine tuning very carefully. It is not suitable for thousands of channel design for ATE system.

2. Isolated Buffer Sensing Approach

Figure 2-9 is isolated sensing topology, "buffer" becomes an isolated circuit.

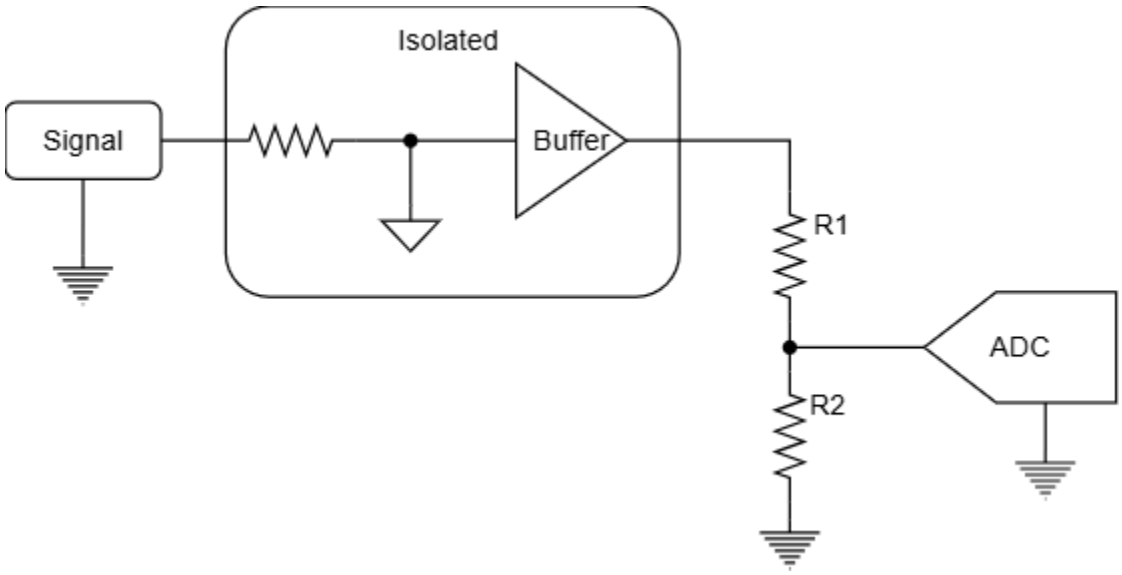

Figure 2-9. Isolated Buffer Sensing Topology

The isolated buffer circuit can accept input signal with very small current leakage and its output have high current driving capability. It will not be affected by capacitors or layout parasitic parameters. Only concern is placement area is a bit big. Following Figure 2-10 is simulation circuit. in this circuit Mosfet can take 490V span such as ±245V or -100V to 390V signal converting.

From simulation result Figure 2-11, Settling time is around 5us from -100 to 390V input to stable signal output.

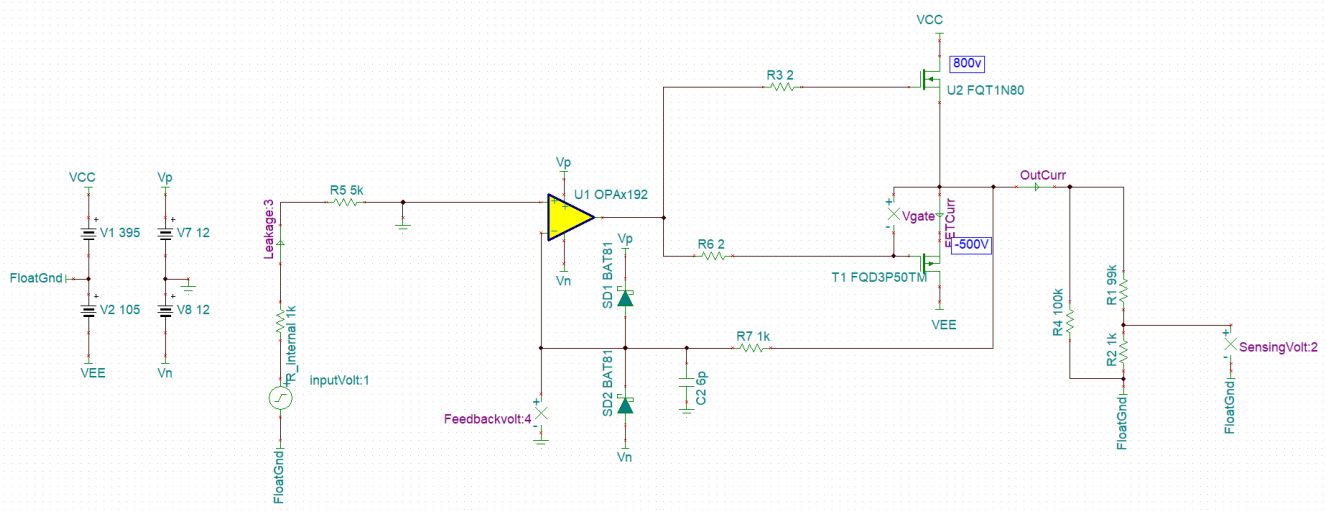

Figure 2-10. Isolated Buffer Simulation Circuit

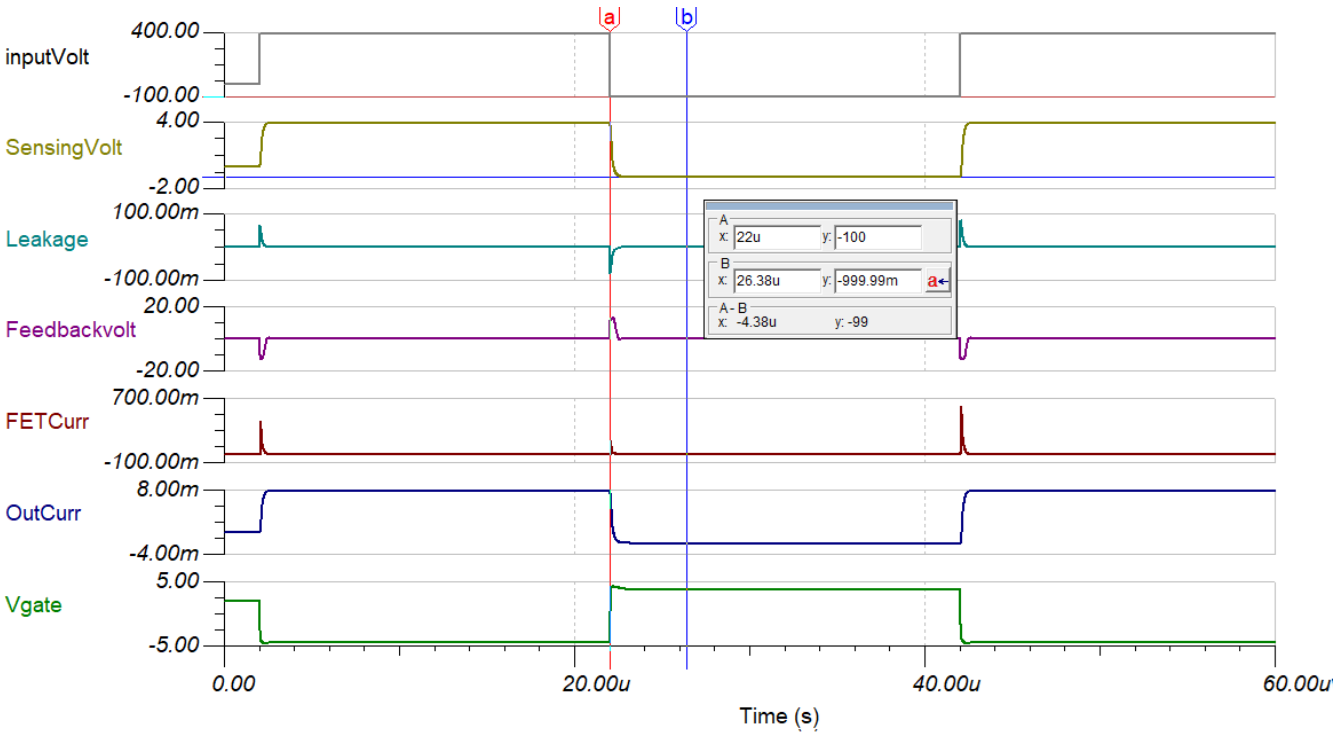

Figure 2-11. Isolated Buffer Settling Time

As Figure 2-12 shown, when start signal 0V, leakage is around 2.5pA, it takes about 10us that current leakage is less than 10pA after input steps up to 390V from 0V. it takes about 12us that current leakage is less than 10pA after input steps down to -100V from 390V

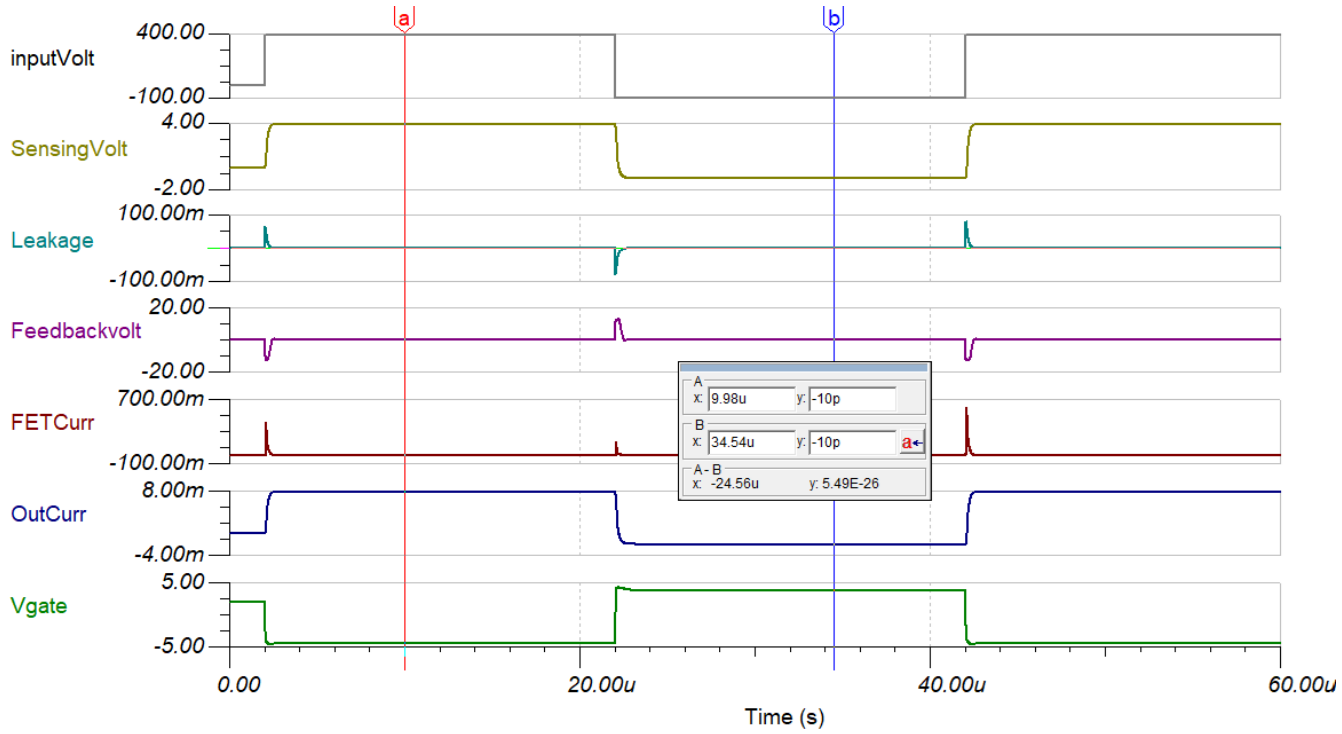

Figure 2-12. Isolated Buffer Current Leakage

3. Floating signal chain approach

It's ok for Isolated buffer sensing approach to take high voltage converting task. But if sensing small current with high common mode voltage, CMRR noise causes a significant reduction for current sensing accuracy. Another issue is it is difficult to find very high voltage P-Mosfet. So, when voltage is over 1000V or 3000V, floating topology is a better choice. Figure 2-13 shows a typical floating signal chain topology.

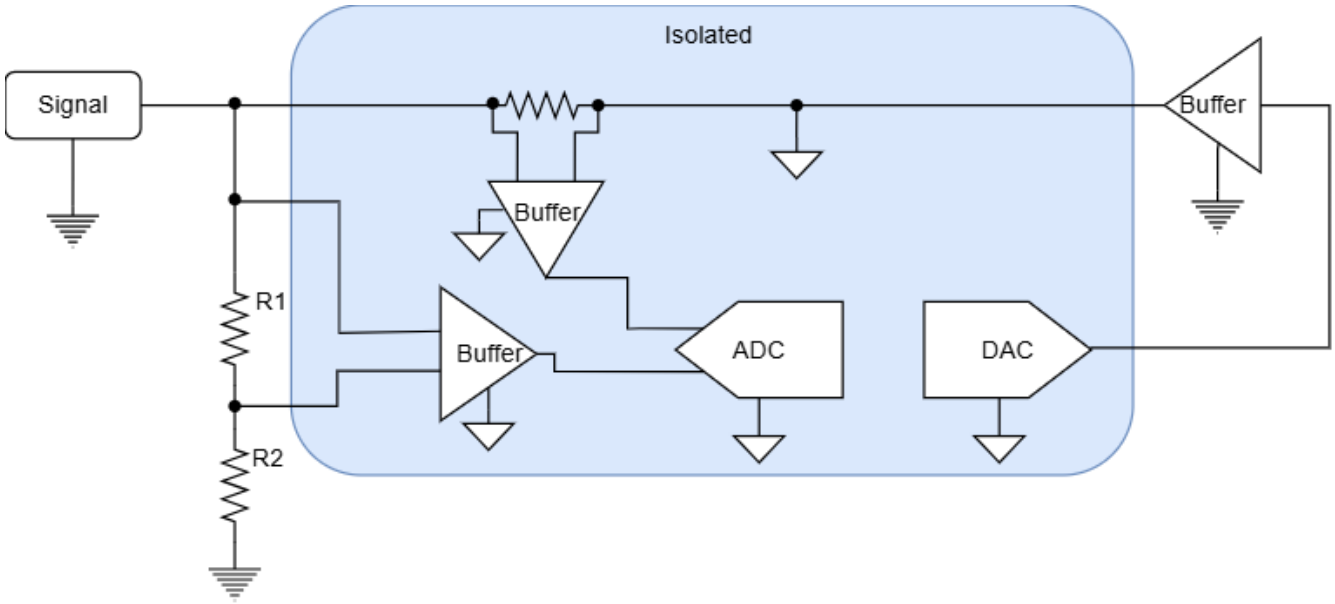

Figure 2-13. Floating Signal Chain

Floating signal chain approach is putting all digital components and signal chain on high voltage side. That will make current sensing common voltage near 0-volt. A low voltage precision amplifier can be used to buffer high output voltage. TIDA-010962 is designed with this topology to implement four quadrant VI sources. With this topology it achieves nearly 20ppm accuracy and fast measurement performance. It also supports Buffer mode

to measure external high voltage such as high voltage digital multimeter. For detail schematic and performance, you can search TIDA-010962 in TI.com

3 Summary

This article discusses several approaches of signal sensing in ATE systems. Based on different use cases, provide TI designs to meet ATE special testing requirements.

4 References

1. Texas Instruments, *Automated Test Equipment (ATE) 80V Discrete Floating VI Reference Design*, design guide.
2. Texas Instruments, *Measurement Cards for Semiconductor Automatic Test Equipment (ATE)*, application brief.
3. Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment*, application brief.
4. Texas Instruments, *Precision labs series: Op amps*, webpage.
5. Texas Instruments, *Precision labs series: Current sense amplifiers*, video series.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025