Application Note

Crystal Oscillator Selection Guide ASM Real-Time Microcontrollers

Joseph Casuga

Abstract

The on-chip Pierce oscillator on Texas Instruments' ASM real-time microcontrollers supports an external quartz crystal as a precision clock source. Selecting the correct crystal and supporting passive components is the single most important factor in oscillator reliability; a mismatched crystal can start up on the bench but fail at voltage or temperature corners. This application note provides a systematic design process covering crystal ESR compliance, load capacitance sizing, damping resistor calculation, negative resistance margin verification, scope probe discipline, and PCB layout best practices. Worked design examples and a quick-check decision tool accompany each step.

Table of Contents

Trademarks

1 Introduction

ASM microcontroller devices such as the C28x and F29x families incorporate a Pierce oscillator that, when paired with an external quartz crystal connected between pins X1 and X2, provides a stable reference clock. The Pierce oscillator is a positive-feedback CMOS inverter forming a resonant tank circuit with the crystal. Unlike a simple RC oscillator, the crystal defines the frequency with high precision; however, the oscillator only functions reliably when the crystal and all external components are properly chosen and laid out.

The most common failure modes seen in field applications and on the TI E2E™ support forums from customers are:

1. Crystal with ESR too high for the oscillator gain, causing failure to start at cold temperature or low voltage
2. Crystal over-driven beyond its maximum rated drive level, causing gradual frequency drift and early failure
3. Excessive PCB stray capacitance reducing negative resistance below the safe margin

This document addresses all three failure modes with concrete calculation procedures referenced to the Crystal Oscillator Specifications section of the C28x and F29x datasheets.

2 Pierce Oscillator and Crystal Model

2.1 Oscillator Block Diagram

The on-chip Pierce oscillator consists of a CMOS inverter amplifier whose output is fed back to the input through the crystal tank circuit. Two external load capacitors (CL1 and CL2) are connected from X1 and X2 to ground. An optional series damping resistor Rd is placed between X2 and the crystal when drive level must be reduced. Figure 2-1 shows the complete circuit topology.

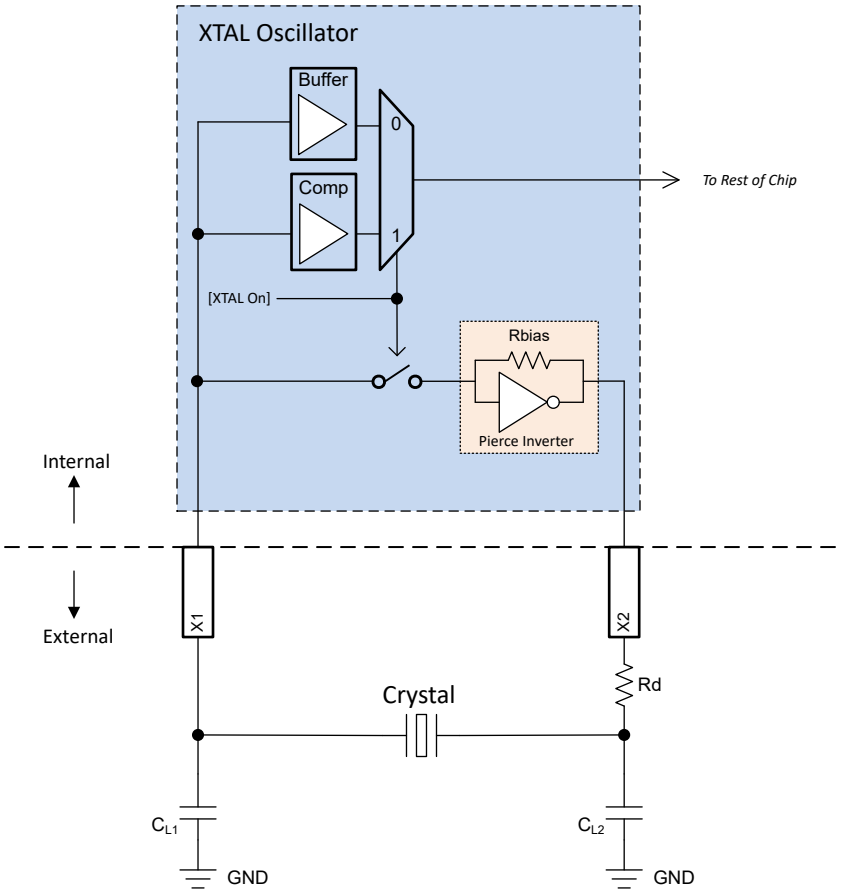


Figure 2-1. Simplified Pierce Oscillator Circuit With External Components

2.2 Quartz Crystal Electrical Model

A quartz crystal is electrically represented by the Butterworth-Van Dyke (BVD) equivalent circuit as shown in Figure 2-2.

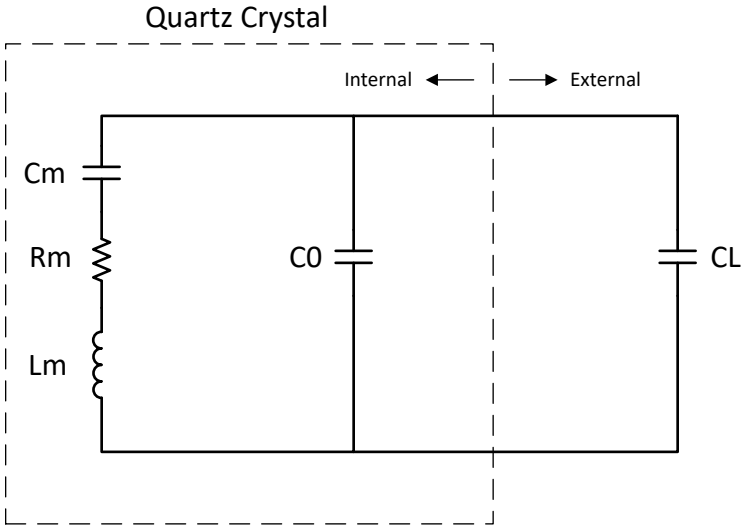


Figure 2-2. Quartz Crystal Electrical Representation

It consists of:

- Lm (motional inductance) - represents the vibrating mechanical mass of the crystal
- Cm (motional capacitance) - represents the mechanical elasticity of the crystal
- Rm (motional resistance) - represents internal resistive losses in the crystal
- C0 (shunt capacitance) - capacitance formed by the crystal electrodes and package parasitics
- CL (load capacitance) - external capacitance seen at the crystal pins; determines frequency

The key derived parameter is equivalent series resistance (ESR), which is the effective resistive load the crystal presents to the oscillator at resonance. ESR is calculated from the crystal component values as:

$$\mathrm{ESR} = \mathrm{Rm} \times (1 + \mathrm{C0} / \mathrm{CL})^2 \quad (1)$$

When CL >> C0, ESR approaches Rm. In practice, C0 is specified in the crystal datasheet (typically 1pF to 7pF), and the design target is to keep it as low as possible. Higher ESR means lower resonator Q, which makes start-up harder and sustained oscillation less stable. ESR increases as CL decreases, so using the minimum required CL is important for keeping ESR low.

3 Crystal Selection Criteria

Table 3-1 defines the maximum allowed ESR as a function of crystal frequency and load capacitor value. This table represents the fundamental gate that every crystal candidate must pass before any other analysis is performed. These tables are available in C28x and F29x datasheets under the *Crystal Oscillator Specifications Section*. The succeeding steps, procedures, and equations in this application note assume that the oscillator requirements table below is available to proceed.

The values in Table 3-1 are derived from the oscillator negative resistance: ESR_max = Rneg_min / 3. The factor of 3 verifies a minimum 3x Rneg-to-ESR margin at worst-case operating conditions (maximum temperature, minimum supply voltage). A 5x margin is preferred in automotive applications. The datasheet notes that C0 must be 7pF or less.

Table 3-1. Crystal ESR Requirements for the Pierce Oscillator Circuit in C28x/ F29x Devices

CRYSTAL FREQUENCY (MHz)	MAXIMUM ESR (Ω) (CL1 = CL2 = 12pF)	MAXIMUM ESR (Ω) (CL1 = CL2 = 24 = pF)
10	55	110
12	50	95
14	50	90
16	45	75
18	45	65
20	45	50

Interpolation for CL1 = CL2 values between table columns. Table 3-1 characterizes ESR_max at two specific external capacitor values. When the required CL1 = CL2 (calculated from Equation 3) falls between 12pF and 24pF, the maximum allowable ESR can be linearly interpolated:

$$\mathrm{ESR\_max(CL1)} = \mathrm{ESR\_max\_12} + (\mathrm{ESR\_max\_24} - \mathrm{ESR\_max\_12}) \times (\mathrm{CL1} - 12) / 12 \quad (2)$$

Inversely, the minimum CL1 = CL2 required to accommodate a crystal with a known ESR is:

$$\mathrm{CL1\_min} = 12 + (\mathrm{ESR\_crystal} - \mathrm{ESR\_max\_12}) \times 12 / (\mathrm{ESR\_max\_24} - \mathrm{ESR\_max\_12}) \quad (3)$$

Three cases apply:

- ESR_crystal ≤ ESR_max_12: Any CL1 in the 12pF to 24pF range is acceptable.
- ESR_max_12 < ESR_crystal ≤ ESR_max_24: Use Equation 3 to find the minimum required CL1.
- ESR_crystal > ESR_max_24: The crystal does not meet oscillator requirements at any CL1 within the device specification. Select a different crystal.

Table 3-1 covers CL1 = CL2 in the 12pF to 24pF range. When the CL_spec is large, the calculated capacitor value CL1 = 2 × (CL_spec − C_stray) can exceed 24pF. Table 3-2 shows where this threshold falls for typical C_stray values:

Table 3-2. Predicted CL_spec That Exceeds CI1 Upper 24pF Bound With Known C_stray

C_stray	CL1 exceeds 24pF when CL_spec >	Typical crystals affected
3pF	15pF	16pF, 18pF, 20pF load crystals
4pF	16pF	18pF, 20pF load crystals
5pF	17pF	18pF, 20pF load crystals

For crystals with CL_spec > 15pF, validate the design using the empirical negative-resistance test in Section 4.5 in addition to the analytical checks.

Note

The ESR values in Table 3-2 are the maximum allowable values computed as Rneg_min / 3 for the specified CL. Crystals with ESR that marginally pass at room temperature can fail at low temperature where crystal ESR increases. A margin of 20% to 30% below the table maximum is recommended for robust designs.

Note

For device datasheets where the crystal frequency range, maximum ESR and CL are not available, see Appendix A at the end of this document. The section provides several methods of deriving the equivalent table for the oscillator.

3.1 Why ESR Governs Crystal Compatibility

The Pierce oscillator sustains oscillation only when the oscillator supplies more energy per cycle than the crystal dissipates; that is, when the negative resistance presented by the oscillator (Rneg) exceeds the crystal ESR. If ESR approaches or exceeds Rneg, the oscillation decays and stops. The 3x margin requirement (Rneg ≥ 3 × ESR) accounts for:

- Process variation in the oscillator gain across device manufacturing lots
- Supply voltage and temperature variation (Rneg decreases at lower VDD and higher temperature)
- Additional Rneg reduction caused by load capacitors CL1 and CL2
- Rneg reduction if a damping resistor Rd is added
- ESR increase in the crystal at temperature extremes

A crystal failing the ESR check (such as one rated at 20.000Mhz at 100Ω versus the 45Ω limit for 20MHz) can appear to work in a lab at room temperature but fail to start up reliably at low temperature (-40℃) or low supply voltage. ESR is the non-negotiable first screen.

3.2 Crystal Frequency

Select the crystal frequency based on the application clock requirements. Supported frequencies for C28x/F29x oscillators are 10MHz to 20MHz. The crystal must operate at its fundamental mode (not overtone). Common choices are 10MHz, 16MHz, and 20MHz. Consult the device datasheet for crystal frequency requirements for other ASM products and refer to Appendix A for the derivation of equivalent ESR and CL requirements for particular crystal frequency range.

3.3 Shunt Capacitance C0

From the ESR formula (Equation 1), it is clear that a higher C0 increases ESR. The device datasheet requires C0 ≤ 7pF. Check the crystal datasheet for the *shunt capacitance* or *parallel capacitance* specification and confirm it is within this limit. If C0 is not explicitly stated, contact the crystal manufacturer.

Note

Do not confuse C0 (crystal shunt capacitance) with CL (load capacitance). C0 and CL are separate parameters with separate specifications. C0 is internal to the crystal; CL is set by the external capacitors on the PCB.

4 Step-by-step Crystal Selection Process

The following procedures can be followed in order. Each step produces a pass or fail result or a calculated value used by subsequent steps. The Crystal Calculation tool GUI interface in Figure 4-1 has been generated according to the steps described in this material to assist with the pass/fail decisions involved in the crystal selection and oscillator design.

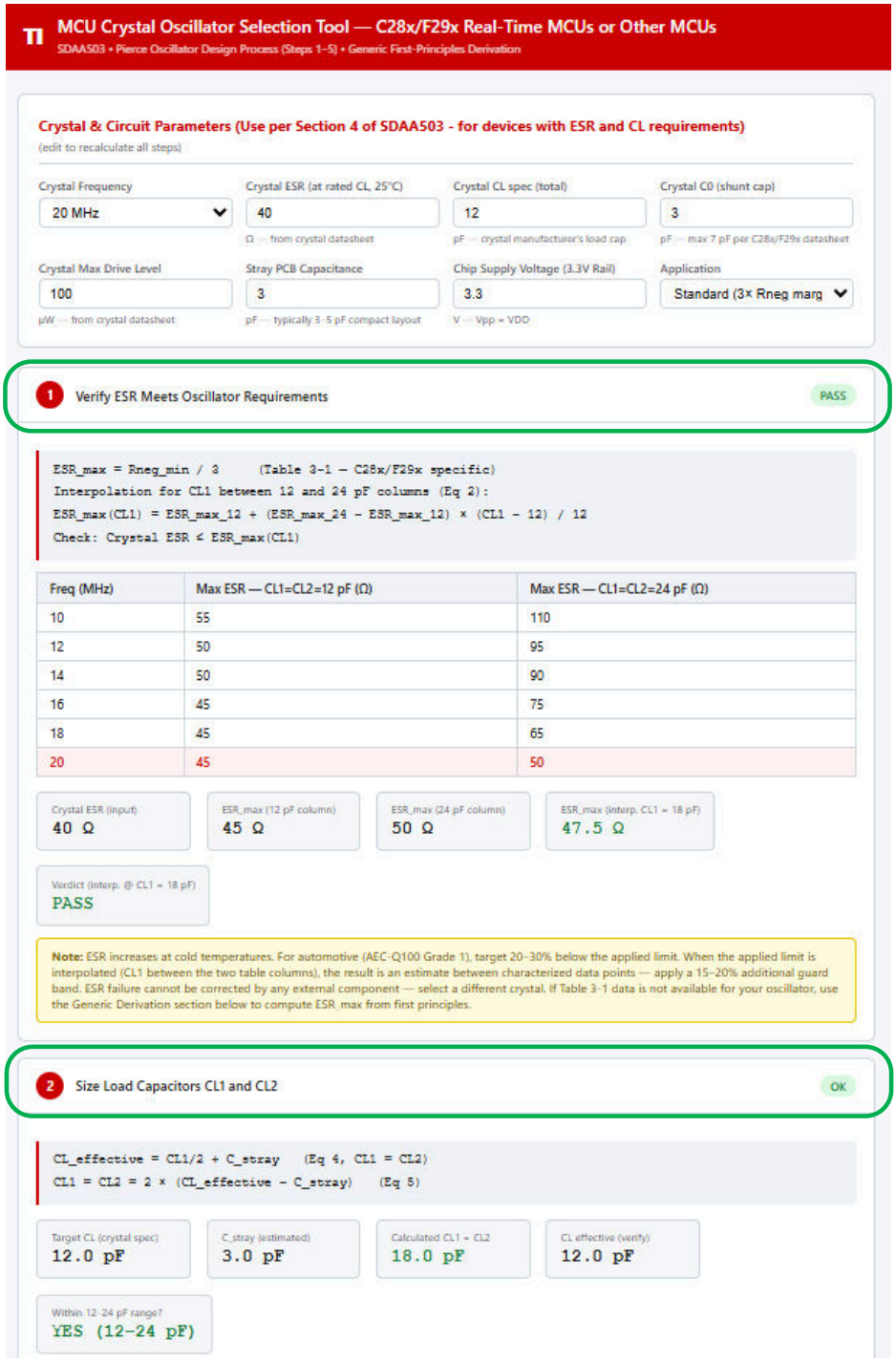


Figure 4-1. GUI Interface for C28x/F29x Crystal Selection

4.1 Step 1 - Verify ESR Meets Oscillator Requirements

Locate the crystal ESR specification in the datasheet of the crystal manufacturer. Crystal datasheets can label this as *ESR*, *max ESR*, or *series resistance*. Look up the maximum allowable ESR from Table 3-1 using the target frequency and intended load capacitor values (CL1 = CL2 = 12pF or 24pF column).

Check: Crystal ESR ≤ Table 3-1 Maximum ESR.

If the crystal ESR exceeds the table value, do not proceed with this crystal. ESR cannot be corrected by any external component. Select a different crystal with lower ESR. For a 20MHz crystal with CL1 = CL2 = 12pF, the maximum ESR is 45Ω.

When CL1 > 24pF: Use the 24pF column of Table 3-1 as a conservative upper bound. This is valid because ESR_{max} increases with CL1 across the table; the 24pF column gives the least restrictive limit that can be read from the characterized data.

Note

ESR is temperature-dependent and typically increases at cold temperatures. Always verify ESR at the lowest operating temperature of the application, not just at 25°C. Request full temperature characterization from the crystal manufacturer if the datasheet only provides a room-temperature ESR value.

4.2 Step 2 - Size Load Capacitors CL1 and CL2

The datasheet from the crystal manufacturer specifies a required load capacitance (CL). This is the capacitance the crystal expects to see at its pins to oscillate at the rated frequency. Setting CL incorrectly causes a frequency offset (frequency pulling).

Clarify with the crystal manufacturer whether their stated CL is:

- The total effective capacitance seen at both pins (most common), or
- The capacitance on one pin only

For the total-capacitance definition (most common), since CL1 and CL2 are in series from the crystal's perspective:

$$\mathrm{CL\_effective} = \mathrm{CL1} \,/\, 2 + \mathrm{C\_stray} \quad (\text{when } \mathrm{CL1} = \mathrm{CL2}) \tag{4}$$

Where C_stray is the estimated PCB stray capacitance (typically 3 to 5pF for a well-designed board). Therefore, to achieve a target CL_effective:

$$\mathrm{CL1} = \mathrm{CL2} = 2 \times (\mathrm{CL\_effective} - \mathrm{C\_stray}) \tag{5}$$

Example: Crystal requires CL = 12pF, C_stray estimated at 3pF:

$$\mathrm{CL1} = \mathrm{CL2} = 2 \times (12 - 3) = 18\mathrm{pF} \tag{6}$$

The device datasheet specifies CL1, CL2 must be between 12pF and 24pF. Select standard capacitor values (18pF or 22pF are common) within this range. Use C0G (NP0) dielectric capacitors for temperature stability; X7R and Y5V dielectrics have significant capacitance change with temperature and must be avoided.

- Higher CL pulls the frequency down slightly (increasing load capacitance slows the crystal)
- Lower CL pulls the frequency up slightly (reducing load capacitance speeds the crystal)
- Effect is small (typically less than 10ppm from nominal) but matters for frequency-critical applications

Note

Stray PCB capacitance is layout-dependent. If the X1 or X2 traces are long or run near ground planes, C_stray canh be higher than 5pF. Measure actual stray capacitance with a capacitance meter or from board-level SPICE simulation for critical applications.

4.3 Step 3 - Determine if Damping Resistor Rd is Required

Rd is a series resistor placed between pin X2 and the crystal (outside the load capacitor), as this has the low impedance path that can source or sink significant current. Placing Rd on X1 high impedance side is not effective in limiting the current drive. The purpose of Rd is to reduce the current delivered to the crystal, thereby reducing its power dissipation. Rd is only needed when the actual crystal drive level exceeds the crystal manufacturer's maximum rated drive level.

First, estimate the crystal drive level from the circuit parameters:

$$\mathrm{DL\_estimated} = \frac{[\mathrm{ESR} \times (\pi \times \mathrm{f} \times \mathrm{C\_total} \times \mathrm{Vpp})]^2}{2} \quad (7)$$

Where:

- ESR = crystal ESR (Ω)
- f = crystal frequency (Hz)
- C_total = CL1 / 2 + C_stray + C0 (F)
- Vpp = peak-to-peak voltage across X1 (approximately VDD = 3.3V)

Decision:

- If DL_estimated ≤ crystal max drive level: Rd is not required (set Rd = 0)
- If DL_estimated > crystal max drive level: Rd IS required; proceed to Step 4

Example calculation for a 20MHz crystal (ESR = 45Ω, Vpp = 3.3V, CL1 = CL2 = 18pF, C_stray = 3pF), C0 = 3pF:

C_total = 18 / 2 + 3 + 3 = 15pF

DL = $[45 \times (\pi \times 20E6 \times 15E\text{-}12 \times 3.3)]^2 / 2$ = approximately 218uW

For a crystal with maximum drive level of 100uW, Rd is required.

When CL1 > 24pF: Use the *actual* calculated CL1 value — do not cap the value at 24pF. C_{total} = CL1 / 2 + C_stray + C0 must reflect the true component value to correctly estimate crystal power.

Note

The drive level formula above is an estimate using a peak voltage approximation. The more accurate method is direct measurement using the procedure in Section 4.4, Method 2 (requires an active differential probe). The estimated value is useful for initial screening before hardware is available.

4.4 Step 4 - Calculate Rd (Damping Resistor)

If Rd is required, the goal is to find the smallest value of Rd that brings the actual drive level at or below the maximum rated drive level of the crystal while still maintaining sufficient Rneg margin for start-up. There is no universal formula that yields an exact Rd value analytically because Rd also reduces Rneg; the correct value must be determined empirically on the actual hardware. The following procedure is recommended:

Method 1: Analytical Estimate (for initial component selection)

To limit crystal power dissipation, solve for Rd that makes power ≤ max DL. The power in the crystal and Rd can be related as follows:

$$P\_XTAL = I\_rms^2 \times ESR \tag{8}$$

$$P\_Rd = I\_rms^2 \times Rd \tag{9}$$

$$I\_rms = V\_rms\_Rd \Big/ Rd = \frac{V\_pk\_Rd / \sqrt{2}}{Rd} \tag{10}$$

The total series impedance of the tank (ESR + Rd) limits the peak current. The ratio of power in the crystal to total dissipated power is ESR / (ESR + Rd). To target crystal power at 70% of the rated maximum DL_max:

$$Rd\_estimate = ESR \times \left(\frac{DL\_estimated}{0.7 \times DL_{max}} - 1\right) \tag{11}$$

This gives an initial Rd starting point. Use the next available standard resistor value (E24 series) and verify empirically.

Method 2: Empirical Measurement (required for final validation). Refer to Figure 4-2 for the required setup.

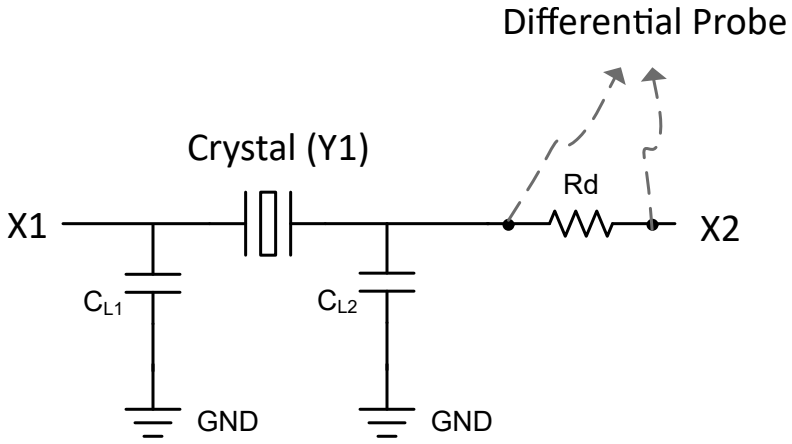


Figure 4-2. Setup for Measuring Crystal Power Dissipation

This method is recommended; always perform this measurement on production hardware:

1. Start with Rd at or near the estimated value from Method 1.
2. Measure V_pk across Rd using a differential active probe with < 1pF input capacitance.
3. Calculate I_rms = (V_pk / $\sqrt{2}$) / Rd
4. Calculate P_XTAL = I_rms^2 × ESR
5. If P_XTAL > DL_max, increase Rd in small steps and repeat.
6. Use the smallest Rd value that achieves P_XTAL ≤ DL_max.
7. After setting Rd, verify Rneg margin (see Section 4.5).

Note

Rd reduces Rneg. Adding too large an Rd can prevent start-up or cause the oscillator to fail at temperature or voltage corners. After determining Rd empirically for drive level, always perform the negative resistance test (Section 6.4) to confirm the Rneg > 3x ESR condition is still met with Rd installed.

Note

Active probes with less than 1pF input capacitance are mandatory for all X1 and X2 measurements. Standard passive 10x oscilloscope probes have 10pF to 15pF of input capacitance that significantly alters the crystal circuit impedance and produces incorrect readings. Do not use passive probes on X1 or X2 for any measurement.

4.5 Step 5 - Verify Negative Resistance (Rneg) Margin

Rneg is the energy the oscillator supplies to overcome crystal losses. Rneg must be sufficiently larger than ESR to verify start-up under all conditions. The required relationship is:

$$\text{Rneg} \geq 3 \times \text{ESR(minimum)} \mid \text{Rneg} \geq 5 \times \text{ESR(recommended for automotive)} \quad (12)$$

Rneg depends on the oscillator circuit gain, C0, CL, and Rd. Figures 6-14 and 6-15 in the F29H85x datasheet show Rneg versus effective CL for 10MHz and 20MHz, with C0 as a parameter.

Key observations:

- Rneg decreases as CL increases - use the minimum CL that meets frequency accuracy
- Rneg decreases as C0 increases - prefer crystals with low C0 (target ≤ 3pF)
- Rneg decreases when Rd is added
- For CL1 = CL2 = 12pF (effective CL approximately 9pF with 3pF stray), Rneg is significantly higher than at CL1 = CL2 = 24pF; however, the available CL range is constrained by the CL requirement of the crystal

From the Rneg versus CL (negative resistance variation) graphs at the target frequency on the C28x/F29x datasheets under Crystal Oscillator Specifications, read off the typical Rneg value at the chosen effective CL and C0. Compute:

$$\text{ESR\_max\_allowed} = \frac{\text{Rneg\_typical}}{3} \quad (13)$$

This must match or exceed the actual ESR of the crystal. For a design using C0 = 3pF and CL_eff = 9pF at 20MHz, the graph shows Rneg approximately 600Ω, giving ESR_max = 200Ω - well above the 45Ω table limit, indicating comfortable margin. For C0 = 7pF and CL_eff = 14pF, Rneg drops to approximately 160Ω, giving ESR_max = 53Ω - much tighter margin, requiring careful crystal selection.

Empirical Rneg test procedure (most reliable - see Section 6.4 for details):

- Insert a potentiometer (Rx) in series with the crystal at the X2 side
- Monitor XCLKOUT for oscillation
- Slowly increase Rx from zero until oscillation stops
- Rneg = Rx_stop + ESR_actual
- Verify Rneg ≥ 3 × ESR

5 PCB Layout Recommendations

The crystal oscillator circuit is one of the most sensitive analog circuits on the PCB. Figure 5-1 shows an example of crystal PCB routing. Layout errors can increase stray capacitance, couple noise into X1/X2, and reduce Rneg below the safe operating margin.

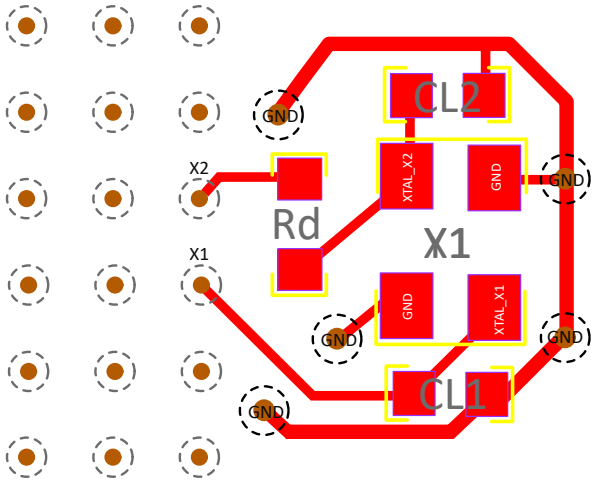


Figure 5-1. External Crystal PCB Routing Example

The following guidelines should be strictly observed.

5.1 Crystal Placement

- Place the crystal as close to the X1 and X2 pins as physically possible. The maximum recommended trace length between X1/X2 and the crystal pads is 200mils (5mm). Every millimeter of additional trace adds approximately 0.3pF to 0.5pF of stray capacitance, increasing the effective CL and reducing Rneg.
- Place the crystal and its load capacitors on the same side of the PCB as the device.
- Do not route crystal traces under or between other high-speed signals, switching regulators, or digital I/O lines. Keep the crystal circuit away from clock sources, switch-mode power converters, and CAN/LIN transceivers.
- Use a keepout zone around the crystal circuit (all layers) to prevent copper pours, vias, and traces from adjacent nets from coupling into X1/X2.

5.2 Load Capacitor Placement

- Place CL1 and CL2 immediately adjacent to the X1 and X2 pins, respectively, with the ground terminal of each capacitor connected directly to the local ground pour. Do not share a single ground via between both capacitors - each must have its own via.
- Keep CL1 and CL2 traces as short and direct as possible. Route them on a single layer without bends or vias between the device pin and the capacitor pad.
- Use C0G/NP0 capacitors for CL1 and CL2.

5.3 Trace Routing

- Route X1 and X2 traces on one layer only (no layer changes). Vias add inductance and capacitance that disturb the tank circuit.
- If Rd is used, place it immediately adjacent to the X2 pin on the board, between the X2 pin pad and the crystal pad, exactly as the schematic shows.
- Keep X1 and X2 traces tightly coupled to a local ground plane. A solid ground pour on the layer beneath the crystal circuit provides shielding from board-level EMI. Make sure the ground pour is uninterrupted and connected to the main ground plane with multiple vias near the perimeter.
- Make sure that no power plane (VDD) is directly under the crystal. VDD switching noise can couple into the high impedance X1/X2 nodes.

5.4 Shielding Considerations

- In high-noise environments (automotive, motor control), consider adding a conductive guard ring connected to ground around the crystal and its load capacitors. Some PCB manufacturers can also provide a ground-fill *moat* that physically isolates the crystal area from the rest of the board.
- In EMI-sensitive applications, a metal crystal can with PCB mounting tabs connected to ground provides additional RF shielding.

Note

Many crystal manufacturers publish PCB layout recommendations specific to their packages (for example, 3225, 2520, 2016 form factors). These guidelines must be followed in addition to the previous device-level guidance.

6 Testing and Validation

6.1 Measurement Equipment Requirements

Note

Standard passive oscilloscope probes (10x, 100x) have input capacitances of 10pF to15pF and must *never* be connected to X1 or X2 for any measurement. Even a 10x passive probe adds enough capacitance to significantly alter the tank impedance, reduce Rneg, and produce incorrect drive level and frequency readings. In severe cases, connecting a passive probe to X1/X2 can stop oscillation entirely.

Required equipment for X1/X2 measurements:

- Active differential probe with < 1pF input capacitance (mandatory for drive level and peak voltage measurements)
- Oscilloscope with bandwidth ≥ 5x the crystal frequency
- XCLKOUT output (GPIO) as the non-invasive frequency and start-up time reference

Where possible, use XCLKOUT (the buffered crystal output available on a configurable GPIO) for all frequency and start-up time measurements, since XCLKOUT loads the oscillator with a controlled GPIO buffer impedance rather than probe capacitance. Refer to the XCLKOUT configuration registers (CLKSRCCTL3.XCLKOUTSEL, XCLKOUTDIVSEL.XCLKOUTDIV) in the device technical reference manual. For devices other than C28x or F29x, consult the device technical reference manual on how to configure the device to output the buffered crystal output for the oscillator measurements in the succeeding sections.

To enable the oscillation with the external crystal, the crystal has to be enabled by calling specific APIs in driverlib or SDK:

- SysCtl_turnOnOsc(SYSCTL_OSCSRC_XTAL) - for C28x devices
- SysCtl_selectXTAL() - for F29x devices

Another option for turning on the crystal oscillator is to write to the XTALCR register, clear the SE bit, and set the OSCOFF bit. For devices other than C28x or F29x, consult the device technical reference manual if the oscillator needs to be configured to enable the external crystal oscillator.

6.2 Frequency Verification

1. Configure XCLKOUT to output the crystal clock (CLKSRCCTL3.XCLKOUTSEL).
2. Connect a frequency counter or oscilloscope to the XCLKOUT GPIO pin (standard passive probe is acceptable here).
3. Measure the output frequency and compare to the crystal nominal frequency.
4. Frequency error > 50ppm indicates CL mismatch. Adjust CL1/CL2 values to correct.

6.3 Start-Up Time Measurement

1. Configure XCLKOUT for crystal clock output.
2. Use XTALCR register to disable the XTAL oscillator.
3. Trigger oscilloscope on the XTAL enable event.
4. Measure elapsed time until XCLKOUT reaches stable 45% to 55% duty cycle.

Note

Start-up time is heavily dependent on the specific crystal used and the tank circuit components. The values above are typical for guidance only. If start-up time is abnormally long, check Rd value, verify ESR is within spec, and check that CL is not significantly higher than the specified value of the crystal.

6.4 Negative Resistance (Rneg) Measurement

The Rneg test is a verification that the oscillator has sufficient gain to start the crystal under all conditions. This test must be performed on all new crystal and PCB combinations. See Figure 6-1

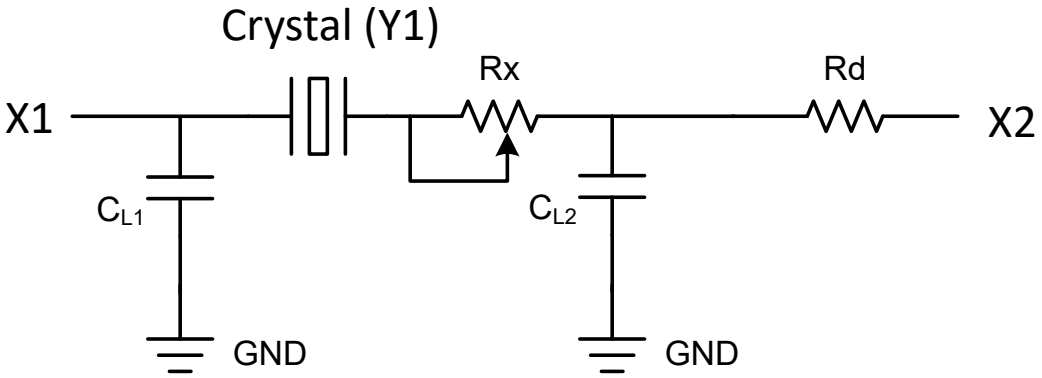


Figure 6-1. Rneg Measurement Setup

1. Configure XCLKOUT for crystal clock output.
2. Place a potentiometer (Rx) in series with the crystal between the load capacitors. A linear potentiometer with a value that is less than 500Ω is recommended. Set Rx to zero initially.
3. Slowly increase Rx from zero while monitoring XCLKOUT frequency.
4. Record the value of Rx at which oscillation stops. This is Rx_stop.
5. Rneg = Rx_stop + ESR_actual
6. Verify: Rneg ≥ 3 × ESR for minimum compliance; ≥ 5 × ESR for automotive applications.
7. If Rneg is marginal, reduce CL1/CL2 values (smaller caps yield higher Rneg), reduce C0 by selecting a different crystal, or reduce Rd.

Note

Perform the Rneg test at room temperature *and* at the lowest operating temperature of your application. Crystal ESR increases at cold temperatures, and oscillator Rneg can decrease at low VDD. Test at both worst-case supply voltage and temperature to confirm margin.

Note

TI strongly recommends having the crystal manufacturer characterize the chosen crystal with the actual PCB and device at the target frequency to obtain measured Rneg, ESR at temperature, and drive level data.

7 Common Issues and Debug Tips

Table 7-1. Common Issues and Debug Tips

Symptom	Probable Cause	Corrective Action
Crystal fails to start	Crystal ESR exceeds the values in Table 3-1	Select crystal with lower ESR
Crystal fails to start	CL too high, reducing Rneg below 3x ESR	Reduce CL1/CL2 to minimum required
Crystal fails to start	External feedback resistance added between X1 and X2	DO NOT ADD external feedback resistor, as it is already added in the C28x/F29x oscillator design
Crystal fails to start at cold temp only	Crystal ESR passes at 25°C but increases at low temperature	Use higher-grade crystal with tighter ESR spec; add margin
Very long start-up time (>10ms)	Rd is too large OR crystal ESR high with no Rd	Reduce Rd; check ESR compliance; reduce CL
Oscillation stops when probe is connected to X1/X2	Passive probe capacitance loads tank below Rneg threshold	Use active probe < 1pF; use XCLKOUT for probing
Frequency is off by > 50ppm	Effective CL does not match crystal specification	Adjust CL1/CL2 to correct effective CL; remeasure stray C
Crystal fails after months in field	Crystal consistently overdriven beyond max DL	Install Rd; verify P_XTAL <= max DL with active probe measurement
Oscillation present at bench but fails in production	PCB stray capacitance varies between boards; ESR margin too low	Increase Rneg margin; tighten PCB layout; re-evaluate crystal

8 Design Example - 20MHz Crystal

This example walks through the complete design process for a 20MHz crystal on a C28x/F29x device in an automotive application (AEC-Q100 Grade 1: -40℃ to 125℃).

Table 8-1. Given Crystal Specification (Ex: Epson)

Manufacturer/Part	Example - Epson FC-135
Frequency	20.000MHz
ESR (max at 25℃)	40Ω
Load Capacitance (CL)	12pF (total, both pins)
C0 (Shunt Capacitance)	3pF (typical)
Drive Level (max)	100uW
Frequency Tolerance	±10ppm at 25℃

Step 1: ESR Check

From Table 3-1, at 20MHz with CL1 = CL2 = 12pF: Maximum ESR = 45Ω.

Crystal ESR = 40Ω ≤ 45Ω. PASS.

Note

For automotive grade, confirm ESR at -40℃. Request temperature characterization from the crystal manufacturer if not already in the datasheet. A 20% to 30% margin is recommended, targeting ESR ≤ 32Ω at -40℃ for robust automotive compliance.

Step 2: Load Capacitor Sizing

Crystal requires CL = 12pF. Estimate C_stray = 3pF (compact layout).

```
CL1 = CL2 = 2 x (12 - 3) = 18pF
```

Select 18pF, C0G (NP0), 0402, 50V capacitors for CL1 and CL2. This is within the 12pF to 24pF device specification range.

Step 3: Drive Level Check

```
C_total = CL1/2 + C_stray + C0= 18/2 + 3 + 3 = 15pF
```

```
DL = (40 x (pi x 20e6 x 15e-12 x 3.3)^2) / 2
```

```
DL = (40 x (3.11e-3)^2) / 2 = approximately 194uW
```

194uW > 100uW crystal max drive level. Rd is *required*.

Step 4: Calculate Rd

```
Rd_estimate = ESR x (DL_estimated / (0.7 x DL_max) - 1)
```

```
Rd_estimate = 40 x (194/(0.7 x 100) - 1) = 40 x (2.771 - 1) = 70.8 Ohm
```

Initial Rd = 75Ω (nearest E24 standard value). Validate on hardware using active probe measurement (Section 4.4). Adjust to smallest Rd that achieves P_XTAL ≤ 100uW.

Step 5: Rneg Verification

From Figure 6-15 of the F29H85x datasheet (Rneg versus 20MHz crystal) at C0 = 3pF, effective CL = 12pF: Rneg approximately 800Ω (typical, no Rd).

```
ESR_max = Rneg / 3 = 800 / 3 = 267 Ohm  >>  crystal ESR of 40Ohm
```

Even with Rd = 33Ω added, the Rneg reduction is modest and the 3x margin is comfortably met. Perform the empirical Rneg potentiometer test at -40°C to confirm.

Final Bill of Materials - Crystal Circuit

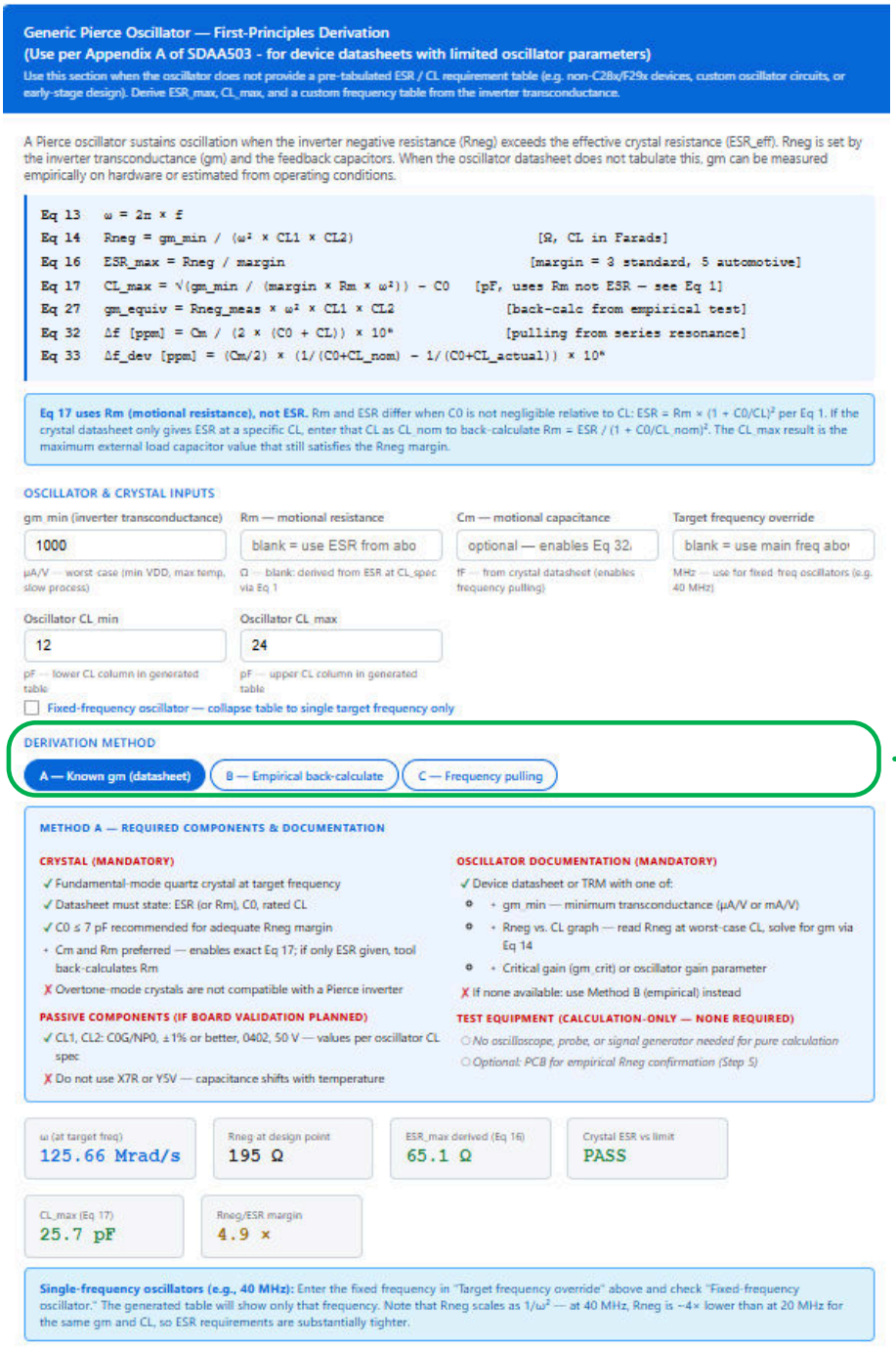
Table 8-2. BOM

Reference	Component	Value/Part	Notes
XTAL1	Quartz Crystal	20MHz, ESR ≤ 40Ω, CLb=b12pF	AEC-Q200, verify ESR at -40°C
CL1	Load Capacitor	18pF, C0G/NP0, 0402	X1 side
CL2	Load Capacitor	18pF, C0G/NP0, 0402	X2 side
Rd	Damping Resistor	75Ω, 0402	Series with X2 - adjust empirically
--	Active Probe (for test only)	< 1pF input capacitance	Required for DL measurement

9 Appendix A

9.1 Crystal Selection for Generic Pierce Oscillators

This appendix section is a supplemental material for characterizing Pierce Oscillators where pre-tabulated ESR/CL data is not available. The Crystal Calculation tool GUI interface in Figure 9-1 has been generated according to the steps described in this material to assist with the pass/fail decisions involved in the crystal selection and oscillator design.



Follows step-by-step procedures from three alternate methods of crystal selection with limited oscillator parameters.

Figure 9-1. GUI Interface for Choosing Crystals with Generic Oscillators

9.1.1 Introduction and Scope

Section 3 assumes that a pre-characterized ESR/CL requirement table (Table 3-1) is available for the target oscillator. That table encodes the measured minimum negative resistance (Rneg_min) of the specific C28x/F29x Pierce oscillator cell across process, voltage, and temperature corners.

This appendix addresses situations where no equivalent table exists:

- Microcontroller oscillator cells for which oscillator parameters are not available or with limited datasheet specifications
- Oscillator designs supporting a single fixed frequency (for example, 25MHz, 40MHz, 48MHz) rather than a range

Three methods are presented in order of increasing measurement complexity. All methods ultimately produce equivalent outputs to Table 3-1: a maximum allowable crystal ESR and a maximum load capacitance CL_max at the target frequency and required safety margin. The companion interactive calculator (`crystal_selector.html`) implements all equations in this appendix.

Note

The equations in this appendix apply to any CMOS inverter-based Pierce oscillator, not only ASM microcontroller devices. All equations use only fundamental circuit parameters and do not assume a specific device family.

9.1.2 Theoretical Background

A Pierce oscillator built around a CMOS inverter sustains oscillation when the negative resistance presented at the crystal terminals (Rneg) exceeds the effective series resistance (ESR) presented by the crystal. The Rneg of the oscillator is governed by the small-signal transconductance of the inverter (gm) and the external load capacitors:

$$\omega = 2\pi \times f \tag{14}$$

$$\text{Rneg} = \text{gm\_min} / \left(\omega^2 \times \text{CL1} \times \text{CL2}\right) \tag{15}$$

where gm_min is the *minimum* transconductance at worst-case process, minimum supply voltage, and maximum operating temperature. CL1 and CL2 are the external load capacitors in Farads.

The crystal presents an effective resistance ESR_eff that increases with the ratio C0/CL (from Equation 1):

$$\text{ESR\_eff} = \text{Rm} \times (1 + \text{C0}/\text{CL})^2 \tag{16}$$

The oscillation sustaining condition is $\text{Rneg} \geq \text{MS} \times \text{ESR\_eff}$, where MS is the safety margin factor (3 for standard, 5 for automotive AEC-Q100). Substituting and solving for the maximum CL that satisfies this condition:

$$\text{ESR\_max} = \text{Rneg} \ / \ \text{MS} \tag{17}$$

$$\text{CL\_max} = \sqrt{\left(\text{gm\_min} \ / \left(\text{MS} \times \text{Rm} \times \omega^2\right)\right)} - \text{C0} \tag{18}$$

Table 3-1 is the pre-computed result of Equation 17 applied to the C28x/F29x oscillator over the 10MHz to 20MHz frequency range, derived from the oscillator characterization data in the device datasheet. For any other oscillator, the same equations apply once gm_min (or equivalently, a measured Rneg) is known.

Note

Equation 18 uses the *motional resistance Rm*, not ESR. If the crystal datasheet specifies ESR at a rated load capacitance CL_nom (the most common format), derive Rm as: $\text{Rm} = \text{ESR} / (1 + \text{C0}/\text{CL\_nom})^2$. Using ESR directly in Equation 18 overestimates CL_max because ESR increases as CL decreases.

9.1.3 Method A - Analytical Derivation from gm_min

This method is a pure calculation. This method requires no hardware test and no laboratory equipment. The inputs are the minimum transconductance of the oscillator from the device datasheet and the crystal's BVD parameters from the datasheet of the crystal manufacturer.

9.1.3.1 Equipment and Component Requirements

Crystal (Mandatory)

- Fundamental-mode quartz crystal at target frequency
- Datasheet must specify: ESR (or Rm), C0, and rated CL
- C0 ≤ 7pF recommended for adequate Rneg margin
- Motional capacitance Cm and Rm preferred (enables Equation 18 without approximation)
- Overtone-mode crystals are not compatible with a Pierce inverter oscillator

Oscillator Documentation (Mandatory)

- Device datasheet or TRM with one of the following:
  - gm_min — minimum transconductance (A/V or µA/V)
  - Rneg versus CL characteristic curve (read Rneg, solve for gm using Equation 15)
  - Critical gain or oscillator gain parameter
- If none of the above are available, use Method B instead

Passive Components (if prototype validation is planned)

- CL1, CL2 load capacitors: C0G/NP0 dielectric, ±1% tolerance or better
- Values covering the oscillator's supported CL range (for example, 12pF, 15pF, 18pF, 22pF, 24pF)
- Package: 0402 or 0603 for minimal parasitic inductance
- Rating: 50V minimum
- Use of X7R or Y5V capacitors not recommended — significant capacitance variation with temperature

- Engineering sample or production PCB (for Step 5 Rneg confirmation)
- No signal generator, probe, or oscilloscope needed for pure calculation

Test Hardware (Optional — for confirmation only)

- Engineering sample or production PCB (for Step 5 Rneg confirmation)
- No signal generator, probe, or oscilloscope needed for pure calculation

9.1.3.2 Procedure

1. From the oscillator datasheet, obtain gm_min at minimum VDD and maximum operating temperature. If the datasheet provides a Rneg vs. CL curve instead, read Rneg at the worst-case (maximum) CL and solve: gm_min = Rneg × ω² × CL1 × CL2.
2. Determine the crystal's C0 (shunt capacitance) and confirm C0 ≤ 7pF. Locate this in the crystal datasheet as *shunt capacitance* or *parallel capacitance*.
3. Obtain Rm. If the datasheet gives Rm directly, use it. If only ESR at rated CL_nom is given: Rm = ESR / (1 + C0/CL_nom)^2.
4. Select the target frequency f and compute ω = 2π × f (Equation 14).
5. Choose initial load capacitor values CL1 = CL2 (start at the crystal's rated CL or the oscillator's minimum allowed CL). Verify CL1 and CL2 are within the specified range of the oscillator.
6. Compute Rneg = gm_min / (ω² × CL1 × CL2) (Equation 15), where CL is in Farads.
7. Compute ESR_max = Rneg / MS (Equation 17), where MS = 3 (standard) or 5 (automotive).
8. Verify crystal ESR ≤ ESR_max. If not, select a crystal with lower ESR or reduce CL1/CL2.
9. Compute CL_max = √(gm_min / (MS × Rm × ω²)) − C0 (Equation 18) to confirm the chosen CL1/CL2 is below CL_max. If CL1/CL2 > CL_max, reduce the load capacitor values.
10. Optionally, perform the empirical Rneg test from Section 6.4 on hardware to confirm the analytical result.

9.1.3.3 Single-Frequency Oscillator Considerations

Oscillator circuits designed for a single fixed frequency (for example, 25MHz for CAN FD timing, 40MHz for high-speed USB, or 48MHz for USB Full Speed reference) require special attention:

- No frequency sweep is relevant. All calculations target the one supported frequency. There is no equivalent of the 10MHz to 20MHz range table in this application note.
- Higher frequencies yield lower Rneg for the same gm and CL. Because Rneg scales as $1/\omega^2$, a 40MHz oscillator presents roughly one-quarter the Rneg of a 20MHz oscillator with identical gm and load caps. ESR requirements are correspondingly tighter.
- The oscillator's supported CL range can differ from the 12pF to 24pF range of C28x/F29x devices. Always use the CL specification from the datasheet of the oscillator, not a default range.
- Crystal selection is more restrictive at higher frequencies. Crystals above 30MHz with ESR ≤ 20Ω can be difficult to source. Verify part availability before design commitment.

9.1.3.4 Worked Example — 40MHz Fixed-Frequency Oscillator

Given Parameters

Table 9-1. 40MHz Oscillator Design Parameters

Parameter	Value	Source
Target frequency (f)	40.000MHz	Application requirement
gm_min	1.5mA/V	Oscillator datasheet, worst-case corner
Crystal ESR (max at 25°C)	20Ω	Crystal datasheet
Crystal CL spec (rated)	15pF	Crystal datasheet
Crystal C0	3pF	Crystal datasheet
Crystal max drive level	50µW	Crystal datasheet
Stray PCB capacitance	2pF	Layout estimate (compact PCB)
Safety margin (MS)	3	Standard; use 5 for automotive
VDD	3.3V	System supply

Step 1: Derive Rm from ESR at rated CL

$$\mathrm{Rm} = 20\ /(1+3\ /\ 15)^2 = 20\ /\left(1.2\right)^2 = 20\ /\ 1.44 = 13.9\Omega \tag{19}$$

Step 2: Compute ω

$$\omega = 2\pi \times 40 \times 10^6 = 2.513 \times 10^8 \mathrm{rad/s} \tag{20}$$

Step 3: Size load capacitors (Equation 3)

$$\mathrm{CL1} = \mathrm{CL2} = 2 \times (15 - 2) = 26\mathrm{pF} \rightarrow \text{round down to nearest standard: } 22\ \mathrm{pF} \tag{21}$$

Check with 22pF: CL_eff = 22 / 2 + 2 = 13pF (slightly below rated 15pF — acceptable; shifts frequency up by a few ppm per Equation 33)

Step 4: Compute Rneg at CL1 = CL2 = 22pF

$$\mathrm{Rneg} = 1.5\times10^{-3}/((2.513\times10^8)^2\times(22\times10^{-12})^2) = 1.5\times10^{-3}/(6.316\times10^{16}\times4.84\times10^{-22}) = 1.5\times10^{-3}/3.057\times10^{-5} \cong 49.1\Omega \tag{22}$$

Step 5: ESR_max and crystal ESR check

$$\mathrm{ESR\_max} = 49.1\ /\ 3 = 16.4\Omega\ \text{Crystal ESR} = 20\Omega > 16.4\Omega \rightarrow \text{FAIL at 22pF} \tag{23}$$

Step 6: Reduce CL — compute CL_max

$$\mathrm{CL\_max} = \sqrt{\left(1.5\times10^{-3}/\left(3\times13.9\times\left(2.513\times10^8\right)^2\right)\right)} - 3\times10^{-12} = \sqrt{\left(1.5\times10^{-3}/2.636\times10^{18}\right)} - 3\times10^{-12} = \sqrt{\left(5.69\times10^{-22}\right)} - 3\times10^{-12} = 2.386\times10^{-11} - 3\times10^{-12} = 20.9\mathrm{pF} \tag{24}$$

Step 7: Re-verify Rneg at CL1 = CL2 = 18pF

$$\text{Rneg} = 1.5 \times 10^{-3} / (6.316 \times 10^{16} \times (18 \times 10^{-12})^2) = 1.5 \times 10^{-3} / (6.316 \times 10^{16} \times 3.24 \times 10^{-22}) = 1.5 \times 10^{-3} / 2.046 \times 10^{-5} \cong 73.3\Omega \text{ESR}_{\text{max}} = 73.3 / 3 = 24.4\Omega \quad (25)$$

$$\text{Crystal ESR} = 20\Omega \leq 24.4\Omega \rightarrow \text{PASS (margin} = 73.3 / 20 = 3.7\times) \quad (26)$$

Table 9-2. Derived ESR and CL Limits at 40MHz -- Equivalent of Table 3-1

CL1 = CL2	CL_eff (pF)	Rneg (Ω)	ESR_max at MS = 3 (Ω)	ESR_max at MS = 5 (Ω)	Crystal ESR = 20Ω
24pF	14.0	41.2	13.7	8.2	FAIL (both)
22pF	13.0	49.1	16.4	9.8	FAIL (both)
18pF ✓	11.0	73.3	24.4	14.7	PASS at MS = 3; FAIL at MS = 5
15pF	9.5	105.6	35.2	21.1	PASS (both)
12pF	8.0	165.0	55.0	33.0	PASS (both)

Note

At 40MHz, crystals with ESR ≤ 20Ω are required even at 18pF load caps with a 3× safety margin. For automotive (5× margin), CL1 = CL2 = 12pF and crystal ESR ≤ 33Ω is needed. This illustrates why higher-frequency fixed-frequency oscillators require crystals with significantly lower ESR than the 45Ω limit at 20MHz in Table 3-1.

9.1.4 Method B - Empirical Derivation using Negative Resistance Test

When gm_min is not published, the oscillator's effective Rneg can be measured directly on hardware using a series potentiometer at the X2 pin. From the measured Rneg, an equivalent transconductance gm_equiv is back-calculated and used to derive ESR_max and CL_max at any frequency and CL combination.

9.1.4.1 Equipment and Component Requirements

Crystal and PCB (Mandatory)

- Candidate crystal soldered to X1/X2 on the engineering or production PCB
- Production CL1, CL2 values installed — C0G/NP0 dielectric, known tolerance
- Rd = 0Ω (DNP or shorted) for this measurement; remove before Rneg test
- XCLKOUT pin accessible at an exposed test point or jumper header
- Do not substitute X7R/Y5V capacitors for CL1/CL2 during this test — capacitance error shifts results

Series Potentiometer Rx (Mandatory)

- Value: 200Ω to 500Ω, linear taper (not audio/log taper)
- Type: cermet or wirewound trimmer — low parasitic capacitance (< 1pF preferred)
- Do NOT use carbon composition pots above 10MHz — parasitic capacitance is typically 2pF to 5pF
- Recommended: Bourns 3296W-1-201LF (200Ω) or 3296W-1-501LF (500Ω)
- Lead length from X2 pad to Rx: ≤ 5mm; minimize stray inductance
- Position: between the X2 device pin and the crystal pad, outside CL2

Test Equipment (Mandatory)

- Oscilloscope: bandwidth ≥ 5 × oscillator frequency (for example, ≥ 200MHz for 40MHz crystal)
- Active differential probe: input capacitance < 1pF, bandwidth ≥ 5 × f_osc
  - Tektronix P6247 / P6248 (1GHz, 0.9pF)
  - Keysight N2795A (1GHz, < 0.5pF)
- Do NOT use standard 10× passive probes on X1 or X2 — 10pF to 15pF input capacitance alter tank impedance and stop oscillation
- Frequency counter (or XCLKOUT on oscilloscope): monitor oscillation state non-invasively
- Precision multimeter with 4-wire (Kelvin) measurement: measure Rx_stop value accurately
- Regulated DC power supply: low noise (<10mV ripple), set to minimum specified VDD

Temperature Chamber (Automotive)

- Range: −40°C to +125°C, accuracy ±2°C

- Cable feed-throughs for probing while at temperature
- Repeat Rneg measurement at min VDD AND min temperature for worst-case gm_min

9.1.4.2 Signal Generator as Crystal Substitute

A frequency generator can substitute for the crystal when a qualified crystal is not yet available for initial gm screening. This is a non-standard approach with significant limitations.

Table 9-3. Signal Generator Substitute Requirements

Requirement	Specification	Notes
Frequency	Equal to target oscillator frequency ±10ppm	Stability not critical; just needs to be at resonant frequency
Output impedance	50Ω	Use a series 50Ω resistor to X1 if generator impedance is higher
Output level	100mV to 500mV peak-to-peak into the load	Low enough to avoid inverter saturation
Waveform	Sinusoidal preferred	Square wave harmonics can excite the inverter at non-target frequencies
Connection	Connect to X1 through 50Ω series resistor; monitor X2 output	Increase Rx at X2 until output drops; record Rx_stop

Note

The CMOS inverter oscillator relies on the reactive impedance of the crystal (motional inductance/capacitance) to establish the correct phase shift for oscillation. A signal generator provides only a resistive driving source and does not replicate the LC tank behavior of the crystal. The gm_equiv derived from a generator-based test can differ from the actual crystal-driven value by up to 30%. Use generator-based measurements only for initial screening. Always validate with the actual crystal before design freeze.

9.1.4.3 Equations

After measuring Rx_stop (the potentiometer value at which oscillation stops), the measured Rneg is:

$$\text{Rneg\_measured} = \text{Rx\_stop} + \text{ESR\_actual} \tag{27}$$

Back-calculate gm_equiv from the measured Rneg at the known test CL:

$$\text{gm\_equiv} = \text{Rneg\_measured} \times \omega^2 \times \text{CL1} \times \text{CL2} \tag{28}$$

Then apply Equation 15 through Equation 18 using gm_equiv in place of gm_min to predict Rneg at any other CL or frequency combination, and to generate the custom ESR/CL requirement table (Section 9.1.4.6).

9.1.4.4 Procedure

1. Assemble the PCB with the target crystal, production CL1 = CL2 capacitors, and Rd = 0Ω. Verify XCLKOUT is routed to a test point.
2. Install Rx (200Ω to 500Ω cermet trimmer) in series with the X2 pin, between the X2 pad and the crystal/CL2 node. Set Rx to 0Ω initially.
3. Apply minimum VDD. Confirm oscillation by monitoring XCLKOUT frequency.
4. Slowly increase Rx from zero (use a small screwdriver or calibrated adjustment). Monitor XCLKOUT for frequency and amplitude stability.
5. Record Rx_stop: the Rx value at which XCLKOUT stops toggling or drops below reliable triggering. Approach Rx_stop slowly — overshoot resets the test.
6. Measure Rx_stop accurately using a 4-wire (Kelvin) DMM connection directly across the potentiometer terminals while it is in-circuit.
7. Compute: Rneg_measured = Rx_stop + ESR_crystal
8. Compute: gm_equiv = Rneg_measured × ω^2 × CL1_F × CL2_F (Equation 28), where CL values are in Farads.
9. For automotive applications, repeat at −40°C (or lowest operating temperature) and minimum VDD. Use the lowest gm_equiv across all test conditions as the conservative gm_min.

10. Apply gm_equiv to Equation 15 through Equation 18 and generate the custom requirement table (Table 9-4).

9.1.4.5 Alternative Experimental Methods for Deriving gm

When the series potentiometer Rx approach (Section 9.1.4.4) is not accessible — for example, if the PCB has no room to insert Rx, or if only a crystal kit and a power supply are available — the following three methods can characterize the effective transconductance of the oscillator. All produce gm at a specific operating corner; use the lowest value across all corners as gm_min.

9.1.4.5.1 Load Capacitance (CL) Sweep

This is the simplest method requiring no modifications to the PCB beyond swapping load capacitors. The margin can be read directly as a ratio without computing gm explicitly.

Equipment required: Precision C0G/NP0 capacitor kit (8pF to 47pF, ±0.5%), XCLKOUT frequency counter.

1. Install production CL1 = CL2 = CL_design. Confirm oscillation through XCLKOUT.
2. Replace CL1 and CL2 simultaneously with progressively larger values (same value both sides). Use the capacitor kit in 2pF to 3pF steps.
3. After each step, wait ≥ 30s and verify oscillation. Record the largest CL value at which oscillation still occurs: this is CL_crit.
4. Compute gm from the critical condition (Rneg = ESR at CL_crit, margin = 1):

$$\mathrm{gm} = \mathrm{ESR} \times \omega^2 \times \mathrm{CL\_crit}^2 \tag{29}$$

The safety margin at the production CL without computing gm is given directly by:

$$\mathrm{Margin} = (\mathrm{CL\_crit} / \mathrm{CL\_design})^2 \tag{30}$$

If $\mathrm{CL\_crit} \geq \sqrt{3} \times \mathrm{CL\_design} \approx 1.73 \times \mathrm{CL\_design}$, the 3× Rneg margin is satisfied. For 5× automotive margin: $\mathrm{CL\_crit} \geq \sqrt{5} \times \mathrm{CL\_design} \approx 2.24 \times \mathrm{CL\_design}$.

Example: CL_design = 18pF, CL_crit = 36pF. Margin = $(36 / 18)^2 = 4\times$. Passes 3× standard; marginal for 5× automotive. gm = $40\Omega \times (2\pi \times 20 \times 10^6)^2 \times (36 \times 10^{-12})^2 = 40 \times 1.58 \times 10^{16} \times 1.30 \times 10^{-21} = 8.2\text{mA/V}$.

Note

CL_crit found at room temperature and nominal VDD is not gm_min. Repeat the sweep at maximum operating temperature and minimum VDD to find the worst-case CL_crit and the true gm_min.

9.1.4.5.2 Supply Voltage (VDD) Sweep

CMOS inverter gm decreases as VDD is reduced and as temperature increases. The VDD sweep identifies the supply voltage at which the oscillator just fails, giving gm at that corner.

Equipment required: Adjustable low-noise DC supply, XCLKOUT frequency counter, optional temperature chamber.

1. Set temperature to maximum operating temperature (T_max) if a chamber is available. Otherwise test at room temperature — results will be optimistic.
2. With production CL1 = CL2 installed, set VDD to nominal. Confirm oscillation.
3. Reduce VDD slowly (1mV/s to 5mV/s). Monitor XCLKOUT for loss of oscillation.
4. Record VDD_crit: the supply voltage at which oscillation stops.
5. At VDD_crit the margin = 1, so:

$$\mathrm{gm}(\mathrm{VDD\_crit},\ \mathrm{T}) = \mathrm{ESR} \times \omega^2 \times \mathrm{CL\_design}^2 \tag{31}$$

Because VDD_min > VDD_crit by design, the oscillator has margin. A first-order estimate of the margin at VDD_min uses the linear gm–VDD relationship (valid for short-channel CMOS in saturation):

$$\mathrm{Margin\_est} \cong \mathrm{gm}(\mathrm{VDD\_min}) \,/\, \mathrm{gm}(\mathrm{VDD\_crit}) \cong \mathrm{VDD\_min} \,/\, \mathrm{VDD\_crit} \tag{32}$$

Note

Equation 32 is a conservative first-order approximation. Actual gm–VDD scaling depends on the process node and operating region (saturation versus subthreshold). For a definitive gm_min, combine this measurement with the Rx sweep (Section 6.4) at VDD_min and T_max simultaneously.

9.1.4.5.3 Temperature Sweep (Thermal Margin Identification)

Crystal ESR increases and oscillator gm decreases at elevated temperature. A temperature ramp identifies the worst-case thermal corner without requiring any circuit modifications.

Equipment required: Temperature chamber (−40°C to T_max + 20°C), XCLKOUT frequency counter, DC supply at VDD_min.

1. Set VDD = VDD_min (worst-case supply).
2. With production CL1, CL2, and Rd installed, ramp temperature upward at ≤ 2°C/min while monitoring XCLKOUT.
3. Record T_crit_high: temperature at which oscillation stops.
4. Ramp back to room temperature, then ramp downward. Record T_crit_low: temperature at which oscillation stops at cold extreme.
5. If T_crit_high > T_max and T_crit_low < T_min, the oscillator has thermal margin over the entire operating range.
6. At T_crit (either extreme), perform the CL sweep (Equation 29) or Rx sweep (Equation 28) to quantify gm_min at that corner.

Note

Crystal ESR increases by 5% to 30% from 25°C to −40°C depending on crystal grade. Request ESR versus temperature characterization from the crystal manufacturer for automotive designs. The cold-corner (T_crit_low) is often the more critical failure mode because ESR rises while gm also decreases at low VDD.

9.1.4.6 Generating a Custom ESR/CL Requirement Table

Once gm_min (from Method A) or gm_equiv (from Method B) is known, a full requirement table equivalent to Table 3-1 can be generated for any frequency range and CL setting. For each target frequency:

1. Compute $\omega = 2\pi \times f$ (Equation 14).
2. For each test CL (for example, CL1 = CL2 = 12pF and CL1 = CL2 = 24pF): compute $Rneg = gm\_min / (\omega^2 \times CL^2)$ (Equation 15).
3. Compute ESR_max = Rneg / MS (Equation 17). This is the table entry for that frequency/CL combination.
4. Compute $CL\_max = \sqrt{(gm\_min / [MS \times Rm \times \omega^2])} - C0$ (Equation 18).
5. Repeat for all frequencies of interest.

The companion calculator (Crystal Calculation tool GUI interface) generates this table automatically in the Generic Derivation section. Table 9-4 shows an example for a 1.5mA/V oscillator covering the 10MHz to 50MHz range:

Table 9-4. Example Custom ESR/CL Requirement Table

Freq (MHz)	Rneg at CL= 12pF (Ω)	ESR_max at 12pF (Ω)	Rneg at CL = 18pF (Ω)	ESR_max at 18pF (Ω)	CL_max (pF)
10	659.5	219.8	293.1	97.7	41.8
15	293.1	97.7	130.3	43.4	27.1
20	164.9	54.9	73.3	24.4	20.3
40	41.2	13.7	18.3	6.1	14.3
50	26.4	8.8	11.7	3.9	12.8

Note

gm_min is typically specified or measured at a single frequency and voltage corner. At higher frequencies, actual gm can be lower due to transistor bandwidth limitations. For frequencies exceeding 20MHz, re-measure or re-derive gm_min at each target frequency if the oscillator datasheet does not explicitly cover the full range.

9.1.5 Method C - Frequency Pulling Characterization

Crystal frequency pulling describes the shift in oscillation frequency when the load capacitance CL differs from the crystal's rated CL specification. When the motional capacitance Cm is known, the frequency offset can be calculated without any measurement. Cm is either provided in the BVD model of the crystal manufacturer or measured with an impedance analyzer.

9.1.5.1 Required Equipment and Components

Crystal (Mandatory)

- Same candidate crystal used in the design
- BVD model parameters required: Rm (or ESR), C0, and Cm
- Source 1: crystal manufacturer characterization sheet — request BVD model by part number
- Source 2: impedance analyzer measurement (see below if Cm not available)
- Cm varies between individual crystals of the same part number; use the manufacturer's typical or maximum Cm for worst-case pulling calculation

Impedance Analyzer (If Cm not in datasheet)

- Instrument: Keysight E4990A, E4991B, or Zurich Instruments MFIA
- Frequency range: must include the crystal's series resonance (f_s)
- Crystal fixture: low-parasitic SMD holder; stray inductance < 5nH (Keysight 16092A or custom)
- Calibration: SOLT at the crystal fixture reference plane before measurement
- Extract Cm from measured impedance: Cm = 1 / (Lm × ω_s^2) where ω_s = 2πf_s
- Do not use a simple LCR meter for this measurement — crystal Q is too high for bridge-type instruments

Precision Capacitor Kit (for empirical pulling measurement)

- C0G/NP0 dielectric only — X7R introduces temperature-dependent error
- Values: 8pF, 10pF, 12pF, 15pF, 18pF, 22pF, 24pF, 27pF, 33pF — covering the oscillator's full CL range
- Tolerance: ±0.5% or better (±1% acceptable when frequency accuracy requirement > 20ppm)
- Package: 0402; solder into CL1/CL2 pads for each measurement

Frequency Measurement

- Frequency counter: resolution ≤ 1Hz at the oscillator frequency (for example, Keysight 53220A or equivalent)
- Connection: through XCLKOUT GPIO (non-invasive) — do not connect counter directly to X1/X2
- Gate time: ≥ 100ms for 10Hz resolution; ≥ 1s for 1Hz resolution
- Allow oscillator to stabilize thermally (> 5 min after cap swap) before measuring frequency

9.1.5.2 Equations

The frequency offset from series resonance (f_series) when the crystal sees load capacitance CL is:

$$\Delta f[\mathrm{ppm}] = \mathrm{Cm}/(2\times(\mathrm{C0}+\mathrm{CL}))\times 10^6 \tag{33}$$

The frequency deviation from the crystal's rated nominal frequency when using a load capacitance CL_actual that differs from the crystal's specified CL_nom is:

$$\Delta f_{\mathrm{d}}\mathrm{ev}[\mathrm{ppm}] = (\mathrm{Cm}/2)\times(1/(\mathrm{C0}+\mathrm{CL}_{\mathrm{n}}\mathrm{om})-1/(\mathrm{C0}+\mathrm{CL}_{\mathrm{a}}\mathrm{ctual}))\times 10^6 \tag{34}$$

A positive Δf_dev means the crystal runs faster than rated (CL_actual < CL_nom); negative means slower (CL_actual > CL_nom).

9.1.5.3 Procedure

1. Obtain Cm from the crystal datasheet (labeled "C1," "Cm," or "motional capacitance" in the BVD model, typically in fF). If not available, measure with an impedance analyzer as described above.
2. Identify the crystal's rated CL_nom (from the frequency specification in the datasheet).
3. For each candidate CL1 = CL2 value in the oscillator's supported range, calculate: CL_actual = CL1/2 + C_stray (Equation 4).
4. Apply Equation 33 to find the frequency offset from series resonance.
5. Apply Equation 34 to find the frequency deviation from the rated nominal frequency.
6. Compare Δf_dev to the application's frequency accuracy requirement. If the deviation exceeds the allowable tolerance, adjust CL1/CL2 or select a crystal spec'd at a different CL_nom.
7. Optionally verify empirically: install each CL1/CL2 set and measure frequency via XCLKOUT. Compare measured deviation to Equation 34 prediction.

9.1.5.4 Worked Example - 40MHz Frequency Pulling

Table 9-5. Frequency Pulling Versus Load Capacitance at 40MHz

CL1 = CL2	CL_actual (pF, + 2pF stray)	Δf from series resonance (ppm) Equation 33	Δf_dev from rated (ppm) Equation 34	Direction
12pF	8.0	363.6	+104.5	Faster than rated
13pF (CL_nom=15pF scenario)	**8.5**	**347.8**	**+88.8**	**Faster than rated**
15pF	9.5	320.0	+61.0	Faster than rated
18pF ✓ (selected)	**11.0**	**285.7**	**+26.7**	**Faster than rated**
22pF	13.0	256.0	−3.0	Slower than rated
24pF	14.0	246.2	−12.8	Slower than rated

Reading the table: With the selected CL1 = CL2 = 18pF, the crystal runs approximately 27ppm faster than the rated 15pF nominal frequency. For applications with ±50ppm or better tolerance (for example, CAN bus, most microcontroller clocks), this deviation is acceptable. For tighter applications (TCXO replacement, GPS disciplining), the CL must be trimmed more precisely to match CL_nom.

9.1.6 Summary Checklist - Generic Pierce Oscillator Crystal Selection

Pre-Design Verification Checklist (No Table 3-1)

- Obtain gm_min from oscillator datasheet or TRM (Section 9.1.3), OR plan empirical Rneg measurement (Section 9.1.4)
- Confirm crystal datasheet provides: ESR (or Rm), C0, CL rated, max drive level
- Confirm C0 ≤ oscillator's maximum shunt capacitance spec (C28x/F29x: 7pF)
- Compute Rneg (Equation 15) at chosen CL1 = CL2; verify ESR ≤ ESR_max (Equation 17)
- Compute CL_max (Equation 18); confirm CL1 = CL2 ≤ CL_max for selected crystal Rm
- Compute drive level (Equation 7) and determine if Rd is required (Equation 11)
- If Cm known: compute frequency pulling deviation (Equation 33 / Equation 34) and confirm within tolerance
- For fixed-frequency oscillators: confirm crystal sourcing with required ESR at target freq
- [Automotive] Repeat analysis at −40°C ESR (request from crystal manufacturer) and minimum VDD
- [Automotive] Perform empirical Rneg test (Method B) at minimum VDD and −40°C to confirm gm_min
- Document derived gm_min and generated Table A-X equivalent in the design review package

10 References

- Matthys, Crystal Oscillator Circuits (Krieger, 1992)
- Vittoz et al., IEEE JSSC 1988, DOI 10.1109/4.318
- Vig, Introduction to Quartz Frequency Standards CECOM-TR-97-3
- AEC-Q100 Rev-H (aecouncil.com)
- Seiko Epson Crystal Unit App Manual (www5.epsondevice.com)
- IQD Tech Note 30: Design Guidelines for Quartz Crystal Oscillators

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025