Application Note

Full-Bridge LLC with UCC25661x

Amrita Mitra, Sanchayan Das, Aditya Madhavan

ABSTRACT

This application note describes the implementation of a Full-Bridge LLC resonant converter based on the UCC25661x LLC controller. Since the controller is primarily intended for Half-Bridge applications, additional circuitry is employed to generate the required gate-drive signals and necessary features for Full-Bridge operation.

Table of Contents

Trademarks

All trademarks are the property of their respective owners.

Copyright © 2026 Texas Instruments Incorporated

1 Introduction

LLC resonant converters are widely used in high-efficiency isolated DC-DC power conversion applications due to their ability to achieve soft-switching operation over a wide load range. By operating the primary switches under Zero Voltage Switching (ZVS) conditions and minimizing switching losses, LLC converters offer high efficiency, reduced electromagnetic interference (EMI), and high-power density. These characteristics make them attractive for server power supplies, telecom power systems, consumer electronics, and industrial power conversion systems.

The Half-Bridge LLC converter is commonly employed in medium-power applications because of its simple implementation and reduced component count. However, as the power level increases, a Full-Bridge LLC topology becomes attractive due to its ability to apply the full input bus voltage across the resonant tank, thereby reducing current stress and conduction losses while enabling higher power capability.

The UCC25661x family is a highly integrated LLC resonant controller primarily intended for Half-Bridge LLC converters. In applications requiring higher output power, it may be desirable to retain the features of the UCC25661x while implementing a Full-Bridge power stage. This can be achieved using an additional interface and gate-drive circuitry.

This application note presents the implementation of a Full-Bridge LLC resonant converter using the UCC25661x controller. The document discusses the operating principle, gate-drive generation method, protection implementation, design considerations, and experimental validation of the proposed design.

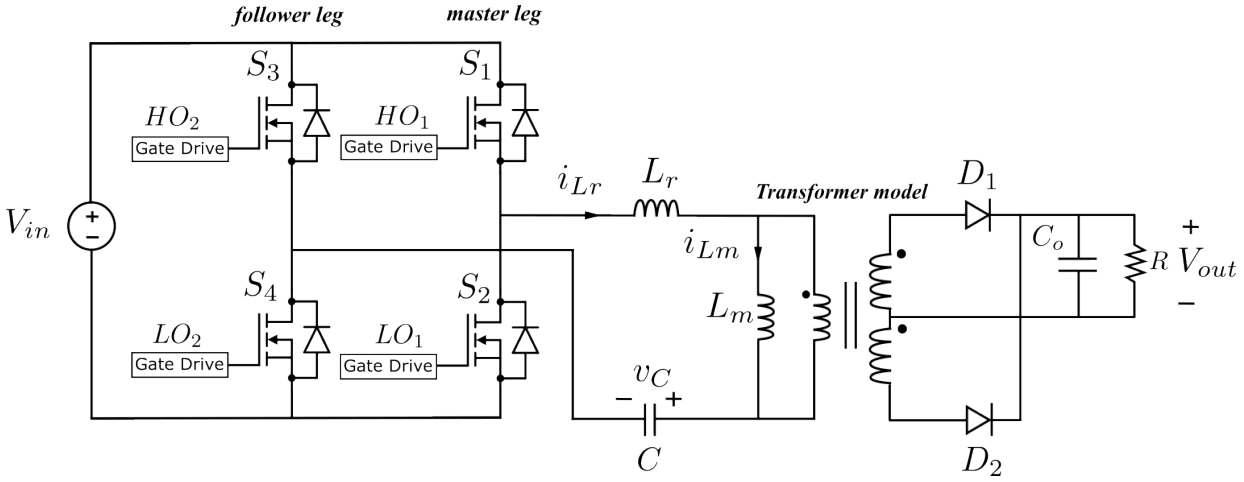

Figure 1-1. Full-Bridge LLC Resonant Converter

Copyright © 2026 Texas Instruments Incorporated

2 Full Bridge LLC Operating Principle

This section provides an overview of the Full-Bridge LLC converter operation. Figure 2-1 shows the complementary switching sequence of the two bridge legs. During steady state operation, diagonally opposite switches are turned on simultaneously, applying alternating polarity across the resonant tank. This results in tank square-wave excitation which generates a near-sinusoidal resonant current that flows through the resonant network and transformer. The AC current is hence scaled, rectified and filtered to produce a regulated DC output voltage.

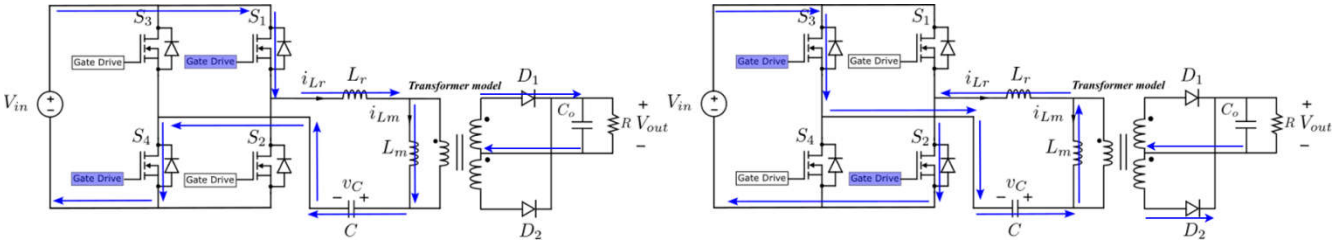

Figure 2-1. Switching States and Resonant Tank Operation of the Full-Bridge LLC Converter

From the resonant tank perspective, the Full-Bridge LLC converter operates similarly to the Half-Bridge LLC converter. The primary difference is that the full input bus voltage is applied across the resonant tank, whereas only half of the bus voltage excites the resonant tank in a Half-Bridge implementation. Consequently, the gain relationship and transformer turns-ratio selection differ by a factor of two, while the resonant tank analysis and frequency-control methodology remain unchanged. The simplified resonant tank gain expression obtained using the First Harmonic Approximation (FHA) is given by : (where Bridge is 0.5 for half bridge and 1 for full bridge topology)

*Normalized Gain = Bridge Gain * N (Transformer turns ratio) * Impedance Ratio Gain*

Figure 2-3 shows the resonant tank gain characteristics for different load conditions. All gain curves intersect at the resonant frequency, while the peak of each curve defines the boundary between capacitive and inductive operation. To verify Zero Voltage Switching (ZVS) and minimize switching losses, LLC converters are designed to operate in the inductive region. The corresponding resonant tank waveforms are shown in Figure 2-2 (for fs < fr).

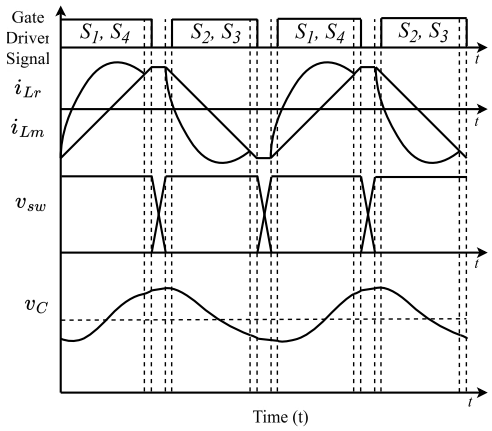

Figure 2-2. FB-LLC Steady State Waveforms

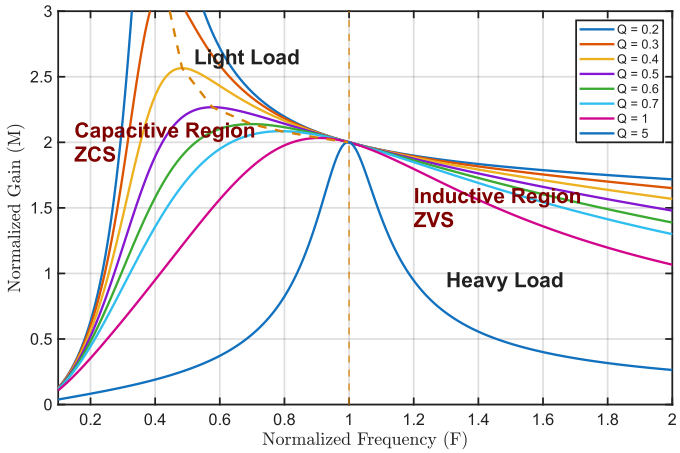

Figure 2-3. Gain Characteristics of the FB-LLC

Copyright © 2026 Texas Instruments Incorporated

3 Implementation With UCC25661x

Gate Drive Architecture

The UCC25661x generates the *HO* and *LO* signals required for Half-Bridge LLC operation. In a Full-Bridge LLC converter, the high-side switches of each leg are referenced to different floating switch nodes rather than to ground (PGND). Therefore, the controller outputs cannot be directly applied to the follower leg. Isolated gate drivers are employed to verify that each gate signal is properly referenced to its corresponding source terminal, enabling correct gate-drive voltage. Similar Gate drivers can be used on the master leg as well to verify delay matching across both the legs. Here, (HO1 and LO1 denote the master leg gate drive signals, and HO2 and LO2 denote the follower leg gate drive signals. HS and HS1 denote the switching node voltage of the master and follower leg respectively.)

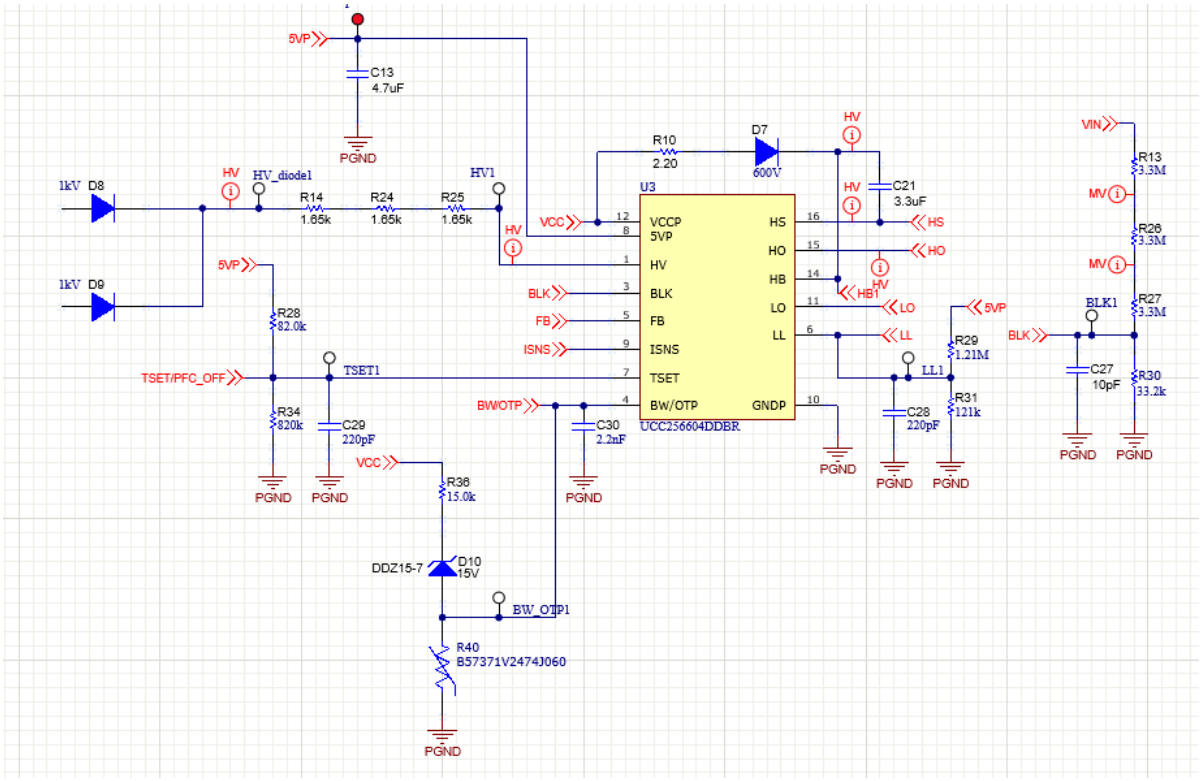

Figure 3-1. UCC25661x Implementation in Half Bridge LLC

Copyright © 2026 Texas Instruments Incorporated

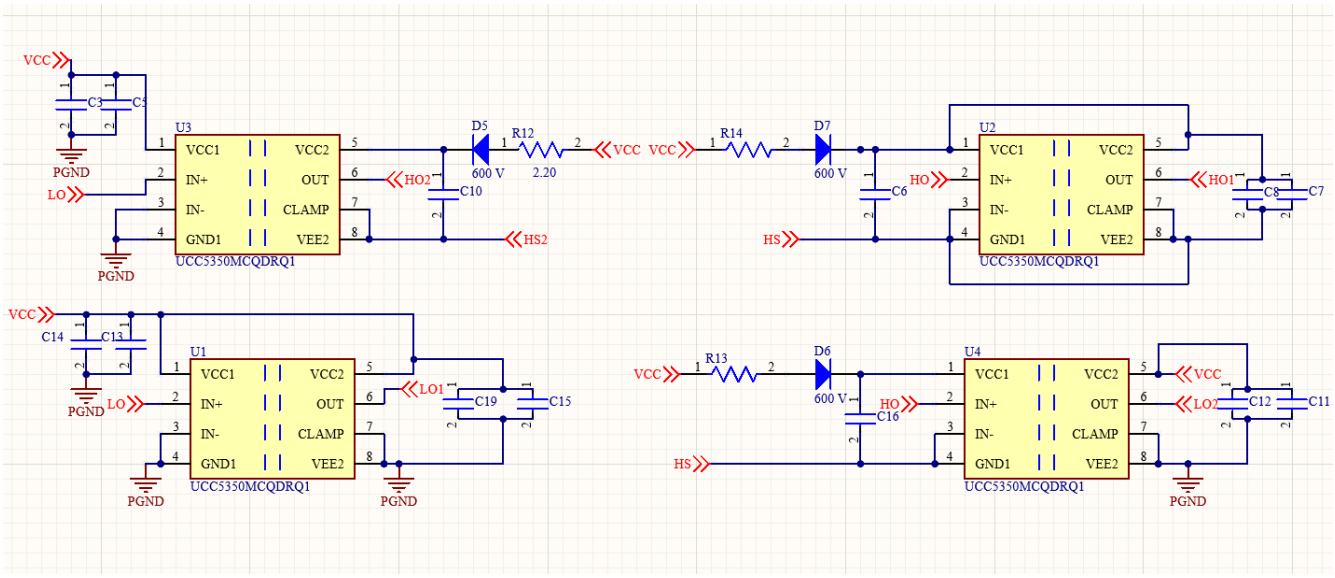

Figure 3-2. Full Bridge LLC Isolated Gate Driver Implementation

The controller outputs HO and LO are routed through four isolated gate drivers to generate the gate-drive signals HO1, LO1, HO2, and LO2 required for the Full-Bridge LLC converter. The high-side gate drivers employ bootstrap circuits to provide the floating gate-drive supply referenced to their respective switching nodes (HS and HS1).

ISNS Circuit Modification

The UCC25661x Half-Bridge LLC EVM uses a split resonant capacitor arrangement and a differentiator-based circuit to sense the resonant tank current at the ISNS pin. In the Full-Bridge LLC implementation, the split capacitor arrangement is no longer required, and both ends of the resonant tank are connected to actively switching bridge nodes. Consequently, the resonant capacitor and tank network no longer possess a fixed reference node (PGND), making the original differentiator-based sensing method unsuitable. Therefore, the differentiator circuit is replaced with a current transformer (CT)-based sensing.

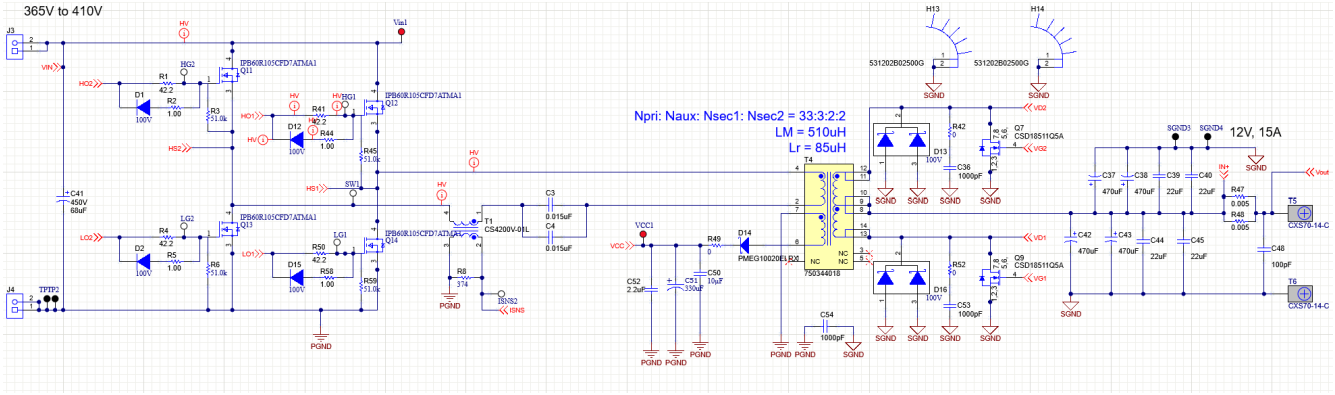

Figure 3-3. FB LLC Power Stage Schematic

The ISNS pin also sets the over current protection level (OCP1). The threshold value of OCP1 is either 3.5V or 4V depending on the TSET pin resistors and the variant being used. For this design, UCC256611 is being used and the OCP1 threshold value (OCP1_Threshold) is 3.5V. If the peak resonant current at full load is known (I_PEAK), then for a CT with turns ratio N (Pri : Sec) the burden resistance (RT) can be chosen as:

RT < OCP1_Threshold * N / I_PEAK. The peak resonant current at OCP1 level (I_PEAK_OCP1) is then calculated using: I_PEAK_OCP1 = OCP1_Threshold * N / RT

Copyright © 2026 Texas Instruments Incorporated

Note: The selected CT should be chosen to provide adequate current rating and volt-sec capability over the intended operating range.

Auxiliary Logic Implementation

During startup, the controller applies an initial 200-µs LO1 pulse to charge the bootstrap capacitor for the high side switch. However, if isolated power supply modules are used for bootstrap charging, the converter immediately enters normal Full-Bridge operation, HO2 turns on simultaneously with LO1. As a result, the resonant tank is subjected to a voltage of V_{IN} + V_{CR} which is applied across the resonant or leakage inductor resulting in a large tank current that may exceed the safe operating limits of the power switches. To avoid this condition, an auxiliary logic circuit forces LO2 to turn on together with LO1 during the startup interval. This effectively connects both ends of the resonant tank to the negative DC Bus, allowing the resonant capacitor to discharge under safe current limits before normal Full-Bridge operation is enabled.

The HO and LO outputs of the controller are first translated to 5-V logic levels, denoted as LO2_5V and LO_5V, to verify compatibility with the digital logic circuitry. During the LLC startup sequence, the TSET signal transitions low before the controller generates the 200µs LO1 startup pulse. The same sequence is repeated during fault-retry operation, where TSET again transitions low following the 1s idle interval. This falling edge is detected using a one-shot circuit to generate a short SET pulse for the SR latch. Similarly, the falling edge of LO_5V is detected using a second one-shot circuit to generate a short RESET pulse. These SET and RESET pulses control the SR latch, whose output Q determines the converter operating mode.

When the latch is set (Q=1), the logic forces Logic level LO2 high and HO2 low, thereby establishing the predefined startup switching state. The latch retains this state until a RESET pulse is generated by the falling edge of LO_5V. Upon receiving the RESET pulse, the latch is cleared (Q=0), removing the forcing action from the logic outputs. Thereafter, LO2 and HO2 follow the translated controller signals, enabling normal Full-Bridge LLC operation.

Logic Level Signal Translation:

1. To implement the auxiliary logic circuit, the HO and LO signals from the controller need to be translated into logic level 5V (LO2_5V and LO_5V) respectively.

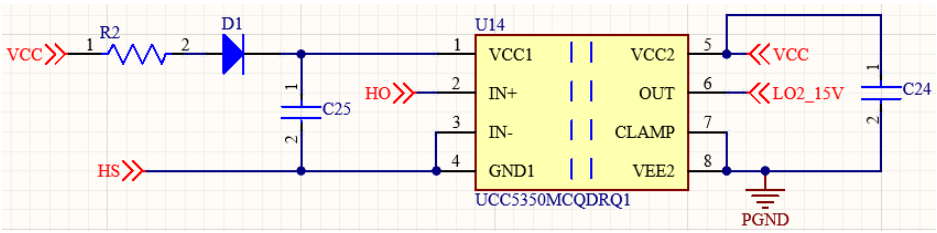

Figure 3-4. Logic-Level Translation of the HO Controller Output - 1

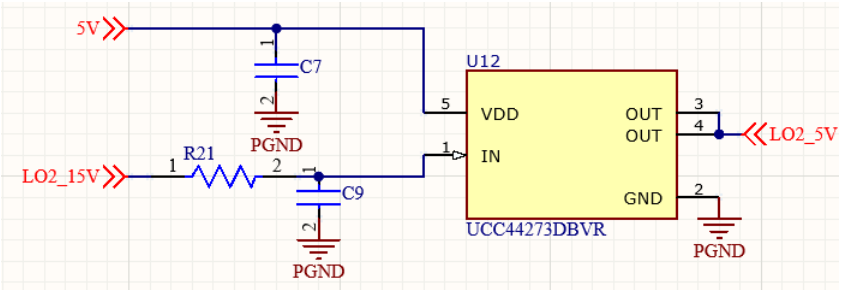

Figure 3-5. Logic-Level Translation of the HO Controller Output - 2

Copyright © 2026 Texas Instruments Incorporated

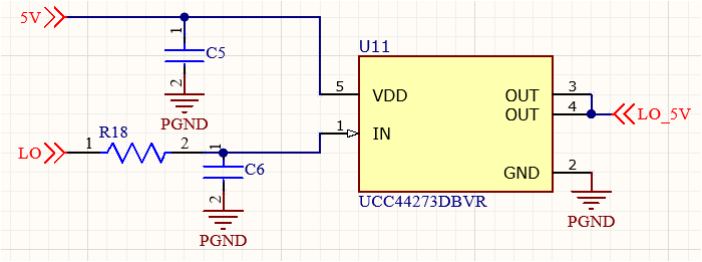

Figure 3-6. Logic-Level Translation of the LO Controller Output

An alternative implementation with reduced component count is shown in Figure 3-7. The floating HO signal is translated using the ISO1211 isolated digital input receiver, while the LO signal is translated using a resistor divider to generate logic-compatible 5-V signals for the auxiliary logic circuit.

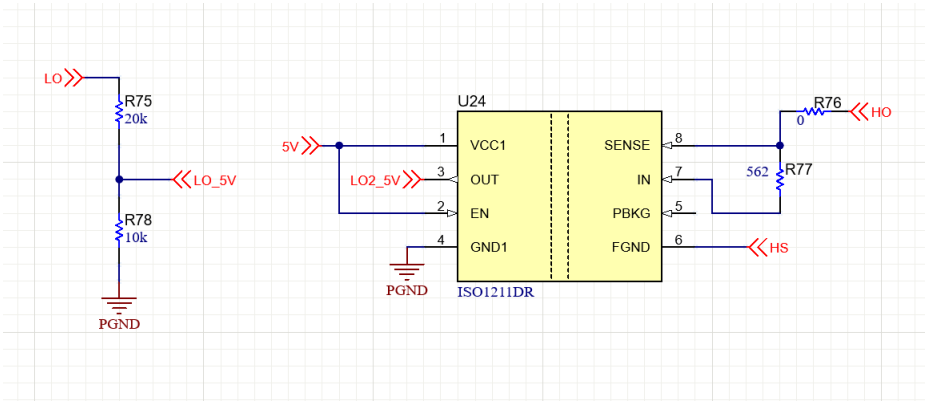

Figure 3-7. Alternative Logic-Level Translation of the HO and LO Controller Outputs

The logic-level outputs HO2 (LO_1_5V) and LO2 (LO2_5V) generated by the auxiliary logic circuit can be interfaced to the power stage using the four isolated gate-driver implementation shown in Figure 3-2. Alternatively, the same functionality can be realized using half-bridge gate drivers, as shown in Figure 3-8.

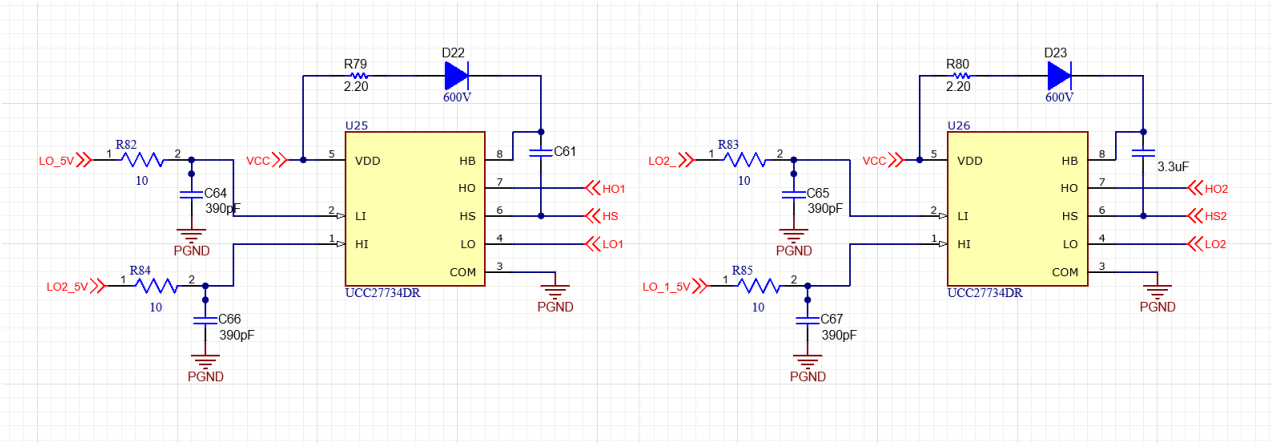

Figure 3-8. Alternative Full Bridge LLC Gate Driver implementation using half bridge gate drivers

Copyright © 2026 Texas Instruments Incorporated

4 Hardware Results

The experimental results for full-bridge LLC in normal resonant mode operation, burst mode operation, start up, load transient and bulk brown out are as shown below.

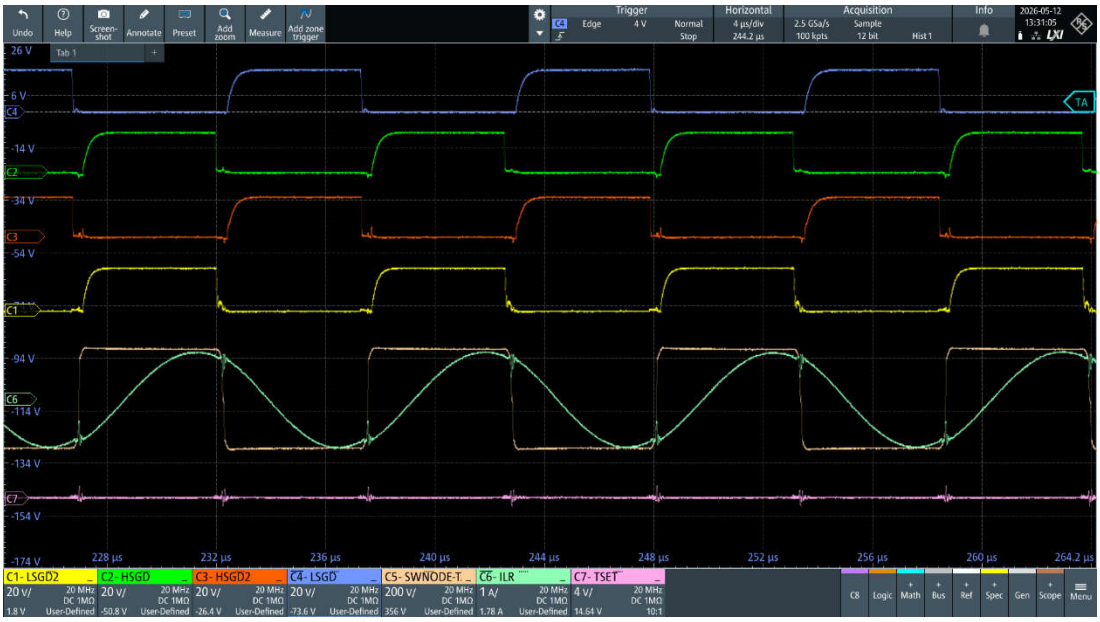

Figure 4-1. Vin = 185V , Vout = 12V , Iout = 7A, Normal Resonant Mode Operation, C1=LO2 Gate Drive, C2= HO1 Gate Drive, C3= HO2 Gate Drive, C4= LO1 Gate Drive C5= Tank Voltage, C6= Tank Current, C7= TSET Pin Voltage

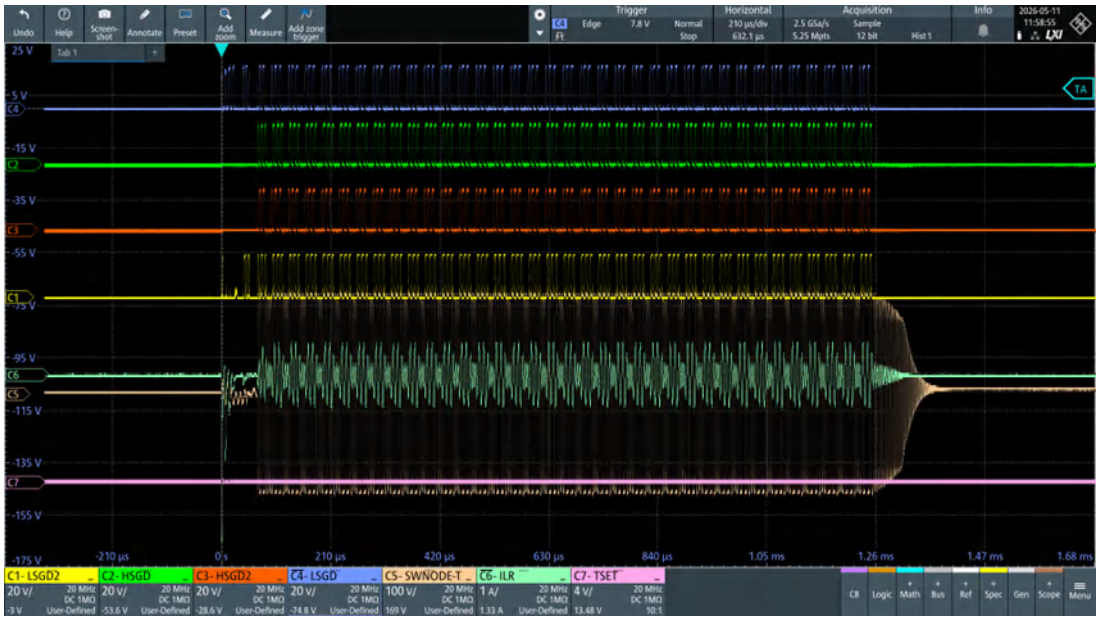

Figure 4-2. Vin = 185V , Vout = 12V , No Load, Burst Mode Operation, C1=LO2 Gate Drive, C2= HO1 Gate Drive, C3= HO2 Gate Drive, C4= LO1 Gate Drive C5= Tank Voltage, C6= Tank Current, C7= TSET Pin Voltage

Copyright © 2026 Texas Instruments Incorporated

Figure 4-3. Auxiliary Logic in Startup – HO2 and LO2 on for 200 us pulse, C1=LO2 Gate Drive, C2= HO1 Gate Drive, C3= HO2 Gate Drive, C4= LO1 Gate Drive, C5= Tank Voltage, C6= Tank Current, C7= TSET Pin Voltage

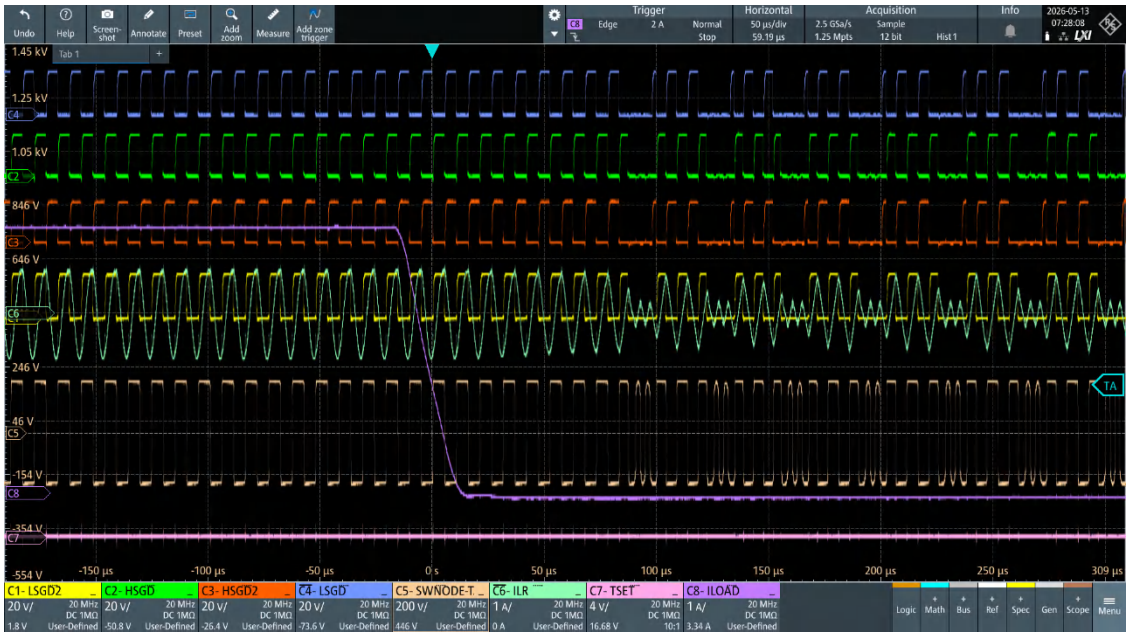

Figure 4-4. Vin = 185V, Vout =12V, Iout = 5A to 0.01A Load Transient (0.2A/us) C1=LO2 Gate Drive, C2= HO1 Gate Drive, C3= HO2 Gate Drive, C4= LO1 Gate Drive C5= Tank Voltage, C6= Tank Current, C7= TSET Pin Voltage, C8 = Load Current

Copyright © 2026 Texas Instruments Incorporated

Figure 4-5. Vin = 185V, Vout = 12V, Iout = 0.01A to 5A Load Transient (0.2A/us) C1=LO2 Gate Drive, C2= HO1 Gate Drive, C3= HO2 Gate Drive, C4= LO1 Gate Drive C5= Tank Voltage, C6= Tank Current, C7= TSET Pin Voltage, C8 = Load Current

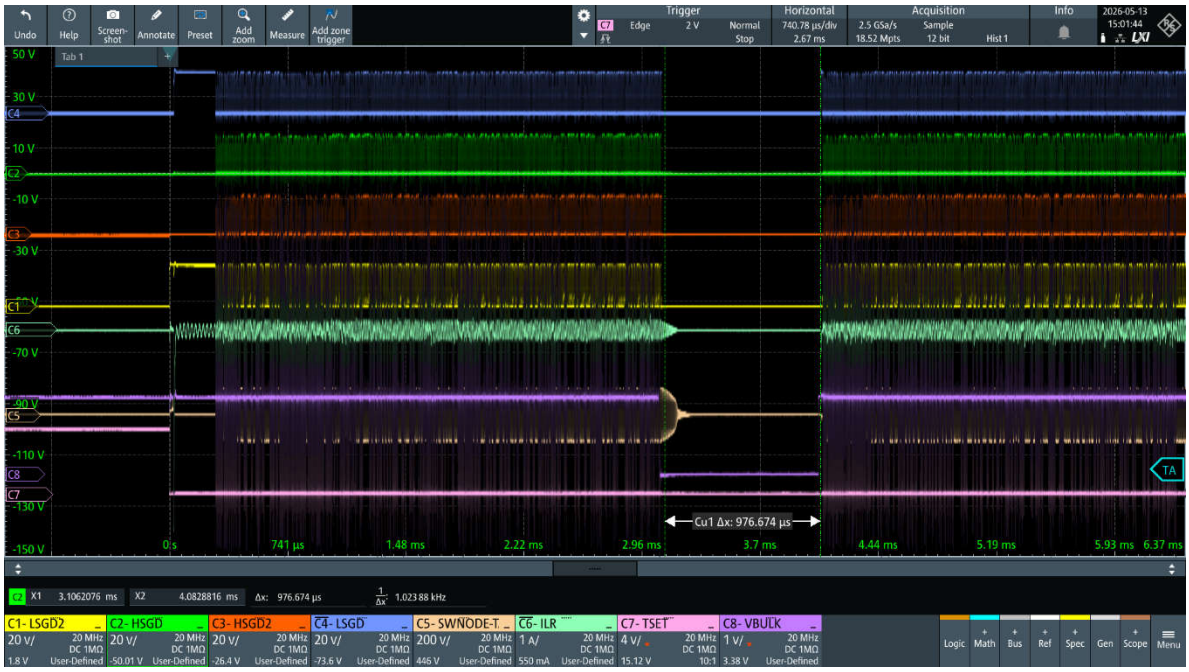

Figure 4-6. BLK Brownout emulated at Vin = 100V, No Load Depicting Auxiliary Logic Operation C1=LO2 Gate Drive, C2= HO1 Gate Drive, C3= HO2 Gate Drive, C4= LO1 Gate Drive C5= Tank Voltage, C6= Tank Current, C7= TSET Pin Voltage, C8 = Bulk Pin Voltage

Copyright © 2026 Texas Instruments Incorporated

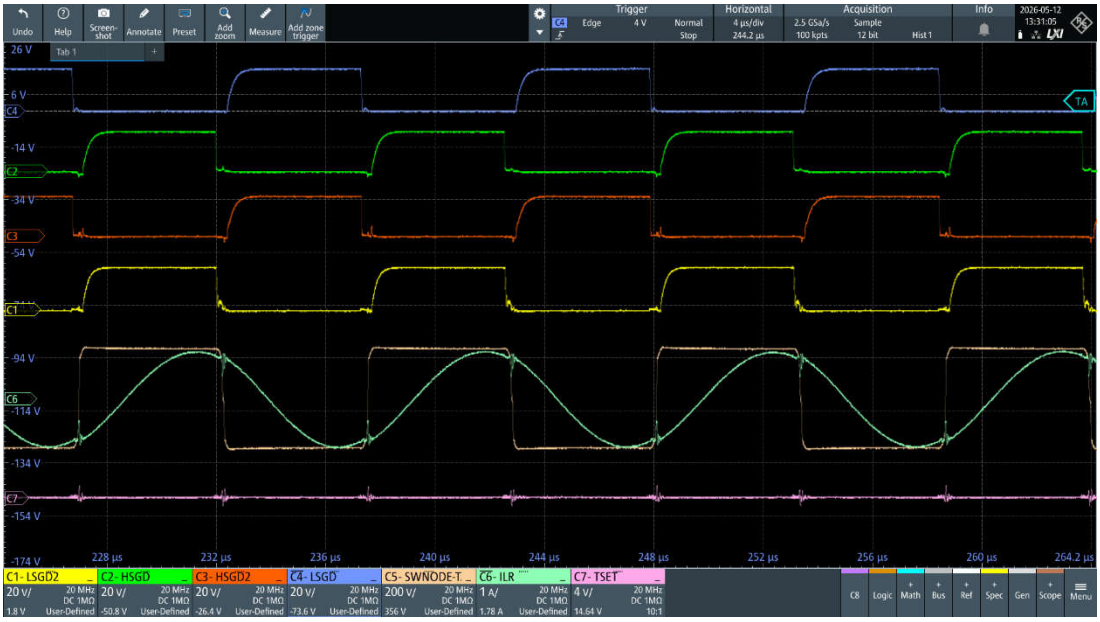

Figure 4-7. Vin = 185V , Vout = 12V , Iout = 7A, Normal Resonant Mode Operation, C1=LO2 Gate Drive, C2= HO1 Gate Drive, C3= HO2 Gate Drive, C4= LO1 Gate Drive, C5= Tank Voltage, C6= Tank Current, C7= TSET Pin Voltage

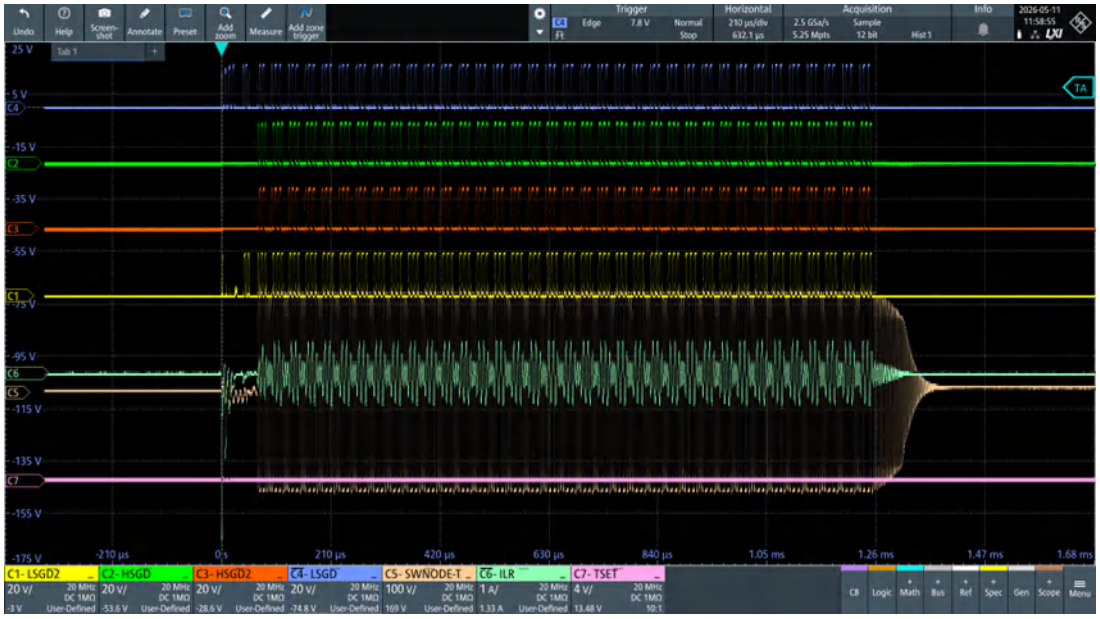

Figure 4-8. Vin = 185V , Vout = 12V , no load, burst mode operation, C1=LO2 Gate Drive, C2= HO1 Gate Drive, C3= HO2 Gate Drive, C4= LO1 Gate Drive C5= Tank Voltage, C6= Tank Current, C7= TSET Pin Voltage

Copyright © 2026 Texas Instruments Incorporated

Figure 4-9. Auxiliary logic in startup – HO2 & LO2 on for 200 us Pulse, C1=LO2 Gate Drive, C2= HO1 Gate Drive, C3= HO2 Gate Drive, C4= LO1 Gate Drive, C5= Tank Voltage, C6= Tank Current, C7= TSET Pin Voltage

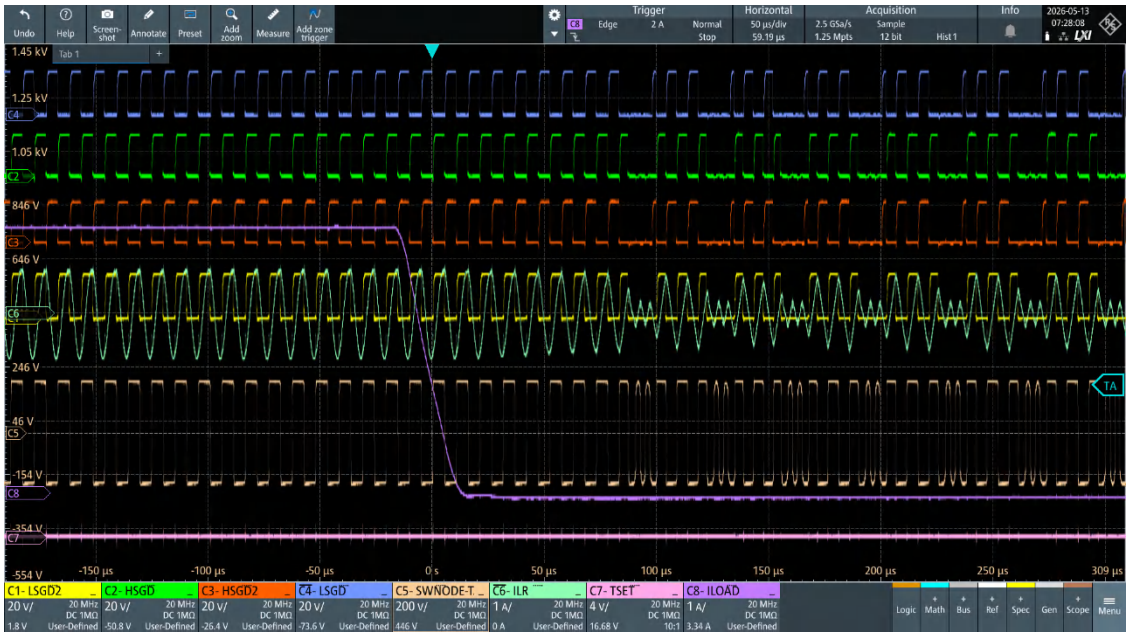

Figure 4-10. Vin = 185V, Vout =12V, Iout = 5A to 0.01A Load Transient (0.2A/us) C1=LO2 gate drive, C2= HO1 Gate Drive, C3= HO2 Gate Drive, C4= LO1 Gate Drive C5= Tank Voltage, C6= Tank Current, C7= TSET Pin Voltage, C8 = Load Current

Copyright © 2026 Texas Instruments Incorporated

Figure 4-11. Vin = 185V, Vout = 12V, Iout = 0.01A to 5A Load Transient (0.2A/us) C1=LO2 Gate Drive, C2= HO1 Gate Drive, C3= HO2 Gate Drive, C4= LO1 Gate Drive C5= Tank Voltage, C6= Tank Current, C7= TSET Pin Voltage, C8 = Load Current

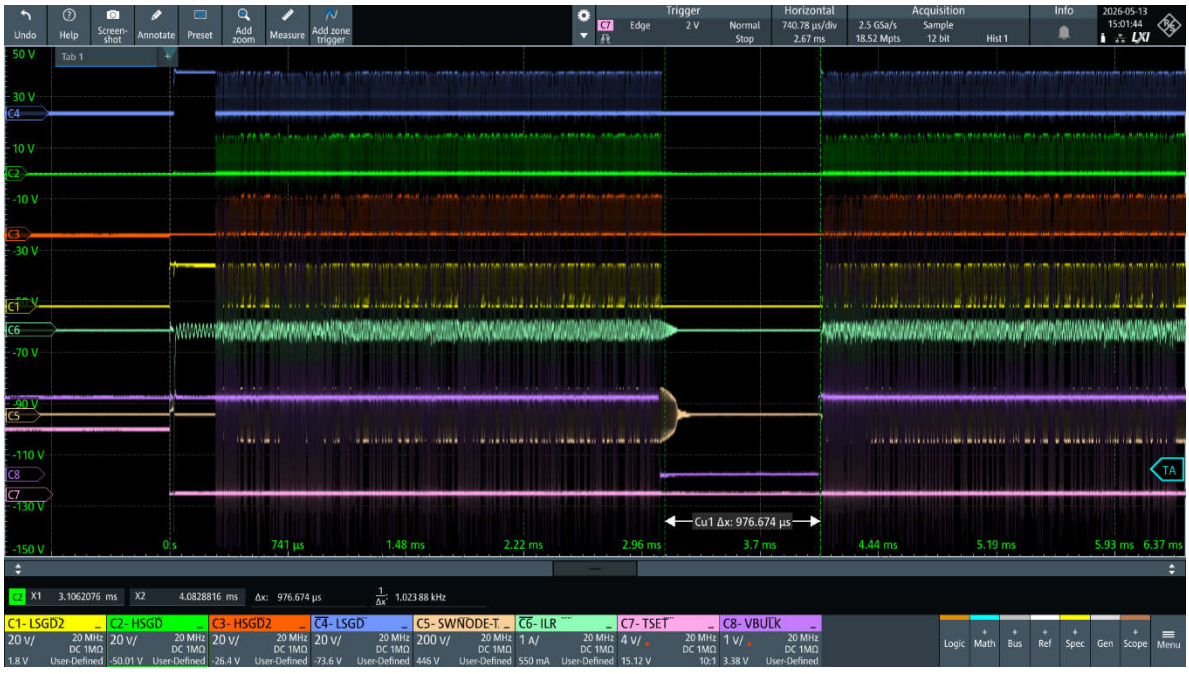

Figure 4-12. BLK Brownout Emulated at Vin = 100V, No Load Depicting Auxiliary Logic Operation C1=LO2 Gate Drive, C2= HO1 Gate Drive, C3= HO2 Gate Drive, C4= LO1 Gate Drive C5= Tank Voltage, C6= Tank Current, C7= TSET Pin Voltage, C8 = Bulk Pin Voltage

Note: All experimental results were obtained on the modified UCC25661x EVM in Full-Bridge configuration with the auxiliary startup circuit enabled (mentioned in section 3). Since the Full-Bridge LLC applies twice the tank voltage of the Half-Bridge LLC, the prototype was tested at 185 VDC using the original EVM magnetics.

Copyright © 2026 Texas Instruments Incorporated

5 Summary

This application note demonstrates the implementation of a Full-Bridge LLC converter using the UCC25661x Half-Bridge LLC controller. The required hardware modifications, including isolated gate-drive implementation, auxiliary startup logic, and current transformer-based resonant current sensing, are presented. Experimental results on the modified UCC25661x EVM validate the proposed implementation and demonstrate reliable Full-Bridge LLC operation.

6 References

1. Texas Instruments, *UCC25661x Family 750kHz Wide VIN /VOUT Range LLC Controller Optimized for Light-Load Efficiency* , datasheet.
2. Texas Instruments, *UCC25661x Half Bridge LLC Evaluation Module*, user's guide.

Copyright © 2026 Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025