Application Note

Designing a Closed-Loop Load Transient Board

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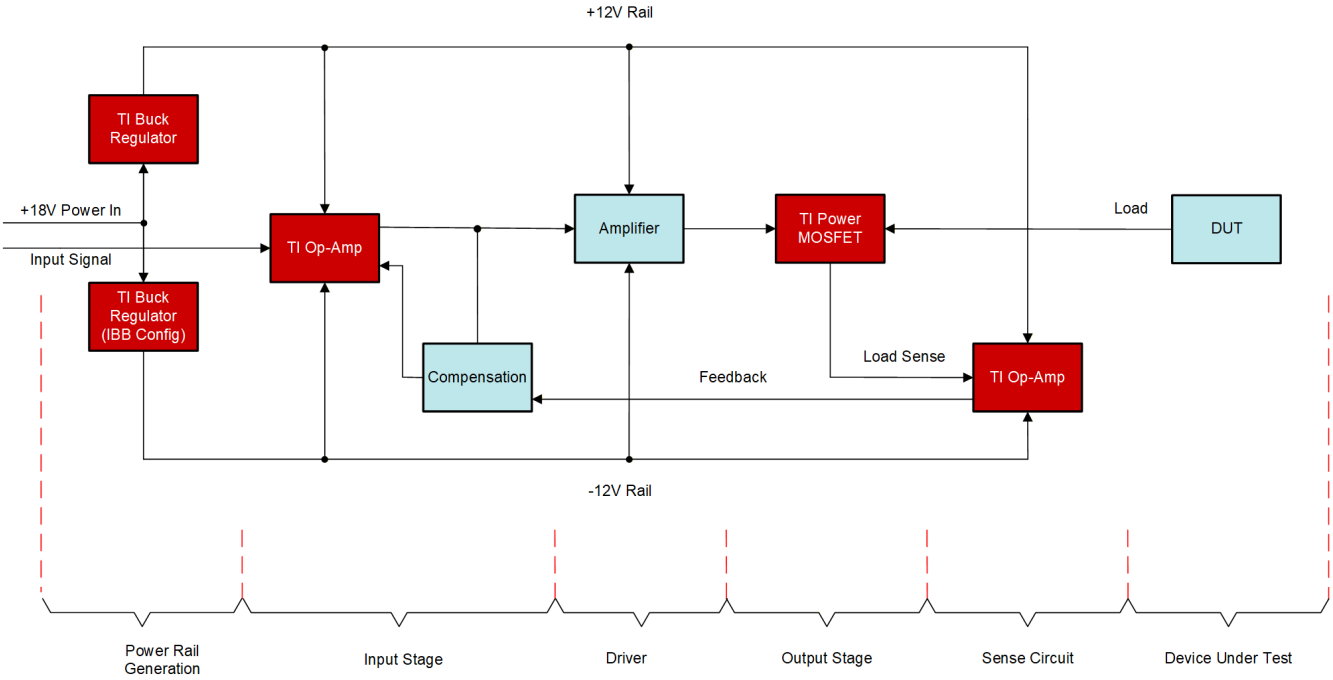
ABSTRACT

This application note describes the process of designing a closed-loop load transient board and examines its performance. Many electronic systems induce load transient events during regular operation, such as a microcontroller (MCU) going from sleep or low-energy mode to an active mode. These events perturb power rails as more current is required to satisfy the suddenly increased load. The power regulator, for example, buck or boost, eventually accommodates the increased load and settles through the regulator's response. The duration and severity of the transient event are of special interest from a power converter perspective, as they can help characterize the power converter's loop response. This document describes how a closed-loop load transient board can be designed to simulate such events, providing a useful means of characterizing power electronics' performance.



System Block Diagram

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1 Introduction

The overall concept of the design explored herein is an expansion on the basic voltage-to-current (V2I) circuit shown in Figure 1-1. The load transient circuit receives an input at the operational amplifier's (op-amp's) positive input terminal. Since the negative terminal is connected to GND through resistance R, the op-amp generates an output proportional to the difference between its input terminals. This causes the transistor to turn on, and current flows through R until a voltage develops across R. The voltage across R continues to rise until the difference between the input terminals is zero volts. The equal potential between the op-amp terminals generates a reference current equal to V_{in}/R. Such circuits are common in analog IC design.

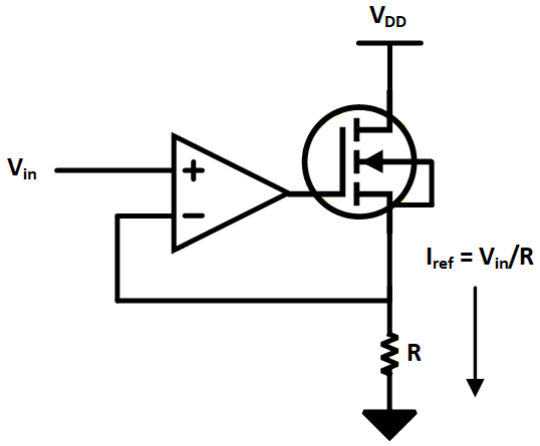

Figure 1-1. Simple V2I Circuit

In this design, however, a driver/buffer added before the load transistor allows the circuit to drive larger gate capacitance of larger transistors that have lower on-resistance, enabling higher load currents. Adding a difference amplifier to detect the voltage across the sense resistor R verifies an accurate voltage-to-current ratio and allows configuration of this ratio through the difference amplifier's gain.

2 Design Overview

This design is comprised of various stages. Each stage plays a distinct role in achieving the overall design objective. The following sections provide a brief overview of each stage.

2.1 Input Stage

The purpose of this design is to create a board that can simulate a system load transient event by applying a known input voltage, without having to characterize the load field-effect transistor (FET). The input stage, the key component of which is an op-amp, is wired in a negative feedback configuration. Negative feedback enables a fixed gain between input voltage and output current. The input signal propagates through any of the input connectors to the positive input terminal of the op-amp. In response, the op-amp drives its output high to force its input terminals to become equal in potential. Multiple input connectors are connected in parallel for convenience; SMB, BNC or alligator clips may be used to interface with the circuit.

The input stage includes a series high-frequency bypass RC network between the op-amp positive and negative terminals. This RC is designed to be a high-impedance (Hi-Z) connection at DC and low frequency, but a low-impedance (Lo-Z) connection at higher frequencies. This shunts high-frequency ringing at the input terminals that could occur when applying sharp step inputs. Finally, the input stage contains several passive components across its output and feedback terminals to ensure stability. The input stage is shown in Figure 2-1.

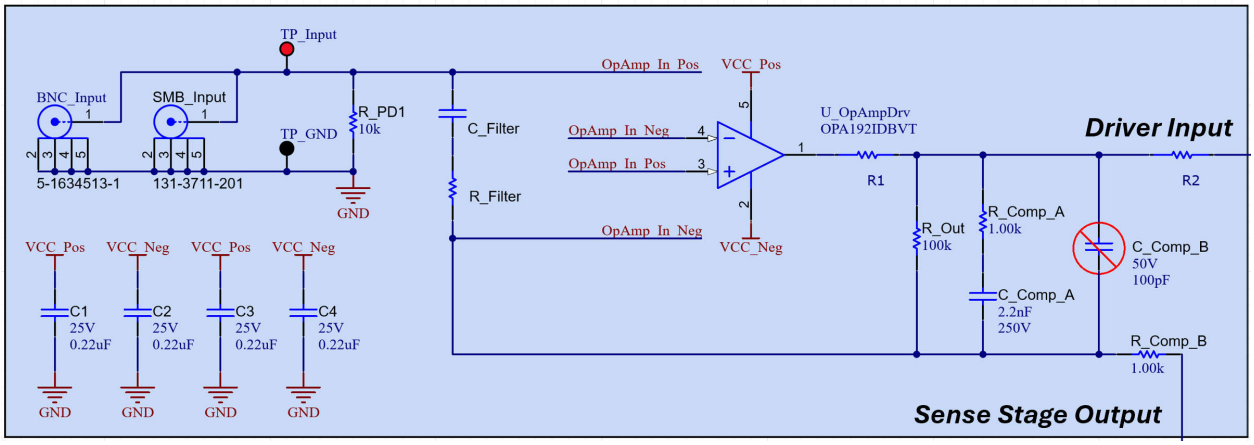

Figure 2-1. Input Stage Schematic

2.2 Driver Stage

The input stage generates the control signal for the driver stage. The load transient events are ultimately generated by one or more power FETs acting as a load. Metal oxide semiconductor field effect transistor (MOSFET) gates are capacitive and thus the signal must be properly buffered to be able to drive a capacitive load [1]. Having the input stage drive the capacitive load directly is not ideal. Larger currents are required, and stability becomes more of a concern as op-amps typically struggle to drive large capacitive loads directly; attempting to do so could result in loop oscillation [2]. This design supports multiple compensation options along with the option to install an isolation resistor. R2, the zero-Ω resistor just before the driver circuit, can be replaced with a 10Ω isolation resistor, or another value tuned for alternative compensation or driver configuration. The current driving capability of the preceding stage determines how large a FET can be driven. To drive larger capacitive loads, such as multiple larger FET gates, a driver stage is typically required. The driver buffers the input stage's output to drive higher loads.

The driver stage used in this board is a class AB push-pull amplifier, but its biasing is closer to a class-B. Class-AB amplifiers have high efficiency and minimal crossover distortion. This design's amplifier consists of two biasing resistors, two biasing diodes, and two Darlington pairs, in place of single bipolar junction transistors (BJTs). In class-AB configuration, the biasing resistors and diodes ensure that the BJT bases are biased such that they are right at the edge of conduction, when the input is at 0V [3]. Diodes can be stacked such that the sum of their forward voltages between the input node and the base of each transistor is approximately equal to the V_{BE} of the respective transistor for true class-AB operation. Application of Kirchhoff's Voltage Law

(KVL) around either the top half or the bottom half of the circuit indicates that if the diode drops match the overall base-to-emitter voltage, then the circuit's output voltage will match the input (with greater current drive capability). Only one half of the circuit is considered, as only one of the Darlington pairs will conduct, depending on whether the input signal is positive or negative. This concept is illustrated in diagram on the right in Figure 2-2, when $V_{in} > 0$.

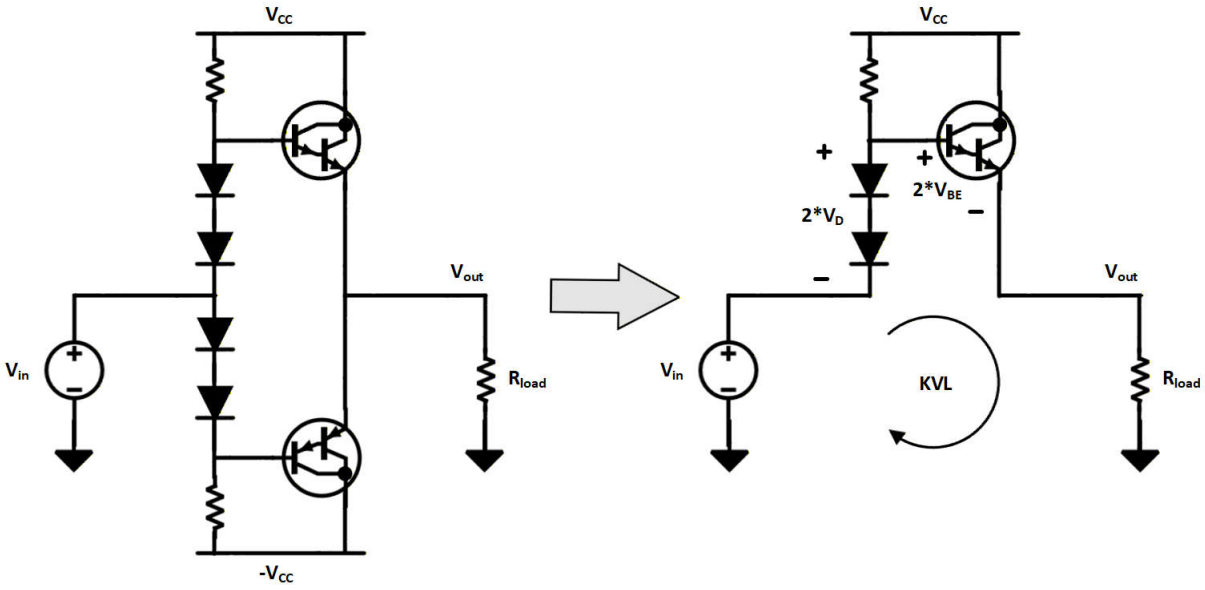

Figure 2-2. Driver Biasing

This design opts to bias the base of each Darlington pair at a voltage below its V_{BE}, to avoid the risk of operating as a class-A amplifier which is "always on" and to ensure that the Darlington pairs remain cool when no input is applied to the board. This design choice results in some latency in the actual transient response and is a trade-off that can be adjusted by changing the number of stacked diodes between the bases of the BJTs, or in this case, Darlington pairs. In an integrated circuit (IC), the diodes' forward voltage can be matched to the V_{BE} of the transistors over temperature, enabling thermal stability and minimizing any crossover distortion; however, this is difficult to achieve with discrete components.

Darlington pairs consist of two stacked BJTs where the emitter of the first BJT drives the base of the second. This results in the final overall emitter current being much higher than that of a regular BJT. The emitter current for a regular BJT is:

$$I_e = \left(h_{fe} + 1\right)^* I_b \tag{1}$$

For a Darlington pair, the emitter current is:

$$I_e = \left(h_{fe} + 1\right)^{2*} I_b \tag{2}$$

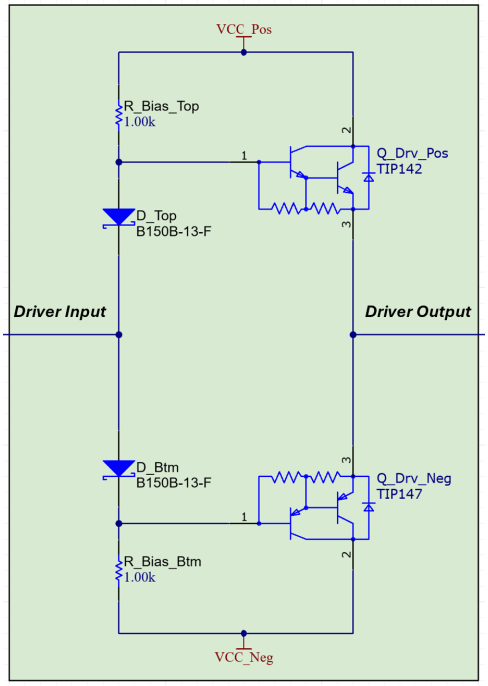

Figure 2-3. Driver Schematic

Note that the driver/buffer stage is only required when the gate capacitance of the load transistor is larger than what the input stage's op-amp can drive. Removing or bypassing this stage could simplify the design, and aid in achieving faster load transients, as the driver bandwidth is finite and contributes to the overall response of the system.

2.3 Output Stage

The output stage consists of the load-transient FET, a series gate resistor, and a 1mΩ ballast resistor. The schematic is shown in Figure 2-4. The input stage passes a control signal to the driver stage where it is buffered and then used to drive the load FET. The profile of the input signal, V_{in}, dictates the profile of the load transient event. The series resistor at the gate of the FET limits the gate voltage's slew rate and improves circuit stability [4]. The ballast resistor ensures current sharing is roughly equal when multiple FETs are used in parallel. For example, if the V_{th} of one FET is lower than the others, it will conduct more current. The resulting voltage across the ballast resistor reduces the gate overdrive voltage of that FET, thereby reducing its current and improving current sharing among the parallel FETs. This board supports paralleling output stages via the right-angle connectors on the right side of the board. Each output stage would include its respective gate resistor, load transistor, and ballast resistor.

The board layout is such that the board itself may be soldered onto the output capacitor bank of a power converter to minimize inductance (DUT output on the PCB top layer, and GND on bottom layer). This short connection reduces the interface impedance and allows for faster transients.

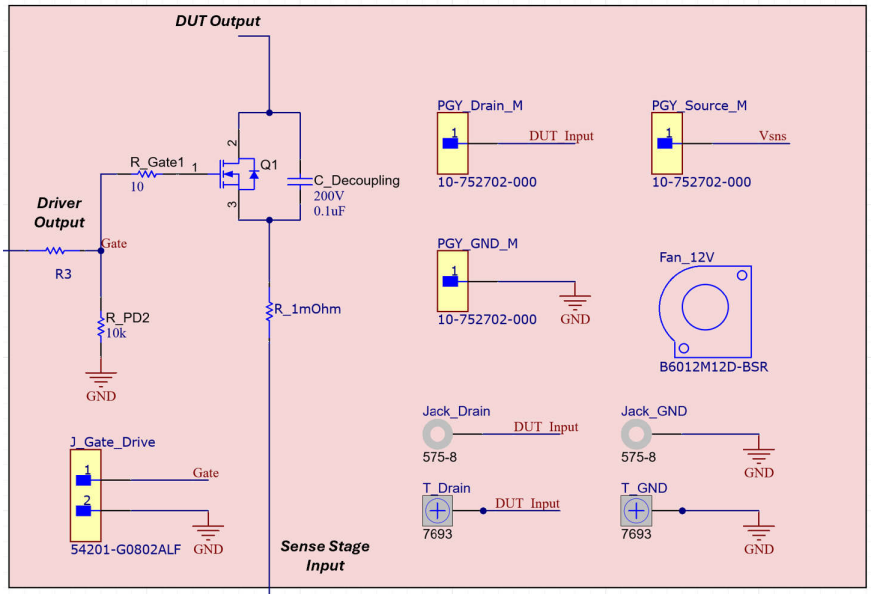

Figure 2-4. Output Stage Schematic

2.4 Sense Stage

To control the load current, it must be measured. The sense stage consists of a 4-terminal current sense resistor (for Kelvin sensing), a filter, and an op-amp configured as a difference amplifier. This allows for analog sensing of very small voltages that can then be amplified and fed back into the input stage's negative input node to close the negative feedback loop. This stage sets the voltage-to-current gain. For example, if 500mV is applied at the input, then the feedback loop will ensure 500mV is applied across the 50mΩ sense resistor, assuming the difference amplifier gain is set to 1. This means that a 500mV input to the board will result in a 10A load. If the difference amplifier has a gain higher than 1, then the voltage-to-current gain will be divided by that factor, e.g., in this design the gain is set to 2, meaning the 500mV input would result in a 5A load (I_{load}/V_{in} = 1A/100mV). This is because the op-amp drives the output to equalize its input terminals; therefore, the negative terminal reaches 500mV only when the voltage across the sense resistor is equal to the 500mV level divided by the gain (2) of the sense stage. The filter can be adjusted to ensure it does not slow down the sense signal too much, while keeping the sense signal free of noise and high-frequency content beyond the op-amp bandwidth.

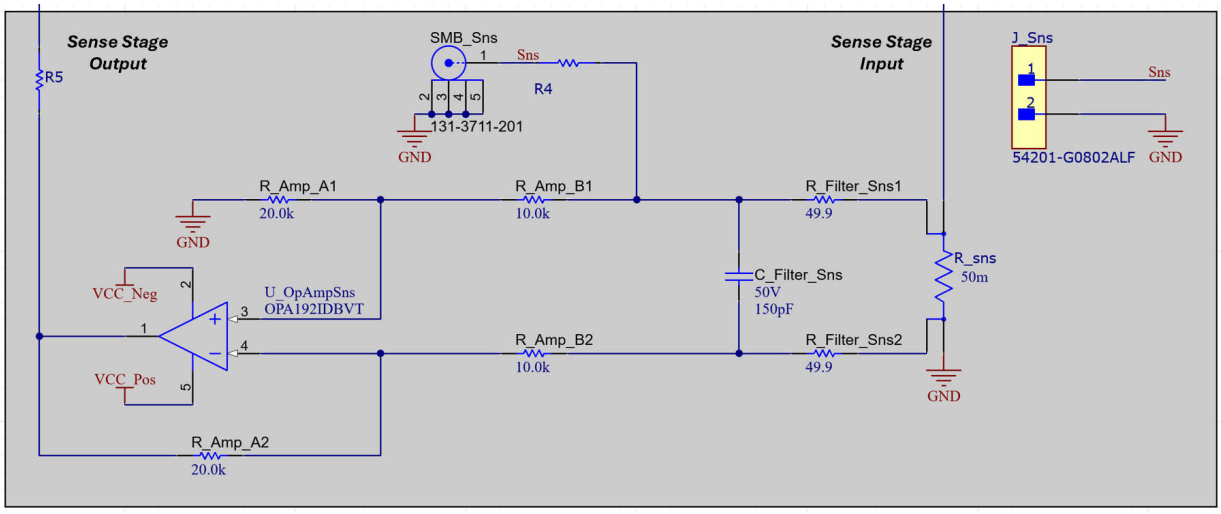

Figure 2-5. Sense Stage Schematic

2.5 Power

This design incorporates various active devices that consume power. Op-amps typically require a positive rail to source current and a negative rail to sink current. The design uses two identical op-amps. It also includes a driver that requires a positive and a negative rail. The wide-rail options on these devices allow for a ±12V rail. The +12V rail is also used to power the fan used to cool the driver and output stages. To generate these rails, the LM67680 is used in standard and inverting buck-boost (IBB) configurations. Most buck converters can be converted to an IBB configuration by grounding the output and using the device's GND as a negative rail [5]. This setup introduces some complications, as the internal logic becomes referenced to the negative rail, and for signals such as EN that are referenced to GND, level shifters are normally used. This design simply has EN tied to V_{in}. The recommended input voltage for the board is 18V, which puts the EN voltage at 18 - (-12) = 30V, which is within the LM67680's EN pin voltage rating; this design does not require the integrated level shifters. The LM67680 current limit is sufficient to meet the current requirements of the driver stage. This buck converter has a wide input voltage rating and can easily support an input of 18V to 24V, the recommended input voltage range for this design. The recommended input current for this closed-loop transient board is 2A, which includes headroom.

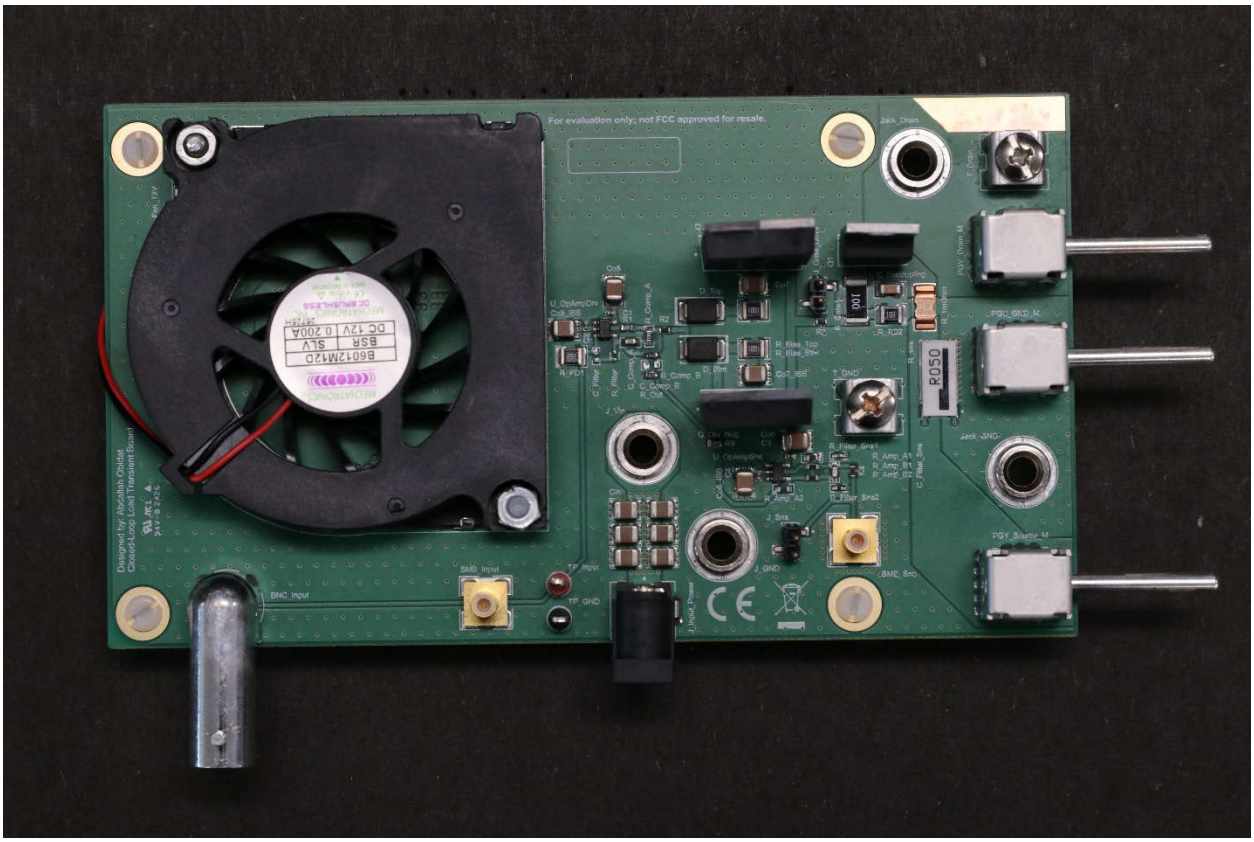

Figure 2-6. Assembled PCB

3 System Design

System designs typically begin with their specifications. These specifications impose restrictions that guide the rest of the design.

Table 3-1. Design Specifications

Specification Name	Specification Value
Max Load	30A @ 5V
Target Slew Rate	1A/µs @ 10A
Max DUT Voltage Supported	80V
Min Voltage Supported	Load Dependent

The maximum load derates based on the output voltage of the device-under-test (DUT), which is the voltage applied to the drain of the load FET as shown in Figure 3-1. This derating is a result of Ohm's law; the load current results in an IR drop across the transistor $R_{ds(on)}$ (when hot ~4mΩ), the ballast resistor (1mΩ), and the current sense resistor (50mΩ). The equation relating the minimum DUT voltage to the maximum applicable load current is:

$$V_{DUT\_Min} = Load^{*}\left(R_{ds(on)} + R_{Ballast} + R_{Current\_Sense}\right) \quad (3)$$

The previous equation does not consider the resistance of any interconnects between the board and the DUT, nor the resistance of the PCB traces. Note that the applied conditions must comply with the FET safe operating area (SOA).

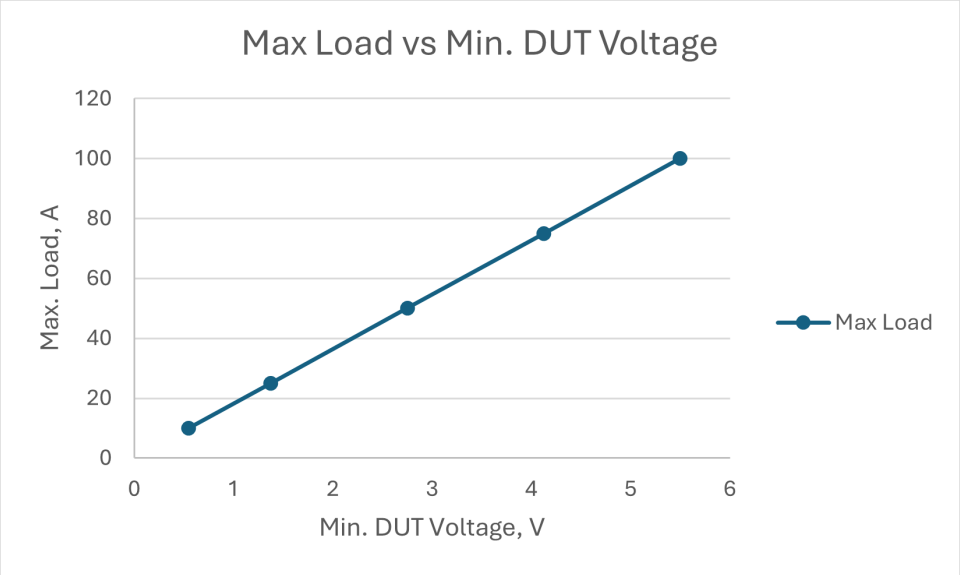

Figure 3-1. Load Derating Over DUT Voltage

The MOSFET simulates the transient load and is arguably the most important component in the system. The CSD19536KCS is a 100V-rated MOSFET that can sustain a continuous current of 150A with adequate cooling [6]. This MOSFET has a low Q_g, making it easier to drive, and its larger package enables the installation of a heatsink. Next, a 1mΩ resistor acts as a ballast resistor and ensures that if multiple FETs are used in parallel to enable higher loads, the FETs will exhibit improved load sharing. The board's connectors allow for this via a secondary PCB with mating connections. Finally, a 50mΩ resistor is used as a current shunt to enable a Kelvin measurement of the voltage that represents the load current.

By selecting the MOSFET, its total gate charge and target rise time can be used to determine the average gate current the driver must supply:

$$I_{gate\_avg} = \frac{Q_{gate}}{t_{rise}} \rightarrow \frac{118nC}{1\mu s} \rightarrow 0.118A \quad (4)$$

A gate resistor is typically installed to limit oscillations. At a 10V drive voltage:

$$I_{peak} = \frac{V_{drive}}{\left(R_{gate} + R_{drive}\right)} \rightarrow \sim\frac{V_{drive}}{R_{gate}} \rightarrow \frac{10V}{(10\Omega)} = 1A \quad (5)$$

The overall current peak requirement for the driver is thus ~1.2A per load stage, including headroom and margin. Lower gate drive voltage lowers the I_{peak} but increase the rise time. The feedback loop will generate the appropriate drive to verify the load profile matches the input voltage profile. In practice, the achieved rise time is governed by the closed-loop bandwidth, the inductance of the connection to the DUT, and the deadband introduced by the sub-V_{BE} driver biasing.

These values set the requirements for the driver stage that precedes the output stage. The driver must supply a 10V drive and provide at least 1.2 A peak current per power stage. The driver stage's transistors along with the target output current enable the calculation of the required input base current. The base current can be back-calculated from the expected emitter current.

$$I_b = \frac{I_e}{\left(h_{fe} + 1\right)} \rightarrow \frac{1.2A}{1001} \approx 1.2\text{mA} \quad (6)$$

The driver stage buffers its input signal and increases its current drive capability. To drive the gate of the subsequent power stage to 10V, the rails of the driver stage need to be higher than that to provide the driver with the required headroom. This design uses ±12V rails to verify that there is always at least 2V of headroom, which is a margin of 20%. The output stage will typically include BJTs that have a high h_{fe} (current gain). The instantaneous power is equal to the peak power consumed by the BJT, given a simple load pulse. The power can be calculated as follows:

$$P_{peak} = (V_{CE}{}^*I_C) + (V_{BE}{}^*I_B) \rightarrow at I_B = 1.2mA \quad (7)$$

$$P_{peak} = \left(V_{rail} - V_{gate\_target}\right)^*I_{peak} + (V_{BE}{}^*I_B) \quad (8)$$

$$P_{peak} = \left(12 - 10\right)^*\left(1.2\right) + \left(3^*0.0012\right) \approx 2.4\text{W} \quad (9)$$

Note that the power consumed due to the base current is insignificant, despite the large max V_{BE} for the Darlington pairs.

If the desired load is periodic, then the average power can be calculated according to:

$$P_{avg} = Q_g{}^*V_{rail}{}^*f_{\text{max\_rep\_rate}} \quad (10)$$

$$P_{avg} = 118nC^*12V^*10kHz = 14.2mW \quad (11)$$

This average power includes the loss in the BJT and the energy consumed as heat in R_{gate}. The value is independent of the actual value for R_{gate}; if R_{gate} is low, then there is higher power consumption for a shorter duration; similarly, if R_{gate} is high, then there is lower power consumption for a longer duration. The value of R_{gate} impacts drive speed and stability.

The selected NPN and PNP transistors need to be able to drive the peak current, at the rail voltage. Many transistor datasheets include a safe operating area graph that could be consulted to verify that the transistor can drive the required current at the given rail voltage (V_{CE}). The TIP142, TIP147 devices are complementary NPN and PNP Darlington pairs. They have a high h_{fe} of greater than 1000 that enables large drive currents with smaller base currents. Both devices are rated for 125W at T_{case} of 25°C, up to 10A, and have a breakdown voltage of 100V, making them robust choices for the output stage. Their large size and low 1°C/W thermal resistance (junction-to-case) enable easier cooling and thermal management.

To bias the driver stage, two resistors and two diodes are used. Each of these diodes has a forward drop of about 0.5V. The bias current is ideally much larger than the actual base current needed to drive the transistors. KVL around the bias branch of the circuit shows the relationship between the bias resistors and the bias current:

$$I_{bias} \approx 10{*}I_{base} = 12mA \tag{12}$$

$$KVL \rightarrow -V_{CC} + (R_{bias}{*}I_{bias}) + V_D + V_D + (R_{bias}{*}I_{bias}) + V_{EE} = 0 \tag{13}$$

$$R_{bias} = \frac{(V_{CC} - V_{EE} - 2V_D)}{2I_{bias}} \tag{14}$$

$$R_{bias} = \frac{(12 - (-12) - (2{*}0.5))}{2{*}0.012} \approx 1\text{k}\Omega \tag{15}$$

The input stage must be able to drive both the driver stage's bias current and transistor base current. When the driver is at its maximum voltage, the bias current through each R_{bias} resistor drops significantly, and the op-amp must supply the difference. This imposes limits on the op-amp drive current and the resistor values. Under these conditions:

$$I_{bias} = \frac{(V_{rail} - V_{drive})}{R_{bias}} = 2mA \tag{16}$$

Under these maximum drive conditions, the op-amp now must supply the full bias current and the base current for the transistors, which the OPA192 can provide given its relatively high 65mA drive capability. It also must support the required voltage rail and input/output requirements. The OPA192 is a 36-V rail-to-rail op-amp. It can support the ±12V rails and can support 10V inputs. It has a low offset voltage of ±5µV [7]. This op-amp has a gain bandwidth product of 10MHz and a slew rate of 20V/µs, both sufficient to support the 1A/µs transient specification.

To eliminate high-frequency oscillations in the overall loop output, a high-frequency bypass RC network lowers the impedance between the positive and negative input terminals of the op-amp at the input stage. At DC and lower frequencies, the capacitor has a large impedance and does not interfere with regular operation; however, if high-frequency oscillations were to occur, the capacitor's impedance would be much lower, effectively creating a low-impedance path between the op-amp inputs, preventing the amplification of the oscillations, thus suppressing them. This minimum impedance value is controlled by the resistor R, which is set to 1kΩ. A 220pF capacitor's reactance would equate to 145Ω at high frequency, for example, 5MHz, thus resulting in an overall network impedance of 1.01kΩ.

$$Z_{filter} = \sqrt{\left(R^2 + \frac{1}{2{*}\pi{*}f{*}C}^2\right)} \tag{17}$$

$$Z_{filter} = \sqrt{\left(1000^2 + \frac{1}{2{*}\pi{*}\left(5{*}10^6\right){*}\left(220{*}10^{-12}\right)}^2\right)} = 1.01\text{k}\Omega \tag{18}$$

4 Stability

This design utilizes negative feedback and therefore is not verified to be stable without compensation. Stability means that there is adequate gain and phase margin. Phase margin is how far the phase is from -180° and is determined by measuring the phase when the gain is equal to 0dB. If the phase shift is equal to or larger than 180°, then the signal phase has inverted, and positive feedback will cause instability. There is a trade-off between speed and stability, and the faster the loop is, the closer it tends to instability. Gain margin is how far the gain is from 0dB at a phase of -180° and is determined by measuring the loop gain magnitude once the phase has lagged by 180°. If the gain is higher than 0dB, then there is negative gain margin, and positive feedback is present in the loop; the loop will not stabilize. If the gain margin is positive and the gain is less than 0dB at a phase shift of 180°, then the loop is theoretically stable.

Several resistors and capacitors are used following the input op-amp to compensate the control loop and verify system stability. There is a larger resistor from the output to the negative input, to verify that at DC the circuit behaves like a voltage follower when a DC voltage is applied to the positive input. A high-frequency capacitor filters high-frequency content to the negative input terminal, so that the loop does not attempt to respond to signals beyond the bandwidth. Finally, the series RC provides compensation by generating a pole and zero. To determine the overall transfer function, the impedance can be calculated and then put into standard form. The selected R and C values can be selected based on the desired poles and zeros to verify an adequate crossover frequency and phase margin.

General rules of thumb when considering the placement of poles and zeros are shown in Figure 4-1 and the bullets below [8]:

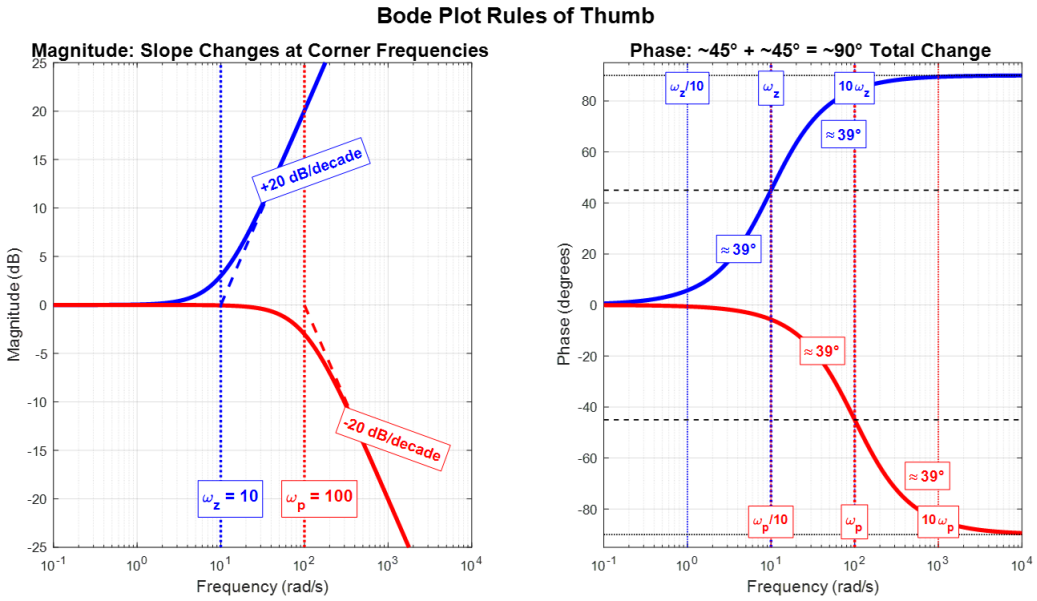

Figure 4-1. Bode Plot Rules of Thumb

- At the zero frequency, the magnitude begins to increase by 20dB/decade
- The phase will increase by approximately 45° between a tenth of the zero frequency and the zero frequency
- The phase will further increase by approximately 45° between the zero frequency and ten times the zero frequency
- At the pole frequency, the magnitude begins to decline by 20dB/decade
- The phase will decrease by approximately 45° between a tenth of the pole frequency and the pole frequency
- The phase will further decrease by approximately 45° between the pole frequency and ten times the pole frequency

Compensating the loop introduces poles and zeros to verify that the system has adequate phase and gain margins. To determine how to compensate the system, an expression for its transfer function is required. A simple negative feedback loop diagram is shown in Figure 4-2:

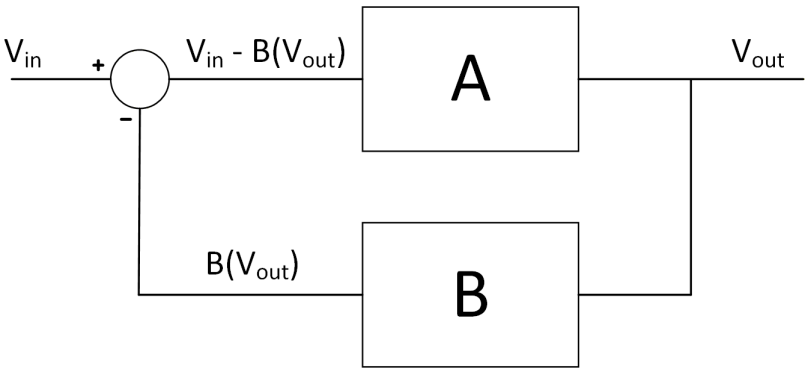

Figure 4-2. Negative Feedback Control Loop Diagram

In the diagram above, the open-loop gain A and the feedback factor B are used to regulate V_{out}.

$$V_{out} = A^*(V_{in} - B^*V_{out}) \quad (19)$$

$$V_{out} = (AV_{in} - ABV_{out}) \quad (20)$$

$$AV_{in} = V_{out} + ABV_{out} \quad (21)$$

$$AV_{in} = V_{out}^*(1 + AB) \quad (22)$$

$$\frac{V_{out}}{V_{in}} = \frac{A}{(1 + AB)} \rightarrow \text{Transfer Function} \quad (23)$$

The relationship between V_{out} and V_{in} is referred to as the transfer function, where AB is the loop gain. From the equation, it is clear that the system gain is reduced significantly when negative feedback is applied. By breaking the loop at a junction by the output where there is low impedance looking in one direction, and high impedance looking in the other, one may analyze the loop via a Bode plot. This injection point is typically where a Bode plot can be measured [9]. Figure 4-3 shows how the loop can be broken and a small signal injected to determine the loop gain directly:

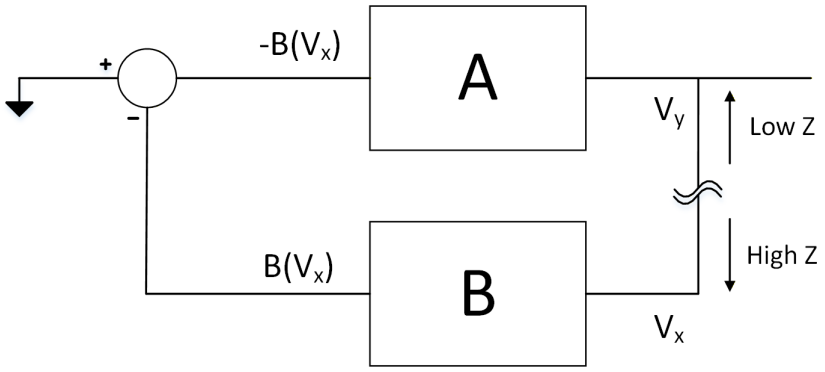

Figure 4-3. General AC Loop Analysis

Starting from V_x, the loop gain can be determined by following V_x's path until it reaches V_y, and the ratio $-V_y/V_x$ is equal to the loop gain. Note that in any AC analysis, ideal voltage sources, such as V_{in}, are low-impedance and are shorted to GND.

$$V_y = A^*\left(0 - B^*V_x\right) \quad (24)$$

$$AB = -\left(\frac{V_y}{V_x}\right) \quad (25)$$

The result above agrees with the transfer function derivation for a simple closed-loop with negative feedback. Using a similar method, the transfer function for the load transient board can be derived:

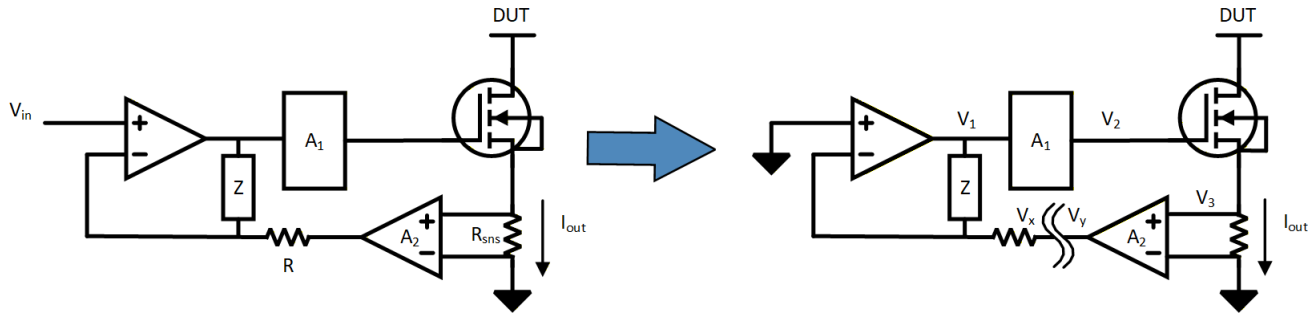

Figure 4-4. Loop Analysis of Closed-Loop Load Transient Board

After breaking the loop and shorting Vin to GND (AC analysis), V_x, as an input to the first op-amp, appears as an input to an inverting amplifier. A_1 is a buffer and has a gain of 1; therefore, $V_1 = V_2$. Since the transistor is connected in a source follower configuration from its gate to source, the gain is $g_m*(R_{sns})/((g_m*R_{sns})+1)$ with $g_m*R_{sns} >> 1$. The transconductance g_m, or g_{fs} can be determined using the I_{DS} vs V_{gs} curve from the datasheet and applying the formula $\Delta I_D/ \Delta V_{gs}$, but for the CSD19536KCS FET it is explicitly provided in the datasheet characteristics table: 307 S. Since $g_m*R_{sns} >> 1$, the transistor's AC gain is also ≈1 and $V_3 = V_2 = V_1$. Finally, the gain of A_2 is set to 2. From this, the loop gain is:

$$V_1 = -V_x*\left(\frac{Z}{R}\right) \tag{26}$$

$$V_2 = V_1*A_1 \tag{27}$$

$$V_3 = V_2*\frac{(g_m*R_{sns})}{(g_m*R_{sns}+1)} \tag{28}$$

$$V_y = V_3*A_2 \tag{29}$$

$$\frac{V_Y}{V_x} = -\left(\frac{Z}{R}\right)*A_1*\left(\frac{g_m*R_{sns}}{g_m*R_{sns}+1}\right)*A_2 \tag{30}$$

$$-\left(\frac{V_y}{V_x}\right) = 2*\left(\frac{Z}{R}\right) \tag{31}$$

$$\text{The Overall Transfer Function} \rightarrow \frac{\left(\frac{2Z}{R}\right)}{1+\left(\frac{2Z}{R}\right)} \tag{32}$$

This transfer function is a function of Z and R. For this design, R was fixed at 1kΩ. The impedance network Z in this design allows for a resistor in parallel with a capacitor that is also in parallel with a series RC. The overall compensation network topology Z is as follows:

$$Z = R_{out} \parallel C_{HF} \parallel \left(R_{comp} + C_{comp}\right) \tag{33}$$

The function is most complex when all components are present. Given $R_{out} >> R_{comp}$ (ratio 100x), and C_{HF} is not utilized in this design, the locations of the poles can be approximated as shown in Table 4-1 (note that the zero is exact and not approximated):

Table 4-1. Pole and Zero Calculations

Root	Type	Expression	Value
f_z	Zero	$1/(2*\pi*R_{comp}*C_{comp})$	~72kHz
f_p	Pole	$1/(2*\pi*(R_{out}+R_{comp})*C_{comp})$	~720Hz

Intuitively, R_out presents a finite impedance at DC and low frequency; without it, the circuit would see an infinite impedance and the input stage's op-amp would saturate when no DUT is connected. The series RC provides a pole at low frequency whose roll-off is arrested by the zero at a higher frequency. The zero helps stabilize the loop. The global R (R_Comp_B = 1kΩ) is a scaling factor that impacts the entire magnitude curve of the closed-loop gain, and as such allows tuning the location of the crossover frequency. The overall result with this configuration is very stable with a phase margin of ~80° as demonstrated by the Bode plot in Figure 4-5. The gain/phase plot was taken in the same location where the loop was broken in Figure 4-4 using a 10Ω injection resistor at the output of the sense stage, in place of R5. The connected DUT was set to 5V and the load was set to a constant 10A by setting the input to 1V. Note that active cooling was required to sustain a constant DC load while measuring the Bode plot, which takes several seconds to complete.

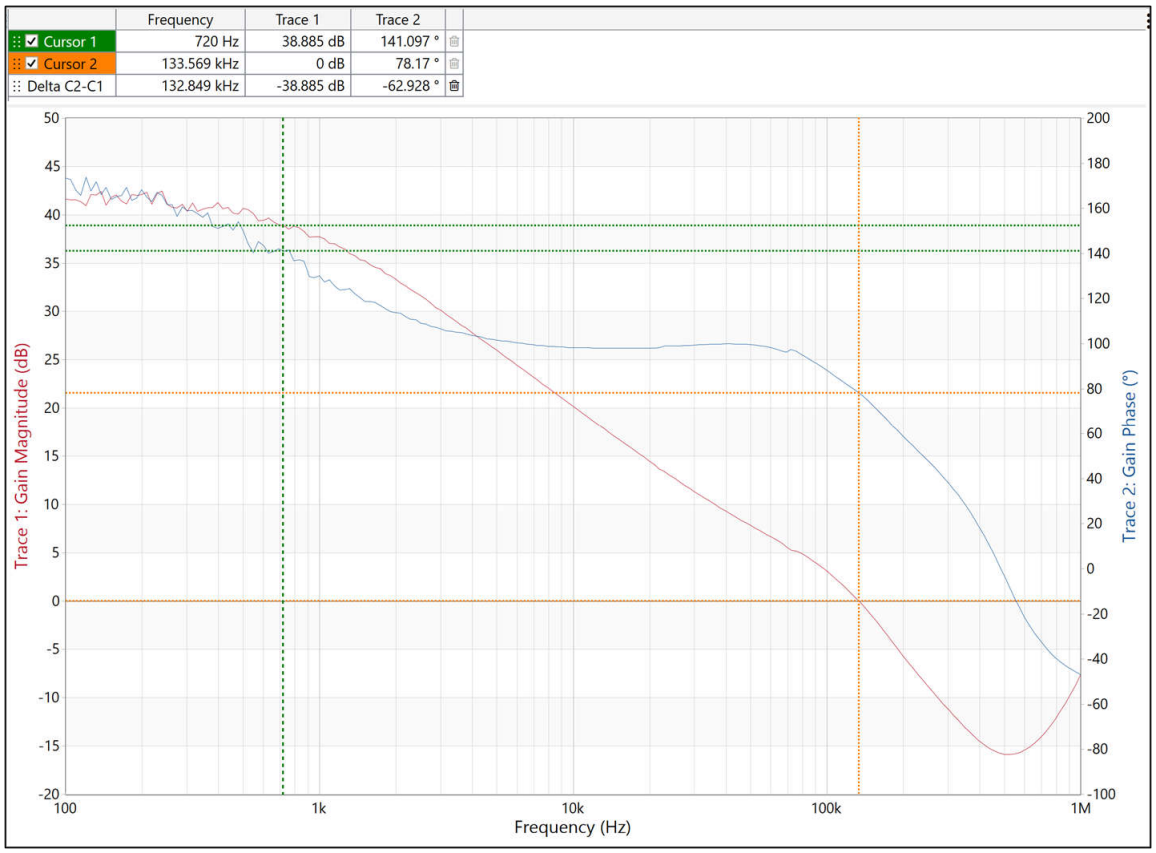

Figure 4-5. Closed-Loop Load Transient Board Bode Plot (I_{load}: 10A, DC)

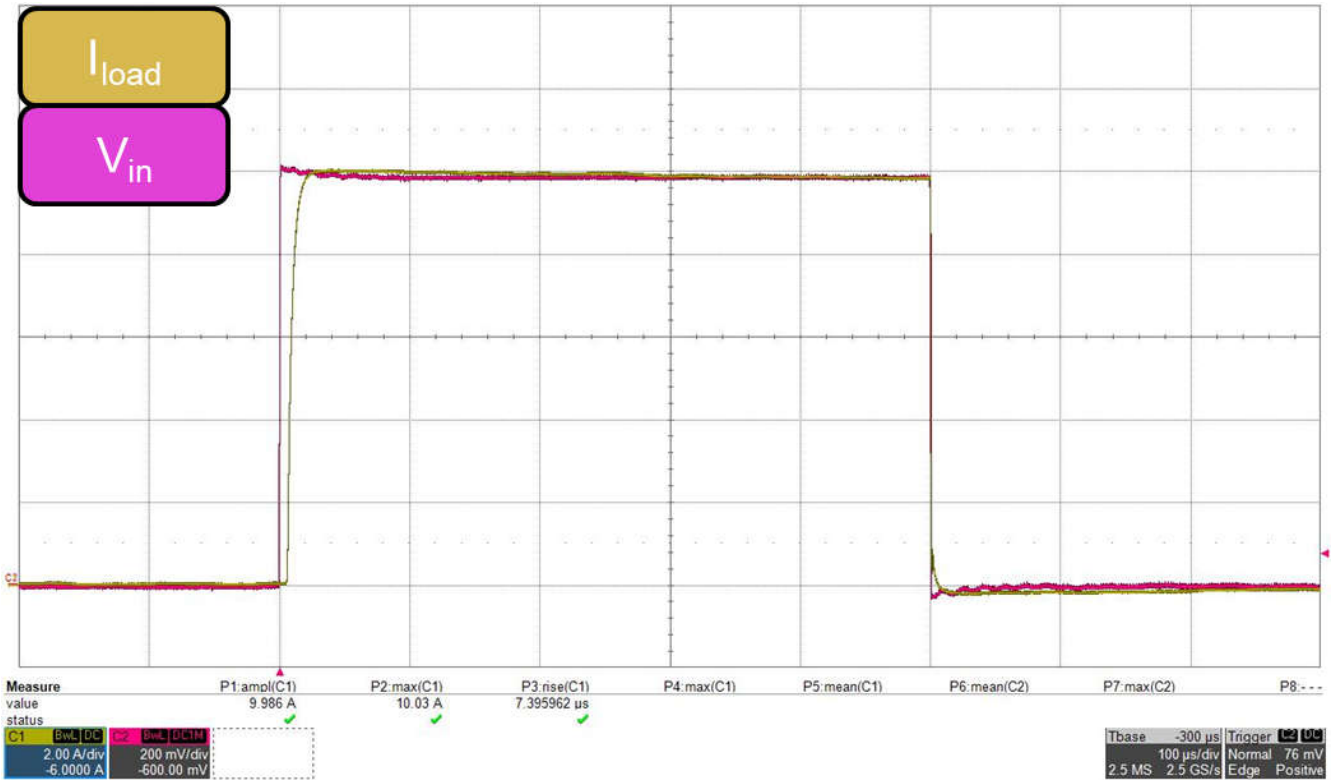

Figure 4-6. Transient Pulse Performance (I_{load}: 10A, 0.5ms)

5 Results

Benchmarking the device with a DUT shows that the tracking error peaks at lower loads, as expected, but is significantly reduced at higher loads. The primary cause of this is the offset that the R_out resistor introduces. Some current flows from the output of the input stage's op-amp across the resistor, instead of all of the current flowing from the sense stage's op-amp. This offset diminishes at higher load currents, as the sense stage op-amp provides more drive. The class-B biasing of the driver reduces power dissipation when no input is applied but also results in a nonlinear soft-start behavior that increases rise times. This effect is more pronounced at lower load currents, where the deadband time represents a larger fraction of the total transition. The results were limited to 30A, as this is a common rating for standard current probes, but the board is capable of driving higher currents. Results were benchmarked with a 5V DUT using short cables and the banana jack connectors. Faster rise times can be achieved by soldering the board to the DUT output capacitor bank; the top right corner of the board exposes the copper for the DUT connection (Top Layer) and GND (Bottom Layer) points for this purpose. The following results were achieved with a 500µs pulse and 1µs rise and fall time input with a swept amplitude (V_{in}).

Table 5-1. Closed-Loop Load Transient Board Benchmark Measurements

V_{in}, V	I_{out}, A	Expected I_{out}, A	Error, %	Slew, A/ µs	t_{rise}, 10% to 90%
0.10	0.75	1	25.00	0.03	23.10
0.20	1.64	2	18.15	0.10	13.24
0.30	2.67	3	11.01	0.20	10.57
0.40	3.69	4	7.65	0.32	9.38
0.50	4.73	5	5.40	0.43	8.70
0.60	5.81	6	3.11	0.57	8.12
0.70	6.79	7	3.00	0.69	7.90
0.80	7.82	8	2.21	0.80	7.81
0.90	8.87	9	1.39	0.94	7.52
1.00	9.88	10	1.18	1.07	7.40
1.50	15.18	15	1.17	1.74	6.98
2.00	20.25	20	1.25	2.41	6.71
2.50	25.46	25	1.84	4.03	5.06
3.00	30.67	30	2.25	3.91	6.28

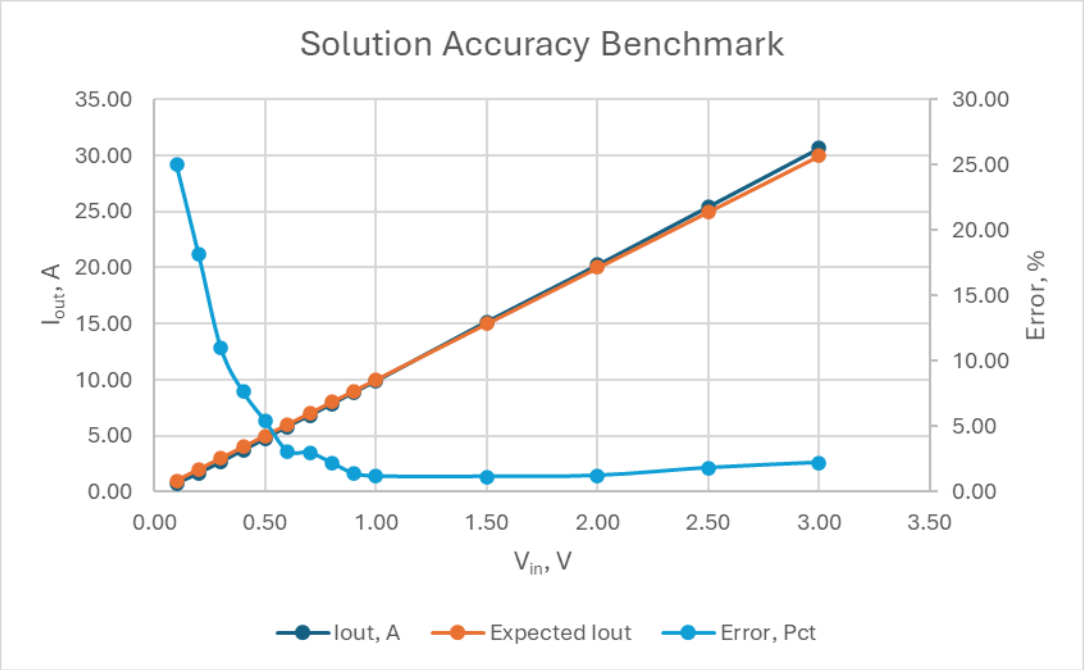

Figure 5-1. Closed-Loop Load Transient Board Benchmark Results

In addition to benchmarking pulse transient performance, various input profiles were applied to observe the corresponding load profiles. One notable aspect was that the output current was distorted near 0A, as a result of the aforementioned driver biasing scheme.

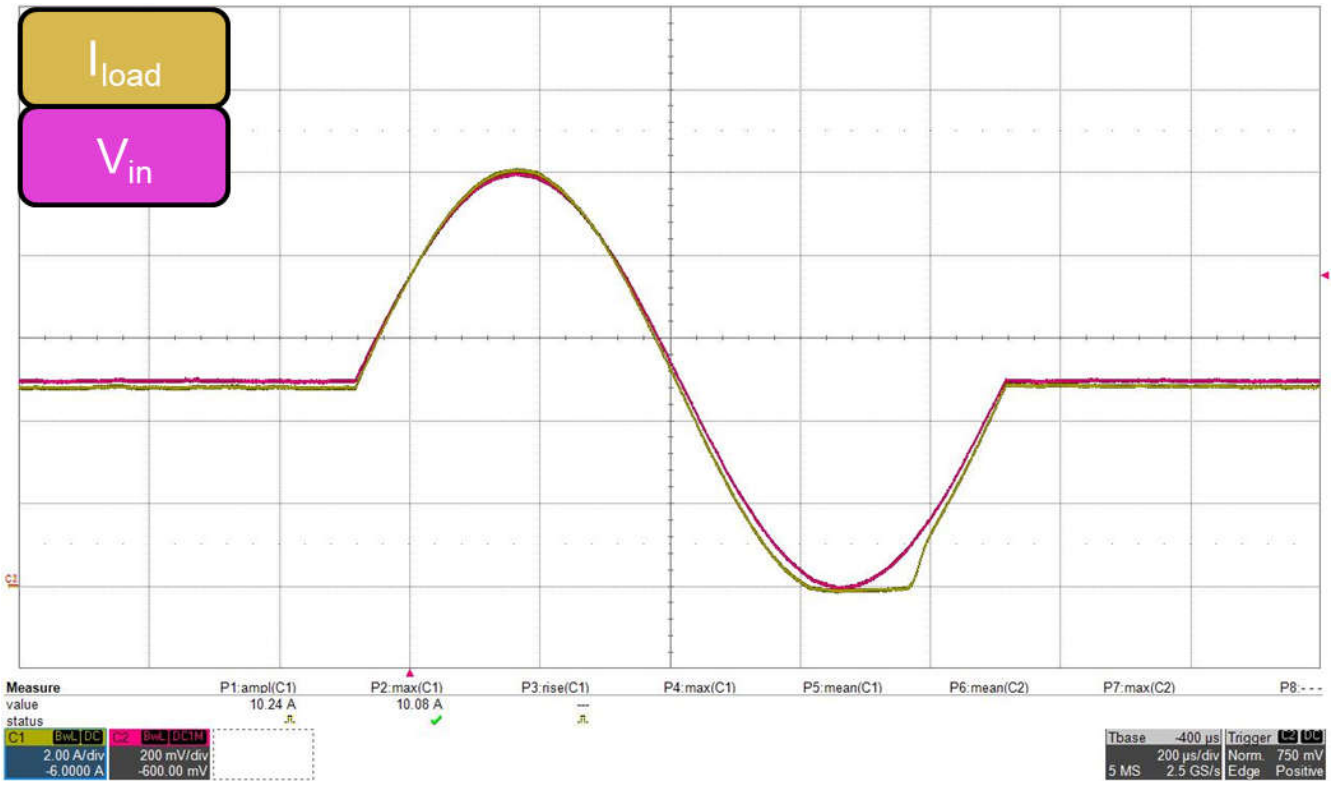

Figure 5-2. Sinewave Tracking

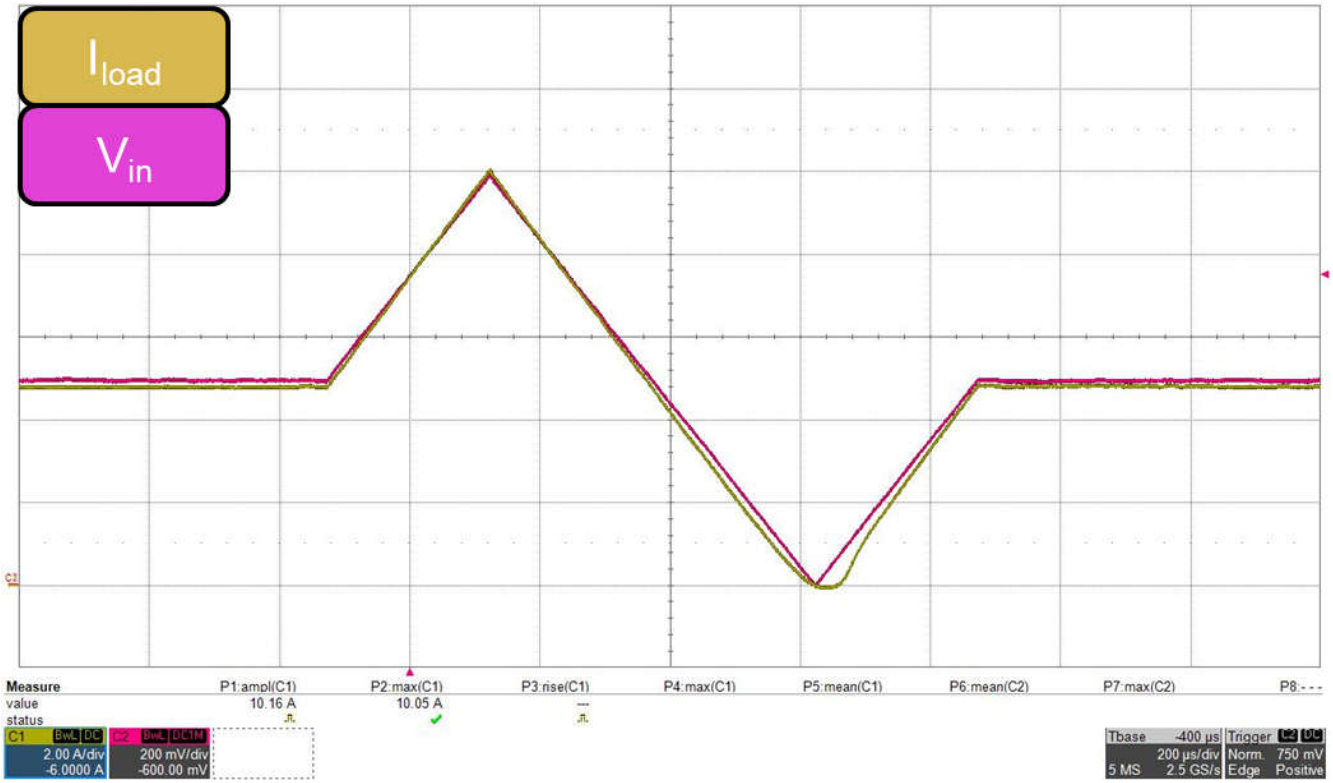

Figure 5-3. Ramp Tracking

6 Summary

In summary, this application note describes the process of designing a practical closed-loop load transient board. This design enables effective load transient testing of power converters. Alternative solutions such as applying a transient pulse via a power transistor without a feedback loop require some level of calibration between the applied gate voltage and the target output current, whereas this solution enables the application of a target current directly without the need for such calibration. The design is easily modified to satisfy different requirements, that is, the sense resistor can be changed to a much smaller value to get a larger input-voltage-to-load-current ratio or the biasing can be changed to reduce or eliminate the deadband and achieve faster rise times. This solution also allows engineers to easily apply complex load profiles to suit custom applications.

7 Appendix

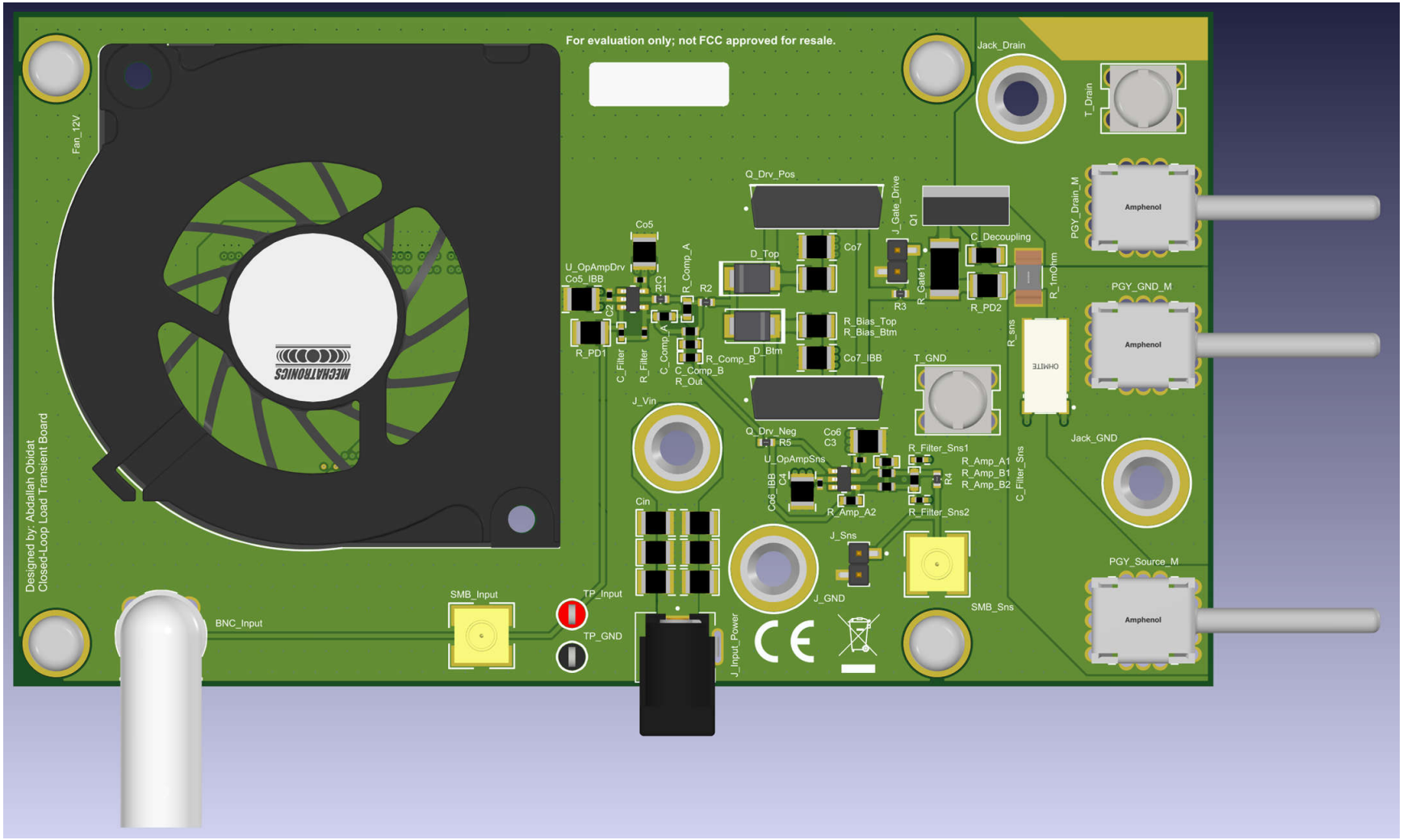

Figure 7-1. Board Render (Top)

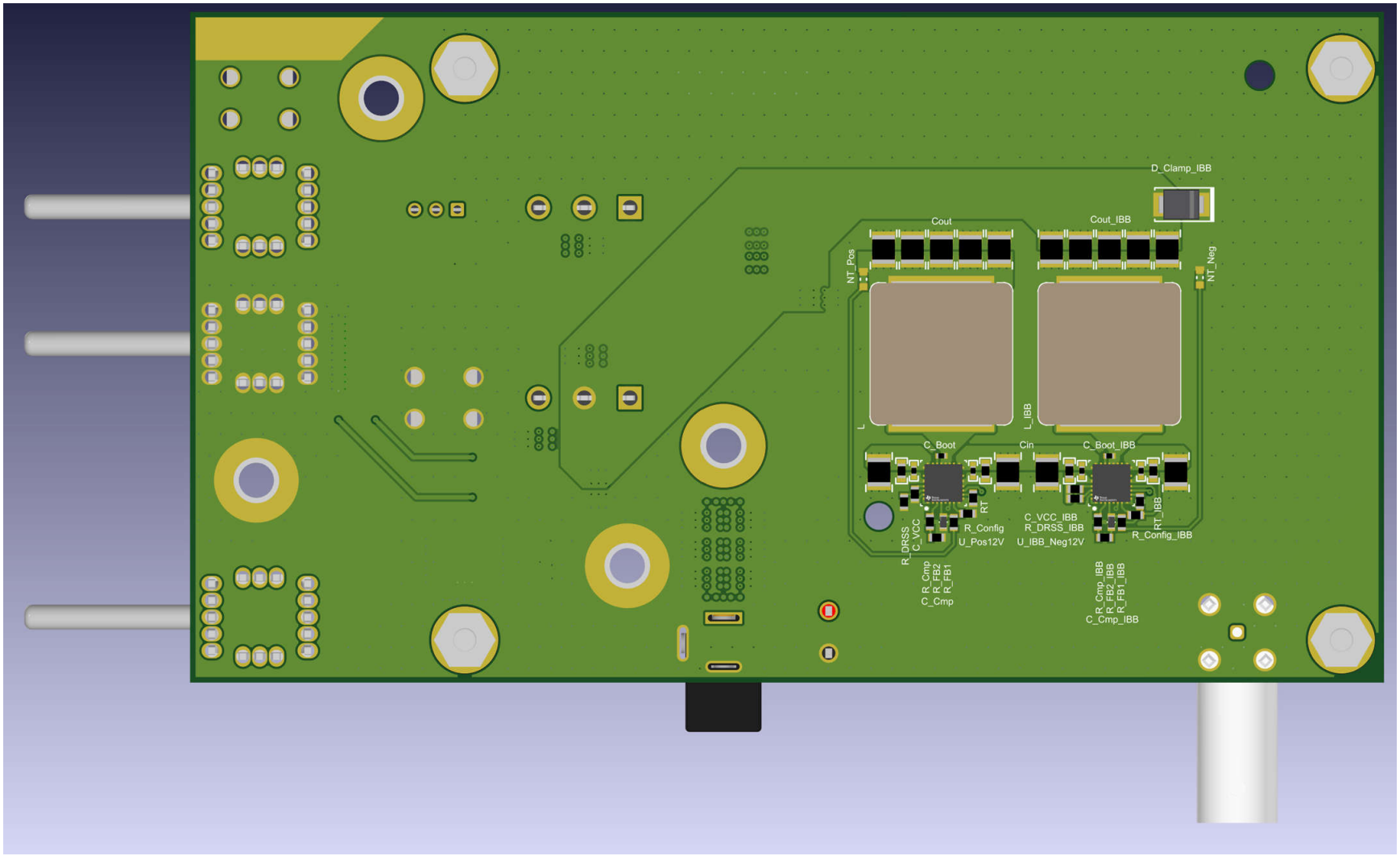

Figure 7-2. Board Render (Btm)

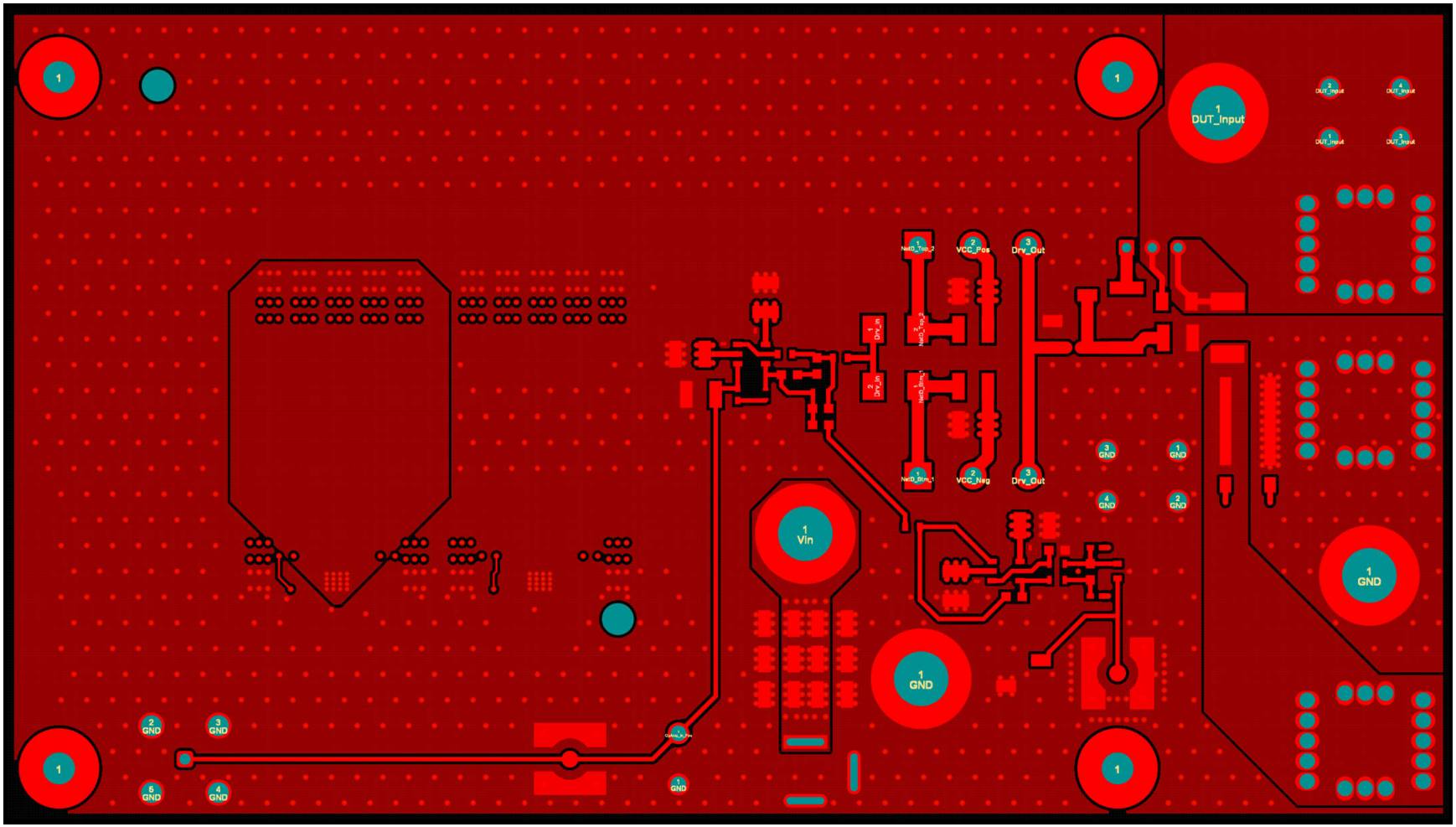

Figure 7-3. Layout - Top Layer

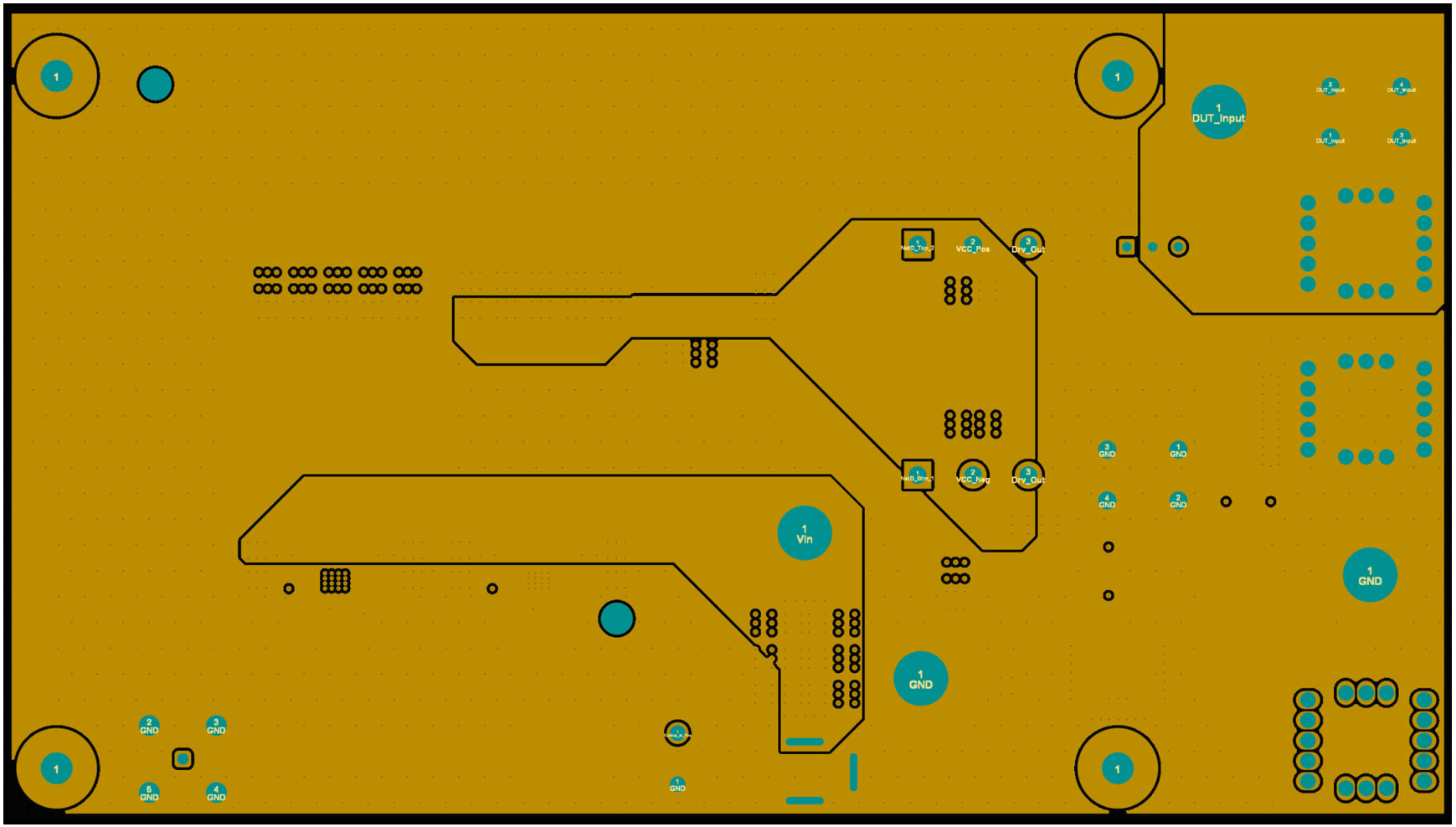

Figure 7-4. Layout - Mid Layer 1

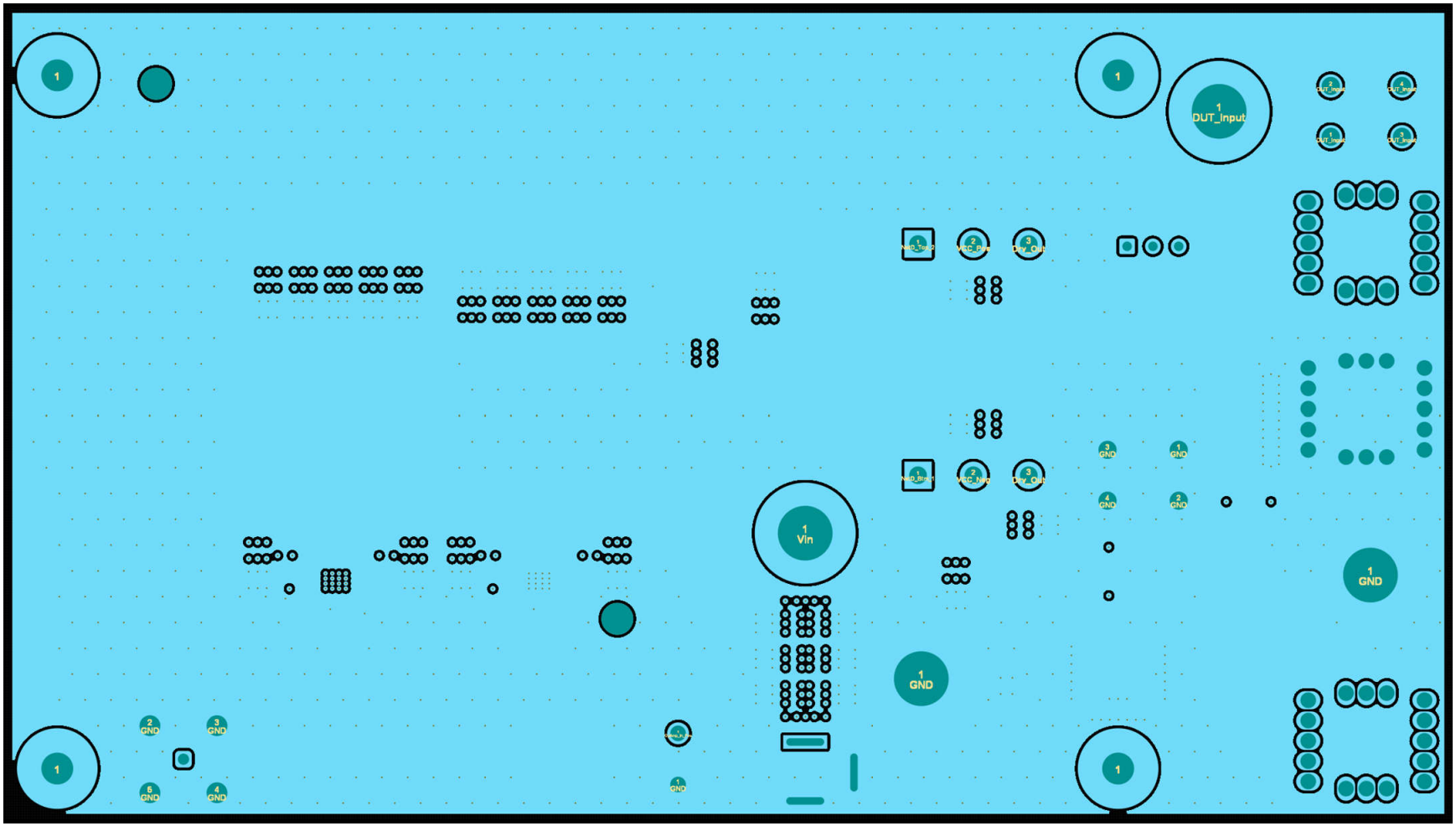

Figure 7-5. Layout - Mid Layer 2

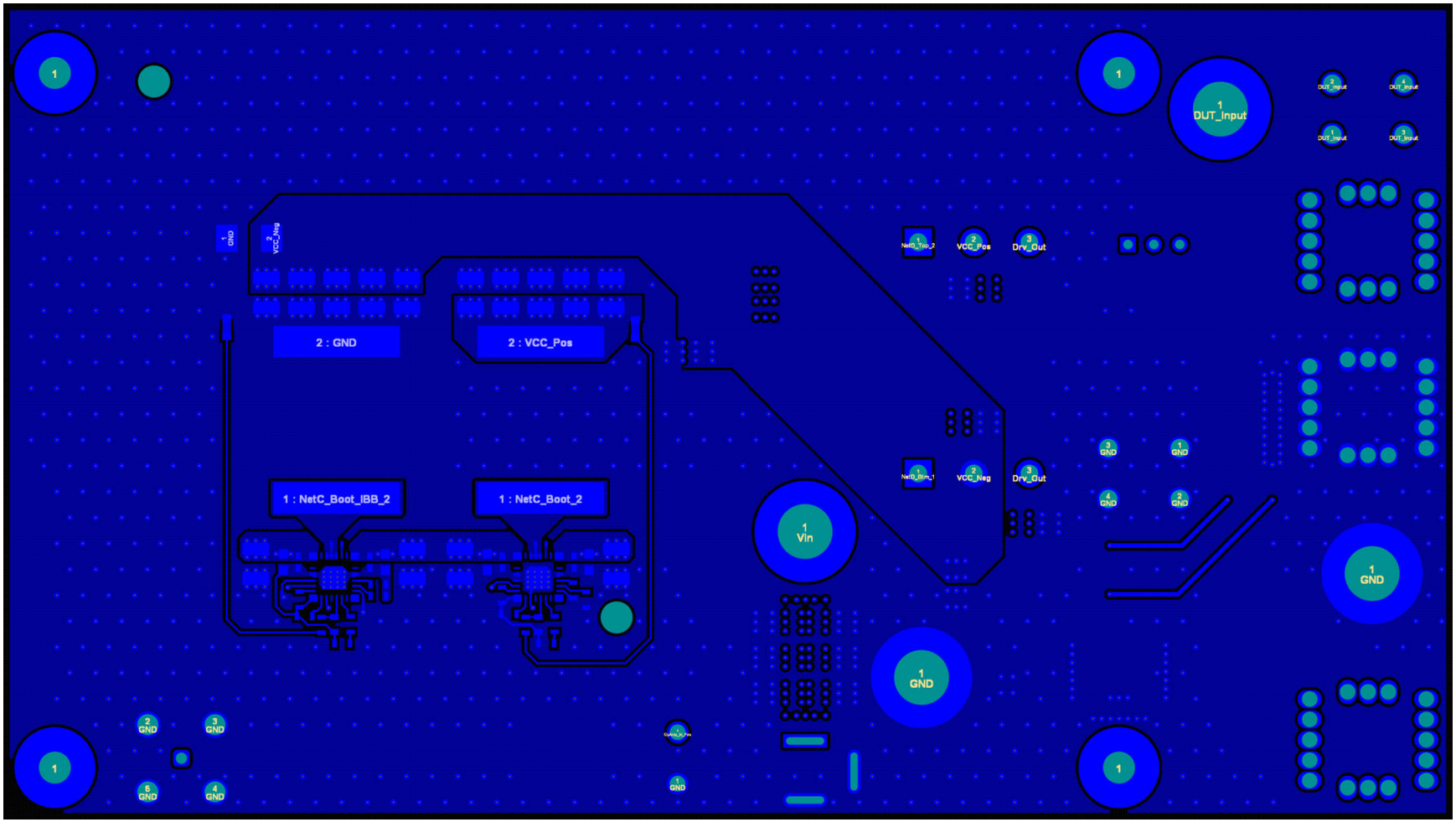

Figure 7-6. Layout - Bottom Layer

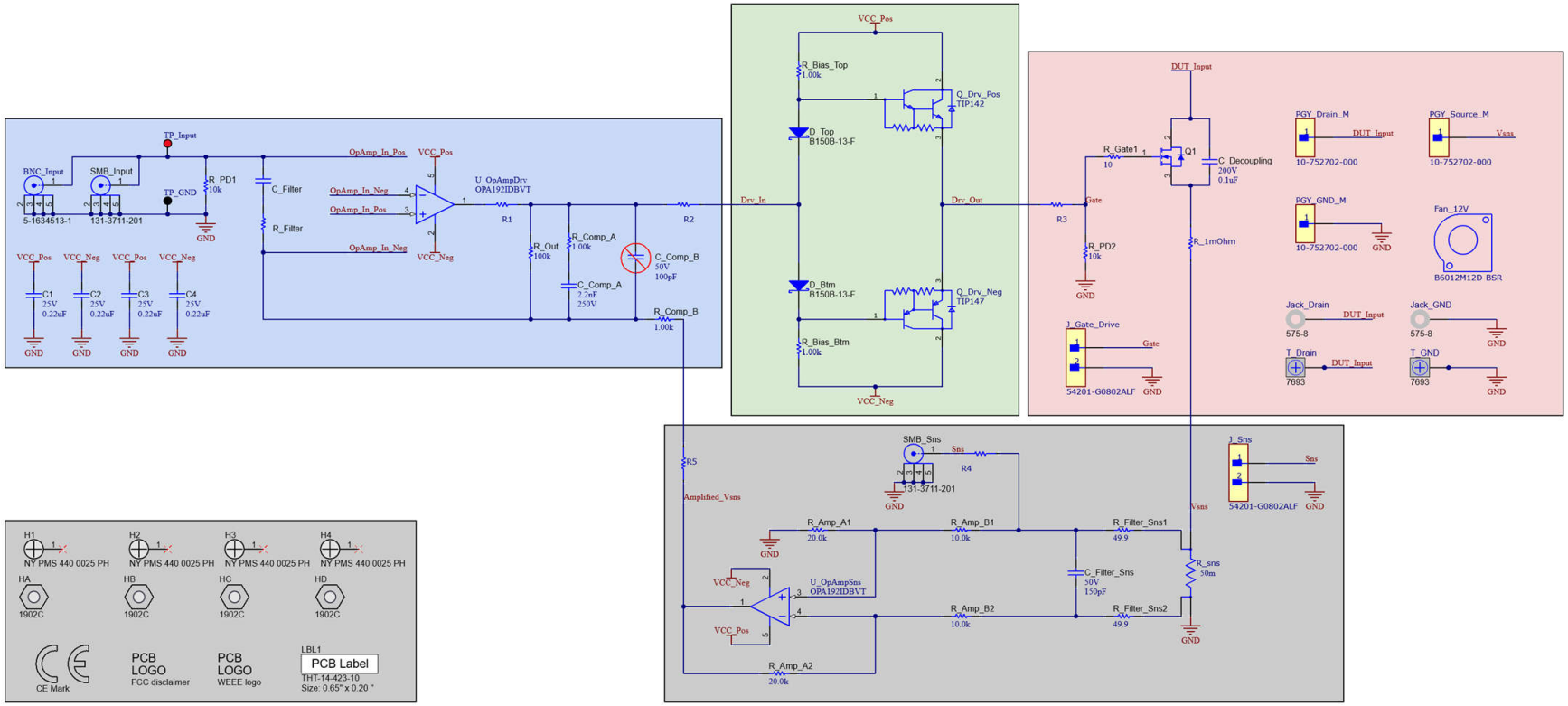

Figure 7-7. Main Schematic

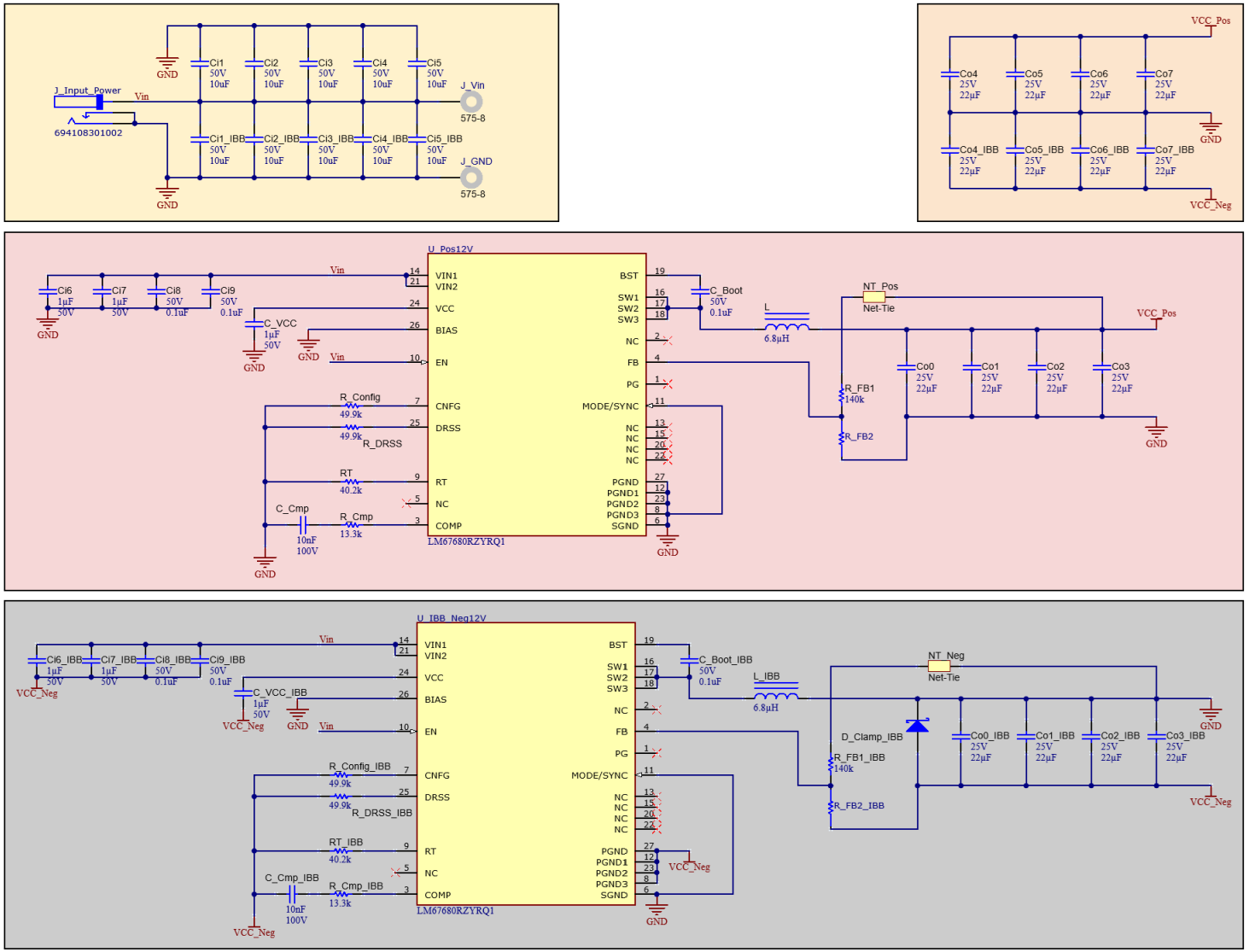

Figure 7-8. Power Sub-schematic

Table 7-1. PCB Bill of Materials (BOM)

Item	Designator	Description	Manufacturer	PartNumber	Quantity
1	BNC_Input	BNC Low Profile Elbow Jack, Gold, R/A, TH	TE Connectivity	5-1634513-1	1
2	C1, C2, C3, C4	CAP, CERM, 0.22 uF, 25 V, +/- 20%, X5R, 0402	TDK	C1005X5R1E224M050BC	4
3	C_Boot, C_Boot_IBB, Ci8, Ci8_IBB, Ci9, Ci9_IBB	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	MuRata	GCM155R71H104KE02D	6
4	C_Cmp, C_Cmp_IBB	CAP, CERM, 0.01 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E2X7R2A103K080AA	2
5	C_Comp_A	CAP, CERM, 2200 pF, 250 V, +/- 10%, X7R, 0603	MuRata	GRM188R72E222KW07D	1
6	C_Comp_B	CAP, CERM, 100 pF, 50 V,+/- 1%, C0G/NP0, 0603	Kemet	C0603C101F5GACTU	1
7	C_Decoupling	CAP, CERM, 0.1 uF, 200 V, +/- 10%, X7R, 1206	Kemet	C1206C104K2RACTU	1
8	C_Filter	CAP, CERM, 0.01 µF, 50 V,+/- 10%, X8R, AEC-Q200 Grade 0, 0402	TDK	CGA2B3X8R1H103K050BB	1
9	C_Filter_Sns	CAP, CERM, 150 pF, 50 V, +/- 5%, C0G/NP0, 0603	Kemet	C0603C151J5GACTU	1
10	C_VCC, C_VCC_IBB, Ci6, Ci6_IBB, Ci7, Ci7_IBB	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0603	Taiyo Yuden	UMK107AB7105KA-T	6
11	Ci1, Ci1_IBB, Ci2, Ci2_IBB, Ci3, Ci3_IBB, Ci4, Ci4_IBB, Ci5, Ci5_IBB	CAP, CERM, 10 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1210	Taiyo Yuden	UMJ325KB7106KMHT	10
12	Co0, Co0_IBB, Co1, Co1_IBB, Co2, Co2_IBB, Co3, Co3_IBB, Co4, Co4_IBB, Co5, Co5_IBB, Co6, Co6_IBB, Co7, Co7_IBB	CAP, CERM, 22 µF, 25 V,+/- 10%, X7R, 1210	Samsung Electro-Mechanics	CL32B226KAJNFNE	16
13	D_Btm, D_Clamp_IBB, D_Top	Diode, Schottky, 50 V, 1 A, SMB	Diodes Inc.	B150B-13-F	3
14	Fan_12V	The DC Blower Fan, 60 X 60 X 12 mm, 12 VDC, Sleeve Bearing, 5 CFM, 34 dBA, 0.3 inH20, 2 Wire Leads,...	Mechatronics	B6012M12D-BSR	1
15	H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	4
16	HA, HB, HC, HD	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	4
17	J_Gate_Drive, J_Sns	Connector	Amphenol ICC	54201-G0802ALF	2
18	J_GND, J_Vin, Jack_Drain, Jack_GND	Standard Banana Jack, Uninsulated, 8.9mm	Keystone	575-8	4
19	J_Input_Power	Connector	Wurth	694108301002	1
20	L, L_IBB	Inductor, Shielded, Powdered Iron, 6.8 µH, 19 A, 0.0092 ohm, AEC-Q200 Grade 0, SMD	Bourns	SRP1770TA-6R8M	2
21	LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10	1
22	PGY_Drain_M, PGY_GND_M, PGY_Source_M	PGY HOLDER WITH 3.0MM PIN	Amphenol	10-752702-000	3
23	Q1	MOSFET, N-CH, 100 V, 150 A, KCS0003B (TO-220-3)	Texas Instruments	CSD19536KCS	1

Table 7-1. PCB Bill of Materials (BOM) (continued)

Item	Designator	Description	Manufacturer	PartNumber	Quantity
24	Q_Drv_Neg	Bipolar (BJT) Transistor PNP - Darlington 100 V 10 A 125 W Through Hole TO-247	STMicroelectronics	TIP147	1
25	**Q_Drv_Pos**	**Bipolar (BJT) Transistor NPN - Darlington 100 V 10 A 125 W Through Hole TO-247**	**STMicroelectronics**	**TIP142**	**1**
26	R1, R2, R3, R4, R5	0 Ohms Jumper 0.125W, 1/8W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	Panasonic	ERJ-H3G0R00V	5
27	R_1mOhm	1 mOhms ±1% 5W Chip Resistor 2512 (6332 Metric) Automotive AEC-Q200, Current Sense Metal Element	Bourns	CSS2H-2512R-1L00FE	1
28	R_Amp_A1, R_Amp_A2	RES, 20.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Panasonic	ERJ-3EKF2002V	2
29	R_Amp_B1, R_Amp_B2	RES, 10.0 k, 1%, 0.1 W, 0603	Panasonic	ERJ-3EKF1002V	2
30	R_Bias_Btm, R_Bias_Top	RES, 1.00 k, 1%, 0.5 W, 1210	Yageo	RC1210FR-071KL	2
31	R_Cmp, R_Cmp_IBB	RES, 13.3 k, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD0713K3L	2
32	R_Comp_A, R_Comp_B	RES, 1.00 k, 1%, 0.1 W, 0603	Yageo	RC0603FR-071KL	1
33	R_Config, R_Config_IBB, R_DRSS, R_DRSS_IBB, R_Out	RES, 49.9 k, 0.5%, 0.1 W, 0603	Yageo America	RT0603DRE0749K9L	5
34	R_FB1, R_FB1_IBB	RES, 140 k, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD07140KL	2
35	R_FB2, R_FB2_IBB	Res Thick Film 0603 10K Ohm 0.1% 0.2W(1/5W) ±50ppm/C Pad SMD Automotive T/R	Panasonic	ERJ-PB3B1002V	2
36	R_Filter	Res Thick Film 0402 10 Ohm 1% 0.1W(1/10W) ±100ppm/C Molded SMD Automotive Punched T/R	Panasonic	ERJ-2RKF10R0X	1
37	R_Filter_Sns1, R_Filter_Sns2	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	Panasonic	ERJ-2RKF49R9X	2
38	R_Gate1	RES, 10, 5%, 1 W, 2512	Panasonic	ERJ-1TYJ100U	1
39	R_PD1, R_PD2	RES, 10 k, 5%, 0.5 W, 1210	Yageo	RC1210JR-0710KL	2
40	R_sns	Res Metal Foil 2043 0.05 Ohm 1% 5W ±50ppm/C Wide Terminal SMD T/R	Ohmite	FC4L110R050FER	1
41	RT, RT_IBB	RES, 40.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Panasonic	ERJ-3EKF4022V	2
42	SMB_Input, SMB_Sns	Connector, SMT, SMB Jack Assembly 50 ohm	Cinch Connectivity	131-3711-201	2
43	T_Drain, T_GND	Terminal screw, vertical, snap-in	Keystone	7693	2
44	TP_GND	Test Point, Multipurpose, Black, TH	Keystone Electronics	5011	1
45	TP_Input	Test Point, Multipurpose, Red, TH	Keystone	5010	1
46	U_IBB_Neg12V, U_Pos12V	65V, 8A Buck Converters Optimized for Inverting or Non-Inverting Outputs	Texas Instruments	LM67680RZYRQ1	2
47	U_OpAmpDrv, U_OpAmpSns	Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with E-trim	Texas Instruments	OPA192IDBVT	2

8 References

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Last updated 10/2025