Application Note

Anti-Islanding Implementation on Single-Phase Grid-Tied Inverter

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Trademarks

1 Introduction

Islanding refers to a condition when a section of an Area Electric Power System (Area EPS), consisting of both load and generation, becomes electrcially isolated from the main grid, and yet, the Distributed Energy Resources (DER) continues to supply power to that isolated section. When this happens unintentionally, it is known as unintentional island and it poses serious risks such as the follwoing:

- Utility line workers may be exposed to energized lines that they believe to be de-energized
- Connected electrical equipment may face damage due to unregulated voltage or frequency
- System fails out of compliance with grid codes

Hence, anti-islanding protection is implemented to enable the DER to recognize and detect an islanding condition and disconnect pompty, verifying safety of personnel, protection of equipment, and compliance with grid codes. The block diagram of the DER connections on a system-level can be seen in Figure 1-1.

It is essential to equip the DER with the capability to detect islanding for all possible loading cases and thus minimizing or eliminitaing non-detection zones (NDZ). NDZ can be defined as any range of loading conditions under which an islanding detection method fails to identify the islanding event.

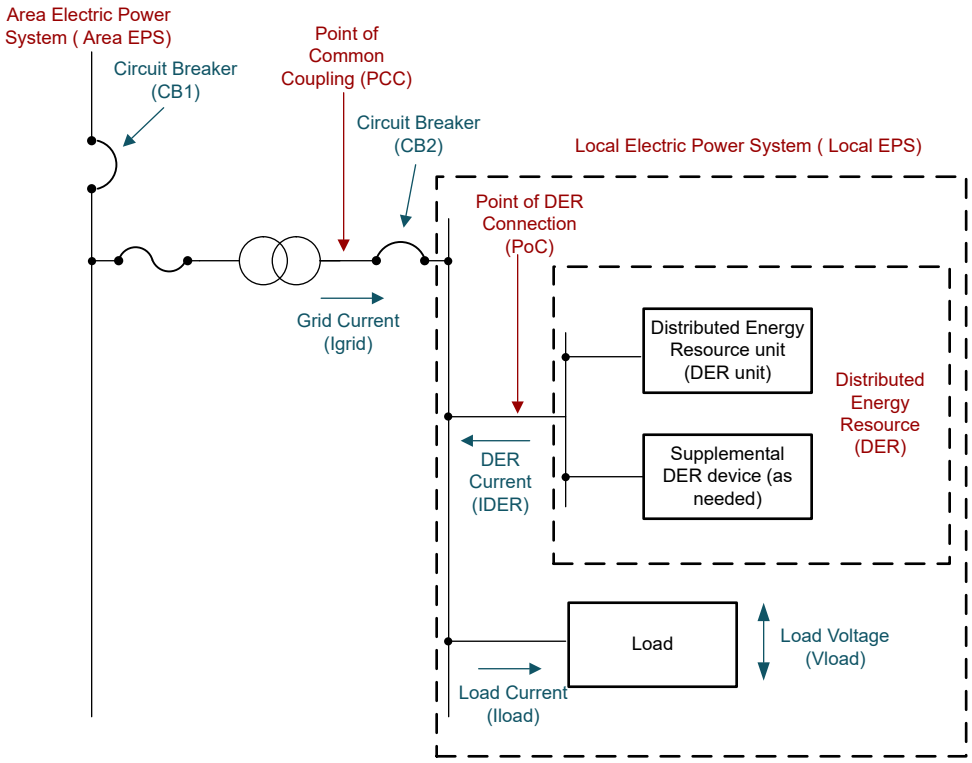

Figure 1-1. Block Diagram of the DER Interconnections Illustrating Anti-Islanding

Several international standards including IEEE 1547, IEC 62116 and VDE-AR-N-4105 define the requirements and scope of anti-islanding testing requirements for grid-connected systems. Among these, IEC 62116 provides a standardized and repeatable test procedure specifically designed to evaluate the anti-islanding performance of PV inverters. A key requirement coming from this standard is that upon detection of an islanding event, the inverter must disconnect from the grid within 2 seconds.

2 Detection Methods

Anti-islanding tests can be categorized mainly into passive or active methods. Passive islanding detection methodsare based on monitoring pone or more system parameters and comparing against a set threshold. If the threshold is exceeded, a fault is detected and the system shuts down.

Passive Methods

Passive methods are well known and largely used because they are simple, inexpensive and do not introduce disturbances such as variations of reactive power or harmonics that could degrade the power quality. However, they suffer from a non-detection zone (NDZ), which means that under some conditions, islanding detection may be compromised, thus reducing their performance.

A generic scheme of detection for passive methods is depicted in Figure 2-1.

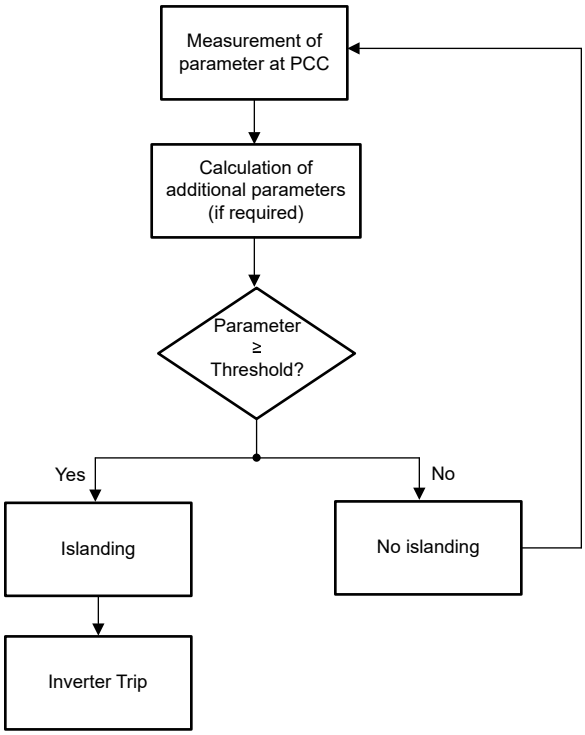

Figure 2-1. Flow Diagram for Passive Anti-Islanding Methods

Some examples of commonly used passive methods are:

- Over Under Voltage (OUV)
- Over Under Frequency (OUF)
- Rate of Change of Output Power (RoCoP)
- Rate of Change of Voltage (RoCoV)/Frequency (RoCoF)/Frequency over Output Power (RoCoFOP)
- Voltage Phase Jump Detection
- Harmonic content of voltage or current

Active Methods

Active methods work by introducing small perturbations to certain inverter parameters in order to detect islanding. When the grid is present, the effect of these perturbations is negligible on the system parameters, since the grid enforces its values. However if the grid is absent, the impact becomes noticeable, which ultimately leads to disconnection.

According to literature, active methods exhibit significantly smaller NDZ compared to passive methods. Hence they can be more effective in detecting islanding in scenarios where passive methods tend to fail, for example

in case where the local generation and consumption are closely balanced. However, it is important to note that continuous introduction of perturbations may lead to some degradation in power quality and system performance.

A generic scheme of detection for active methods is depicted in Figure 2-2.

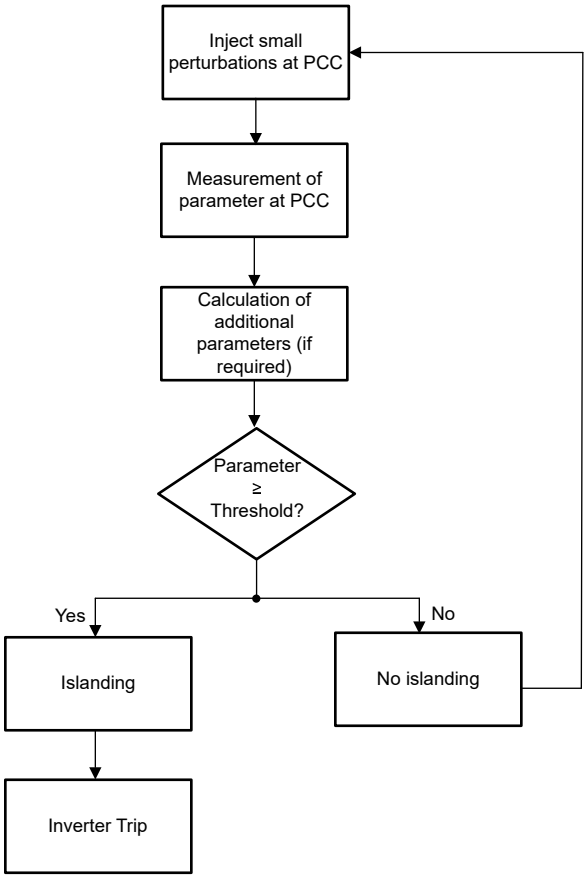

Figure 2-2. Flow Diagram for Active Anti-Islanding Methods

Some examples of commonly used active methods are:

- Change of Impedance
- Active Impedance Detection
- Slip Mode Frequency Shift (SMS)
- Active Frequency Drift (AFD)
- Sandia Frequency Shift (SFS)
- Sandia Voltage Shift (SVS)
- Frequency Jump (FJ)
- Variation of Active Power/Reactive Power

This document focuses on two of the most widely used active anti-islanding methods: Sandia Frequency Shift (SFS) and Sandia Voltage Shift (SVS).

Sandia Frequency Shift (SFS)

Sandia Frequency Shift (SFS) is an active anti-islanding method operates by introducing a positive feedback into the frequency at the Point of Common Coupling (PCC) voltage. Under normal grid-connected operation, the utility grid acts as a strong reference, absorbing any introduced perturbations, hence maintaining a stable frequency. However, when the inverter becomes islanded, even a slight frequency deviation is amplified progressively through the positive feedback loop, causing the frequency to drift continuously, until it exceeds the Over/Under Frequency (OUF) protection threshold, triggering disconnection.

The chopping frequency c_{f0} can be calculated from the next expression, in which c_{f0} is the chopping factor, k_{SFS} is the gain, f_{inv} is the output frequency of the inverter and f_{grid} is the frequency of the grid:

$$c_f = c_{f0} + k_{SFS}\left(f_{inv} - f_{grid}\right) \quad (1)$$

- k_{SFS} is a frequency which is injected when there is a deviation in the measured grid frequency from nominal value
- c_{f0} is a constant frequency bias term that is injected in the system even under no suspicion of islanding hence it is kept very small

Figure 2-3 shows the control diagram for this method.

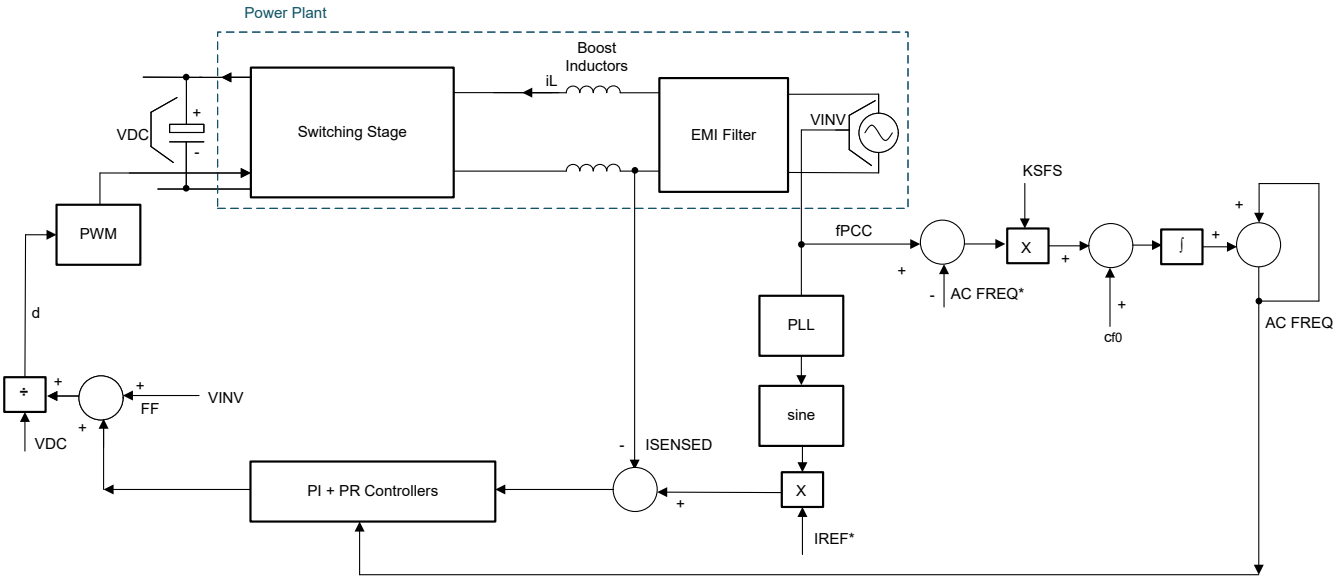

Figure 2-3. SFS Control Diagram

Sandia Voltage Shift (SVS)

Sandia Voltage Shift (SVS) is an active anti-islanding method that introduces positive feedback on the voltage magnitude at the Point of Common Coupling (PCC). During normal grid-connected operation, the grid voltage is tightly regulated, and the SVS mechanism does not produce any significant perturbation. However, upon grid disconnection, the voltage at the PCC is no longer regulated by the grid, and any small voltage deviation is amplified through the positive feedback loop. This causes the voltage magnitude to drift rapidly outside the Over/Under Voltage (OUV) protection thresholds, triggering islanding detection and disconnection. It can be said that a variation of the injected current by the inverter is linked directly proportional to a variation of the inverter voltage

$$I_{ref-dis} = k_{SVS}\left(V_e\right) \quad (2)$$

where $I_{ref-dis}$ is the disconnection reference current, k_{SVS} is the gain to adjust the response time of the algorithm, V_e the voltage error variation

- $I_{ref-dis}$ is then added to the current reference of the inverter

Figure 2-4 shows the control diagram for this method.

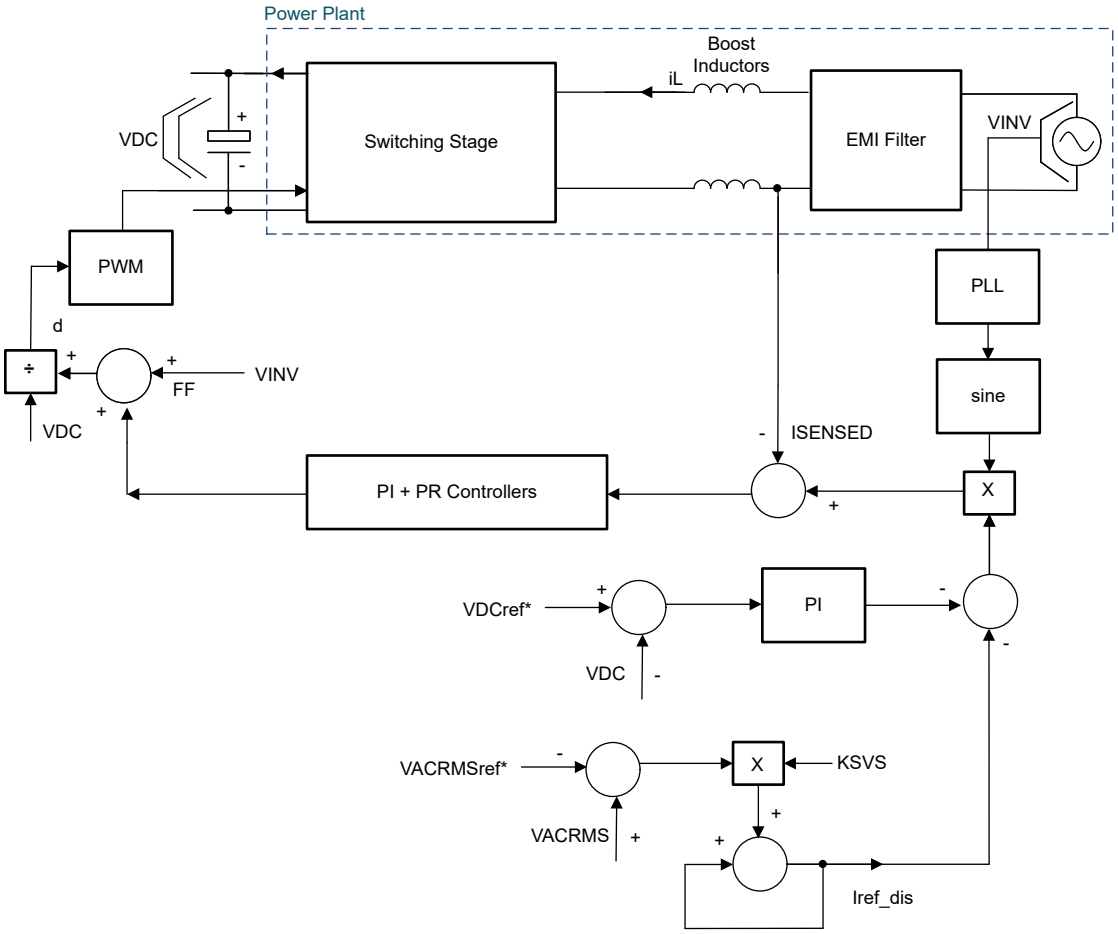

Figure 2-4. SVS Control Diagram

Although this method achieves a small NDZ, it may degrade power quality under certain operating conditions. It can, however, be effectively combined with the Sandia Frequency Shift method, and the two methods together demonstrate significantly improved anti-islanding detection performance.

3 IEC 62116 Test Setup and Procedure

IEC 62116 titled *"Utility-Interconnected Photovoltaic Inverters – Test Procedure of Islanding Prevention Measures,"* defines a standardized and repeatable procedure for evaluating the anti-islanding performance of photovoltaic (PV) inverters. An equipment that meets the requirements of IEC 62116 can be classified as non-islanding, meaning it is capable of detecting an islanding condition and promptly ceasing to energize the grid under all applicable operating conditions. This section describes the test setup and methodology defined by the standard.

Test Circuit and Components

The IEC 62116 test circuit simulates real-world grid conditions with precise control over power flow and load balance. Its primary goal is to replicate the worst-case scenario for anti-islanding detection, where the inverter's output closely matches the connected load.

Key Components:

- EUT (Equipment Under Test): Typically a PV inverter, connected between a DC source and an AC source representing the grid
- Adjustable RLC load network: Connected in parallel on the AC side, allowing fine-tuned load balancing
- Measuring instruments to monitor voltage, current, and power flow in real time

An example of the test setup with TIDA-010938 can be seen in Figure 3-1.

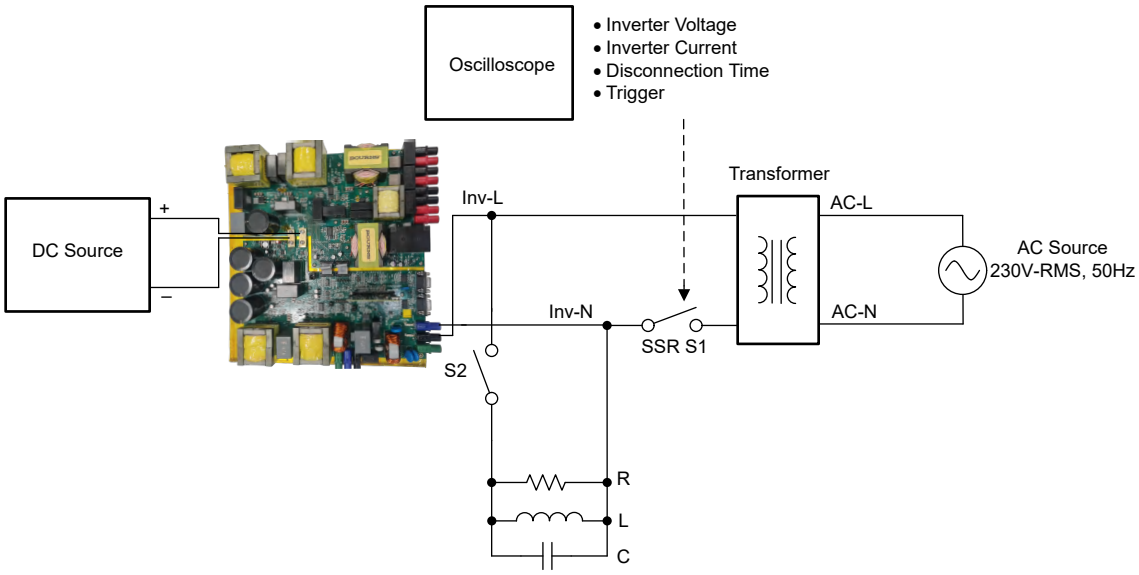

Figure 3-1. Anti-islanding Testing of TIDA-010938

What the Setup Enables:

- Simulation of balanced and imbalanced power conditions
- Controlled grid switching (simulating grid disconnection)
- Monitoring of the inverter's islanding detection response time

Test Procedure

IEC 62116 provides a standardized method to evaluate anti-islanding performance in PV inverters across three output power conditions:

- Condition A: Maximum output
- Condition B: 50–66% of maximum
- Condition C: 25–33% of maximum

This can be seen in Table 3-1.

Table 3-1. Trial Conditions

Trial	Inverter Output Power	Inverter Input Voltage (VDC)	Shutdown Settings
A	Nominal	>90% Nominal	Nominal V & f shutdown
B	50-66% Nominal	50% Nominal, +/-10%	Nominal V & f shutdown
C	25-33% Nominal	<10% Nominal	Nominal V & f shutdown

- The test uses an RLC load tuned to a quality factor of Q_f = 1.0 +/- 0.05, simulating the worst-case balanced island. The load is balanced so that current through the grid switch S_1 is 0 A (+/-1% rated current), representing a perfect power match between inverter output and local load. The islanding test is triggered by opening S_1, and the run-on time is recorded until the inverter output current is zero.
- Load imbalances are then applied across the test conditions defined by the standard. This includes varying the active load and/or one reactive component (either L or C); the test is repeated after each adjustment, and the run-on time is recorded. Detailed information regarding the test conditions for power unbalance for Trials A, B and C can be found in the IEC-62116 standard.
- Pass/Fail Criterion: Run-on time**<** 2 seconds for all tested conditions.

To evaluate the anti-islanding performance under demanding operating conditions, the TIDA-010938 was tested against the worst-case scenarios defined by IEC 62116 for Trials A, B, and C, without load imbalancing. The detailed test results and analysis are provided in the design guide.

4 Summary

Anti-islanding protection is a critical safety requirement for single-phase grid-connected inverter systems. When the utility grid disconnects, an inverter must rapidly detect the condition and cease energizing the local load, failure to do so poses serious risks to personnel, equipment, and grid integrity. Both passive and active anti-islanding methods exist, each with distinct trade-offs between simplicity and detection reliability. Active methods, particularly Sandia Frequency Shift (SFS) and Sandia Voltage Shift (SVS), offer superior performance by leveraging positive feedback mechanisms at the PCC to drive system parameters outside protection thresholds, significantly reducing the Non-Detection Zone. Testing conducted in accordance with IEC 62116 provides a standardized and repeatable framework to validate these methods, simulating worst-case conditions and requiring disconnection within 2 seconds of grid loss. Depending on the required performance targets, the appropriate anti-islanding method can be selected to ensure careful method selection and thorough compliance testing in the design of safe, grid-ready inverter systems.

5 References

- Texas Instruments, *TIDA-010938 Reference Design*, webpage.
- MDPI, *A Survey of Islanding Detection Methods for Microgrids and Assessment of Non-Detection Zones in Comparison with Grid Codes.*, webpage.
- IEEE, *1547-2018 - IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces | IEEE Standard | IEEE Xplore.*, webpage.
- IEEE, *Test of anti-islanding protections according to IEC 62116: An experimental feasibility assessment | IEEE Conference Publication | IEEE Xplore.*, webpage.
- IEEE, *Development of a single-phase anti-island analysis platform according to NBR-IEC 62116 standard.*, webpage.

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