Application Note

TPLD1202 Application in BMS System

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ABSTRACT

Discrete logic devices are extensively used in battery management systems (BMS) for fault diagnostics and state retention but present notable challenges of PCB size and low-power design. Texas Instruments' Programmable Logic Devices (TPLDs) enable designers to configure internal macro-cells to integrate different logic designs into a single-chip design. This paper serves as a practical implementation guide for designers on how to deploy TPLD architectures in BMS applications, effectively optimizing board space and hardware development flexibility.

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Trademarks

1 Introduction

In automotive and industrial energy storage systems (ESS) & Battery Management Systems (BMS), implementing independent hardware redundancy is crucial to meet stringent functional safety standards. Consequently, discrete logic devices are widely deployed across BMS designs. These components primarily include: (1) watchdog ICs and analog multiplexers; (2) Fault & Protection logic integration; (3) Latch networks & flip-flops for state retention under EMI noise.

To resolve these layout and cost limitations, this application note introduces a highly integrated hardware redundancy solution using Texas Instruments' Programmable Logic Devices (TPLD). By utilizing the low power, graphically programmed internal macro-cells of a single TPLD chip, engineers can consolidate disparate logic paths into a compact silicon footprint. This document serves as a practical deployment guide for optimizing board space and development flexibility in next-generation BMS platforms.

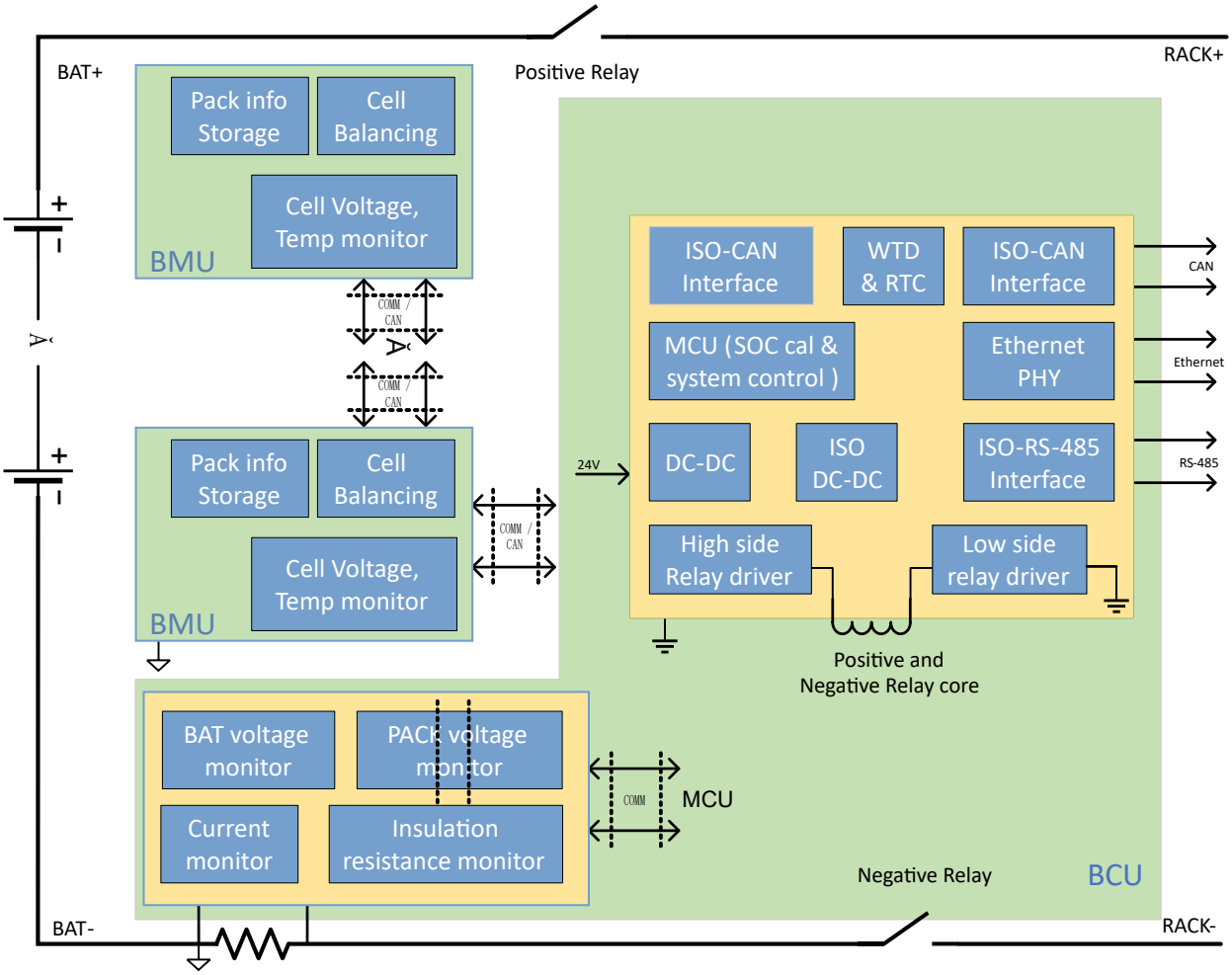

Figure 1-1. General BMS Block Diagram

2 TPLD Application in BMS System

2.1 Low-Power Wake-Up

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8V ± 0.09V			V_{CC} = 3.3V ± 0.3V			V_{CC} = 5V ± 0.5V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Standby													
I_{CC}	Quiescent current		Inputs = static, Outputs = open, I_O = 0, OSC powered off, ACMP powered off		0.88			0.88			0.90		µA
Oscillator													
I_{CC}	Quiescent current	OSC0 enabled: 2kHz	Predivide = 1		1.94			2.03			2.57		µA
I_{CC}	Quiescent current	OSC0 enabled: 2kHz	Predivide = 8		1.95			2.03			2.57		µA
I_{CC}	Quiescent current	OSC0 enabled: 10kHz	Predivide = 1		1.96			2.05			2.59		µA
I_{CC}	Quiescent current	OSC0 enabled: 10kHz	Predivide = 8		1.95			2.05			2.56		µA
I_{CC}	Quiescent current	OSC1 enabled: 25MHz	Predivide = 1		431.0			432.9			433.1		µA
I_{CC}	Quiescent current	OSC1 enabled: 25MHz	Predivide = 8		264.6			266.0			266.2		µA

Figure 2-1. TPLD Supply Current Characteristics

The TPLD achieves an ultra-low quiescent current (<1uA) in standby states. This exceptional efficiency allows the device to remain connected to an always-on supply rail directly from the battery. Within InterConnect Studio (ICS), the primary clock routing is optimized by enabling the internal low-frequency oscillator (LF_OSC). This configuration minimizes dynamic switching losses and verifies a highly reliable hardware supervisory baseline before the main microcontroller (MCU) system initializes. For more details, see *Low Power Operation in TI Programmable Logic Devices (TPLD)*.

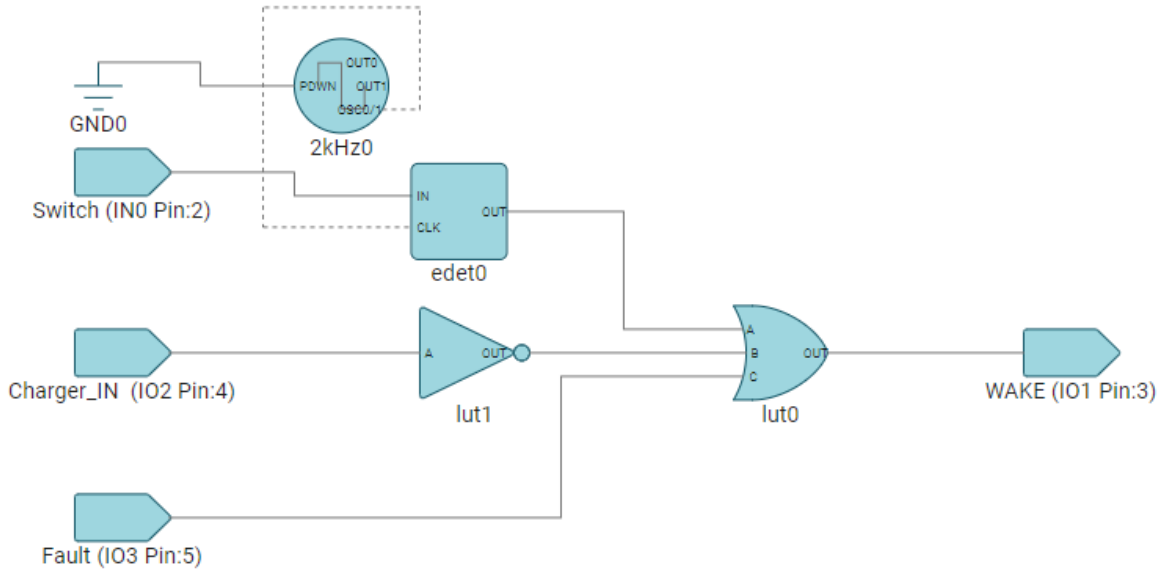

Figure 2-2. BMS Wake-Up Diagram of TPLD

In BMS systems, the host MCU/AFE shuts down in shipping or storage mode and must wake up when pressing the button, when the charger is plugged in or there is a fault occurring with different asynchronous external signals: pulse, active high, or active low. During system operation, the window watchdog timer (WDT) is implemented to mitigate MCU firmware freeze risks. It is simple to design wakeup orchestration and WDT with TPLD in one chip to reduce layout size and quiescent current.

As shown in Figure 2-2, the TPLD utilizes a three-input OR gate to aggregate distinct wake-up signals. Within this simulation model, the TPLD incorporates inverters to configure the required signal logic inversion and employs edge-triggered flip-flops to robustly capture transient or pulse signals.

2.2 Protection Logic and Watchdog Integration

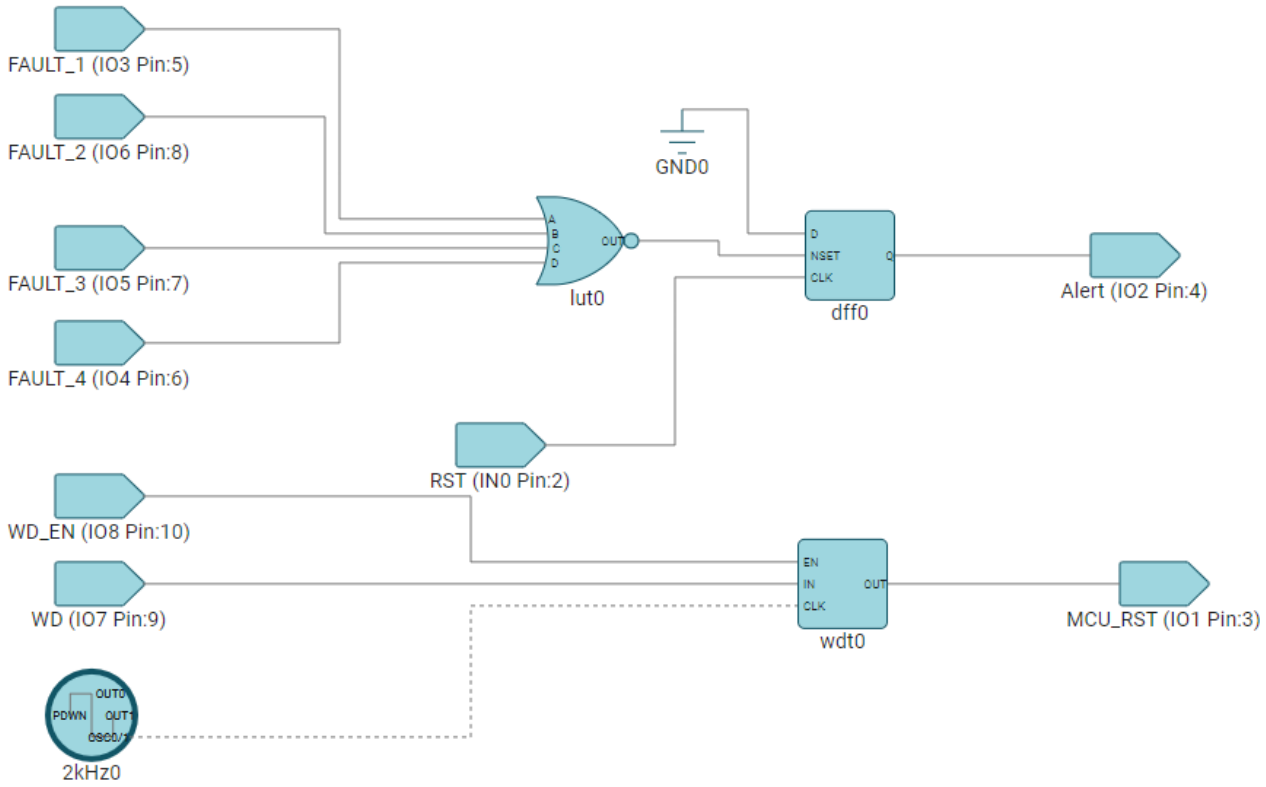

Figure 2-3. TPLD Diagram in BMS Housekeeping

During the operation of BMS system, the host microcontroller must instantly enter an interrupt routine upon fault occurrence. The majority of protection interrupts are directly dispatched by the BMS AFE, but there are still some safety boundaries or redundant faults that need to be identified by the host. The TPLD can capture multiple fault signals driven by external analog sensing circuits such as charge overcurrent, discharge overcurrent, overvoltage, and undervoltage and latch the fault to alert the host. As shown in Figure 2-3, distinct asynchronous fault signals are securely captured through internal RS flip-flops, with clearing routines multiplexed through a dedicated hardware reset (RST) pin. Furthermore, the TPLD features built-in analog comparators, providing an avenue to further minimize external analog peripheral count and optimize the total board footprint. For more details for another workaround for one shot latch, see *Configure a One Shot With TI Programmable Logic Devices*.

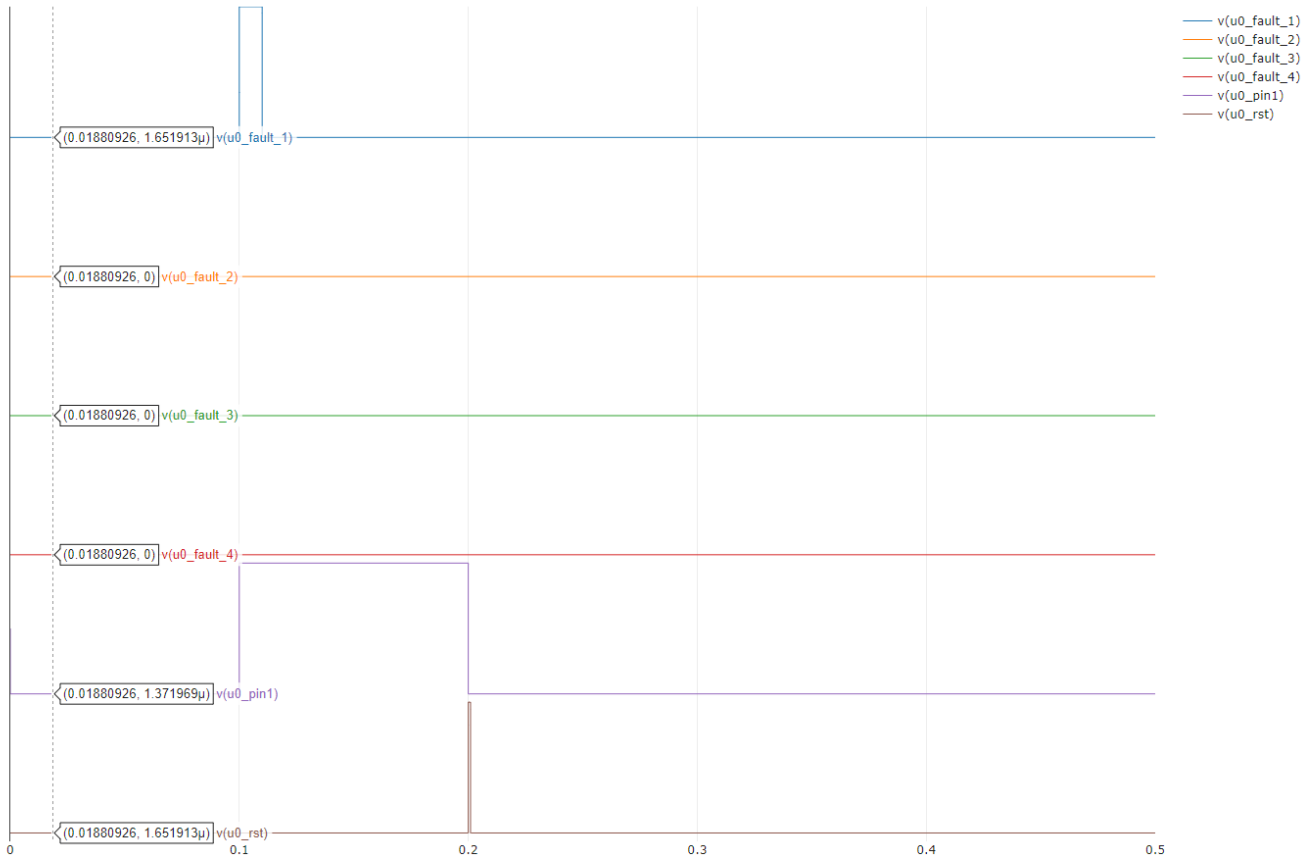

Figure 2-4. Multichannel Fault Latch Simulation Result

TPLD can also be configured as an autonomous Watchdog Timer (WDT) for host supervision. As shown in Figure 2-3, the WDT leverages the internal low-frequency oscillator (LF_OSC) as its timebase. During normal execution, the host MCU periodically toggles a GPIO to send a Watchdog Input (WDI) pulse, which clears the TPLD counter. To prevent an infinite reset loop caused by the MCU's boot-up blanking window, the simplest approach utilizes the WDT enable function. By routing a passive RC delay network or an early MCU power-good signal to the EN pin, the TPLD pre-allocates an extended startup delay, keeping the WDT temporarily disabled until the host completes firmware initialization. For more details about watchdog timer settings, see *Using a Watchdog Timer Within TPLD*.

2.3 State Latching and Glitch Filtering

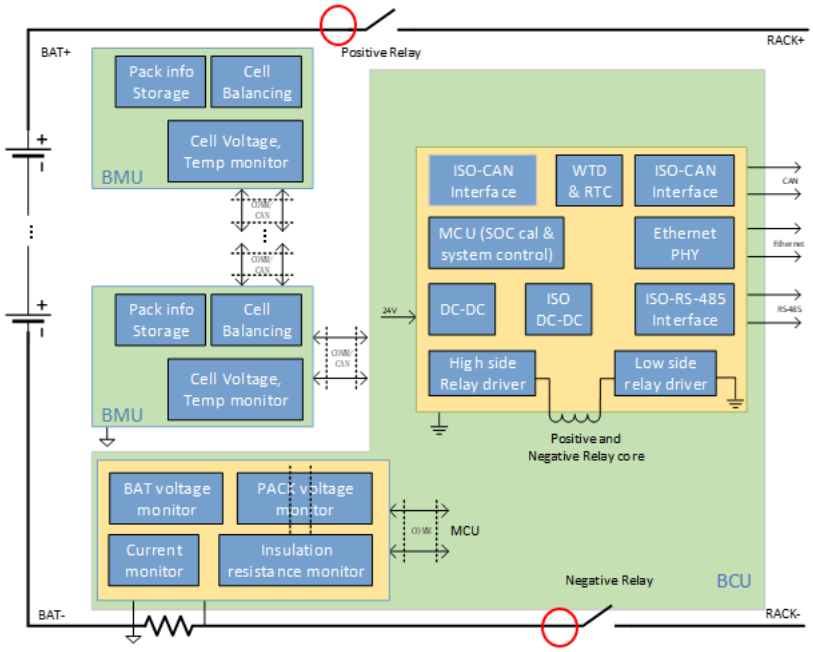

Figure 2-5. BMS Relay and FET Latching

During the transition of a BMS system from active mode to low-power mode, or during an unpredictable software reset of the host controller, GPIO pins of host will instantaneously convert into high-impedance (Hi-Z) or floating states. If the driver of the high voltage relay is driven directly by these host GPIOs, the floating stage can easily induce unintended relay chattering or false state switching. In high-voltage, high-current application, such floating transients cause catastrophic arcing damage across the physical contactor terminals. In the common BMS design, discrete logic such as SN74HC373/SN74HC175 is widely applied as the driver latch, which has high quiescent current.

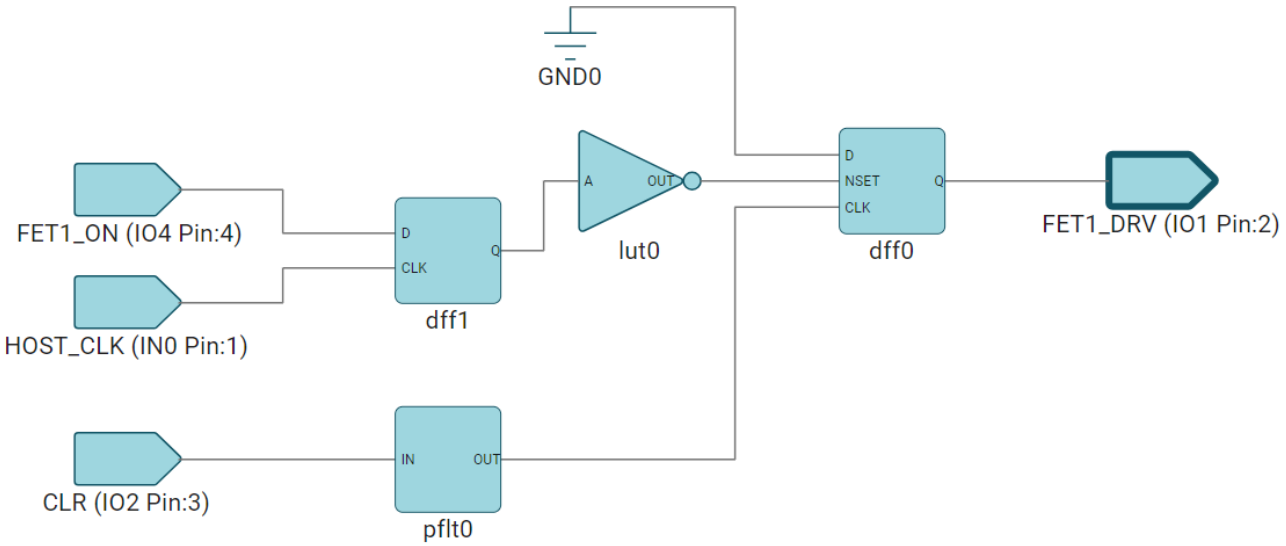

Figure 2-6. TPLD Stage Latching and Glitch Filter

As shown in Figure 2-6, TPLD can freeze and hold the driving state levels prior to host power-down or reset execution. Even if the subsequent host controller pins completely lose driving capability and float, the TPLD independently sustains the stable output through the pure hardware architecture, verifying absolute state stabilization of the HVDU loop across the entire transient power-down window.

Furthermore, high-frequency electromagnetic interference (EMI) noise spikes are universally generated during the instantaneous engagement of high-voltage contactors or high-power switching transients. In this design, the TPLD configures its input stages as digital pins with integrated Schmitt triggers and routes the signals through the internal Programmable Filter (PFLT) modules. By graphically configuring a nanosecond-scale blanking window, the TPLD executes hardware-level digital noise suppression to completely filter out high-frequency switching glitches. This approach fundamentally blocks noise crosstalk and parasitic false triggering during transition states, significantly enhancing the system-level robustness of the hardware redundancy topology.

3 Summary

By leveraging low-power, graphically programmed macro-cells, TPLD can consolidate an autonomous watchdog, low-power wake-up routing, fault protection aggregation, and floating state retention. Design analysis indicates this scheme replaces multiple discrete logic ICs, multiplexers, and external watchdog timers, achieving a critical PCB area reduction. Ultimately, this topology eliminates host IO drift during hibernation, suppresses EMI switching transients, and facilitates rapid, highly flexible development for hardware engineers. For more details about TPLD, see *Engineer's guide to programmable logic*.

4 References

1. Texas Instruments, *TPLD1202 Programmable Logic Device With I2 C/SPI and 10-GPIO* , datasheet.
2. Texas Instruments, *Using a Watchdog Timer Within TPLD*, application brief.
3. Texas Instruments, *Power Sequencing With Feedback Using TI Programmable Logic Devices*, application brief.
4. Texas Instruments, *Configure a One Shot With TI Programmable Logic Devices*, application brief.

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