Application Note

Automotive E-latch Systems Design Guideline using TPS61383-Q1

Travis Wang, Mason Chen

ABSTRACT

The automotive industry's shift toward electronic latch (e-Latch) systems replaces traditional mechanical linkages with electronically controlled actuators, offering crash unlock safety, quieter operation, seamless user experience, and greater design flexibility. However, e-latch systems present a critical challenge: balancing limited system cost, high peak current, and PCB size. Also, the aging characteristics of super capacitor and multistage load profile often place great difficulty on designing backup energy. TPS61383-Q1 is a bi-directional boost converter and buck charger designed for back up power applications such as e-latch. This IC provides an integrated power design on backup supercap system. This paper presents a systematic design guideline for implementing TPS61383-Q1 in automotive e-Latch systems, covering key design considerations, component selection and performance optimization.

Table of Contents

Trademarks

1 Introduction

An *Electronic Latch (E-latch)* is a next-generation automotive door locking and releasing mechanism that replaces the traditional mechanical latch with an electromechanical actuation system and super capacitor energy backup for emergency case. According to Chinese automotive safety standard GB+48001-2026, every vehicle sold in China must be capable of unlocking from both inside and outside without reliance on the main battery. This regulation has far-reaching implications: even vehicles equipped with conventional mechanical door latches must now incorporate an E-latch system to support speed-sensitive door unlocking from outside, effectively making E-latch integration a universal requirement across all passenger vehicle segments in the Chinese automotive market. TPS61383-Q1 is a bi-directional boost converter/buck charger designed for back up power applications such as e-latch. This application note provides guidance on how to design Automotive e-latch system with the TPS61383-Q1 to achieve correct function, stable operation, and good thermal and low EMI performance.

2 Design Requirement and System Structure

2.1 Design Requirements

Automotive e-Latch system is designed to replace or backup traditional mechanical door latches. A proper designed e-latch system integrates local backup power system to handle main battery malfunction, safety logic for emergency condition and backup battery health detection function. Functional requirement of typical e-latch system is listed below:

1. Secure Latching: The system must verify that a door can be opened when requested, whether from an interior handle, exterior handle, or remote command, even during severe battery voltage transients like cold crank
2. Crash safety compliance: In the event of a collision, the e-latch must either remain latched to prevent ejection or, if required by regulation, actively unlock to enable rescue access. This demands a backup energy storage system that operates independently of the main power bus.
3. Electronic Release: E-latch system must integrate electronically controlled actuators (Usually BDC) which allows the door to open via electronic switch.
4. Power Management: E-latch system integrates a local super capacitor as backup power system to verify operation during main battery malfunction.
5. Self-detection: E-latch system detects its backup battery state of health and report to central BCM or gateway.
6. Safety Logic: The e-latch system integrates safety logic to receive emergency signal and unlock when vehicle accident happens. E-latch system communicates with other vehicle systems like gear position and speed sensor to prevent accidental door opening when car is in motion.
7. Functional safety (ISO 26262 ASIL): Door latches are safety-related elements. The e-latch power supply and control logic must be designed to avoid unintended unlocking or failure to unlock. Typical ASIL targets range from ASIL A to ASIL B, depending on the vehicle architecture.

2.2 System Structure

The physical location of the crash-unlock module (the actuator responsible for releasing the latch under crash conditions) defines two major system architectures: centralized and distributed.

2.2.1 Centralized E-Latch System

In a centralized architecture, a single crash-unlock actuator is installed at the central body control module (BCM) or a dedicated door zone module. From there, mechanical rods or cables distribute the crash-unlock force to all four doors simultaneously.

Energy Requirement：

1. 6-10 locks for 4 doors, around 200J for unlocking all locks
2. 3-4 cells super capacitor

Advantages:

1. Only one high-reliability crash actuator needed, lower system cost.
2. Easier functional safety validation for the crash path.

Disadvantages

1. Mechanical linkage from central actuator to each door still have the risk of damage.
2. If the central actuator fails, all doors lose crash-unlock capability.
3. Slower crash response due to mechanical transmission delay.

There are two different type of structure for centralized e-Latch system.

- CPM (Crash Power Module) – The backup power system responsible for unlatching operations. CPM provides only the backup power supply and does not integrate execution unit in e-latch module. When a car accident occurs, the CPM powers the door module and the unlock is executed by door module.

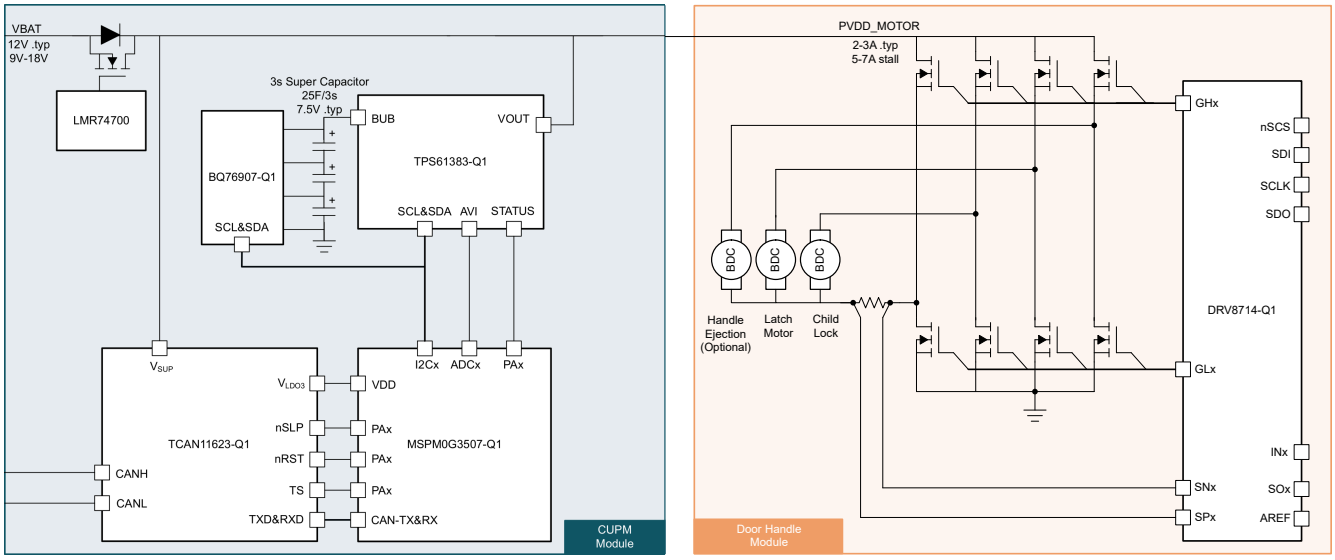


Figure 2-1. CPM Structure

- CUPM (Crash Unlock Power Module) – A secondary module that provides a backup unlocking capability when the primary system fails. The ‘U’ signifies ‘Unlock’. CUPM not only provides backup power supply but also integrates secondary execution unit. When a car accident occurs, the CUPM is able to unlock by itself even if motor driver in door module is damaged. There are two different types of structure for CUPM:

For cars which integrates latch motor driver inside the car body, CUPM usually uses the centralized motor driver as excution unit:

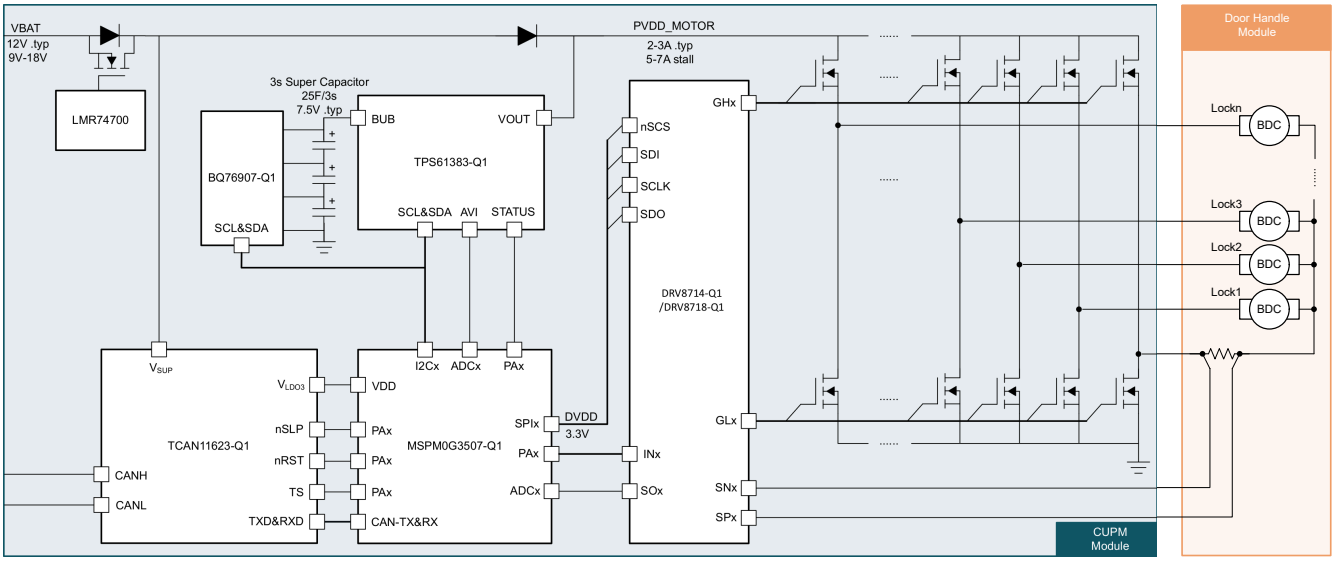


Figure 2-2. CUPM Structure with Centralized Motor Driver

Other cars place the motor driver locally in the door module. In this case the CUPM needs additional high side switch as backup execution unit:

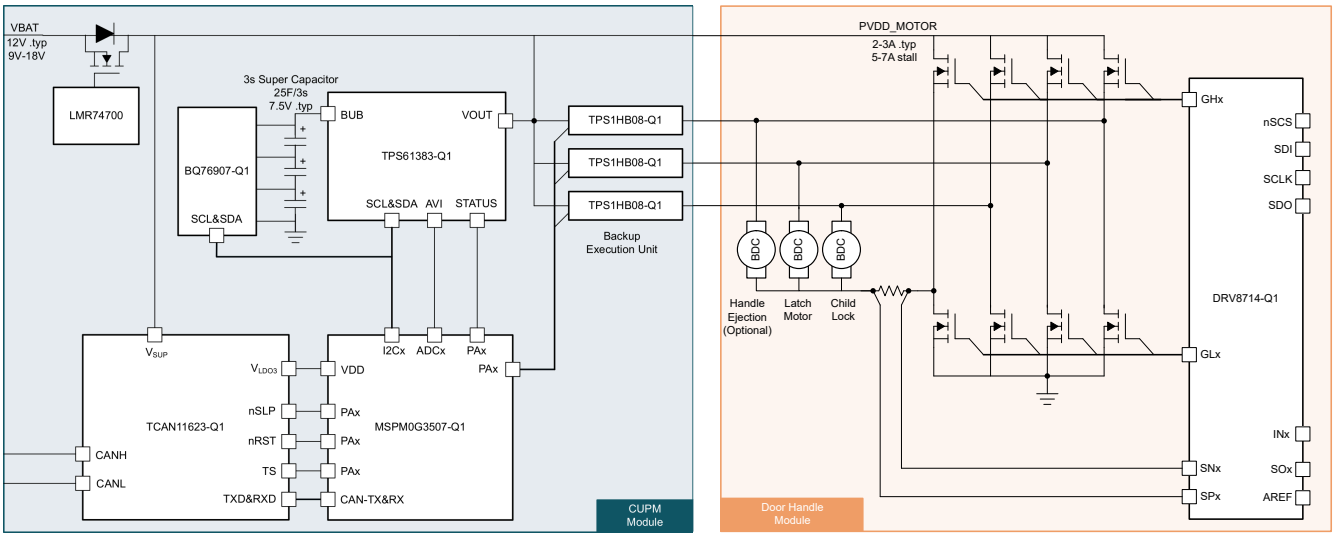


Figure 2-3. CUPM Structure with Centralized Motor Driver

2.2.2 Distributed E-Latch System

In a distributed architecture, each door contains its own dedicated crash-unlock actuator, collocated with the normal e-latch mechanism. The crash command is transmitted over the vehicle network (CAN/LIN) or through a dedicated hardwired trigger line. The TPS61383-Q1 in each door powers both the normal-mode motor and the local crash actuator (if electrically triggered, for example, a pyrotechnic squib or a high-current solenoid).

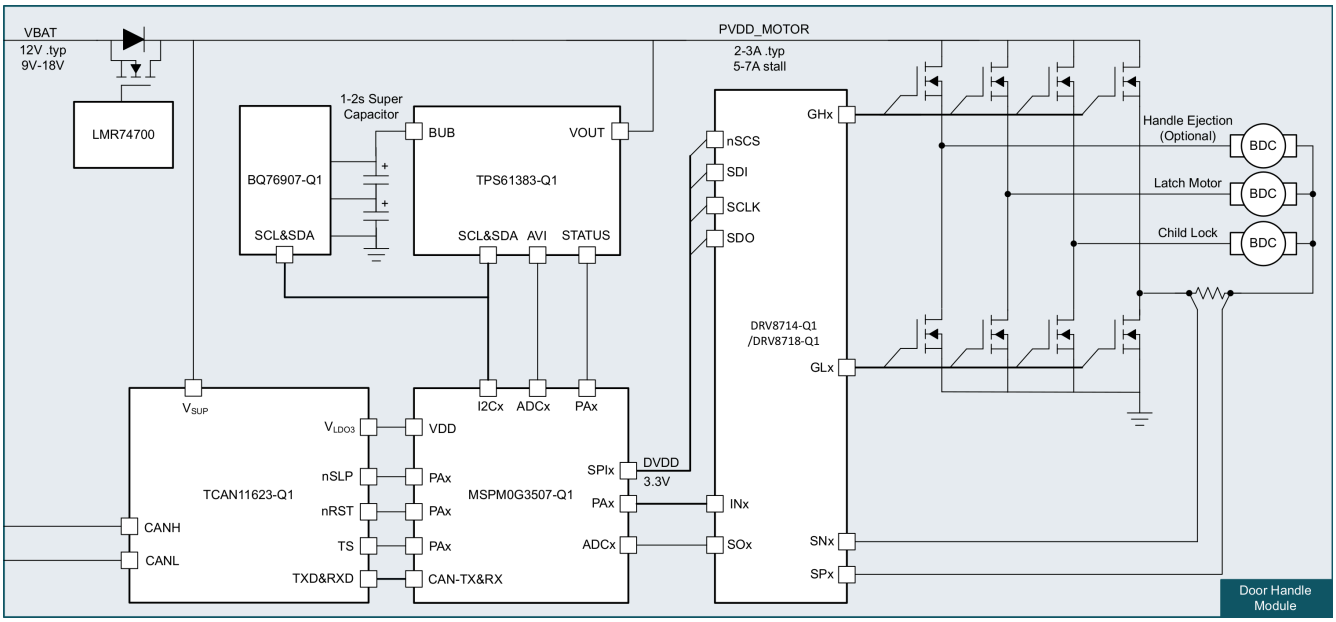


Figure 2-4. Single Cell E-latch System

Energy Requirements:

1. 1-2 locks for 1 door, around 60J for unlocking the locks
2. 1-2 cells super capacitor

Advantages

1. No mechanical linkages – fully electronic, reducing door weight and assembly time.
2. Redundancy: failure of one door's crash module does not affect other doors.
3. Faster, more predictable crash response (microsecond-level electrical trigger).
4. Enables advanced features such as *soft-open* after crash or selective unlocking.
5. 1 cell super capacitor is enough for some cars. No need for cell balance when using one cell.

Disadvantages

1. Higher component cost (multiple backup super capacitor pack and 4 local boost converters on each doors).
2. Lower space constraint: Limited space on door module increases challenge on super capacitor placement.
3. More complex safety validation per door.

3 Power Train

The power train of an automotive e-latch system consists of a battery charger to charge the super capacitor and boost converter to boost super capacitor energy to motor. A proper designed e-latch system power train must be able to achieve the following requirements

- Fast Charging for super capacitor from 0V to target

The e-latch system starts charging super capacitor by vehicle ignition. If the car accident occurs immediately after the driver starts up the car, the supercap energy must be ready before the car reaches a dangerous speed. So most OEM requires the supercap charging to complete within one minute, requiring a charging current over 3-4A.

- Low quiescent current

After the supercap is fully charged, the e-latch system works in a standby mode for most of its lifetime. This places stringent requirements on system quiescent current.

- High boost current limit

E-latch system powers motor (usually BDC) which requires up to 10A (120W) during motor stall. This requires a high current limit boost for the discharge operation. But most OEM applies stall monitoring to turn off motor after stall operation is detected. So in real operation the 120W stall current only lasts for 20-100ms. In this case, selecting a boost converter rated to handle 120 W of continuous thermal dissipation would be overspecified. A high current boost converter is more suitable and cost efficient solution.

- Super capacitor bleeding

Super capacitor lifetime is fundamentally governed by its operating voltage, as voltage is the primary thermodynamic driving force behind the electrochemical degradation mechanisms that determine device longevity. In order to avoid degradation of the super capacitor and improve super capacitor health, it'll be necessary to design discharge circuits to discharge the super capacitor during car parking (ignition off) and avoid staying in maximum charge for most of its lifetime.

- Seamless transition between charger mode and boost discharge mode

The e-latch system needs to detect the voltage of the 12V battery and transition between charger mode and boost discharge mode. Seamless transition is required to avoid voltage dip and system shutdown.

TPS61383-Q1 is a bi-directional DC-DC converter that integrates charger, boost and battery health detection. This IC provides an integrated power train design for e-latch systems.

3.1 Integrated E-Latch Power Train with TPS61383-Q1

Figure 3-1 shows a typical E-latch system using the TPS61383-Q1. This device is designed to charge super capacitor when 12V main battery is normal and boost back-up battery energy to Vsystem when 12V battery is disconnected.

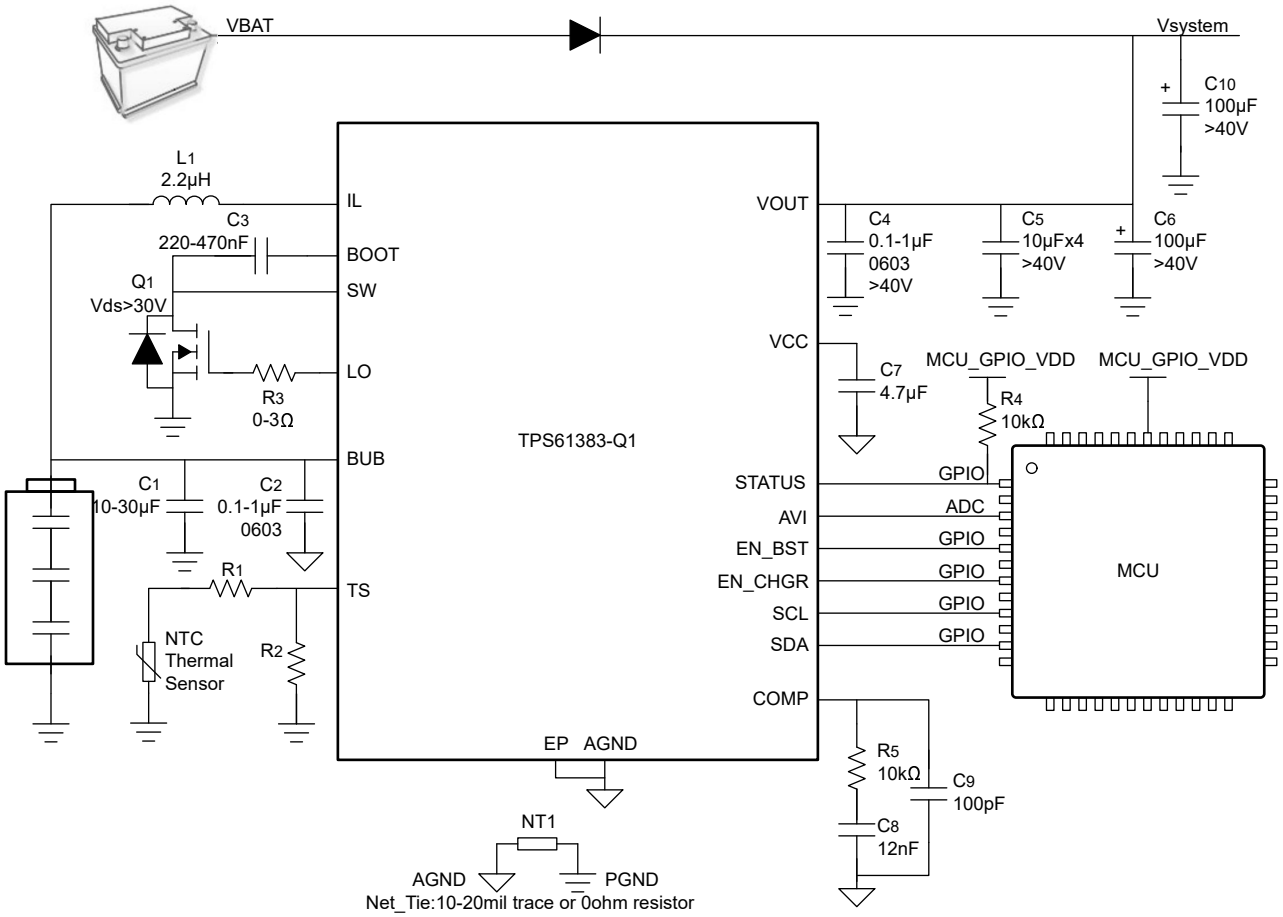


Figure 3-1. Typical E-Latch Application

TPS61383-Q1 supports four functional modes for its main functions: charger mode, boost mode, State-of-Health (SOH) mode and standby mode. The power structure of each modes are depicted by the following images.

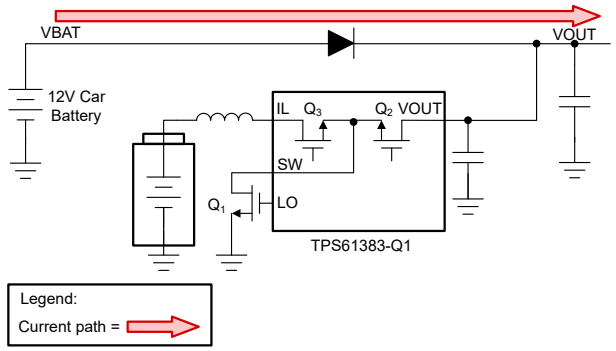


Figure 3-2. Standby Mode

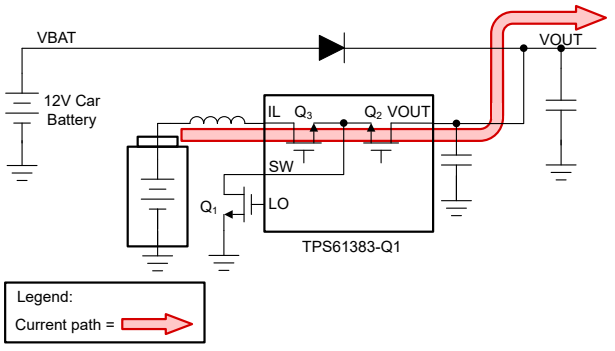


Figure 3-3. Boost Mode

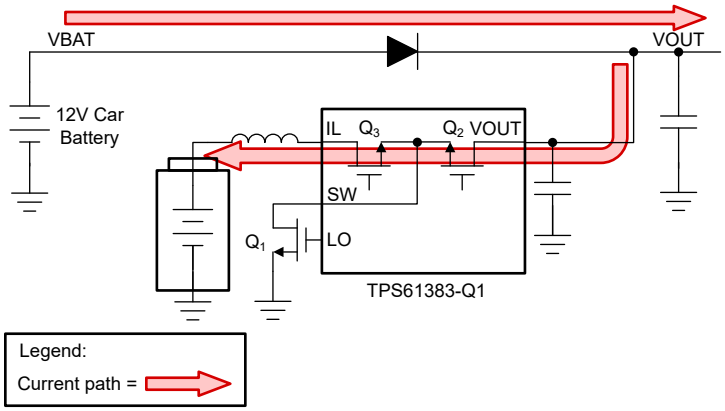


Figure 3-4. Charger Mode

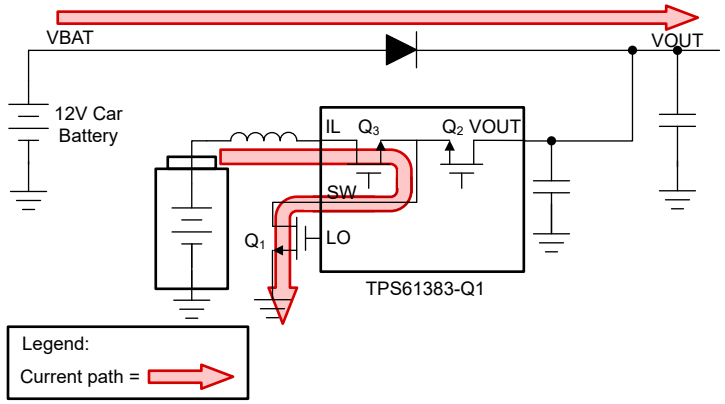


Figure 3-5. SOH Mode

TPS61383-Q1 applies AND logic on its EN pins and I2C EN bits. The boost function is enabled when EN_BST pin and BST_EN bit is both high. Charger is enabled when EN_CHGR pin is high and CHGR_SOH_EN bit is 01b. SOH is enabled when EN_CHGR pin is high and CHGR_SOH_EN bit is 10b.

Table 3-1. Operating Modes Control Logic

Boost Enable: EN_BST pin AND BST_EN Bit	Charger/SOH Enable: EN_CHGR AND CHGR_SOH_EN Bit	Device State	Device Operation
EN_BST = 0 or BST_EN = 0	EN_CHGR = 1 and CHGR_SOH_EN = 01b	Pure charger	Charger Active.
EN_BST = 0 or BST_EN = 0	EN_CHGR = 1 and CHGR_SOH_EN = 10b	Pure SOH	SOH Active.
EN_BST = 1 and BST_EN = 1	EN_CHGR = 0 or CHGR_SOH_EN=00b	Automatic boost and standby	• Boost Active: V_{OUT} < BST_WAKE • Standby Active: V_{OUT} > $V_{OUT\_STANDBY}$(106%V_{OUT_TARGET})
EN_BST = 1 and BST_EN = 1	EN_CHGR = 1 and CHGR_SOH_EN = 01b	Automatic boost and charger mode	• Boost Active: V_{OUT} < BST_WAKE • Charger Active: V_{OUT} > $V_{OUT\_STANDBY}$(106%V_{OUT_TARGET})
EN_BST = 1 and BST_EN = 1	EN_CHGR = 1 and CHGR_SOH_EN = 10b	Automatic boost and SOH mode	• Boost Active: V_{OUT} < BST_WAKE • SOH Active: V_{OUT} > $V_{OUT\_STANDBY}$(106%V_{OUT_TARGET})

When multiple functions are enabled, TPS61383-Q1 monitors system voltage by VOUT pin to decide which function mode to enter. The IC stays in standby/ charger or SOH mode (depending on which function is enabled) when system voltage is sufficient and automatically transition into boost mode when car battery malfunction occurs and voltage drop on system voltage is detected. The different operation modes are shown in the Figure 3-6

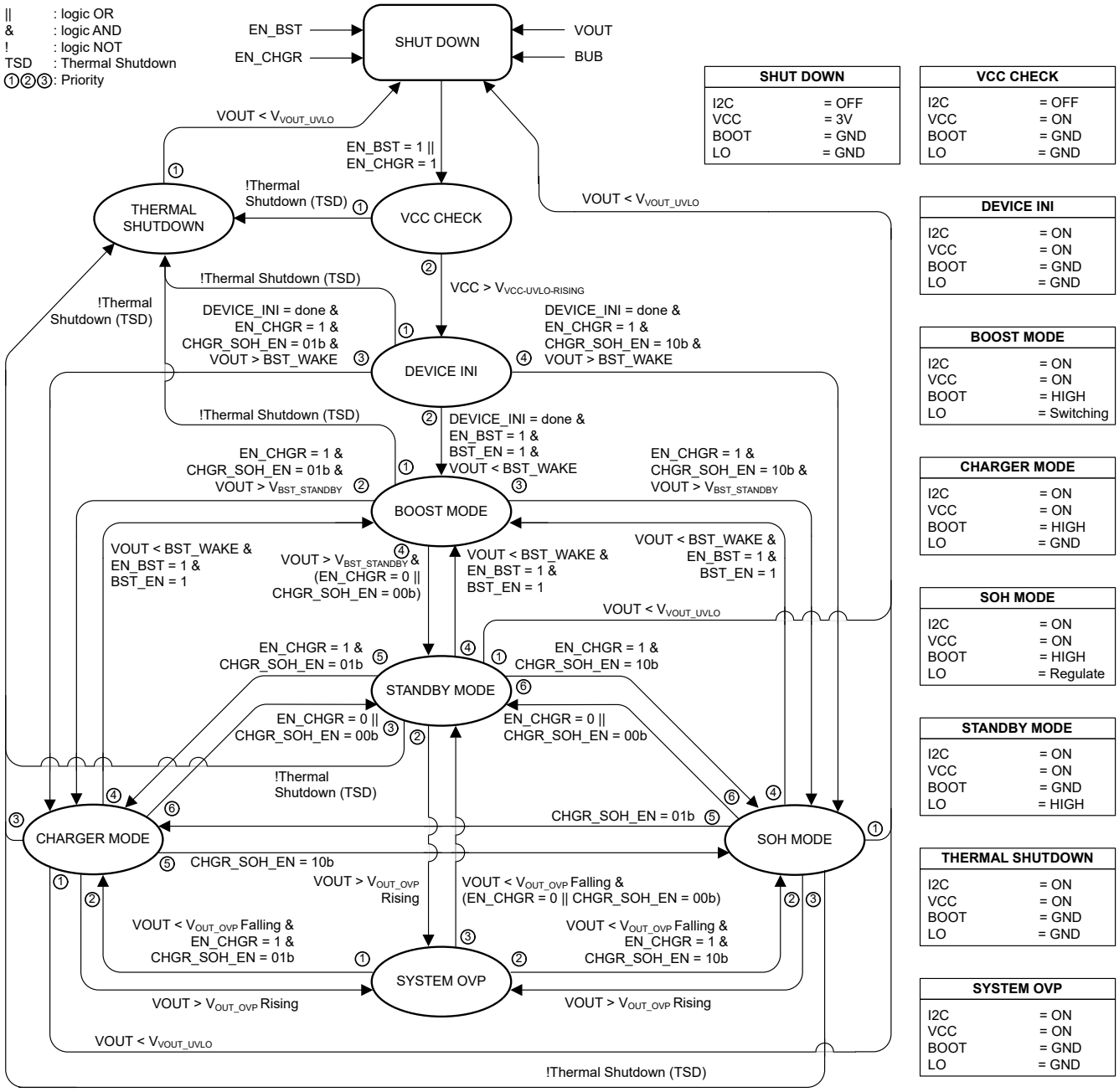


Figure 3-6. Functional State Diagram

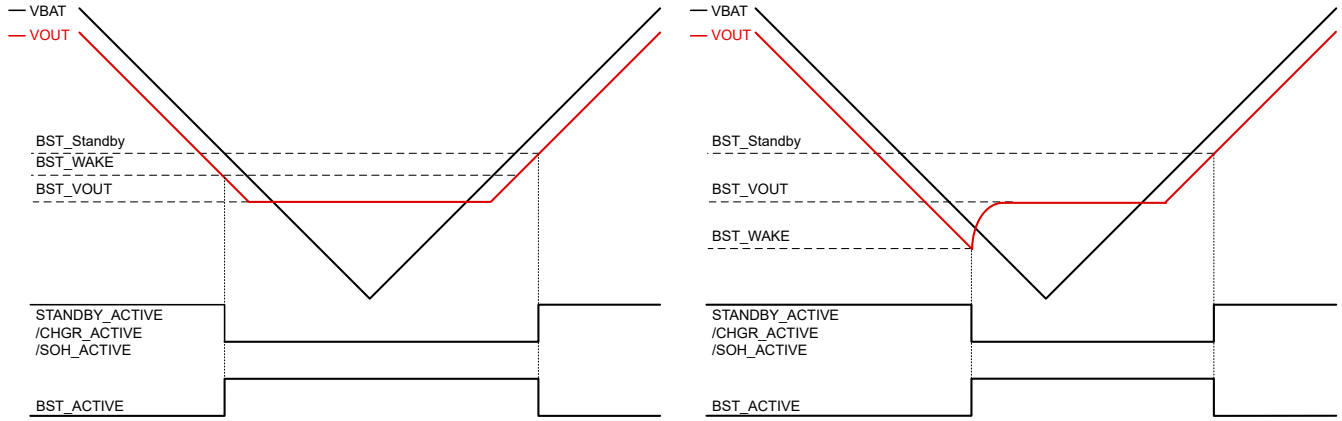


Figure 3-7. Automatic Boost and Standby/Charger/SOH Transition Logic

3.1.1 Super Capacitor Charger Function Introduction

TPS61383-Q1 integrates buck charger function with I2C selectable charging current up to 7A. The buck charger folds its frequency when super capacitor voltage is 0V and volt-second balance cannot be achieved. In this way, the IC achieves high current charging even with 0V super capacitor. In buck charger mode, Q2 and Q1 switches as buck leg while Q3 is fully turned on.

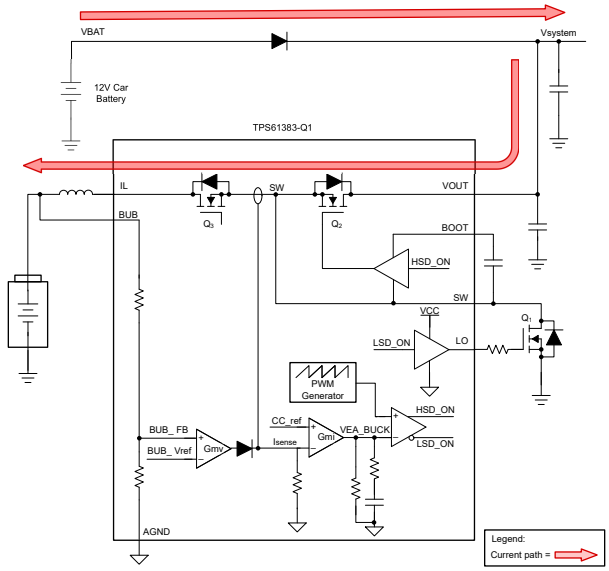


Figure 3-8. Buck Charger Structure

TPS61383-Q1 charges back up battery with the integrated charging profile for the super capacitor. When the back up super capacitor voltage is below target voltage (Set by I2C bits BUB_CV and BUB_CELL) , the device enters CC charge phase. In this phase, the device charges the super capacitor by CC current configured by BUB_CC bits.

After super capacitor is charged to its target voltage, TPS61383-Q1 enters CV charge phase. The device decrease charging current to regulate the super capacitor voltage until the current drops below a pre-set threshold, then the device terminates charging.

If configured as recharge disabled (By I2C bits BUB_TER), the device does not re-charge after terminated unless the EN_CHGR pin or CHGR_EN bit is toggled.

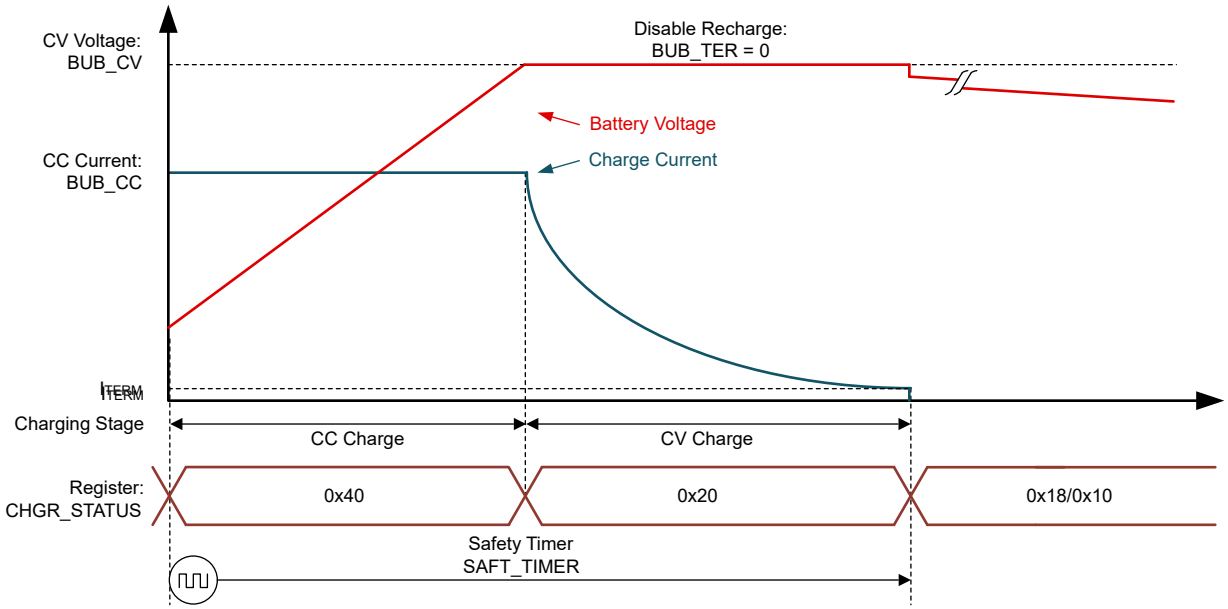
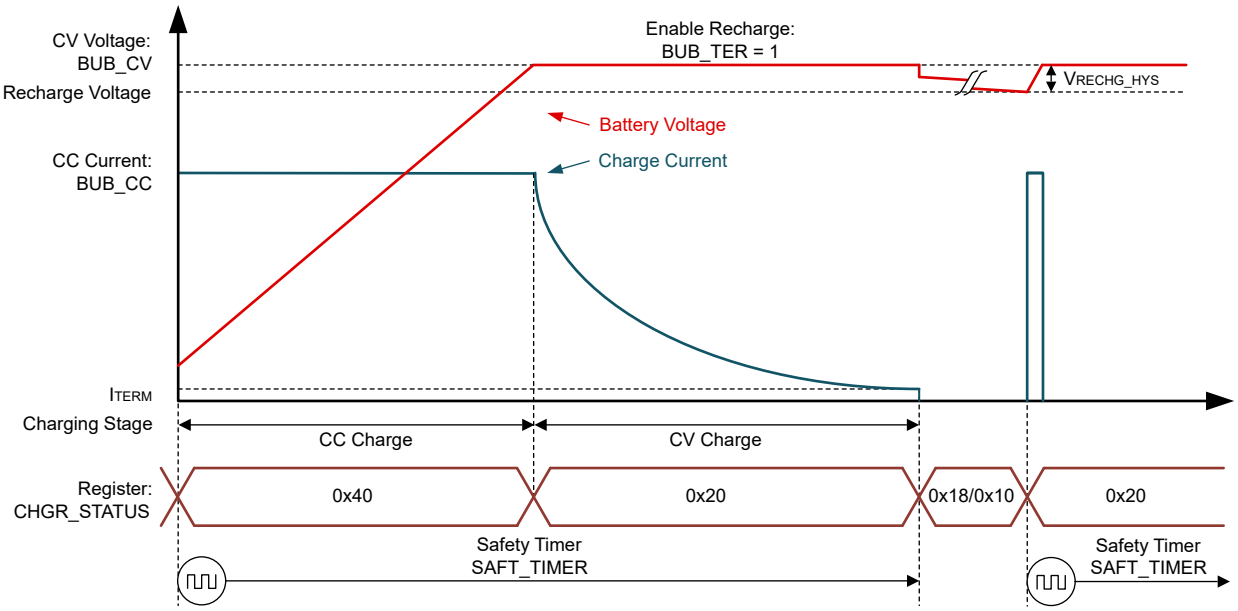


Figure 3-9. Super Capacitor Charging Profile, Re-Charge Disabled

If recharge is enabled, the device pauses charging temporarily and automatically re-charges when BUB voltage drops below V_{RECHG} threshold.

Figure 3-10. Super Capacitor Charging Profile, Re-Charge Enabled



For buck charger, the device available duty range is limited by minimum on-time of the Q1 and Q2, so 400kHz buck operation is only available when BUB voltage is between 1V and 92.6% VOUT. If BUB voltage is below 1V or above 92.6% VOUT, TPS61383-Q1 triggers duty fault logic.

TPS61383-Q1 folds its frequency when the duty fault logic is triggered. When BUB voltage is lower than 1V, the TPS61383-Q1 fold its frequency to 100kHz.This allows the device to charge a 0V super capacitor without hiccup operation.

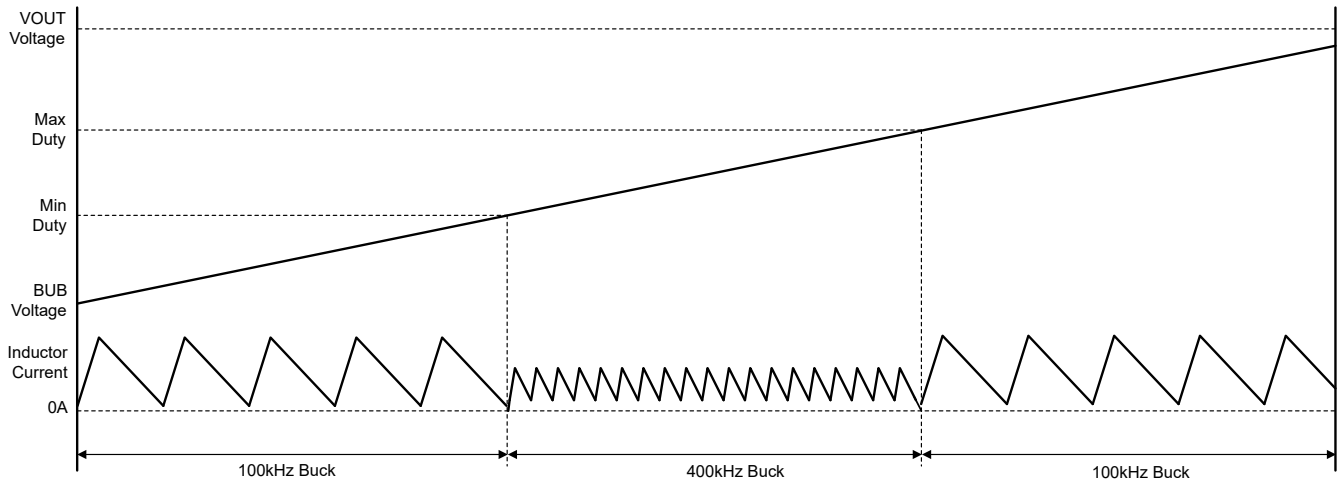


Figure 3-11. 400kHz Buck Charging Operation

3.1.2 Boost Function Introduction

The TPS61383-Q1 integrates synchronous boost converter with load disconnect function. The boost function supports input voltage from 0.5V to 12V and output voltage up to 12V with 5-30A programmable average input current limit.

For back-up power application, when boost function is enabled, TPS61383-Q1 detects system voltage with VOUT pin (Connected to your system power rail) and automatically transition into boost mode when a power interruption of the system is detected. Taking automatic boost and standby mode as an example, the device works in standby mode when Vout is normal. When the power failure occurs and Vout drops below than min{V_{BST_WAKEUP}(Set by I2C bits BST_WAKE), $V_{BST\_STANDBY}$ (BST_VOUT ×106%)}, the device enters boost mode to maintain the output voltage.

When the 12V main battery recovers and Vout rises higher than $V_{BST\_STANDBY}$, the device enter standby mode.

The V_{BST_WAKEUP} is configured to BST_VOUT ×103% (BST_WAKE = 111b) by default to achieve smaller voltage drop during transition into boost mode. But TPS61383-Q1 also allows configuring V_{BST_WAKEUP} lower than boost output voltage to avoid entering boost mode at temporary voltage drop like cold crank conditions. Choose higher V_{BST_WAKEUP} for smaller voltage drop or choose lower V_{BST_WAKEUP} to avoid entering boost mode at cold crank condition and improve back up battery life.

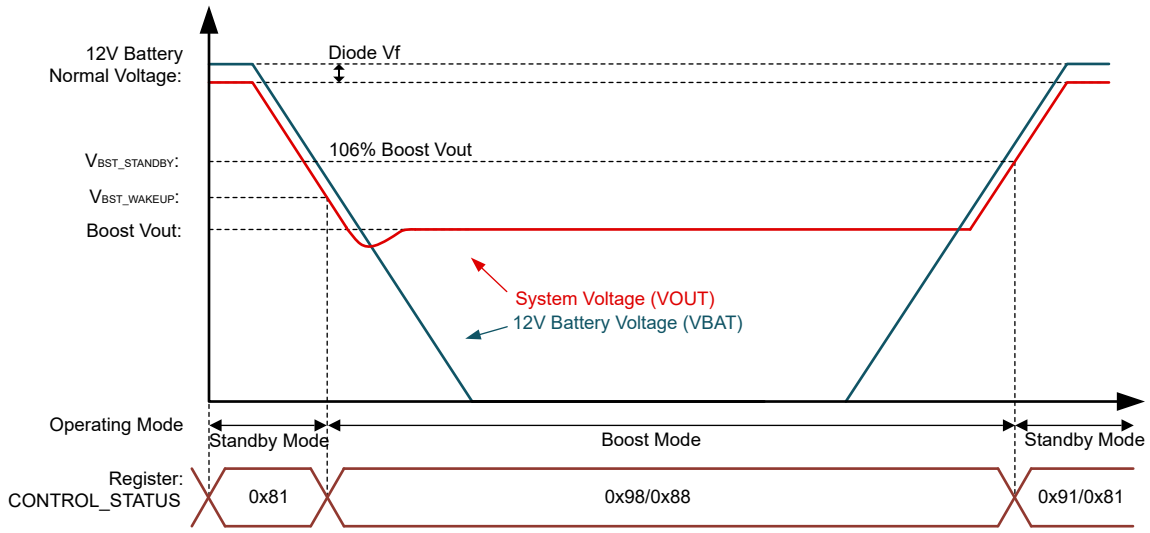


Figure 3-12. Case1: V_{BST_WAKEUP} > BST_VOUT

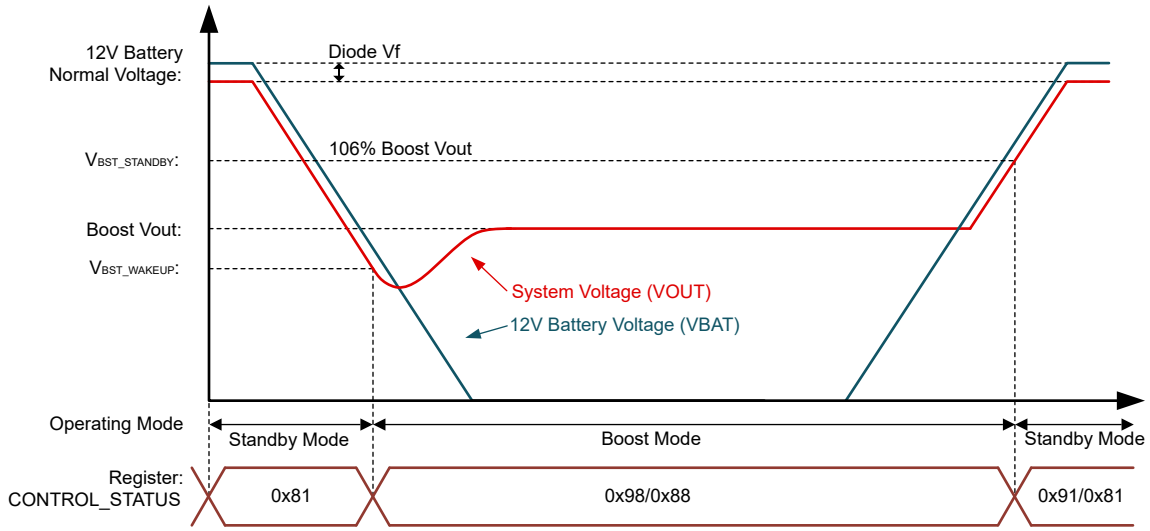


Figure 3-13. Case2: V_{BST_WAKEUP} < BST_VOUT

TPS61383-Q1 also supports manual transition into boost mode by controlling external EN pins. Manual transition by EN pins allows user to shutdown the IC when 12V battery voltage is normal and saves quiescent current. But external voltage detection circuit and MCU are required to control EN pins.

The device requires 50us(t_{EN_delay1}) delay time to initialize its internal circuit from shutdown mode. After initialized, the device takes approximately 20μs(t_{EN_delay2}) delay time from standby mode to boost mode.

For back up power applications, TI suggests setting up two threshold to enable our device. Use the $V_{Pre\text{-}ENABLE}$ threshold to control EN_CHGR pin and initialize the device in advance. And use the V_{BST_EN} threshold to control EN_BST pin. This EN sequence reduce the delay time entering boost mode (Only t_{EN_delay2}).

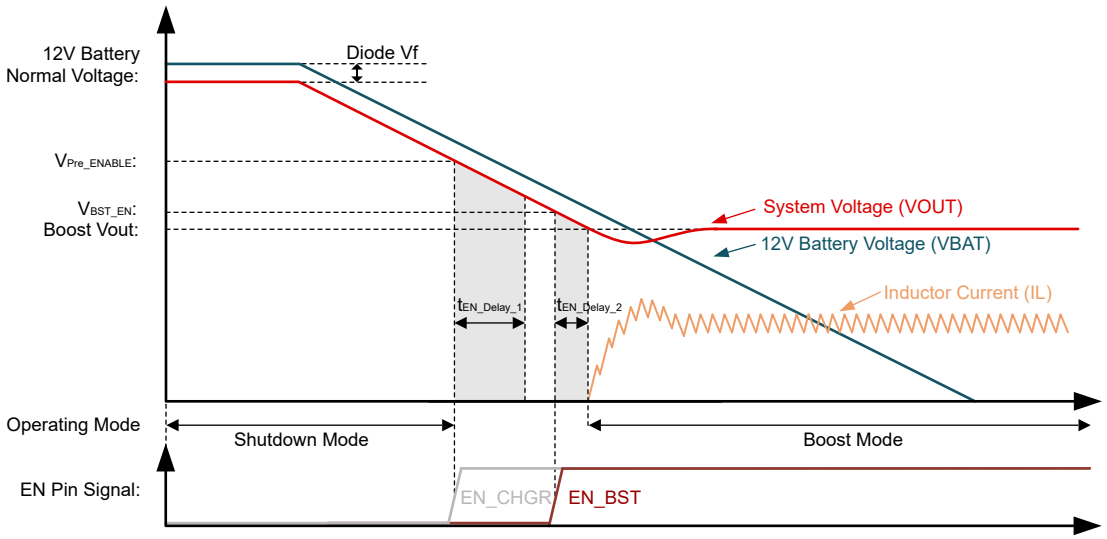


Figure 3-14. Manual Transition into Boost Mode

3.1.3 Super Capacitor Bleeding

In order to avoid degradation of the super capacitor and improve super capacitor health, it'll be necessay to design discharge circuits to discharge the super capacitor during car parking (ignition off) and avoid staying in maximum charge for most of its lifetime. TPS61383-Q1 integrates constant current discharge function that can be used for super capacitor state of health detection and bleeding. The steps below give an example on how to bleed the super capacitor with the system MCU:

- Enable SOH mode (Register 0x0B: CONTROL_STATUS, CHGR_SOH_EN bits)
- Set SOH discharge current to 100mA (Register 0x09: SOH_SET1, SOH_I bits)

3.2 Hardware Design Procedure

The following table provides the parameters for our detailed design procedure example:

Table 3-2. Design Requirements

Parameters	Values
Car Battery Input Voltage:	Typical: 6~18V, load damp: up to 40V
Back-up Battery	3s super capacitor
Back-up Battery Voltage:	1 ~ 7.5V
Charging Current:	3A
Charging Time	25s
Battery Health Detection Current:	1A
Boost Output Voltage:	12V
Boost Output Current:	4A
Mode Selection	Automatic Charger and Boost Mode
Voltage Drop during Mode Transient	<=500mV

3.2.1 Selecting the External MOSFET

TPS61383-Q1 requires an external MOSFET (Q1) as its boost low side switch and SOH discharge switch. The external MOSFET is selected depending on its thermal performance, V_{DS} voltage and I_d current.

- TPS61383-Q1 supports only n-channel MOSFET as Q1.
- Recommend Qgd< 5nC. Qgd do not exceed 10nC at most.
- Vplateau 2-3V. Do not exceed 3.5V at most.
- Rdson low as possible. Recommend Rdson less than 15mohm at most
- The drain-source breakdown voltage, V(BR)DSS >= 30V
- The continuous drain current is larger than the maximum peak current in the boost mode:

$$I_{peak} = \frac{I_{OUT}}{(1-D)\cdot eff} + \frac{V_{BUB}\cdot D}{2L\cdot f_{SW}} \quad (1)$$

where

- I_{OUT} is the maximum load current in boost mode.
- D is the duty cycle of boost operation
- eff is the boost mode efficiency
- L is the boost inductance
- f_{sw} is the switching frequency in boost mode
- V_{BUB} is the input voltage on BUB pin

3.2.2 Inductor Selection

TI suggests 2.2µH for TPS61383-Q1.

The current flowing through the inductor is the inductor ripple current plus the average input current. During power up, load faults, or transient load conditions, the inductor current increases above the peak inductor current calculated.

Inductor values has ±20%, or even ±30%, tolerance with no current bias. When the inductor current approaches the saturation level, the inductance decreases 20% to 35% from the value at 0-A bias current, depending on how the inductor vendor defines saturation. When selecting an inductor, make sure the rated current, especially the saturation current, is larger than its peak current during the operation.

The inductor peak current varies as a function of the load, switching frequency, and input and output voltages. The peak current is calculated by:

$$I_{peak} = \frac{I_{OUT}}{(1-D)\cdot eff} + \frac{V_{BUB}\cdot D}{2L\cdot f_{SW}} \quad (2)$$

Select the inductor with a saturation current rating higher than the maximum inductor current.

where

- I_{peak} is the peak current of the inductor
- I_{OUT} is the output current
- D is the duty cycle
- eff is the efficiency
- V_{BUB} is the input voltage
- L is the inductance
- f_{SW} is the switching frequency

The heat rating current (RMS) is calculated with:

$$I_{LRMS} = \sqrt{\left(I_{BUB}^2 + \Delta I_L{}^2\right)/12} \quad (3)$$

where

- I_{LRMS} is the RMS current of the inductor
- I_{BUB} is the input current of the inductor
- ΔI_L is the ripple current of the inductor

It is important that the peak current does not exceed the inductor saturation current and the RMS current is not over the temperature-related rating current of the inductors.

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and also the frequency-dependent loss. An inductor with lower DCR is basically recommended for higher efficiency. However, it is usually a tradeoff between the loss and foot print. Table 3-3 lists some recommended inductors. In this application example, the Coilcraft inductor XGL1060-222 is selected for its small size, high saturation current, and small DCR.

Table 3-3. Recommended Inductors for the TPS61383-Q1

PART NUMBER	L (µH)	DCR TYPICAL(mΩ)	SATURATION CURRENT (A)	HEAT RATING CURRENT (A)	SIZE (L × W × H)	VENDOR (1)
XGL1313-222MED	2.2	1.4	33.5 (20% Drop)	28.5 (ΔT 40K)	13.4 × 15.0 × 13.0	Coilcraft
XGL1060-222MED	2.2	3.8	21.5 (20% Drop)	25.3 (ΔT 40K)	10.0 × 11.3 × 6.0	Coilcraft
IHLP-4040DZ-ER2R2	2.2	8.2	25.6 (20% Drop)	12.0 (ΔT 40K)	10.16 × 10.195 × 4.0	Vishay
IHLP-6767DZ-ER2R2	2.2	4.57	17.5 (20% Drop)	26 (ΔT 40K)	17.15 × 11.94 × 4.0	Vishay
SPM10065VC-2R2M-D	2.2	4.2	39.2(30% Drop)	17.4 (ΔT 40K)	10.5 × 10.0 × 6.5	TDK
7843340220	2.2	10	14.7 (30% Drop)	8.4 (ΔT 50K)	8.1 × 8.1 ×9.0	Würth Elektronik
784373680022	2.2	7.8	25.7 (30% Drop)	13.6 (ΔT 50K)	10 × 10.85 ×3.8	Würth Elektronik

3.2.3 Capacitor in Super Capacitor Side

The capacitance in the back-up battery side affects BUB loop stability. TI recommends placing several MLCCs with the total effective capacitance around 20µF to30µF.

If the backup battery is connected to the IC through a long cable, TI recommend adding extra 100-200uF electrolytic capacitors on BUB side. This capacitor helps suppress LC ringing caused by parasite inductance on back up battery cable. Note that the electrolytic capacitor does not replace ceramic capacitor and the ceramic capacitor still needs to be placed near the IC.

Care needs to be taken when evaluating the effective capacitance of a ceramic capacitor. For ceramic capacitors, the derating under dc bias voltage, aging, and AC signal needs to be taken into consideration. Taking Murata GCM21BR71C475KA73K as an example, the effective capacitance reduces by 56% when 8V DC voltage is applied.

3.2.4 Boost Output Capacitor

Main consideration for designing the output capacitor is the requirements for the output voltage drop when main battery fails and the device transition into boost mode. The minimum Cout is calculated by:

$$C_{out} > \frac{I_{outmax} \times 20us}{\Delta V_{outmax}} \quad (4)$$

Where

- C_{OUT} is the output capacitance
- I_{OUTMAX} is the maximum output current
- ΔV_{OUTMAX} is the maximum output voltage drop allowed when transition into boost mode

20us is the maximum transition time for the device to enter boost mode and start switching

The output ripple voltage is another factor that affects the Cout selection. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple is calculated by

$$C_{out} > \frac{I_{outmax} \times (V_{out} - V_{BUB})}{f_{sw} \times \Delta V \times V_{out}} \quad (5)$$

Where

- I_{OUT} is the output current
- V_{OUT} is the output DC voltage
- V_{BUB} is the back up battery voltage
- ΔV is the output voltage ripple required
- f_{sw} is the switching frequency

Typically, a combination of ceramic capacitors and bulk electrolytic capacitors is needed to provide low ESR, high ripple current, and small output voltage ripple.

Ceramic capacitors have DC-bias derating that significantly reduce the effective capacitance when a DC-voltage is applied. So please check the DC-bias curve at Boost Vout target voltage when calculating the capacitance.

Electrolytic capacitors has large ESR and the ESR of electrolytic capacitor increases by over 10 times under low temperature condition and seriously affect loop stability. So make sure low temperature ESR is considered when calculating loop stability. Poly-hybrid capacitors usually have smaller ESR under low temperature and is therefore more recommended.

Based on the application requirement, this application choose 100uF electrolytic capacitor with four 10uF ceramic capacitors in parallel.

3.2.5 Loop Compensation Design

TPS61383-Q1 offers Excel Design Calculation Tool on ti.com which can be used to calculate loop compensation. This section gives an example on calculating loop compensation with Excel tool.

1. Input System Parameters

   Different voltage, load current condition and different external component needs different compensation. Before calculating loop compensation, system parameters like Vin, Vout, Iload, inductance and Cout parameters should be input according to the BOM selection. Care must be taken on ESR parameters. ESR of Aluminum Electrolytic Capacitor increases up to 10 times under -40C which greatly affects loop stability. For example, if a Electrolytic Capacitor has 300mΩ typical ESR under room temperature, the ESR is able to reach 3Ω under low temperature and aging. Make sure that both typical ESR and max ESR are calculated and the loop stability is achieved under all condition.
2. Set the Crossover Frequency, f_C.

After all system parameters are ready, the calculation on loop compensation can be started. The first step is to set the loop crossover frequency, f_C. The higher the crossover frequency, the faster the loop response is. It is generally accepted that the loop gain crosses over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{zRHP}.

3. Set the Compensation Resistance, R_{COMP}.

   For a well compensated boost system, the f_C is determined by R_{COMP}.Set your desired f_C and the calculation tool can output recommended R_{COMP}.

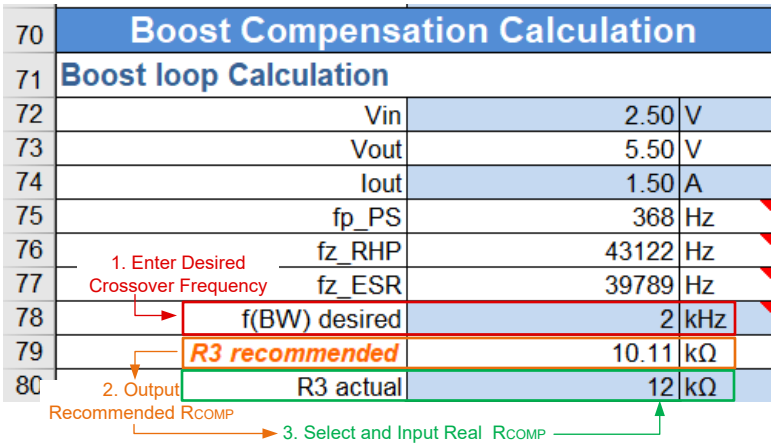


Figure 3-15. Set the Compensation Resistance

The calculation tool recommends the Rout under these assumptions: For a properly designed boost system, f_{zCOMP} must be placed below f_C to make sure of phase margin. For common R_{COMP} range, R_{COMP} must be far smaller than the amplifier output resistance R_{EA}, which makes R_{COMP} | | R_{EA} ~ = R_{COMP}. Therefore, looking at Equation 6, the initial gain $R_{COMP} \times G_{COMP} \times K_{FB}$ is determined by R_{COMP}. Therefore the f_c can be calculated by the equation that the close loop total gain $T_{(s)} = K_{PS}(s) + H_{COMP}(s)$ is zero at f_C.

$$H_{COMP} = 20lg\left(G_{COMP} \times R_{COMP} \times \frac{R_{down}}{R_{up} + R_{down}}\right) = -K_{PS}(f_c) \quad (6)$$

where

- K_{PS} is the gain of the power stage
- G_{EA} is the transconductance of the amplifier, the typical value of G_{EA} = 24μS

4. Set the Compensation Zero capacitor, C_{COMP}.

   The compensation zero needs to be placed at the power stage pole f_{pPS} to compensate the phase drop near f_{pPS}. Set $f_Z = f_P$, the C_{COMP} can be calculated . The calculation tool outputs the recommended C_{COMP} when the actual R_{COMP} is entered in line 80.

$$C_{COMP} = \frac{R_{out} \times C_{out}}{2R_{COMP}} \quad (7)$$

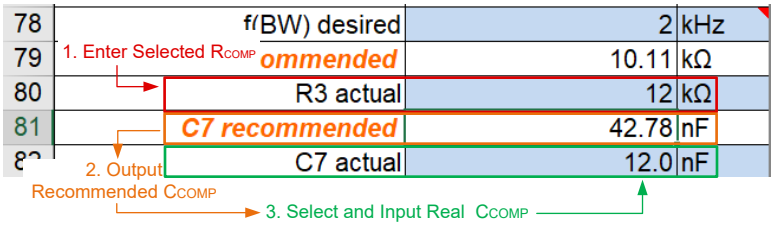


Figure 3-16. Set the Compensation Capacitance

5. Set the Compensation Pole Capacitor, C_{HF}.

The compensation pole is placed to eliminate the ESR zero produced by R_{ESR} and C_{out}. Set f_{pCOMP2} = f_{zESR}, and get:

$$C_{HF} = \frac{R_{ESR} \times C_{out}}{R_{COMP}} \quad (8)$$

The recommended C_{HF} is located at the calculation tool line 84 after the ESR and Cout is correctly entered in line 15-16.

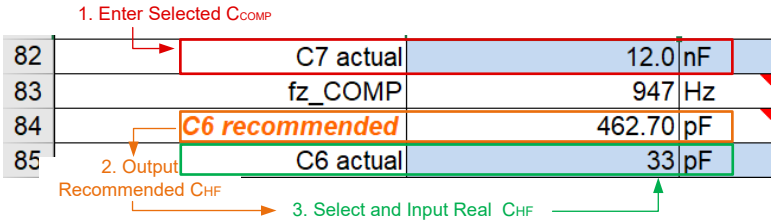


Figure 3-17. Set the Compensation Capacitance

6. Check Phase Margin and Gain Margin

The calculated compensation parameters does not always mean stability. Especially when the Cout has big ESR which bring f_{zESR} into bandwidth. TI provide excel calculation tool which generates bode plot after all compensation parameters are selected. Check the bode plot for stability after step 1-4. TI recommend Phase margin > 60deg and gain margin > 10db. Reduce desired f_c and re-calculate compensation in step1-4 if the margin does not meet requirement.

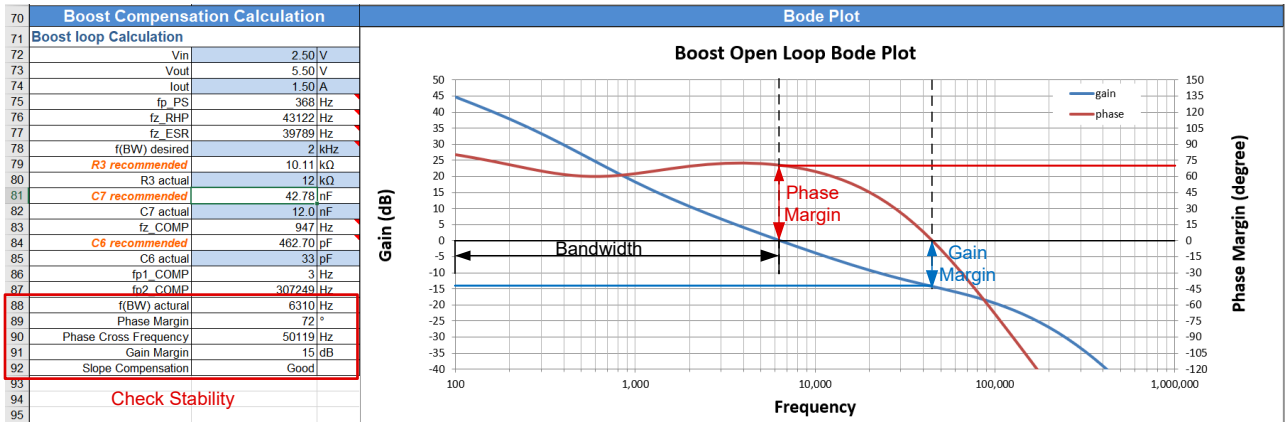


Figure 3-18. Evaluate Loop Stability

3.2.6 Key Considerations

The Schematic and Layout Guideline is available on ti.com. Please follow the design guidelines on schematic design, proper external components selection and board layout.

3.3 Software Initial Process

TPS61383-Q1 is a I2C configured device which needs to be configured to verify proper function. TI offers GUI which helps generating I2C initial content. A graphical user interface (GUI) is available at: TPS61382A-Q1_TPS61383-Q1 GUI download

The Figure 3-19 shows a register-wise view of all parameters. A detailed description of each register bit can be found in this screen. Enter this screen to read the register bits description and check register content. Select initial configuration on the right sheet and the initial content is generated on the register map.

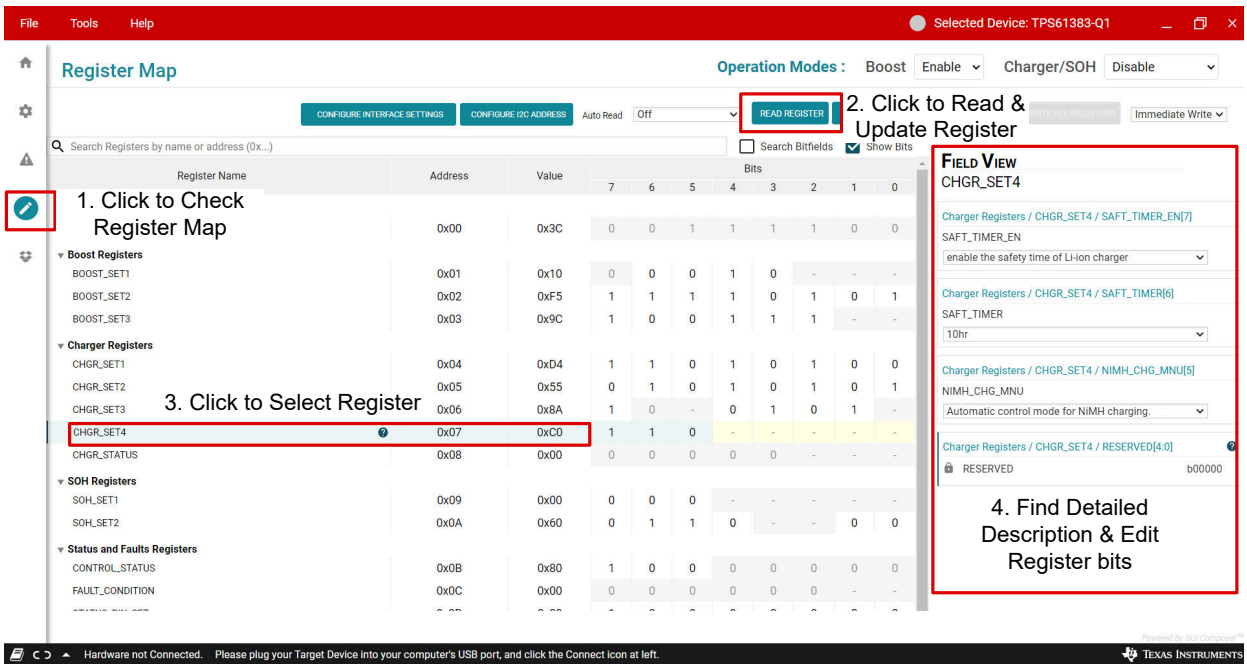


Figure 3-19. Register Map Screen

4 Super Capacitor Energy Modeling Basis and Selection

Unlike conventional electrochemical backup , super capacitor characteristics is more similar to a electrolytic capacitor. However, calculating energy by pure capacitor model $E=CV^2/2$ also does not reflect discharge progress correctly. The super capacitor internal resistance greatly affects the discharge cut-off voltage and system efficiency, especially when the motor has high stall current and big IR drop across internal resistance, the internal resistance generates huge error and makes it very hard to calculate and select the super capacitor correctly. TI offers a super capacitor calculation tool at TPS61383Q-SCAP-CALC Calculation tool:

This section explains the basic method to calculate super capacitor energy correctly and how to use the calculation tool.

4.1 Discharge Profile and Cut-off Voltage

In boost discharge mode, the boost converter (TPS61383-Q1) draws energy from this capacitor and delivers a regulated output voltage to the load. As the super capacitor discharges, the terminal voltage drops until it reaches the system cut-off voltage. The discharged energy depends on the voltage difference before and after the discharge, but the practical discharge cut-off voltage is not simply the converter's minimum input rating; it is limited by three interdependent factors:

- Boost Converter Current Limit

As super capacitor voltage drops during discharge, the super capacitor current increase. TPS61383-Q1 applies input average current limit. If super capacitor current exceeds the current limit I_{LIM}, current cannot increase and the VOUT cannot sustain. The minimum voltage V_{IN_MIN} allowed by boost current limit can be calculated as:

$$V_{IN\_MIN} = \frac{V_{OUT} I_{OUT}}{\eta_{BST} I_{LIM}} \quad (9)$$

where η_{BST} is the efficiency of the boost converter.

Considering the IR drop across super capacitor ESR, the minimum V_{SCAP} (voltage inside super capacitor) allowed by boost current limit can be calculated as:

$$V_{SCAP\_MIN} = \frac{P_{OUT}}{\eta_{BST} I_{LIM}} + I_{LIM} R_{SCAP} \quad (10)$$

- Supercapacitor Equivalent Series Resistance (ESR)

As super capacitor voltage drops and the capacitor current increases, IR drop across internal resistance increases, making super capacitor voltage further reduce. Such positive feedback greatly affects cut-off voltage and often causes discharged energy reduce far from expectation. The equivalent model has to be established to calculate the minimum voltage V_{IN_MIN} allowed by ESR:

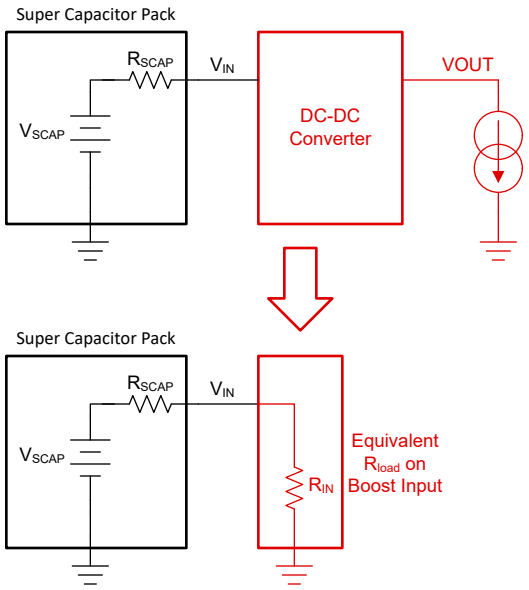


Figure 4-1. Equivalent Model

If Vout is regulated corrrectly and Iout is constant, the whole DC-DC converter can be equivalent to a constant power load. Equivalent resistance R_{IN} is given by Equation 11:

$$\left(\frac{V_{SCAP}}{R_{SCAP}+R_{IN}}\right)^2 R_{IN} = P_{OUT} \tag{11}$$

So R_{IN} is given by Equation 12

$$R_{IN} = \frac{V_{SCAP}^2 - 2R_{SCAP}P_{OUT} + \sqrt{V_{SCAP}^2\left(V_{SCAP}^2 - 4R_{SCAP}P_{OUT}\right)}}{2P_{OUT}} \tag{12}$$

As V_{SCAP} drops during discharge, R_{IN} also decreases rapidly. From the equivalent circuit, the super capacitor reaches maximum output power when $R_{IN} = R_{SCAP}$. So when the super capacitor discharges and R_{IN} decreases to $R_{IN} < R_{SCAP}$, the DC-DC converter cannot output enough power by increasing the current (even if there is an ideal DC-DC) and Vout collapse.

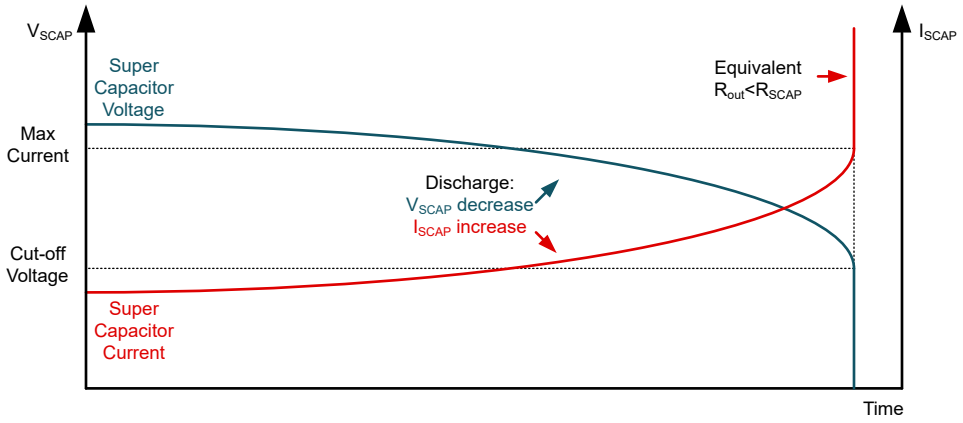


Figure 4-2. Super Capacitor Discharge

The minimum allowed voltage limited by super capacitor ESR is given by:

$$V_{SCAP\_MIN} = \sqrt{2P_{OUT}R_{SCAP}} \tag{13}$$

- Boost Undervoltage Lockout (UVLO)

Of course, boost converters have an undervoltage lockout feature that protects the device from input undervoltage. TPS61383-Q1 supports UVLO threshold down to 0.5V to support fully discharging the super capacitor. Therefore, the UVLO threshold does not limit cut-off voltage for most of the cases

In real operation, all three interdependent factors causes boost shutdown. So cut-off voltage can be given by Equation 14:

$$V_{CUT\_OFF} = MAX\left(\frac{P_{OUT}}{\eta_{BST} I_{LIM}} + I_{LIM} R_{SCAP}, \sqrt{2 P_{OUT} R_{SCAP}}\right) \quad (14)$$

4.2 Super Capacitor Discharge Energy Modeling

After calculating cut-off voltage, it is still hard to calculate super capacitor discharge energy correctly. Super capacitor internal resistance is usually 5-10 times larger than the IC MOSFET Rds-on. So total discharge efficiency becomes much lower than boost voltage, making the calculation based on $E=CV^2/2$ far from accurate. This section explains the basic method to calculate super capacitor energy correctly.

During the entire scap discharge, the loss on internal resistance can be given by Equation 15

$$loss_{RSCAP} = \int_0^T I_{scap}^2 R_{SCAP} dt \quad (15)$$

Where:

- R_{SCAP} is the internal resistance of super capacitor
- T is the duration of load
- I_{SCAP} is the discharge current on super capacitor

For I_{SCAP} , use Equation 16:

$$I_{scap} = -\frac{V_{out} I_{out}}{V_{IN} \eta_{BST}} = \frac{V_{out} I_{out}}{(V_{SCAP} - I_{SCAP} R_{SCAP}) \eta_{BST}} \quad (16)$$

Obtain I_{SCAP} as :

$$I_{SCAP} = \frac{V_{SCAP} - \sqrt{-\frac{4 V_{out} I_{out} R_{SCAP} - V_{SCAP}^2 \eta_{BST}}{\eta_{BST}}}}{2 R_{SCAP}} \quad (17)$$

In the previous equation, V_{out}, I_{out}, R_{SCAP} and η_{BST} are constant parameters, while V_{SCAP} is a unknown function of t to be solved. Based on the equivalent circuit, build the following differential equation:

$$C_{SCAP} \frac{dV_{SCAP}}{dt} = -I_{SCAP} = -\frac{V_{SCAP} - \sqrt{-\frac{4 V_{out} I_{out} R_{SCAP} - V_{SCAP}^2 \eta_{BST}}{\eta_{BST}}}}{2 R_{SCAP}} \quad (18)$$

The differential equation is separable, so the user can obtain a general solution in implicit form.

$$\frac{V_{SCAP}^2}{2b} + \frac{V_{SCAP}\sqrt{V_{SCAP}^2 - b}}{2b} - \frac{1}{2} ln\left(V_{SCAP} + \sqrt{V_{SCAP}^2 - b}\right) = -\frac{t}{2 R_{SCAP} C_{SCAP}} + C_1 \quad (19)$$

Where

$$b = \frac{4 V_{out} I_{out} R_{SCAP}}{\eta_{BST}} \quad (20)$$

The now we have Vscap, and Iscap can be solved by numerical approach. But since it's not clear enough to calculate loss by numerical methods. Do not use the implicit form to calculate I_{SCAP} and loss. Referring back to Equation 15, substitute Equation 17 and Equation 18 into Equation 15:

$$
\begin{aligned}
loss_{RSCAP} &= \int_0^T I_{SCAP}^2 R_{SCAP} dt \\
&= \int_0^T \left(-C_{SCAP}\frac{dV_{SCAP}}{dt}\right)\frac{V_{SCAP} - \sqrt{-\frac{4V_{out}I_{out}R_{SCAP} - V_{SCAP}^2\eta_{BST}}{\eta_{BST}}}}{2R_{SCAP}} R_{SCAP} dt \\
&= -\frac{C_{SCAP}}{2}\int_0^T V'_{SCAP}\left(V_{SCAP} - \sqrt{V_{SCAP}^2 - \frac{4V_{out}I_{out}R_{SCAP}}{\eta_{BST}}}\right) dt \\
&= -\frac{C_{SCAP}}{2}\int_0^T V'_{SCAP}V_{SCAP} - V'_{SCAP}\sqrt{V_{SCAP}^2 - b}\, dt
\end{aligned}
\tag{21}
$$

The integral is standard integral multiplied by differentiation. This type integral can easily be solved by substitution. Let u=V_{SCAP}:

$$
\begin{aligned}
loss_{RSCAP} &= -\frac{C_{SCAP}}{2}\int_0^T u - \sqrt{u^2 - b}\, du \\
&= \frac{C_{SCAP}}{4}\left(-V_{SCAP}^2 + V_{SCAP}\sqrt{V_{SCAP}^2 - b} - b\cdot\ln\left(V_{SCAP} + \sqrt{V_{SCAP}^2 - b}\right)\right)\Big|_0^T
\end{aligned}
\tag{22}
$$

The V_{SCAP} voltage at t=0 and t=T are given VCH and VCL. So the definite integral can be calculated by:

$$
loss_{RSCAP} = \frac{C_{SCAP}}{4}\left[V_{CH}^2 - V_{CL}^2 + V_{CL}\sqrt{V_{CL}^2 - b} - V_{CH}\sqrt{V_{CH}^2 - b} + b\left(\ln\left(V_{CH} + \sqrt{V_{CH}^2 - b}\right) - \ln\left(V_{CL} + \sqrt{V_{CL}^2 - b}\right)\right)\right] \tag{23}
$$

The VCH, VCL and b are known parameters while the only unknown parameter left is Cscap. So the loss can be given by:

$$
loss_{RSCAP} = k\, C_{SCAP} \tag{24}
$$

Where k is:

$$
k = \left[V_{CH}^2 - V_{CL}^2 + V_{CL}\sqrt{V_{CL}^2 - b} - V_{CH}\sqrt{V_{CH}^2 - b} + b\left(\ln\left(V_{CH} + \sqrt{V_{CH}^2 - b}\right) - \ln\left(V_{CL} + \sqrt{V_{CL}^2 - b}\right)\right)\right]/4 \tag{25}
$$

So the minimum C_{SCAP} can be calculated as:

$$
\begin{aligned}
C_{min} &= \frac{2V_{out}I_{out}T}{\eta_{BST}\left(V_{CH}^2 - V_{CL}^2\right)\left(1 - \frac{loss_{Rin}}{V_{out}I_{out}T + loss_{Rin}}\right)} \\
&= \frac{2V_{out}I_{out}T}{\eta_{BST}\left(V_{CH}^2 - V_{CL}^2\right)\left(1 - \frac{kC_{min}}{V_{out}I_{out}T + kC_{min}}\right)}
\end{aligned}
\tag{26}
$$

So the final minimum Cscap can be solved as:

$$
C_{min} = \frac{2V_{out}I_{out}T}{\eta_{BST}\left(V_{CH}^2 - V_{CL}^2\right) - 2k} \tag{27}
$$

Where:

$$
k = \left[V_{CH}^2 - V_{CL}^2 + V_{CL}\sqrt{V_{CL}^2 - b} - V_{CH}\sqrt{V_{CH}^2 - b} + b\left(\ln\left(V_{CH} + \sqrt{V_{CH}^2 - b}\right) - \ln\left(V_{CL} + \sqrt{V_{CL}^2 - b}\right)\right)\right]/4 \tag{28}
$$

$$
b = \frac{4V_{out}I_{out}R_{in}}{\eta} \tag{29}
$$

4.3 Calculation Example

With the previous analysis on super capacitor, calculate the requirements on the super capacitor. This section gives an example on calculating minimum Cscap. Assume an e-latch system with the following design targets:

Table 4-1. Design Requirement Example

Item	Parameter
Cell Number	3s
Super Capacitor Voltage	2.5V per cell, 7.5V total
Super Capacitor Internal Resistance	30mΩ per cell, 90mΩ total
Load Power	72W (12V, 6A)
Load Duration	10 locks, 100ms each, 1s total time
Boost Efficiency	90%
Boost Current Limit	25A

1. Calculate VCL

$$\begin{aligned} V_{CUT\_OFF} &= MAX\left(\frac{P_{OUT}}{\eta_{BST} I_{LIM}} + I_{LIM} R_{SCAP},\ \sqrt{2 P_{OUT} R_{SCAP}}\right) \\ &= MAX\left(\frac{72W}{0.9 \times 25A} + 25A \times 90m\Omega,\ \sqrt{2 \times 72W \times 90m\Omega}\right) \\ &= MAX(5.45V,\ 3.6V) \\ &= 5.45V \end{aligned} \tag{30}$$

2. Calculate parameter b and k

$$b = \frac{4 V_{out} I_{out} R_{SCAP}}{\eta_{BST}} = 28.8W.\Omega \tag{31}$$

$$\begin{aligned} k &= \left[V_{CH}^2 - V_{CL}^2 + V_{CL}\sqrt{V_{CL}^2 - b} - V_{CH}\sqrt{V_{CH}^2 - b} + b\left(\ln\left(V_{CH} + \sqrt{V_{CH}^2 - b}\right) - \ln\left(V_{CL} + \sqrt{V_{CL}^2 - b}\right)\right)\right]/4 \\ &= 3.064V^2 \end{aligned} \tag{32}$$

3. Calculate Cmin

$$\begin{aligned} C_{min} &= \frac{2 V_{out} I_{out} T}{\eta_{BST}\left(V_{CH}^2 - V_{CL}^2\right) - 2k} \\ &= \frac{2 \times 72W \times 1s}{0.9\left(7.5^2 - 5.45^2\right) - 2 \times 3.064V^2} \\ &= 8.1F \end{aligned} \tag{33}$$

4. Verifying Results

   According to the previous calculation results, a 25F per cell (8.333F for total of three cell) super capacitor is selected. So the maximum energy that can be discharged is:

$$E_{SCAP} = \frac{1}{2} C_{SCAP} V_{CH}^2 - \frac{1}{2} C_{SCAP} V_{CL}^2 = 110.61J \tag{34}$$

   The energy consumption for load is:

$$E_{load} = V_{out} I_{out} T = 72J \tag{35}$$

   The loss on TPS61383 is:

$$loss_{BST} = E_{load}\left(\frac{1}{\eta_{BST}} - 1\right) = 8J \tag{36}$$

   The loss on super capacitor internal resistor is:

$$loss_{RSCAP} = k\,C_{SCAP} = 2.553J \quad (37)$$

The total energy consumption is:

$$E_{total} = E_{load} + loss_{BST} + loss_{RSCAP} = 82.533J \quad (38)$$

The energy margin is:

$$E_{margin} = E_{SCAP} - E_{total} = 27.4J \quad (39)$$

4.4 Super Capacitor Excel Calculation Tool

The e-latch actuator is typically a small brushed DC motor (rated 6V–12V) that drives a gear train to release the latch mechanism. A typical motor unlock load profile consists of three stages: *Start up*, *Steady state* and *Stall*. This load profile cycle continues for 12-20 times, which complicates the calculation on super capacitor energy. TI provides an Excel calculation tool to achieve fast, accurate calculation and help with the system design. The calculation tool is availablehere:

Assuming a e-latch system with below load profile:

Table 4-2. Design Requirement Example

Item	Parameter
Cell Number	3s
Super Capacitor Voltage	2.7V per cell, 8.1V total
Super Capacitor Capacitance	25F per cell, 8.33F total
Super Capacitor Internal Resistance	25mΩ per cell, 90mΩ total
Load Profile	Start State: 5A, 20ms
	Steady State: 3A, 150ms
	Stall: 8A, 50ms
Unlock Rounds	6 locks, 2 rounds each, 12 rounds total

Input these parameters and click the button to calculate discharge profile. The calculation can take some time. After calculation is completed, the tool shows *Calculation Complete* and update discharge curve.

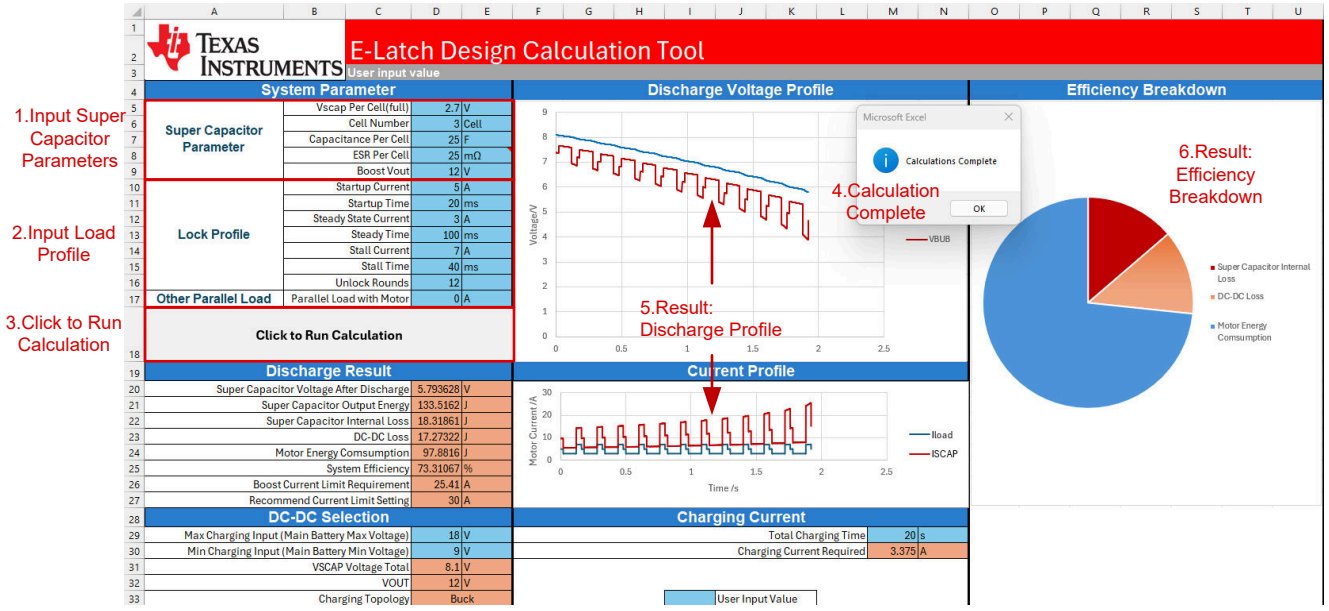


Figure 4-3. Super Capacitor Calculation Tool

As previously mentioned in Figure 4-2. When high current is applied and equivalent ROUT is lower than internal resistance RIN, the Vout drops and cannot be sustained. In this case, TI recommends selecting a super capacitor with lower ESR or adding cell number.

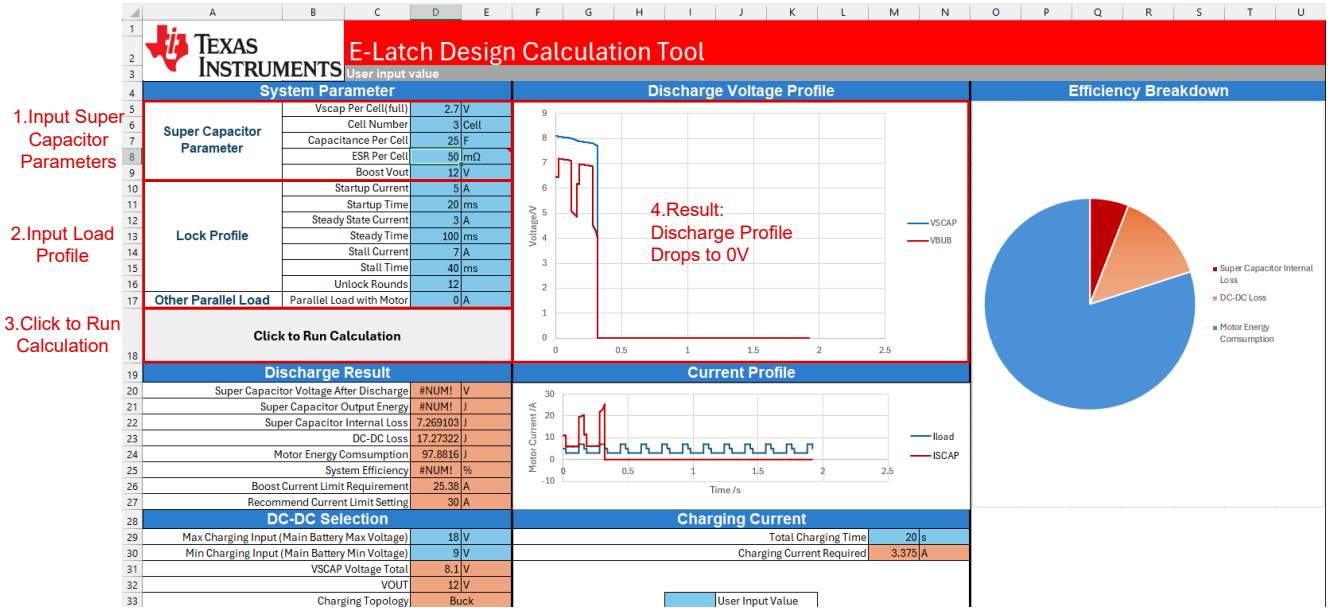


Figure 4-4. Voltage Cannot Sustain

5 Super Capacitor Management

In e-latch systems, an Analog Front End (AFE) monitor and protector is required to monitor and manage the supercapacitor cells. The AFE performs three essential functions:

1. Cell Balance: Cell balancing is an essential function for multi-cell super capacitor system. Cells in a series string have slight variations in capacitance and leakage current, causing voltages drift apart over repeated charge-discharge cycles. Without balancing, the weakest cell may experience overvoltage (during charging) or premature undervoltage (during discharging), reducing usable capacity and lifespan.
2. Voltage Detection for Each Cell: Each supercapacitor cell in the series stack must be individually monitored to prevent overvoltage or undervoltage conditions.
3. Health Diagnosis (State-of-Health, SOH): Supercapacitor cells degrade due to aging, temperature cycling, and charge-discharge stress. Health detection for each cell is mandatory to verify system safety.

This section introduces how to monitor and manage the supercapacitor cells with TI monitor and protector BQ76907-Q1.

5.1 Voltage Monitoring with BQ76907-Q1

The BQ76907-Q1 battery monitor integrates a multiplexed voltage ADC that measures individual cell voltages differentially, processes the results with on-chip calibration, and exposes each result as a signed 16-bit integer via I²C direct commands. The ADC runs a continuous ADSCAN loop in NORMAL mode. Each loop slot width is independently programmable (366µs, 732µs, 1.46ms, 2.93ms), trading conversion speed for effective resolution (13–16 bits). The default cell slot width of 2.93 ms delivers 16-bit effective resolution. In SLEEP mode the ADC runs a full burst on a programmable timer interval and then idles to save power. Taking normal mode as an example, this section describes the basic steps to implement a reliable cell voltage readout in firmware.

Table 5-1. NORMAL Mode ADSCAN Slot Assignment (7-Cell Configuration)

Slot	Measurement
0	Cell 1 Voltage (VC1 − VC0)
1	Cell 2 Voltage (VC2 − VC1)
2	Cell 3 Voltage (VC3 − VC2)
3	Cell 4 Voltage (VC4 − VC3)
4	Cell 5 Voltage (VC5 − VC4)
5	Cell 6 Voltage (VC6 − VC5)
6	Cell 7 Voltage (VC7 − VC6)
7	Shared Slot (rotates: TS, Int Temp, Stack, REG18, VSS)

- Step 1: I2C Write Direct Commands

All cell voltages are exposed as direct I²C commands. Each command occupies two consecutive register addresses containing the little-endian signed 16-bit result in millivolts. The low byte is at the even (base) address; the high byte is at the odd (base+1) address.

Table 5-2. Cell Voltage Direct Commands

Address	Name	Type	Unit	Access
0x14–0x15	Cell 1 Voltage	I2	mV	R
0x16–0x17	Cell 2 Voltage	I2	mV	R
0x18–0x19	Cell 3 Voltage	I2	mV	R
0x1A–0x1B	Cell 4 Voltage	I2	mV	R
0x1C–0x1D	Cell 5 Voltage	I2	mV	R
0x1E–0x1F	Cell 6 Voltage	I2	mV	R
0x20–0x21	Cell 7 Voltage	I2	mV	R
0x26–0x27	Stack Voltage	U2	mV	R

- Step 2: I2C Readout ADC Data

BQ76907-Q1 returns 16 bits ADC data in little-endian order. Taking Cell 1 voltage as an example. Register 0x14 holds bits [7:0] (LSB); register 0x15 holds bits [15:8] (MSB). The value is in millivolts, so no scaling is required. Negative values (possible if a cell input is driven slightly below its reference, within the −0.2 V minimum) are encoded in two's complement.

Table 5-3. Cell 1 Voltage: Register Byte Layout

Register	Byte Role	Bit Range	Example (2700 mV)	Hex Value
0x14	LSB (Byte 0)	bits [7:0]	2700 = 0x0A8C	0x8C
0x15	MSB (Byte 1)	bits [15:8]	2700 = 0x0A8C	0x0A

Therefore the reconstruction formula: **voltage_mV = int16_t((Byte 1 << 8) | Byte 0)**

The auto-increment behavior of the I²C block-read means that issuing a 2-byte read starting at address 0x14 returns Byte 0 first, then Byte 1 automatically, with no need to re-address. Cast the concatenated result to int16_t before use to correctly handle the two's-complement sign. Therefore the byte format of reading the Cell 1 is:

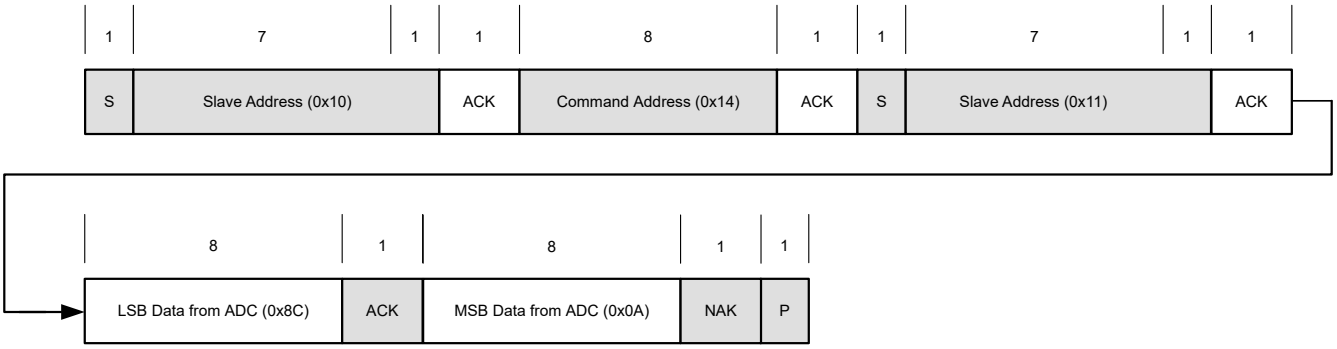


Figure 5-1. Voltage Readback of Cell 1

- Multi-Read: Readback all Cells:

For BQ76907-Q1, all 7 cell voltages occupy 14 consecutive bytes at addresses 0x14–0x21. This allows user to read one single transaction starting at 0x14 with a multi-byte read returns all cell voltages automatically:

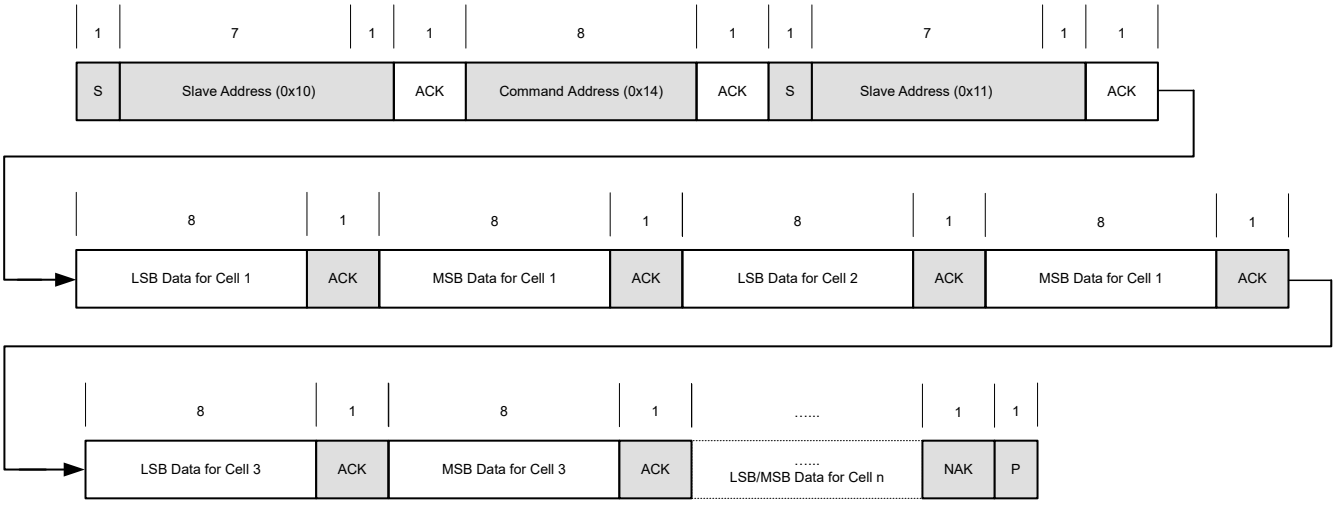


Figure 5-2. Multi Read for Cell Voltages

5.2 Cell Balancing with BQ76907-Q1

Super capacitor cell balancing is an essential function for multi-cell super capacitor system. Cells in a series string have slight variations in capacitance and leakage current, causing voltages drift apart over repeated charge-discharge cycles. Without balancing, the weakest cell may experience overvoltage (during charging) or premature undervoltage (during discharging), reducing usable capacity and lifespan. The BQ76907-Q1 integrates passive balancing switch (internal NMOS FET, R_{st}(ON) equals approximately 80Ω) per cell input pair. When the host enables a cell, the internal FET shorts VC_n to VC_{n-1}, and balancing current flows through the two cell-input filter resistors R_n and the FET.

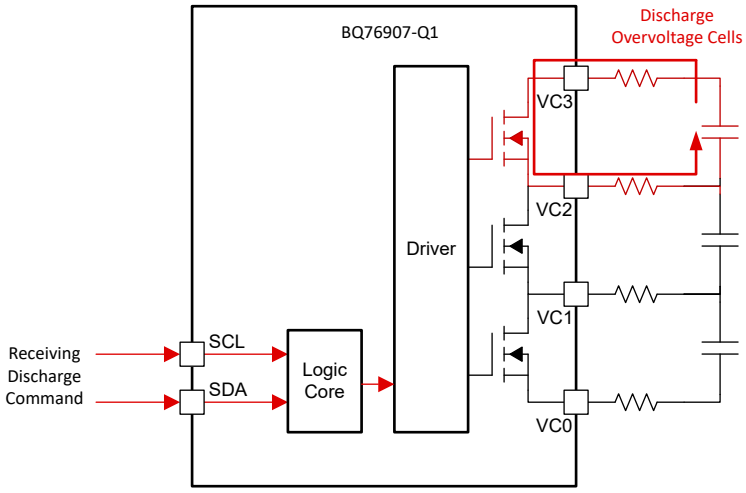


Figure 5-3. Hardware Principle of Passive Cell Balancing

5.2.1 Balancing Strategy

BQ76907-Q1 requires host to control the balancing switches. Because of the external current limit resistors, the voltage across VC pin only reflects cell voltage correctly when the balancing switch is turned off. Therefore, in a multi-cell balancing process, the workflow must be divided into two alternating phases: a **voltage detection phase** and a **discharge phase**, which are executed sequentially in an iterative manner.

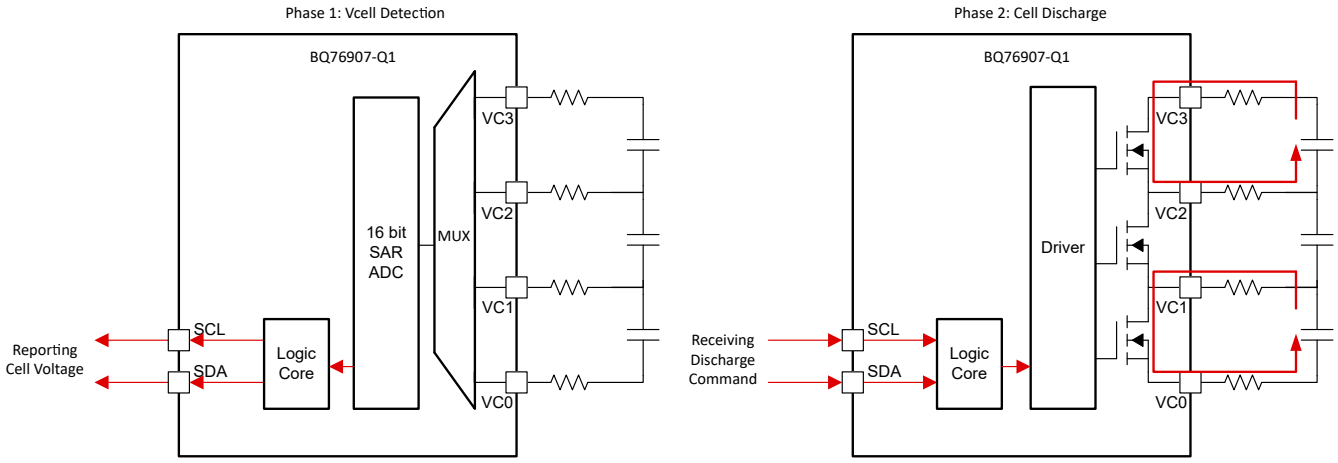


Figure 5-4. Phases of Passive Cell Balancing

BQ76907-Q1 applies passive cell balancing which discharge the over voltage cells to balance the cells. Therefore the key method is to detect the cell with lowest voltage (V_{MIN}), and discharge those cells whose voltage is far over V_{MIN}. For example , if cell 1 is 2.75V, cell 2 is 2.65V, cell 3 is 2.73V, then V_{MIN} is on cell 2.

So host should command BQ76907-Q1 to discharge cell1 and cell 3 for a period and then go back to voltage detection phase. The flowchart of super capacitor cell balancing is given below:

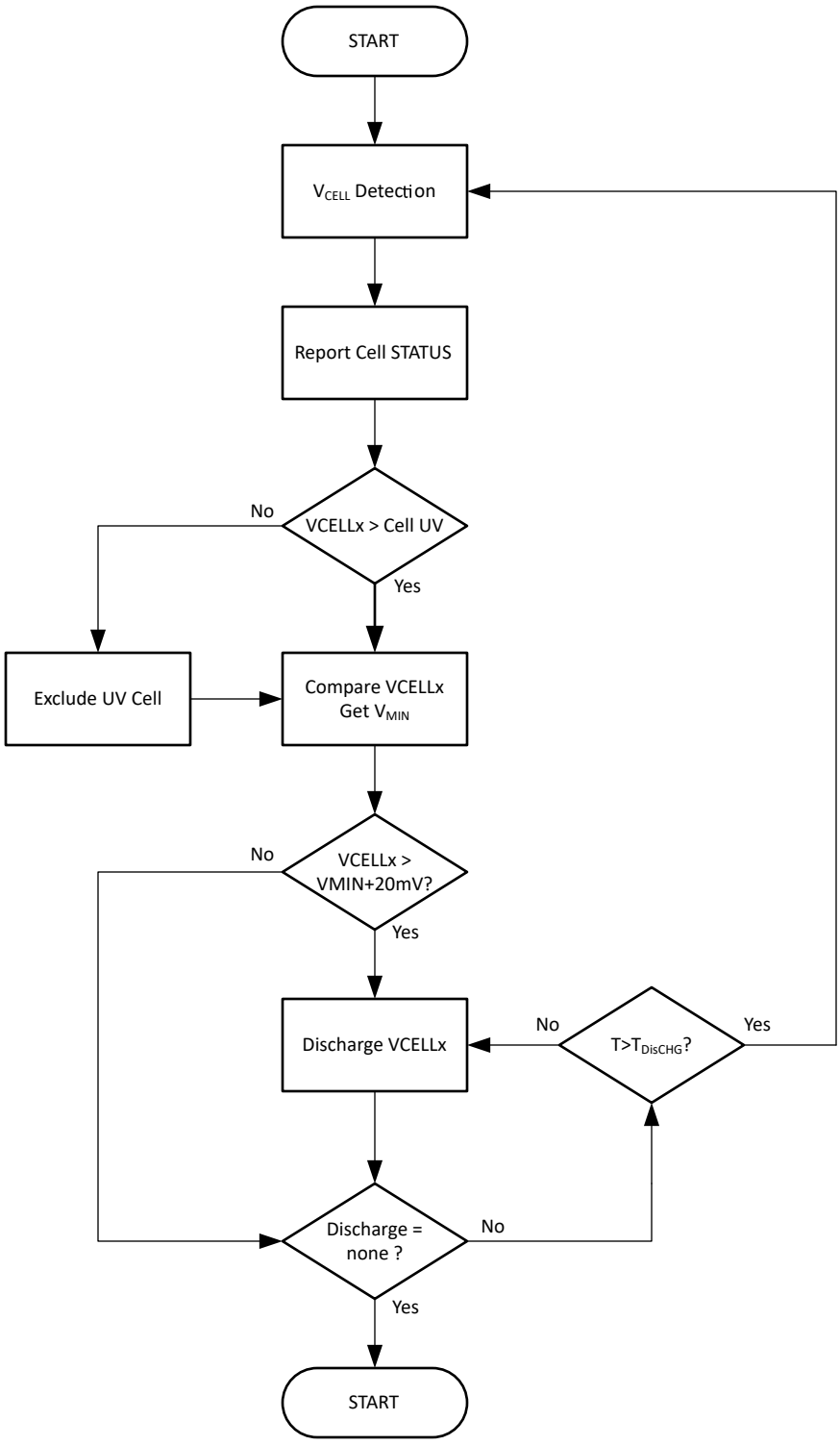


Figure 5-5. Super Capacitor Cell Balancing Flow

5.2.2 I2C Implementation

Cell balancing is controlled through the 0x0083 CB_ACTIVE_CELLS subcommand. Unlike the direct-command cell voltage registers, subcommands use an indirect addressing mechanism:

1. Send slave address (0x10)
2. Send sub-command address (0x3E)
3. Write two-byte subcommand address (0x0083)
4. Write mask data. Taking *discharge cell 1 and cell 3* as an example, in the 8 bits mask data, cell 1 and cell3 are 1. Therefore mask data should be 0b00001010 (0x0A)
5. Stop and Start
6. A checksum is written to 0x60 to commit the transaction. The checksum covers only the subcommand payload — not the I²C address bytes — using the formula: Checksum = ~(SubCmd_Lo + SubCmd_Hi + DataByte) & 0xFF
7. A checklength is written to 0x61 to commit the transaction. 0x61 provides the length of the buffer data plus 4 (that is, length of the buffer data plus the length of sub-command address 0x3E and 0x3F plus the length of 0x60 and 0x61).

Therefore, taking *discharge cell 1 and cell 3* as an example, the whole byte format is:

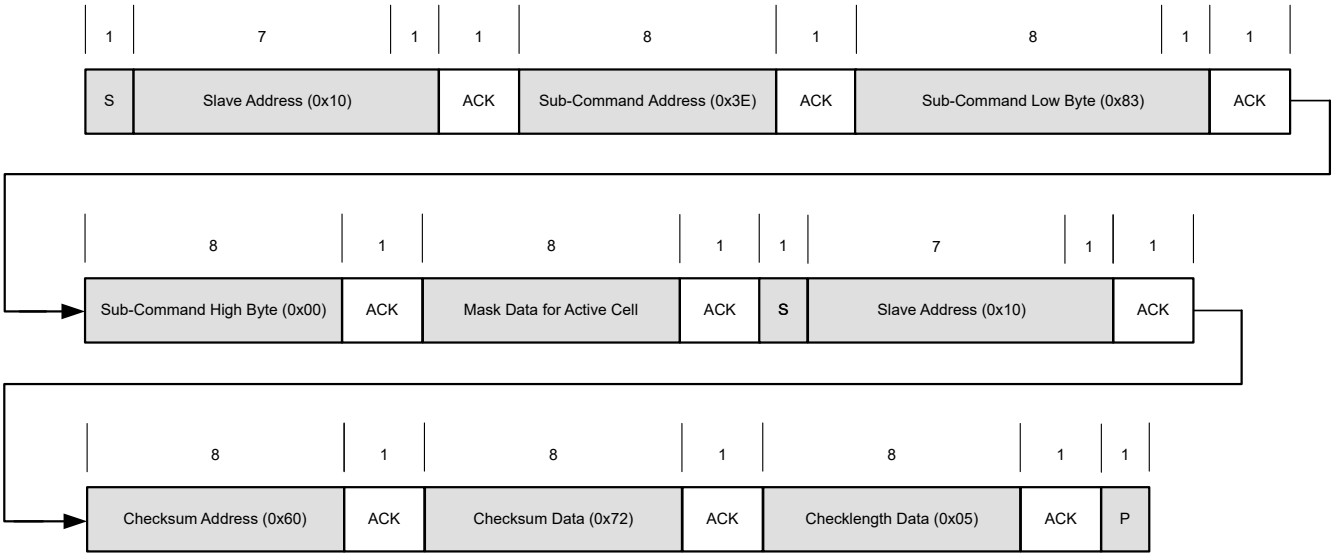


Figure 5-6. Discharge Cell 1 and Cell 3

5.2.3 Cell Balancing Current

Properly setting the battery balancing current is important for optimizing the cell-balancing function. The balancing current magnitude is jointly determined by the on-chip NMOS FET and the resistance value of the input filter resistor. The recommended minimum value of the input filter resistors when using internal balancing is 20Ω. This results in a balancing current of approximately 35mA.

$$I_{B\_alance} = \frac{V_{CELL}}{2 \times R_n + R_{CB}} = \frac{4.2}{2 \times 20 + 80} = 35mA \quad (40)$$

If OEM require a faster balancing speed than 35mA , external balancing bypass circuit can be implemented. One feasible solution is to deploy external FETs or BJTs. More design details can refer to Cell Balancing With BQ7690x Battery Monitors .

5.2.4 Low-Side Protection Circuit Design Considerations

The BQ76907-Q1 applies back to back NMOS on low side of the super capacitor pack to cut charging / dicharging path and protect the super capacitor in case of fault condition. Both charge tube CFET and discharge tube DFET are positioned between B- and PACK- and situated at the low-side of the battery pack.

For E-Latch applications, if the initial total series voltage of the supercapacitor stack falls below 3 V, the minimum supply voltage requirement of the BQ76907-Q1 cannot be satisfied. The CFET and DFET low-side switches will be disabled, isolating the battery pack ground from the system ground, which prevents charging of the supercapacitors. Accordingly, once protection is activated and the charge/discharge FETs are shut down, direct communication between the battery domain and system domain is lost. These limitations introduced by low-side protection switches must be addressed. The most straightforward workaround is to disable the low-side protection feature of the BQ76907-Q1; however, this disables the chip's core protection mechanisms including overcurrent, overvoltage and overtemperature protection.

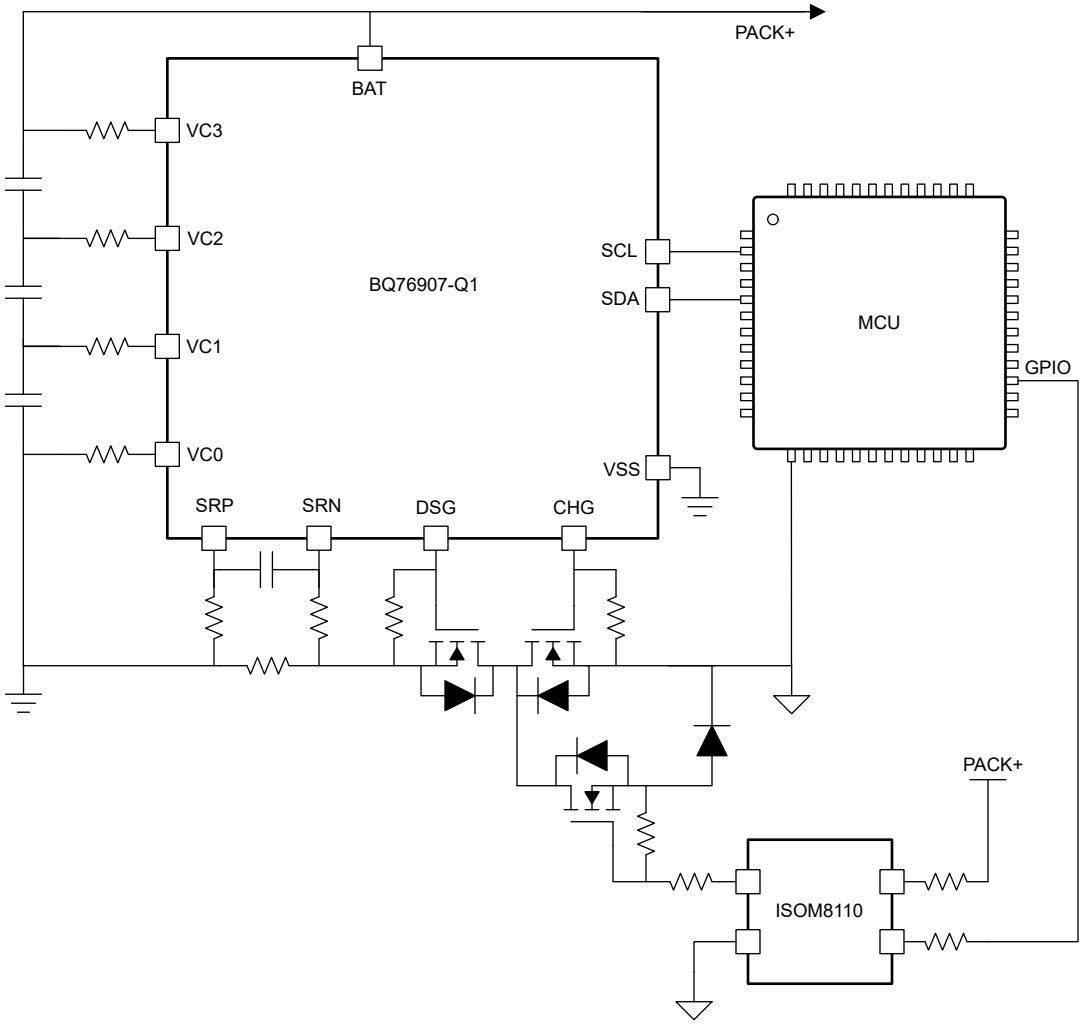


Figure 5-7. Low-side Protection Solution of BQ76907-Q1

An MCU is mandatory in E-Latch systems to support motor control logic. When the supercapacitor voltage drops below 3 V, the MCU can take independent control of the CHG FET to charge the supercapacitor stack and boost its voltage. After the supply voltage of the BQ76907-Q1 rises above 3 V, the MCU hands back CHG FET control authority to the BQ76907-Q1 to re-enable all on-chip protection functions. This design use an external MOSFET to bypass the CHG FET, enabling MCU-controlled charging of the supercapacitors.

5.3 Super Capacitor Health Detection: Combined Solution of TPS61383-Q1 and BQ76907-Q1

The degradation of a supercapacitor is fundamentally manifested through two measurable parameters: a reduction in capacitance (C) and an increase in equivalent series resistance (ESR). Of these two, ESR has been established in the literature as the more sensitive and practically accessible indicator of super capacitor health. The standard test methodology for ESR extraction is based on the instantaneous voltage response to an imposed constant current discharge. When a known constant current is applied to or withdrawn from a supercapacitor, the terminal voltage exhibits an immediate drop, ΔV, which is directly attributable to the ESR. This relationship is formally expressed as $ESR = \Delta V / I$.

The BQ76907 incorporates delta-sigma ADC with 16-bit resolution and a typical measurement accuracy of ±2 mV, making it highly capable of resolving small voltage perturbations across individual cells or supercapacitor modules. However, because of the cell balancing resistor, the BQ76907 cannot measure voltage while discharging current. ESR detection using the BQ76907 alone would require an external, independently controlled discharge path.

TPS61383-Q1 integrates State-of-Health (SOH) operating mode whichsinks a programmable and stable discharge current from the connected supercapacitor. This feature and the BQ76907's ability to measure terminal voltage with high accuracy — motivates their combined deployment in a unified SOH detection architecture. The proposed system is illustrated conceptually as follows:

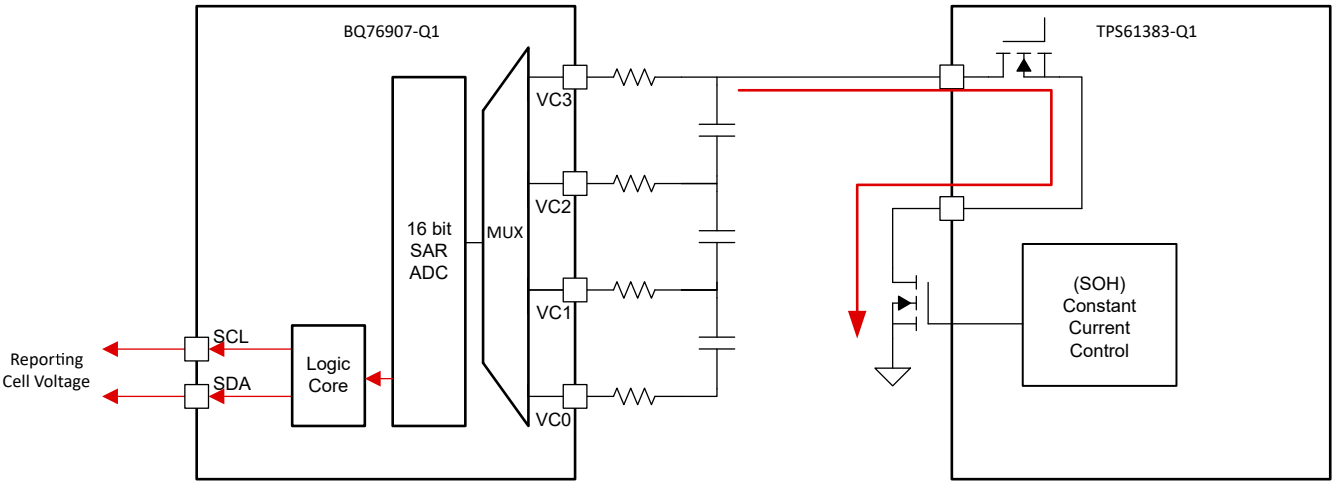


Figure 5-8. Combined Solution for Individual Cells ESR Detection

The measurement procedure is shown in the following steps:

1. Pre-test voltage acquisition:The MCU commands the BQ76907 to acquire and record the initial open-circuit terminal voltage,V_o, of the supercapacitor module.
2. SOH mode activation:The MCU asserts the TPS61383 SOH pin, causing the device to commence a programmable constant-current discharge at a known current magnitude$I$. The discharge current value is pre-calibrated via the external resistor during system design.
3. IR drop voltage acquisition:Immediately following the onset of the discharge current — within a measurement window sufficiently short to exclude capacitive effects — the BQ76907 samples the new terminal voltage,V_1. The delta-sigma ADC's high resolution (16-bit, ±2 mV accuracy) ensures that the small voltage perturbation caused by the ESR can be resolved reliably.
4. ESR Calculation:The host MCU computes the ESR from the measured IR drop: $ESR = (V_o - V_1) / I = \Delta V / I$
5. SOH mode deactivation:The MCU de-asserts the TPS61383 SOH pin, returning the device to its normal boost operating mode and restoring the backup power supply function.
6. Health assessment:The computed ESR value is compared against the end-of-life (EOL) threshold specified by the supercapacitor manufacturer (typically defined as twice the initial ESR, per IEC 62576). If the measured ESR exceeds the threshold, the system can flag a maintenance or replacement alert.

6 Control Unit and Communication

An e-latch system receives crash detection signal from other modules System Basis Chip (SBC). An SBC is a highly integrated mixed-signal device that combines multiple fundamental building blocks of an automotive electronic control unit (ECU) into a single package. As shown in Figure 3, SBCs primarily integrate one or more bus transceivers (CAN, CAN-FD, CAN-SIC, or LIN) together with power supply components, thereby eliminating the need for discrete implementations of these functions

6.1 Control Unit Design Consideration

The e-latch system integrate an embedded electronic control unit (ECU) within the e-latch module. The primary functions of the control unit include receiving user commands (for example, from door handle sensors or the crash detection signal from other system), processing these commands, and driving the latch actuator accordingly. The control unit communicates with the central body control module (BCM) via CAN or LIN while maintaining a degree of local autonomy.

For automotive e-latch applications, the Texas Instruments MSPM0G series of mixed-signal microcontrollers is highly recommended. The MSPM0G devices are based on an enhanced Arm® 32-bit Cortex®-M0+ CPU operating at up to 80 MHz and are AEC-Q100 qualified for automotive application.

The design consideration of the MSPM0G series are shown in *MSPM0 G-Series MCUs Hardware Development Guide*.

6.2 SBC Selection

Texas Instruments offers a comprehensive portfolio of automotive-qualified SBCs preferred for e-latch applications. Selection of the appropriate SBC family depends on the communication protocol used and the compatibility of the system MCU.

- Communication protocol:

First purpose of SBC is the transceiver which communicates with body control module. TCAN116x-Q1 series integrates basic CAN or LIN transceiver to cover most cases for e-latch. If additional function like Partial Networking and CAN SIC is needed, TCAN21x9-Q1 series meets the requirement.

- MCU Power Compatibility:

SBC integrates step down converters which powers MCU or other digital components. The maximum output current must match the MCU current consumption. SBCs with integrated LDO such as TCAN116x-Q1 must be enough for most e-latch systems. However, if the MCU and digital part of the system consumes over 200mA, TI recommends selecting a SBC with integrated buck converter (such as TCAN241x-Q1 or TCAN245x-Q1). A MCU Power Compatibility Chart for SBC is available here.

7 Execution Unit

The e-latch execution unit constitutes the physical actuation of the electronic latch system. E-latch execution unit consists of three primary components: the actuator (Usually BDC), the motor driver (typically an H-bridge) and position sensors. Together, these components deliver the electromechanical force and positional awareness required for reliable e-latch operation.

7.1 Motor Driver Structure

The motor driver architecture constitutes a fundamental design dimension in automotive electronic latch (e-latch) systems, as it directly governs system integration complexity, wiring harness topology, fault isolation capability, and overall cost structure. Depending on the physical placement of the motor driver module, whether centralized within the body control unit or distributed across individual door modules, one motor driver needs to drive 2-7 motors. Therefore DRV8714 / DRV8718 is selected for the door motor. In most cases, multiple motors do not operate simultaneously, therefore multiple channels shares one sense resistor and motor drivers are connected as shown in Figure 7-1

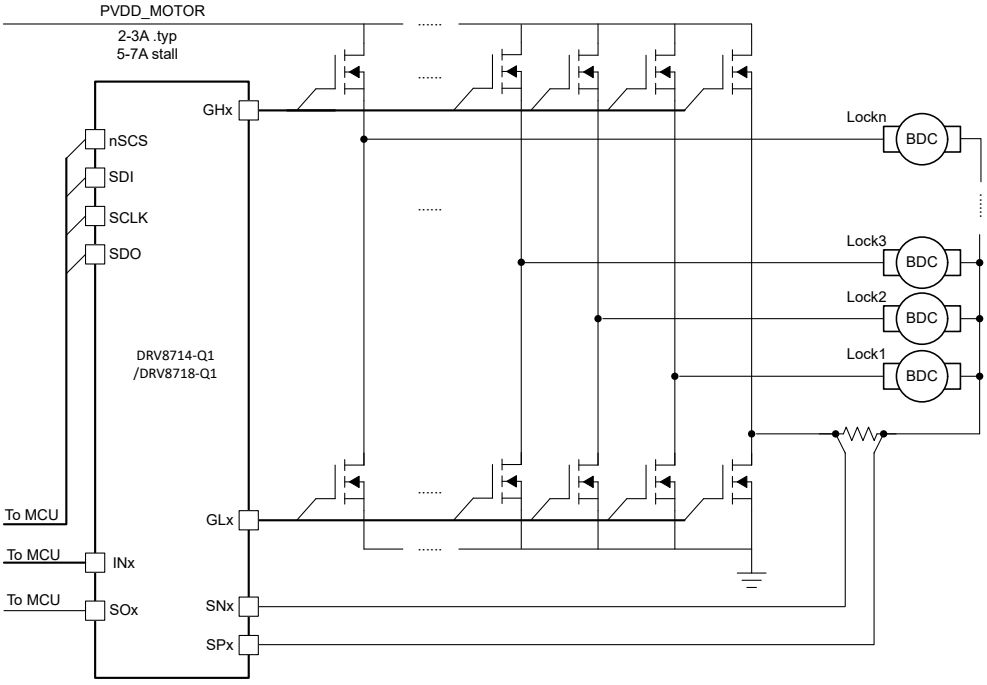


Figure 7-1. Motor Driver Connection

When any of the motors starts operating , the shared return leg turns on and the corresponding leg for the motor starts switching to control motor speed. The following figure uses Lock3 as an example:

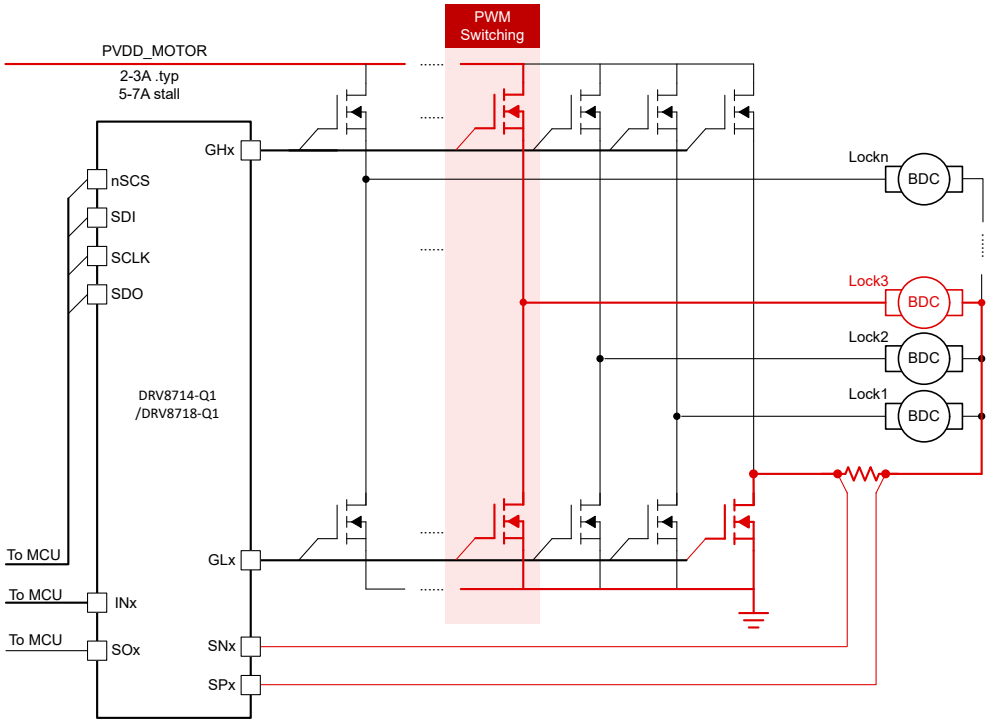


Figure 7-2. Motor Driver Control (Unlock)

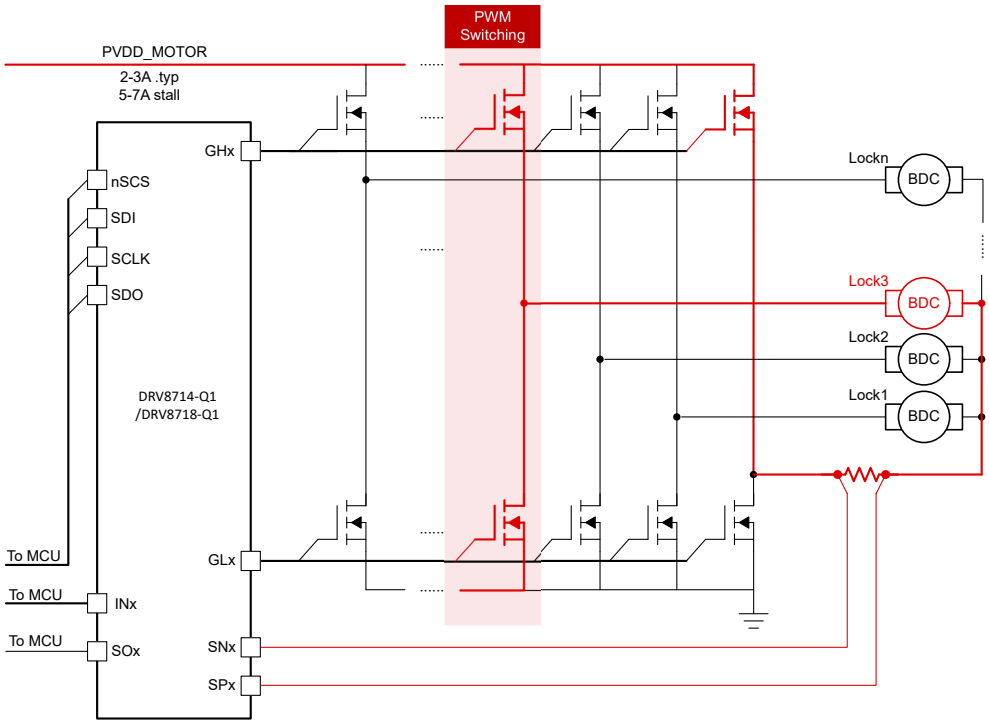


Figure 7-3. Motor Driver Control (Lock)

More design resources for BDC drivers can be found in *Brushed Motor Control User Guide*.

7.2 Motor Driver Design Considerations

In e-latch systems, the stall current for motors can reach 10A. Therefore PCB design of motor drive systems is not trivial and requires special considerations and techniques to achieve the best performance. Motor driver design considerations can be found in:*Best Practices for Board Layout of Motor Drivers*.

8 Summary

This application note presents how to design automotive e-Latch systems, covering key design considerations, component selection and performance optimization.

9 References

1. Texas Instruments, *TPS61383-Q1 Automotive 400kHz, 40V, 30A Boost Converter With Buck/LDO Charger and Battery State of Health Detection*, datasheet.
2. Texas Instruments, *BQ76907-Q1 2-Series to 7-Series High Accuracy Automotive Battery Monitor and Protector for Li-Ion, Li-Polymer, LiFePO4 (LFP), and LTO Battery Packs and Supercaps*, datasheet.
3. Texas Instruments, TCAN1162x-Q1 Automotive CAN FD System Basis Chip with Sleep Mode and LDO Output, datasheet.
4. Texas Instruments, *MSPM0 G-Series MCUs Hardware Development Guide*, application note.
5. Texas Instruments, *Best Practices for Board Layout of Motor Drivers*, application note.

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