EVM User's Guide: ADS125R14EVM-PDK

ADS125R14 Evaluation Module

Description

The ADS125R14 evaluation module (EVM) is a platform for evaluating the performance of the ADS125R14, which is a 24-bit, 8-channel, 320kSPS, multiplexed delta-sigma (ΔΣ) analog-to-digital converter (ADC) designed for low-latency, high precision data acquisition systems. The ADS125R14 integrates a highly-flexible input multiplexer, a high-impedance buffer, a clock oscillator, and different power modes to balance current consumption and noise performance. The ADS125R14EVM-PDK eases the evaluation of the device with hardware, software, and computer connectivity through the universal serial bus (USB) interface.

Get Started

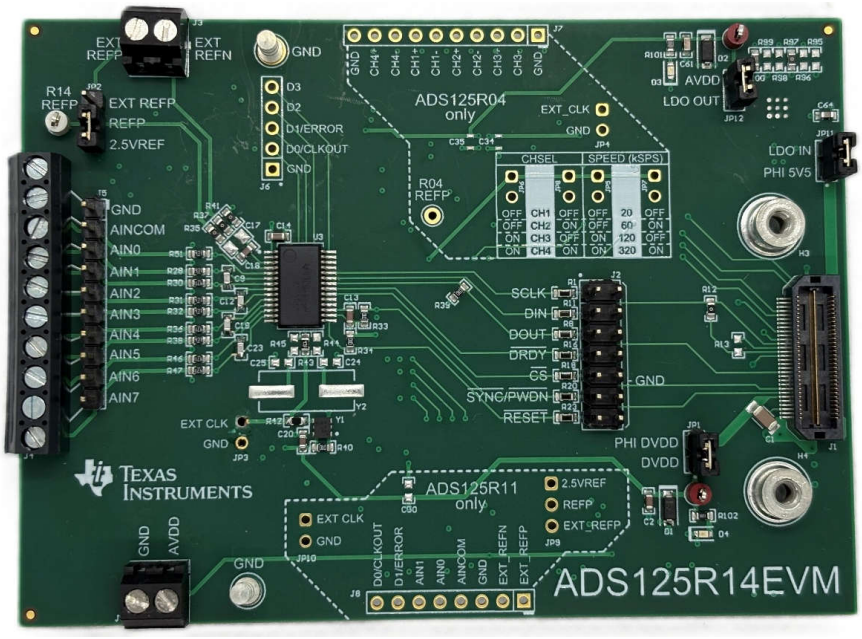
1. Order the EVM from ti.com.
2. Download the latest software from the ADS125R14EVM-PDK tool folder.
3. Connect the ADS125R14 EVM to the PHI controller board.
4. Connect the PHI board to the computer running the ADS125R14 EVM GUI.
5. Launch the ADS125R14 EVM GUI from the start menu.

Features

- Hardware and software required for ADS125R14 diagnostic testing and performance evaluation
- The PHI controller provides a convenient communication interface to the ADS125R14 over USB 2.0 (or higher) for digital input and output
- Easy-to-use evaluation software for 64-bit
- Microsoft® Windows® 10 operating system
- Software suite with graphical tools for data capture and spectral analysis
- Data exporting to a text file for post-processing

Applications

- PLC analog input modules
- Test and Measurement: Weigh Scale; Battery Formation
- Medical: Bio-chemistry analyzer



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1 Evaluation Module Overview

1.1 Introduction

The ADS125R14EVM-PDK is a platform for evaluating the performance of the ADS125R14, a 24-bit, 8-channel, 320-kSPS multiplexed delta-sigma ADC designed for low-latency, high-precision data acquisition systems. The evaluation kit includes the ADS125R14 EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture and analysis. The ADS125R14 EVM includes the ADS125R14 and all the peripheral analog circuits and components required to evaluate the performance of the ADS125R14. The PHI board provides a communication interface from the ADS125R14 EVM to the computer through a USB port.

This EVM user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS125R14EVM.

1.2 Kit Contents

Figure 1-1 shows that the ADS125R14EVM-PDK includes the following components:

- The PHI controller board
- The ADS125R14 EVM that includes the ADS125R14 and peripheral circuitry required for device operation and communication with the PHI board
- An A-to-Micro-B USB cable for communication between the PHI board and the EVM GUI
- The EVM GUI, which can be found online in the ADS125R14 EVM tool folder

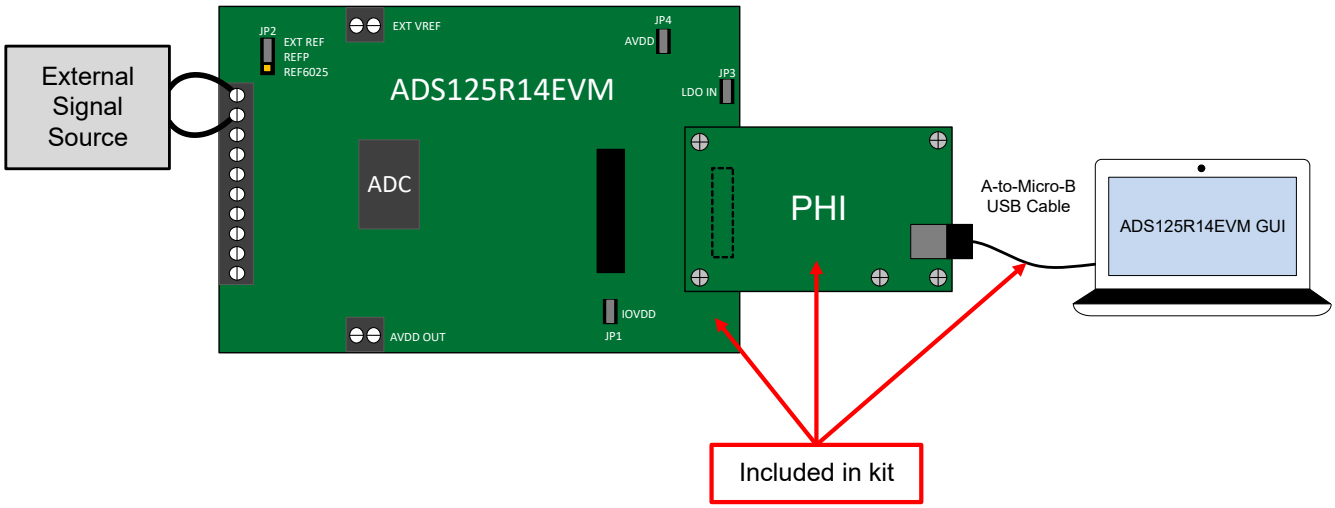


Figure 1-1. System Connection for Evaluation

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1.3 Specification

Table 1-1 shows specifications applicable to the ADS125R14 EVM and the PHI board:

Table 1-1. ADS125R41EVM and PHI Board Specifications

PARAMETER	CONDITIONS		VALUE
Temperature	Recommended operating free-air temperature range, T_A		15°C ≤ T_A ≤ 35°C
Power supply input range	Recommended voltage input range for JP2-2 with respect to GND		5.5V ≤ +Vin ≤ 7V
	Supply current range $\|I_s\|$		0.25A ≤ $\|I_s\|$ ≤ 0.5A
Input voltage range	Absolute input voltage with respect to DGND for AIN0 to AIN7 and AINCOM inputs	Input buffer off	AGND - 0.1V ≤ AINx ≤ AVDD + 0.1V
		Input buffer on	AGND - 0.05V ≤ AINx ≤ AVDD – 1.45V
EXT clock	Recommended frequency range (f_{CLK})		0.1MHz ≤ f_{CLK} ≤ 8.4MHz
External digital IO (including EXT clock)	Recommended logic levels (applied to header J2) with respect to DGND	Logic level low (V_{IOl})	0V ≤ V_{IL} ≤ 0.3 × DVDD
		Logic level high (V_{IOh})	0.7 × DVDD ≤ V_{IH} ≤ DVDD
ADS125R14 AVDD to AGND	Recommended voltage range (applied to JP4-1), external source	High-speed mode	3V ≤ AVDD ≤ 5.5V
		All other speed modes	2.85V ≤ AVDD ≤ 5.5V
ADS125R14 DVDD to DGND	Recommended voltage range (applied to JP1-1), external source		1.65V ≤ DVDD ≤ 5.5V
ADS125R14 REFP to AGND	Recommended voltage range (applied to J3-2), external source	Input buffer off	V_{REFN} + 0.5V ≤ AINx ≤ AVDD + 0.1V
		Input buffer on	V_{REFN} + 0.5V ≤ AINx ≤ AVDD + 0.1V
ADS125R14 REFN to AGND	Recommended voltage range (applied to J3-1), external source	Input buffer off	AGND - 0.1V ≤ AINx ≤ V_{REFP} – 0.5V
		Input buffer on	AGND ≤ AINx ≤ V_{REFP} – 0.5V

1.4 Device Information

Table 1-2 provides important specifications for the ADS125R14. Refer to the ADS125R14 datasheet for complete specifications:

Table 1-2. ADS125R14 Device Family Key Features and Parameters

PARAMETER	VALUE
ADC resolution	24 bits
Maximum data rate	320kSPS
Channel count	9 (8 AINx + 1 AINCOM); fully flexible multiplexer
Integrated features	• Programmable gain amplifier (PGA) • Selectable speed modes • Oscillator
Package	TSSOP-28
Package size	10.2mm × 7.8mm
Specified temperature range	-40°C ≤ T_A ≤ 125°C

The ADS125R14 EVM is provided with an ADS125R14 installed. The ADS125R14 EVM GUI is intended to operate specifically with the ADS125R14. The user can remove the ADS125R14 and the accompanying circuitry and install any device listed in Table 1-3; however, the user cannot use the ADS125R14 EVM GUI or PHI controller card if the user replaces the ADS125R14 already installed on the EVM. Refer to Section 2.7 for more information about using the ADS125R14 EVM with an external controller. The rest of this document assumes that the ADS125R14 is installed on the EVM, unless otherwise noted.

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Table 1-3. ADC Options in the ADS125R14 Device Family

Device	Differential Channels	Features
ADS125R14	4	• PGA • Internal oscillator • Register programmable – 4-wire SPI
ADS125R11	1	
ADS125R04	4	• Separate AVDD and DVDD supplies • Internal oscillator • Pin programmable – 2-wire serial interface
ADS125R03	4	• Internal oscillator • Pin programmable – 2-wire serial interface

Figure 1-2 shows the ADS125R14 device block diagram:

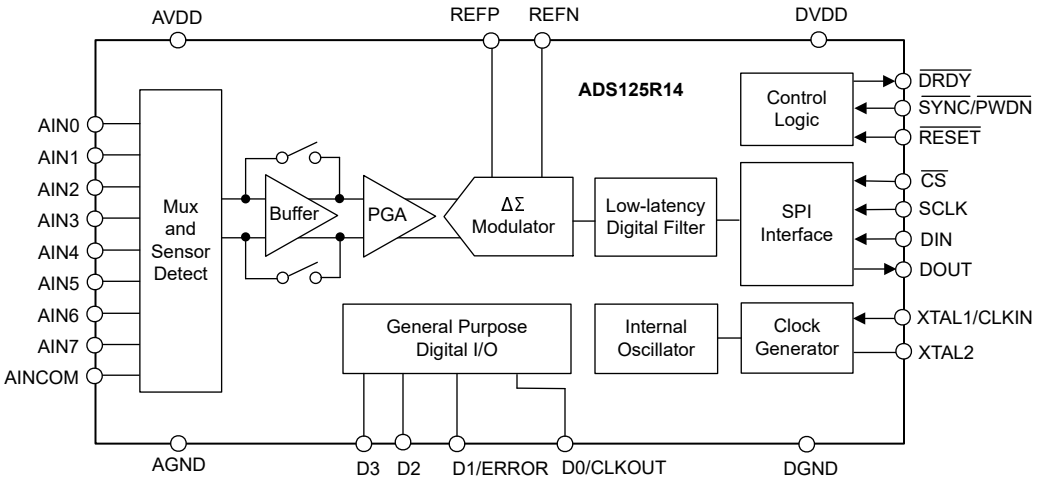


Figure 1-2. ADS125R14 Block Diagram

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2 Hardware

The following sections describe the ADS125R14 EVM hardware in detail.

2.1 Analog Inputs

The ADS125R14 EVM provides external connection points and input filtering for all nine channels. Figure 2-1 shows the schematic for analog inputs AIN0 to AIN7, as well as AINCOM. Figure 2-1 also shows terminal block J4 and header J5 that allow the user to easily apply and measure signals with the ADC.

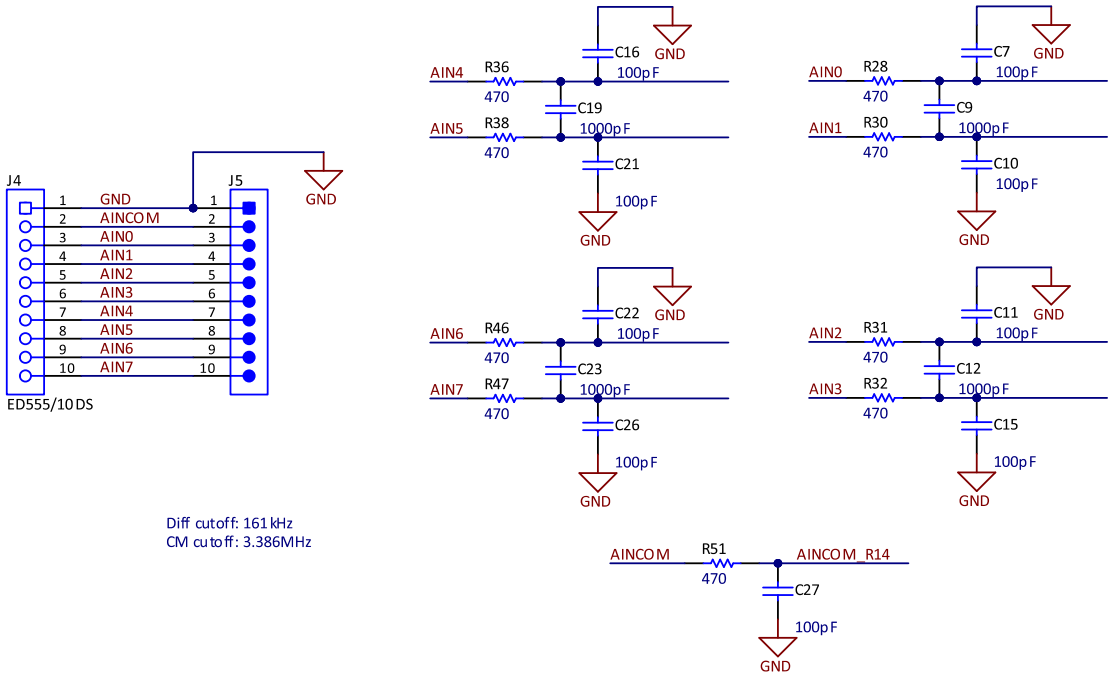


Figure 2-1. EVM Input Terminal Block and Anti-Aliasing Filters

Each adjacent analog input pair includes a set of low-pass filters to prevent aliasing. The differential filters have a 3dB cutoff of 161kHz. As an example, Figure 2-1 shows that capacitor C9 and resistors R28 and R30 create the differential filter between analog inputs AIN0 and AIN1. The common-mode filters have a 3dB cutoff of 3.386MHz. As an example, Figure 2-1 shows that capacitor C7 and resistor R28 create the common-mode filter for analog input AIN0. Precision 5% C0G or NPO-type capacitors and 0.1% resistors are used in the analog signal chain to reduce measurement error.

Verify that the signal source voltage and current levels applied to terminal blocks J4 and header J5 meet the specifications listed in Table 1-1.

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2.2 ADC Connections and Decoupling

Figure 2-2 shows all connections to the ADS125R14 data converter. AVDD and DVDD each have a 10µF decoupling capacitor. Make sure these capacitors are physically close to the device and have a good connection to the ground plane. Also, digital inputs $\overline{\text{RESET}}$ and $\overline{\text{SYNC/PWDN}}$ each have 100kΩ pullup resistors to DVDD to make sure that the ADC powers up in a known state.

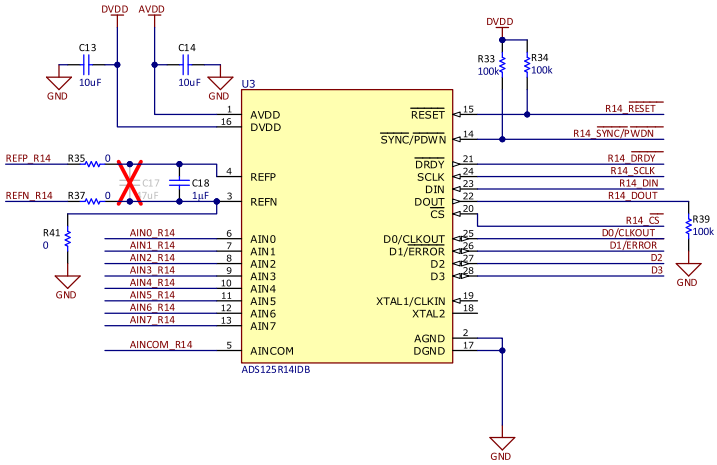


Figure 2-2. ADC Connections and Decoupling Capacitors

2.3 Digital Interface

Section 1.1 notes that the EVM interfaces with the PHI and communicates with the computer over the USB. The PHI communicates with two devices on the EVM: the ADS125R14 (over SPI) and the EEPROM (over I2C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS125R14 platform. The EEPROM is no longer used after the hardware is initialized.

The ADS125R14 requires SPI serial communication where the SCLK signal idles lows and data is captured on the falling edge of SCLK (CPOL = 0 and CPHA = 1). Figure 2-3 shows that header J2 provides test points to probe the digital signals with a logic analyzer. Additionally, header J2 can be used to connect communication signals from an external controller. Remove the PHI controller card from connector J1 before applying external signals to header J2.

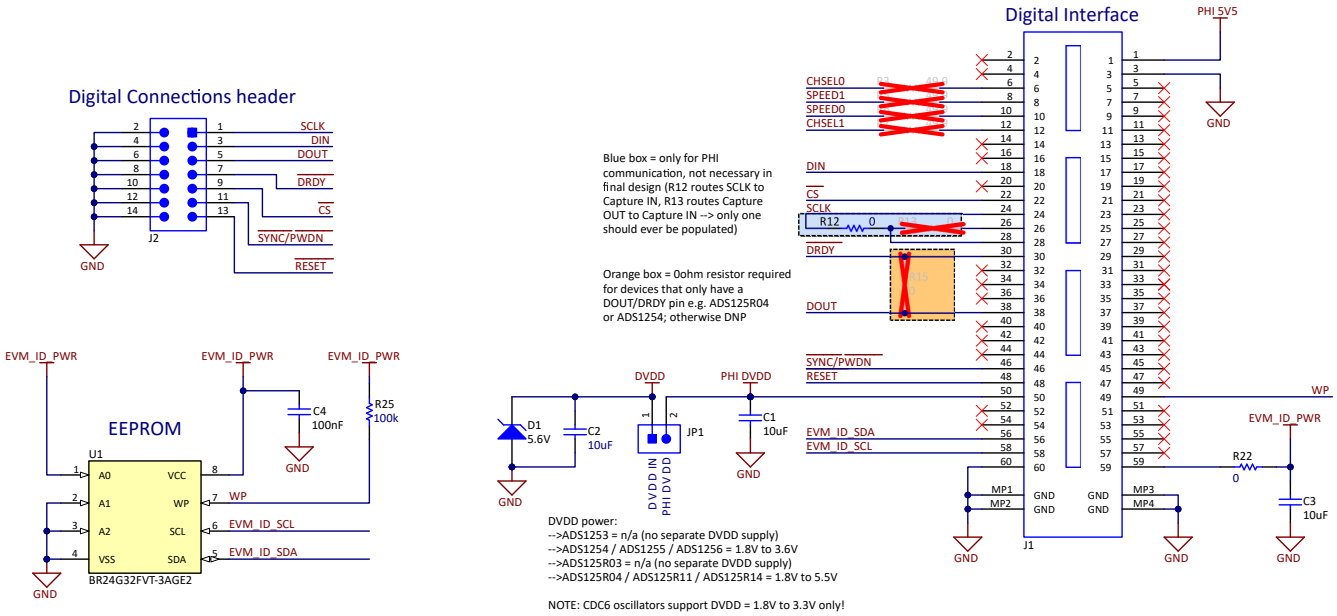


Figure 2-3. EVM Digital Interface and EEPROM

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Figure 2-3 also shows that jumper JP1 connects the PHI_DVDD and DVDD nets. The PHI_DVDD net by default provides 3.3V to the ADC digital supply (DVDD) pin through jumper JP1. Remove the shunt on JP1 and apply a current meter (ammeter) to measure the digital current consumed by the ADC. Removing the shunt on jumper JP1 also enables connection of an external DVDD power source to pin 1 of jumper JP1. Verify that the DVDD voltage applied to pin 1 of jumper JP1 is the same as the I/O voltage used by the PHI or the external controller, if applicable. Also verify that any voltage applied to the ADC meets the voltage requirements as described in Table 1-1.

Figure 2-4 shows how each digital pin has a 49.9Ω series resistor near the driving source. These resistors smooth the digital signal edges to minimize overshoot and ringing. These components can be included in the final design to improve digital signal integrity but are not strictly required.

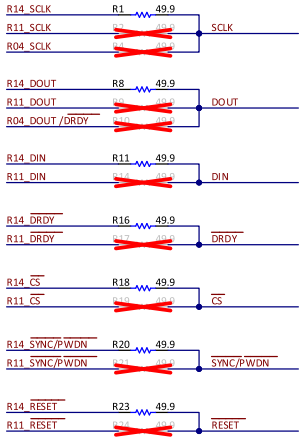


Figure 2-4. Series Resistance on ADS125R14 EVM Digital Pins

2.4 Power Supplies

Figure 2-5 shows the power supply circuitry included on the ADS125R14 EVM. The default configuration applies a unipolar, 5V voltage to the ADC analog supply (AVDD) pin using the low-noise TPS7A4700 low dropout (LDO) voltage regulator. The user can change the LDO output voltage by installing or removing the 0Ω resistors connected to pins 6 to 12 on the LDO.

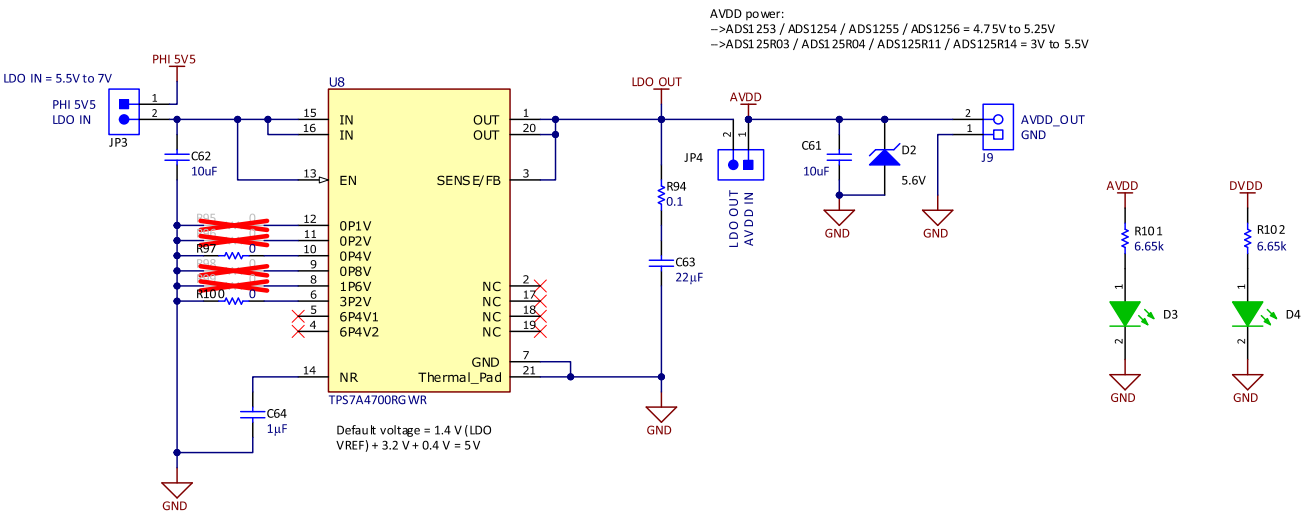


Figure 2-5. EVM Power Tree

The user can also provide an external supply voltage to the LDO using jumper JP3 or directly to the ADC AVDD pin using jumper JP4. Verify that any voltage applied to the ADC meets the voltage requirements as described in Table 1-1. In all cases LEDs indicate if the supply voltages are valid.

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2.5 Voltage Reference

Figure 2-6 shows the ADS125R14 EVM external voltage reference circuit. By default, the EVM uses a low noise, low drift 2.5V REF6025 as the ADC voltage reference. Alternatively, the user can supply an external reference voltage using terminal block J3 and connecting a shunt between pins 2 and 3 on jumper JP2. Verify that any external reference voltage applied to the ADC meets the voltage requirements as described in Table 1-1. Additionally, the ADC registers need to be configured to use an external reference. See the ADC datasheet for more information.

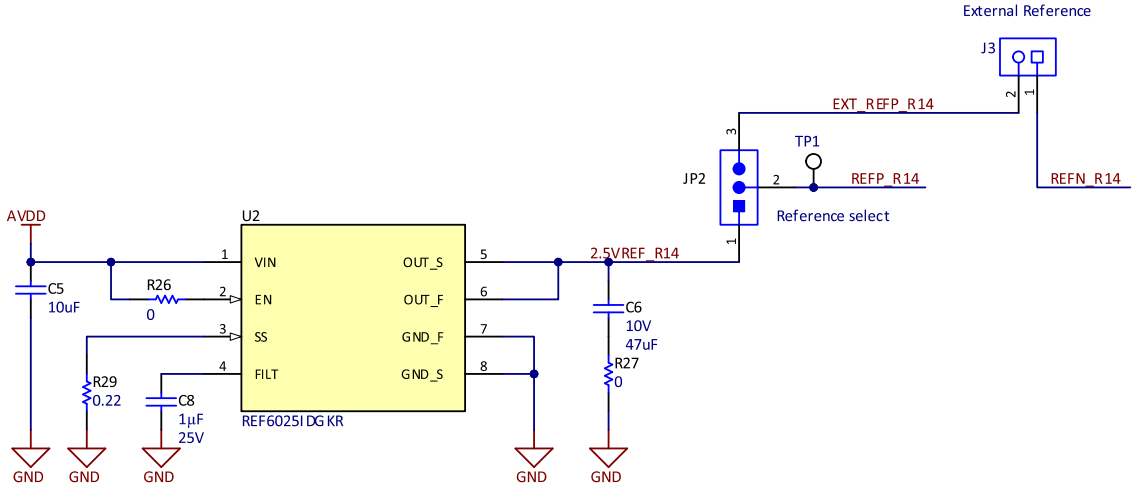


Figure 2-6. EVM Voltage Reference

2.6 Clocking

Figure 2-7 shows the ADS125R14 EVM clock tree. The ADS125R14 integrates a high-accuracy oscillator that is sufficient for most applications. The ADS125R14 EVM also includes an external, 7.68MHz CDC6C clock oscillator that is enabled by default. Alternatively, the user can apply an external clock source using header JP11. Verify that any external clock signal applied to the ADC meets the clocking requirements as described in Table 1-1. Additionally, the ADC registers need to be configured to use an external clock. See the ADC datasheet for more information.

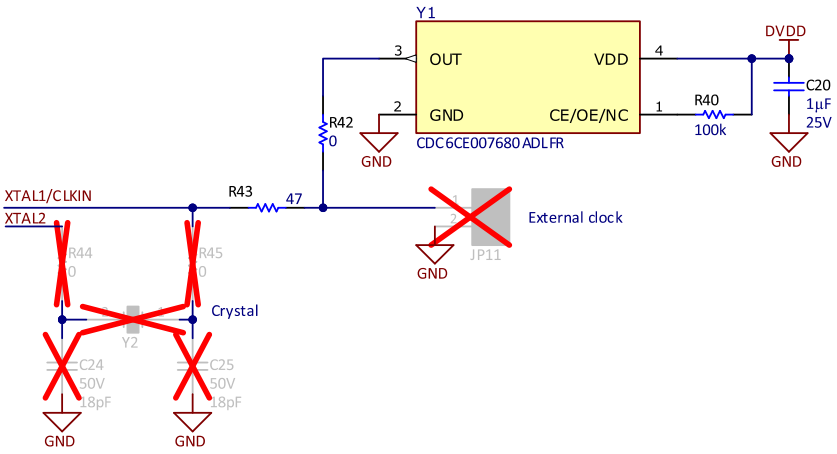


Figure 2-7. EVM Clock Tree

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2.7 Using the ADS125R14 EVM With an External Controller

The ADS125R14 EVM is designed to easily connect to an external controller. This design enables the user to test application code and firmware on the ADS125R14 without having to develop a custom PCB. This section describes the specific connections required to use the ADS125R14 EVM with an external controller. Figure 2-8 shows the location of various headers, connectors, and terminal blocks described in this section.

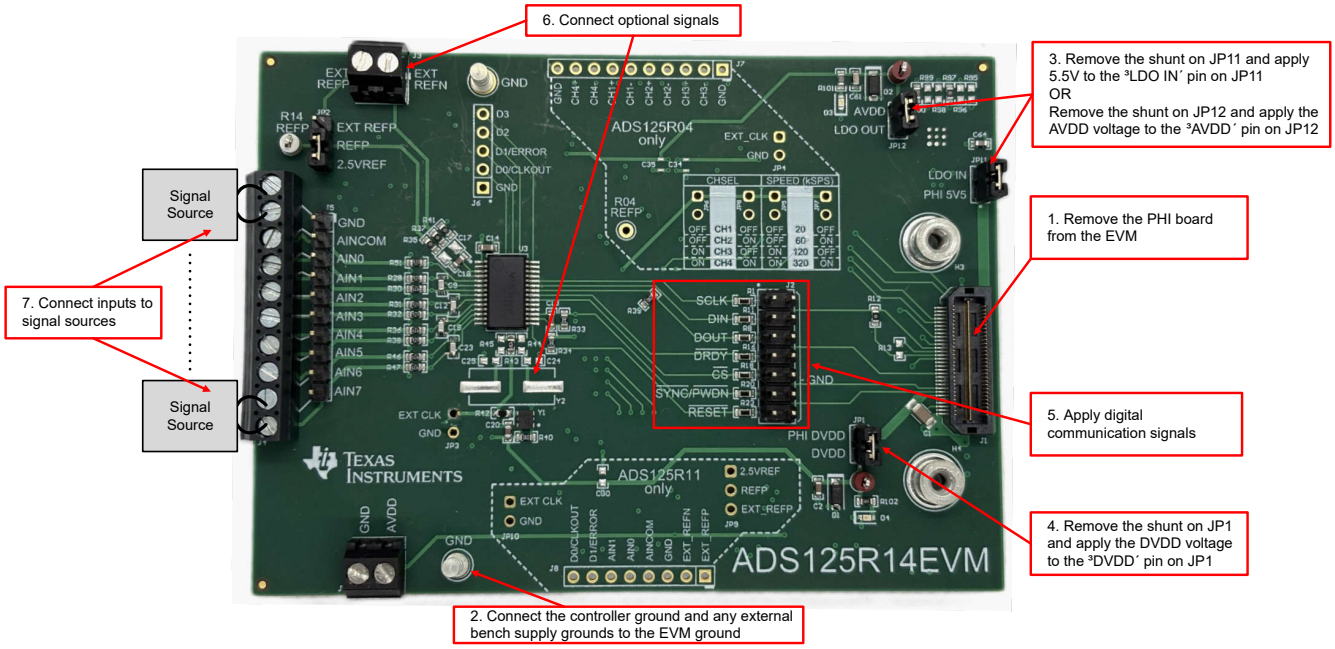


Figure 2-8. Connecting an External Controller to the ADS125R14 EVM

Complete the following steps to prepare the ADS125R14 EVM for use with an external controller:

1. Remove the PHI board if still connected to the EVM.
2. Connect the external controller ground and bench supply ground to the GND pins on the EVM.
3. Connect an external bench supply to the ADC AVDD pin by performing **only one** of the following two options:
   a. Remove the shunt on jumper JP11 and apply 5.5V to the "LDO IN" pin on jumper JP11.
   b. Remove the shunt on jumper JP12 and apply the AVDD voltage to the "AVDD" pin on jumper JP12.
4. Connect an external bench supply to the ADC DVDD pin by removing the shunt on jumper JP1 and applying the DVDD voltage to the "DVDD" pin on jumper JP1.
5. Apply digital communication signals to header J2 on the EVM:
   a. Connect POCI (peripheral out, controller in) from the controller to the DOUT pin.
   b. Connect PICO (peripheral in, controller out) from the controller to the DIN pin.
   c. Connect SCLK from the controller to the SCLK pin.
   d. Connect $\overline{CS}$ from the controller to the $\overline{CS}$ pin.
   e. Connect an I/O pin from the controller to the $\overline{DRDY}$ pin. $\overline{DRDY}$ is an output from the ADC that indicates when new data are ready to be clocked out of the ADC. Write a user-defined data collection routine that monitors this pin (polling or interrupt) and only transfers data after a falling edge.
   f. (Optional) Connect I/O pins from the controller to the $\overline{SYNC/PWDN}$ and $\overline{RESET}$ pins to control conversions and reset the device, respectively.
6. (Optional) Connect an external Voltage Reference or Clock.
7. Connect the signal source to the terminal blocks.

Verify that the external power supply voltages, communication signal levels, and applied input signals meet the specifications listed in Table 1-1.

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3 Software Installation and Hardware Connections

3.1 ADS125R14 EVM GUI Installation

Download the latest version of the EVM GUI installer from the ADS125R14 EVM tool folder. Run the GUI installer to install the EVM GUI software on your computer.

Note

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message can appear or the installer.exe file can be deleted.

Figure 3-1 through Figure 3-5 show the prompts seen by the user during the GUI installation process. Accept the license agreement and follow the on-screen instructions to complete the installation.

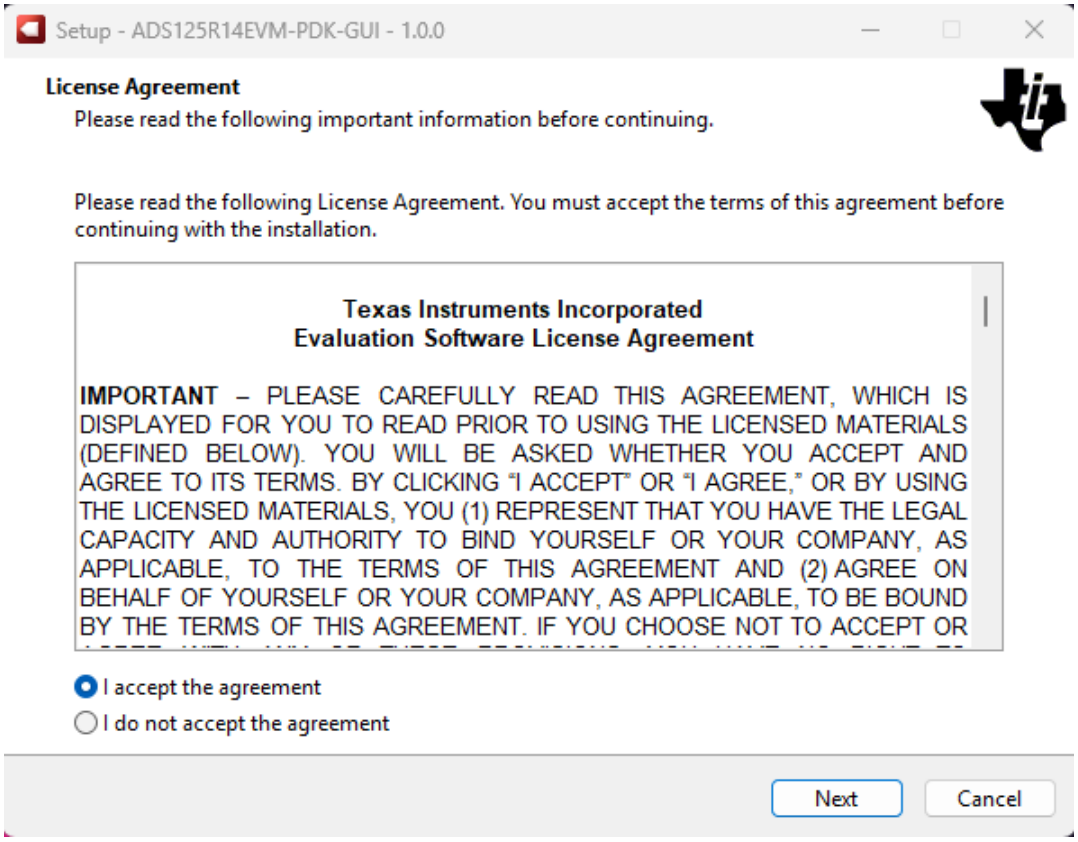


Figure 3-1. ADS125R14 EVM GUI Install Welcome Screen

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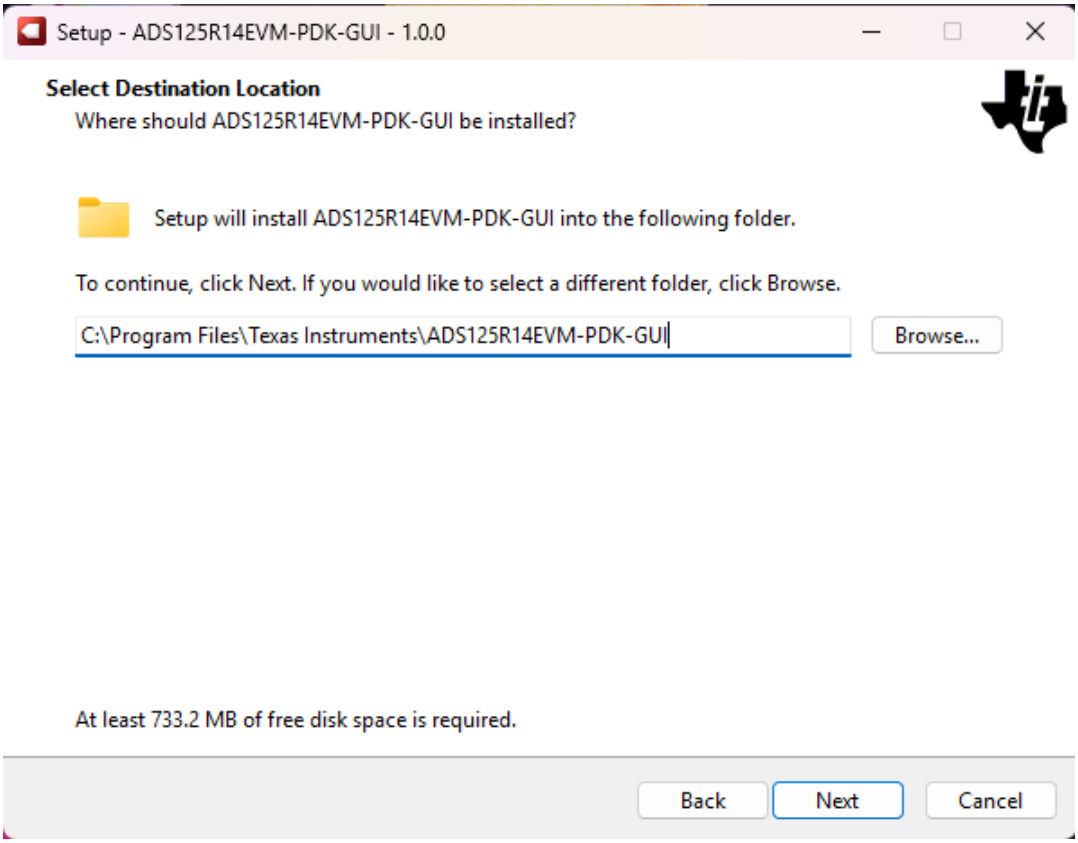


Figure 3-2. ADS125R14 EVM GUI Install Destination Location

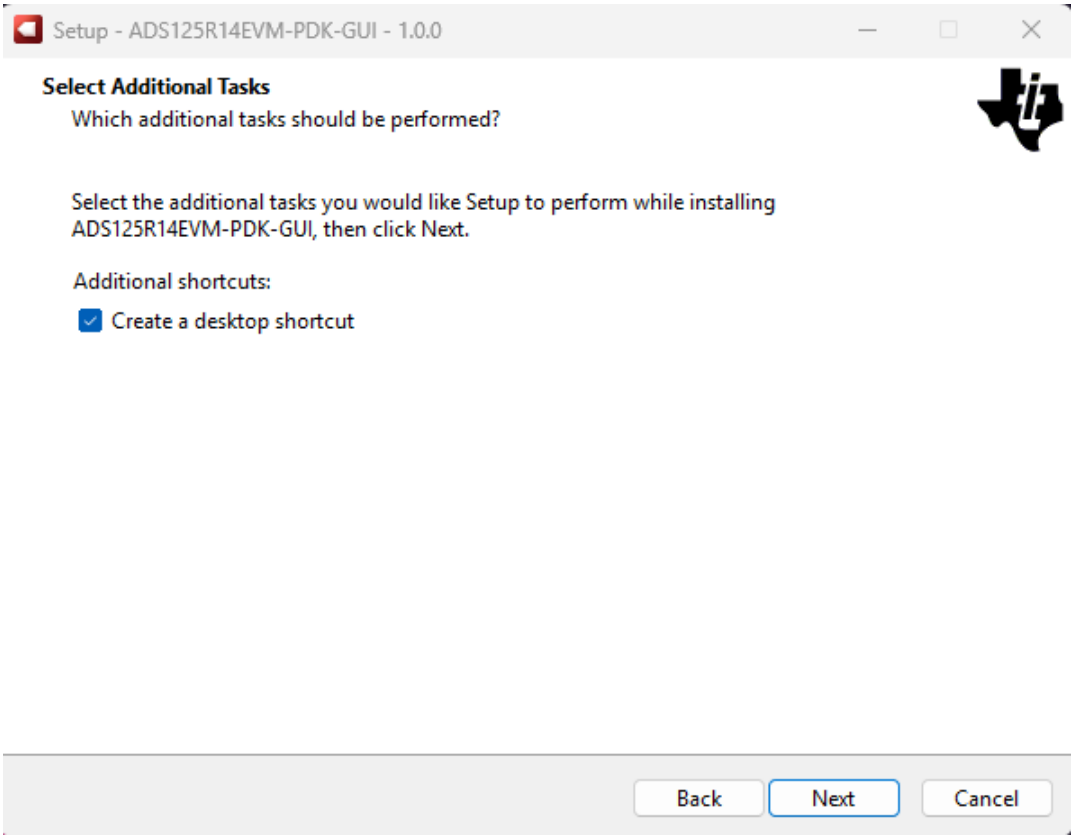


Figure 3-3. ADS125R14 EVM GUI Install Desktop Shortcut

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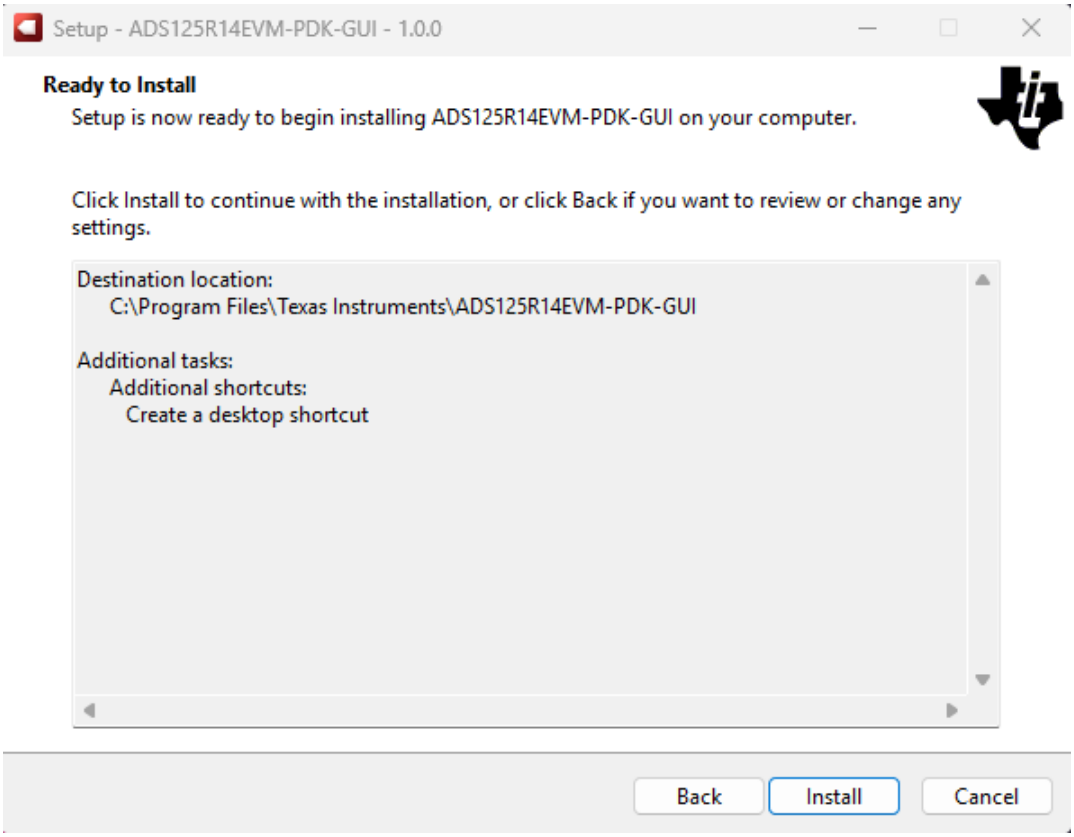


Figure 3-4. ADS125R14 EVM GUI Ready to Install

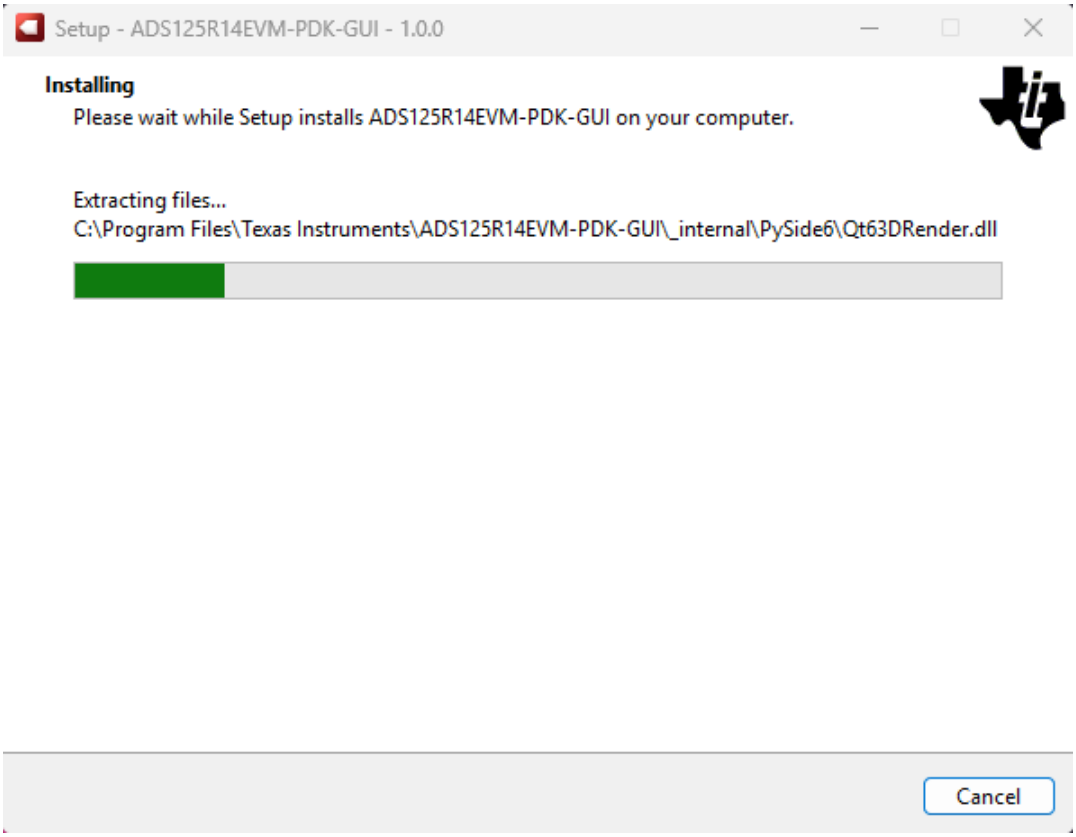


Figure 3-5. ADS125R14 EVM GUI Install in Process

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Figure 3-6 shows the final prompt after the installation process completes.

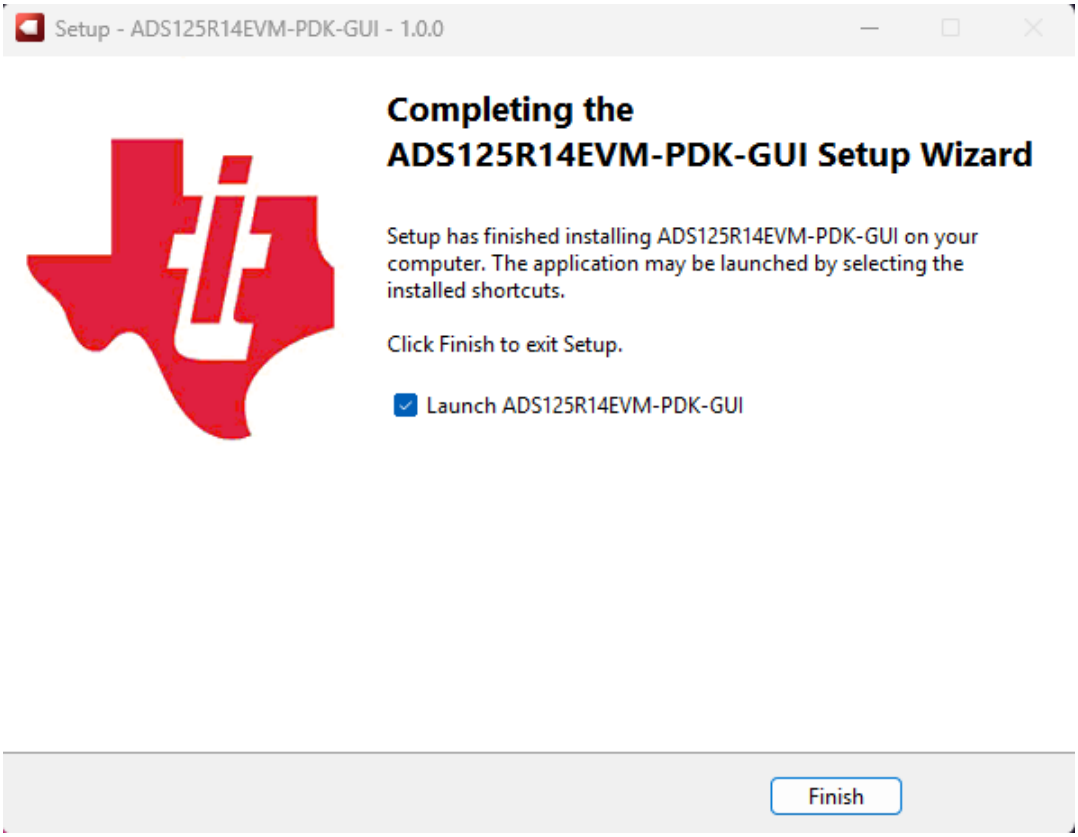


Figure 3-6. ADS125R14 EVM GUI Install Complete

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3.2 ADS125R14 EVM Hardware Connections

Connect the EVM as shown in Figure 3-7 after installing the software:

1. Physically connect P2 of the PHI to connector J1 on the ADS125R14 EVM. Install the included screws to provide a robust connection.
2. (Optional) Connect an external Power Supply, Clock, or Voltage Reference, as described in those sections.
3. Verify that all shunts are installed on jumpers JP1, JP2, JP11, and JP12.
4. Connect the USB connector on the PHI to the computer.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; Figure 3-7 shows the resulting LED indicators.
5. Start the software GUI as shown in Figure 3-7. Note that the LEDs blink slowly when the FPGA firmware is loaded on the PHI. This loading takes a few seconds.
6. Connect the signal source to the terminal block or input header. Verify that the signal source voltage and current levels meet the specifications listed in Table 1-1.

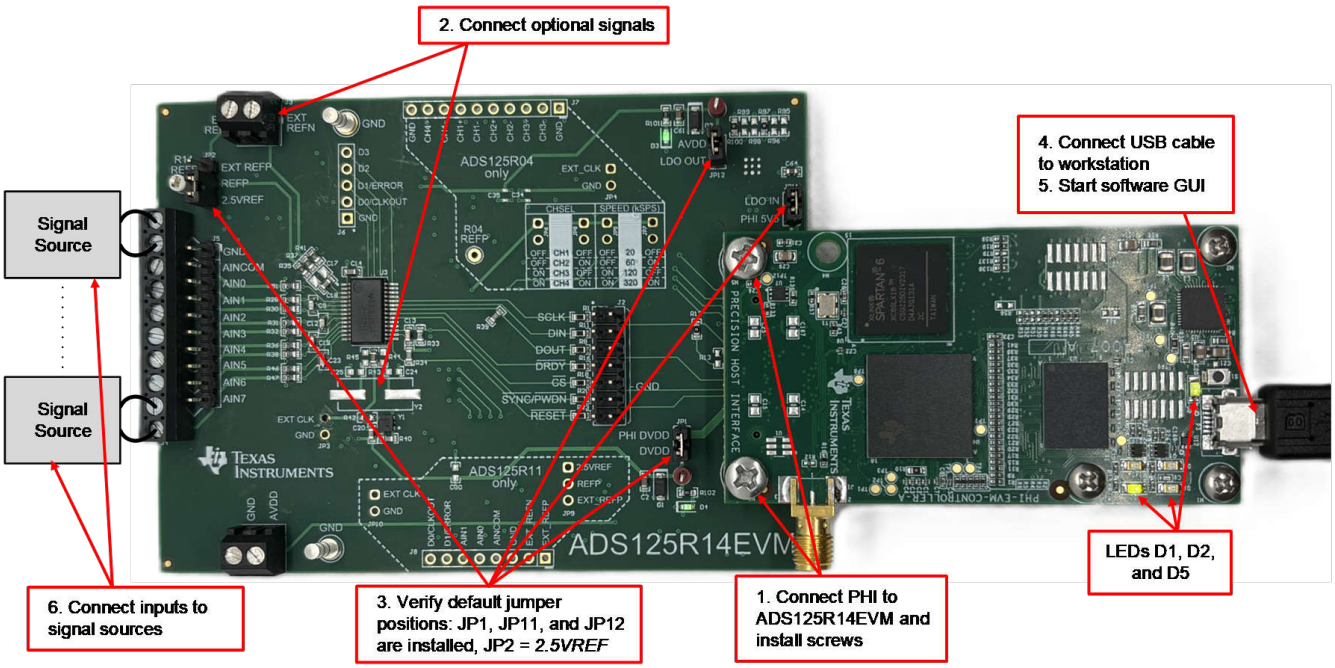


Figure 3-7. Connecting the Hardware to the ADS125R14EVM

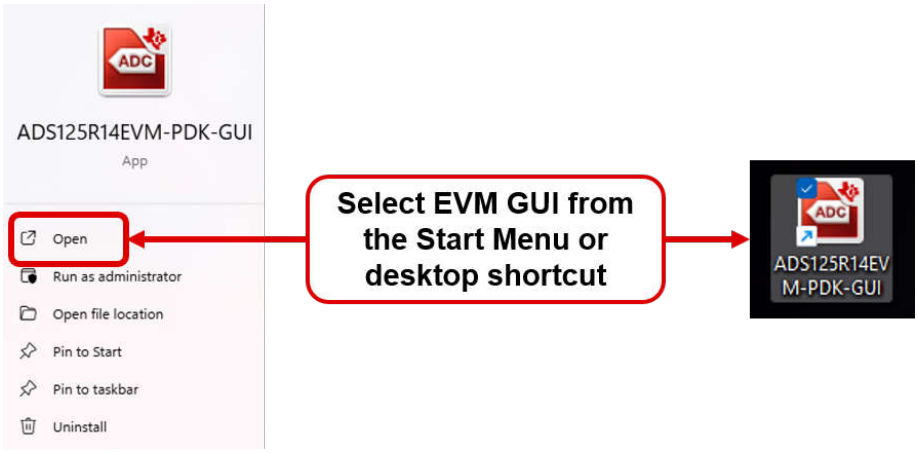


Figure 3-8. Launch the EVM GUI Software

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4 GUI Operation

The following sections describe the operation and behavior of the ADS125R14 EVM GUI.

4.1 GUI Navigation and Home Page

Figure 4-1 shows the ADS125R14 EVM GUI *Home* page that appears after opening the GUI. Select the *Connect* button to connect the EVM to the host as well as to provide power to the EVM.

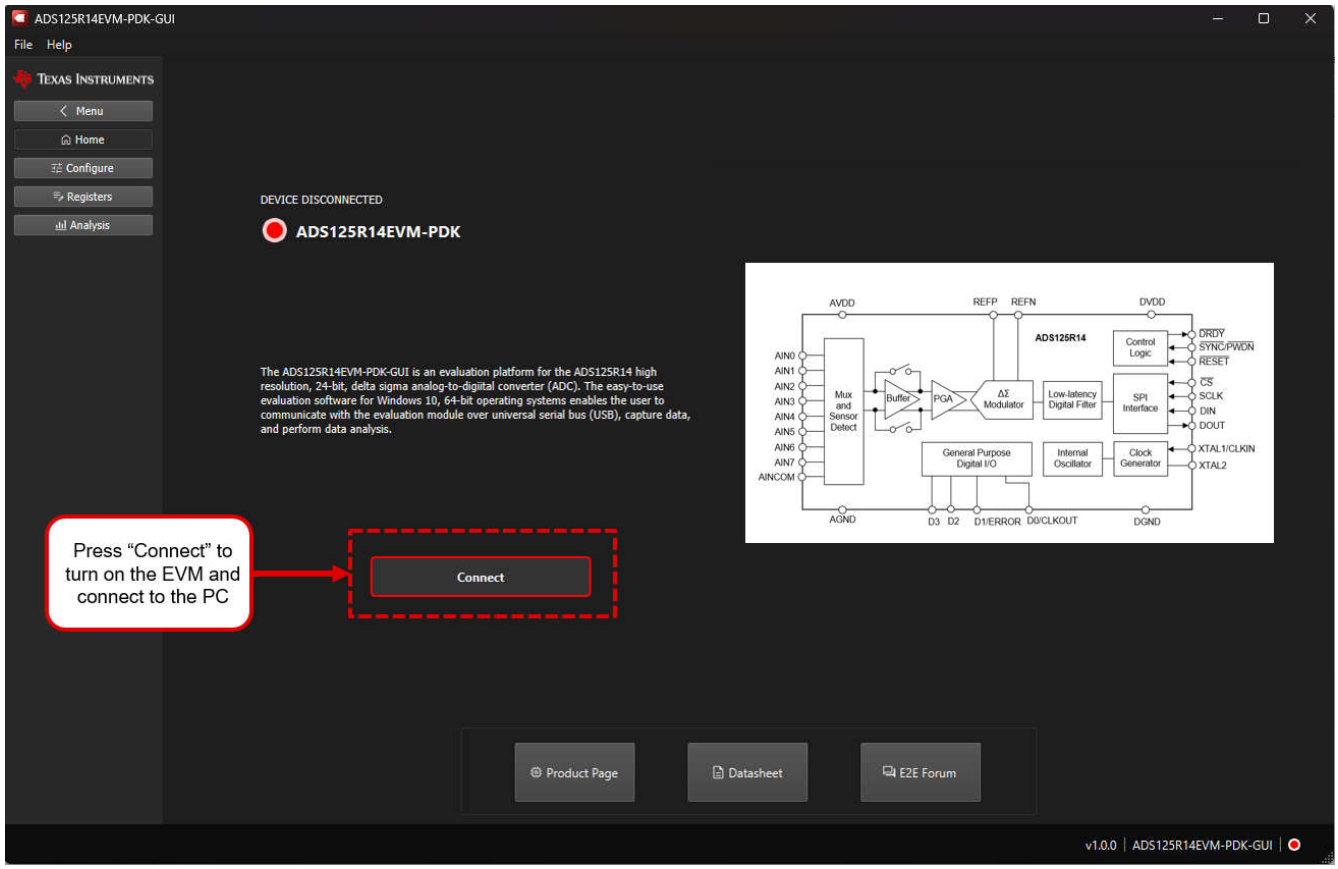


Figure 4-1. ADS125R14 EVM GUI Home Page - Disconnected

Figure 4-2 shows how the GUI changes after establishing a successful connection. Specifically, the GUI displays "Device Connected" above the GUI name in the middle of the screen and includes multiple, green "Connected" indicators. Figure 4-2 also shows how the navigation control on the left side of the GUI allows access to the other pages in the GUI. Navigate to any of the GUI pages using these controls.

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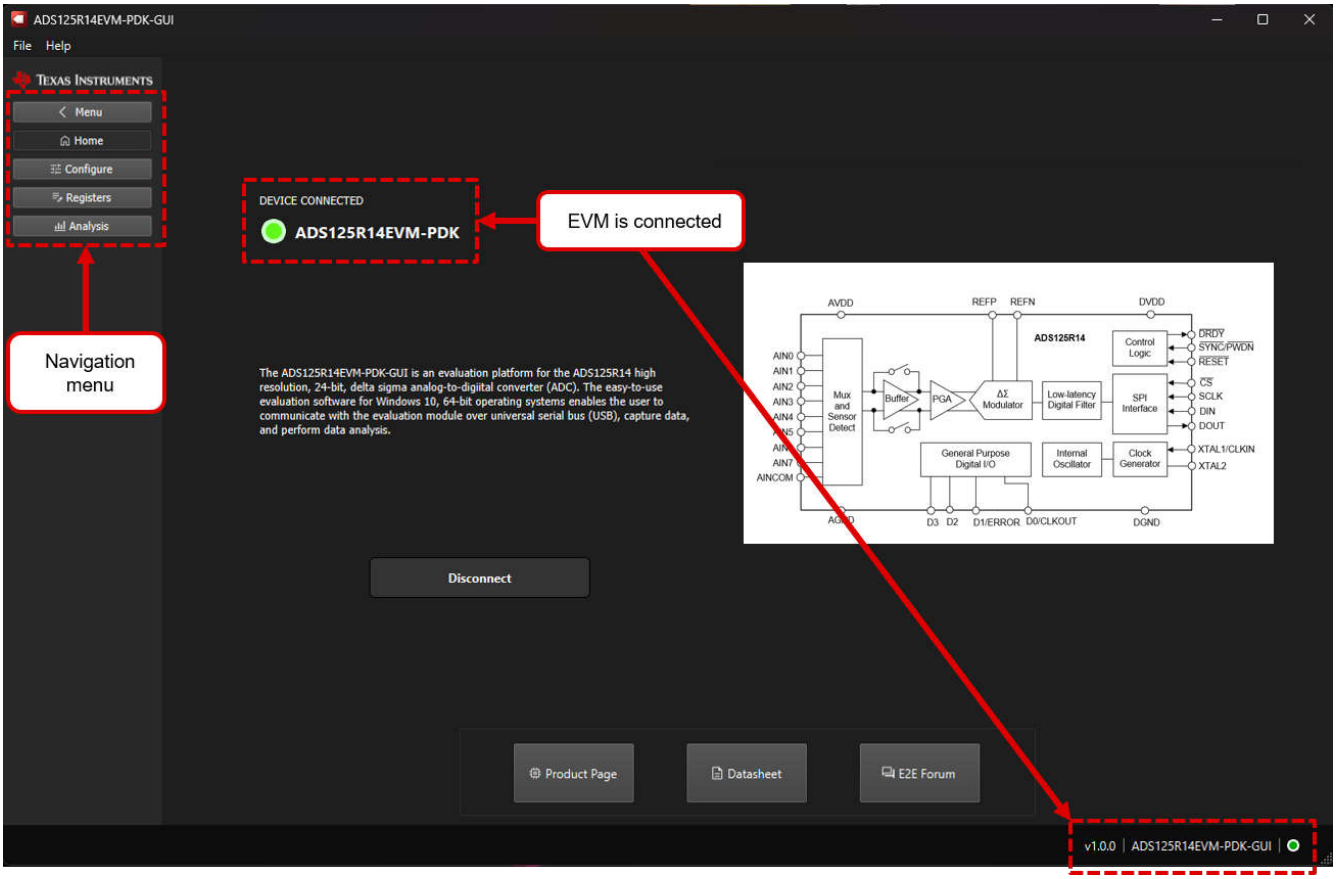


Figure 4-2. ADS125R14 EVM GUI Home Page - Connected

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4.2 ADC Configuration

Figure 4-3 shows the ADC *Configure* page. Use the options on this page to configure the most commonly-used device and board-level features available on the EVM. Certain parameters include tooltips that enable the user to select appropriate input values. Hover over the tooltip without clicking to enable the message.

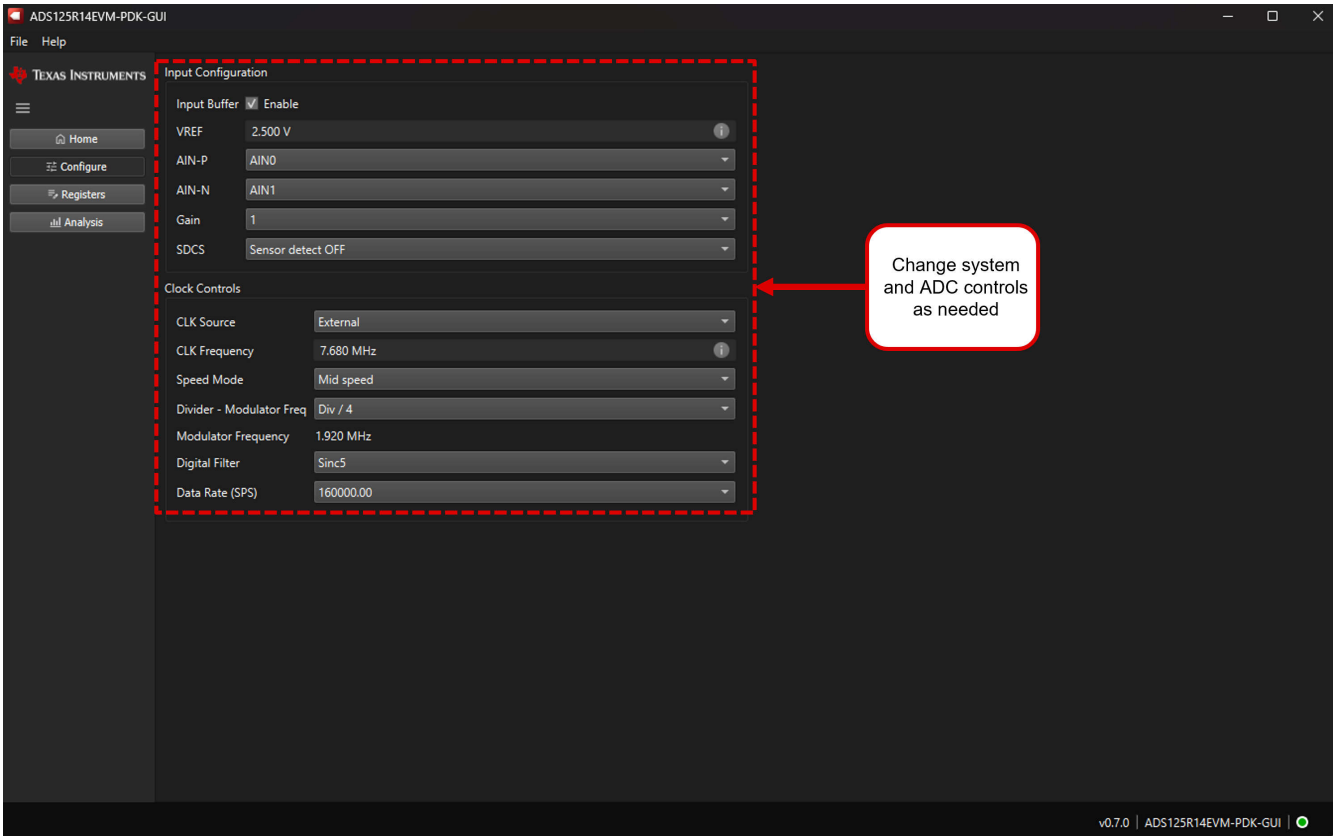


Figure 4-3. ADS125R14 EVM GUI Configuration Page

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4.3 Register Settings

Figure 4-4 shows the ADS125R14 EVM GUI register map. Use the *Registers* page to configure additional ADC functions not included on the *Configure* page. Change the register settings by selecting each bit or by typing a value directly into the Value column. The user can also *Read All* registers, *Reset All* registers, *Save* a specific configuration, or *Load* a specific configuration using the buttons at the top of the GUI.



Figure 4-4. ADS125R14 EVM GUI Register Settings Page

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4.4 Analysis Page

Figure 4-5 shows how the ADS125R14 EVM GUI *Analysis* page allows the user to collect data:

1. Use the *Samples* dropdown to select from a pre-determined number of samples or choose the "Other" option to collect an arbitrary number of samples.
2. Use the *Plot View* dropdown to select between "Time-Domain" or "Frequency-Domain" analysis. Switching between analysis types causes calculations to be performed on the same set of data.
3. Select the *Capture* button to start the conversion process and collect the desired number of samples from the ADC.

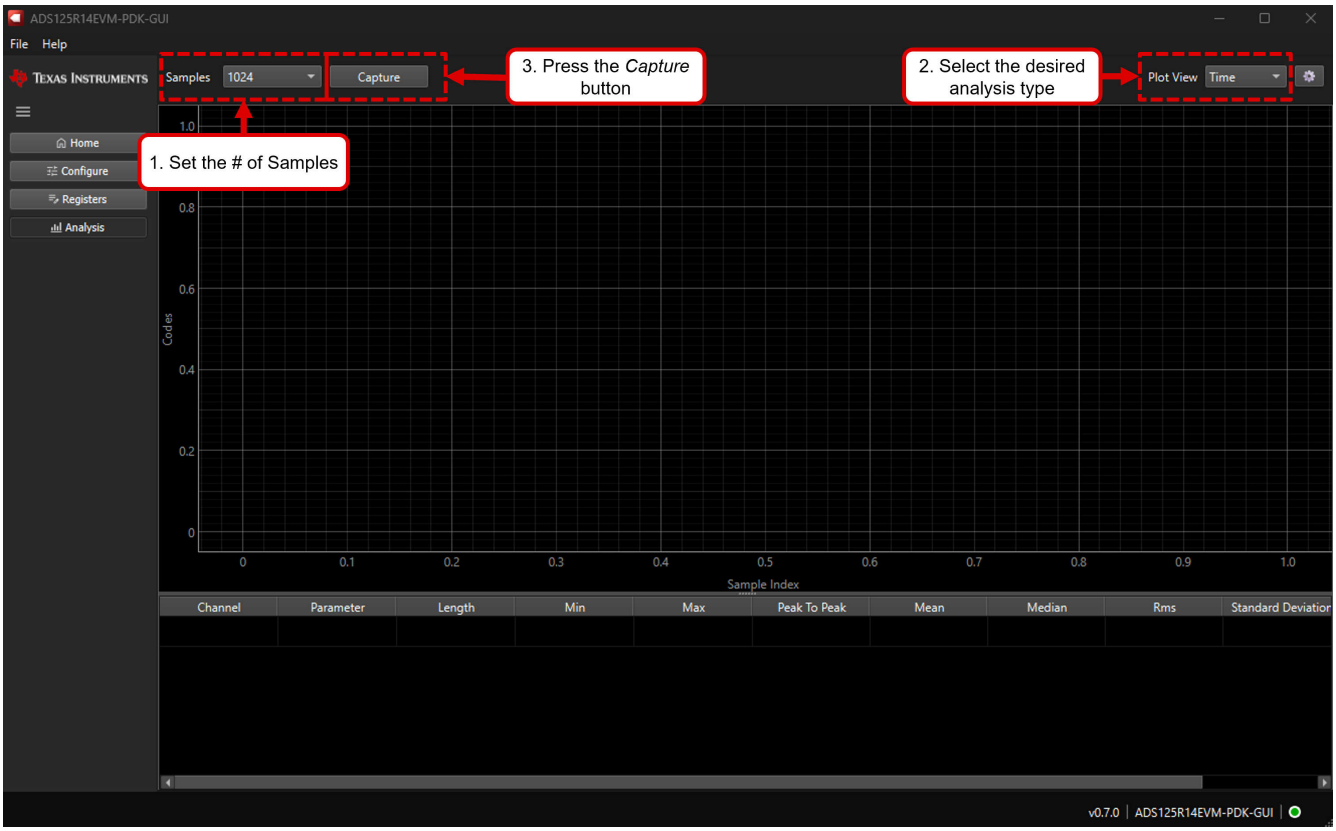


Figure 4-5. ADS125R14 EVM GUI Analysis Page

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4.4.1 Time-Domain Plot View

Figure 4-6 shows how the time-domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for studying the behavior of and debugging any gross problems with the ADC or drive circuits.



Figure 4-6. ADS125R14 EVM GUI Analysis Page - Time-Domain View

The default time-domain plot has *Samples* on the x-axis and *Codes* on the y-axis. Change the default values using the *Graph* controls in the top right. The output underneath the plot calculates several important parameters in both codes and voltage including the mean value, the peak-to-peak range, and the standard deviation.

Figure 4-7 shows how the user can right-click on the plot to export the raw data to a comma-separated variable (CSV) file or other output formats.

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Figure 4-7. ADS125R14 EVM GUI Analysis Page - Exporting Data

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4.4.2 Frequency-Domain Plot View

Figure 4-8 shows the spectral analysis tool that evaluates the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS125R14. This dynamic performance is calculated by single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The 7-term Blackman-Harris window has sufficient dynamic range to resolve the frequency components of a 24-bit ADC.

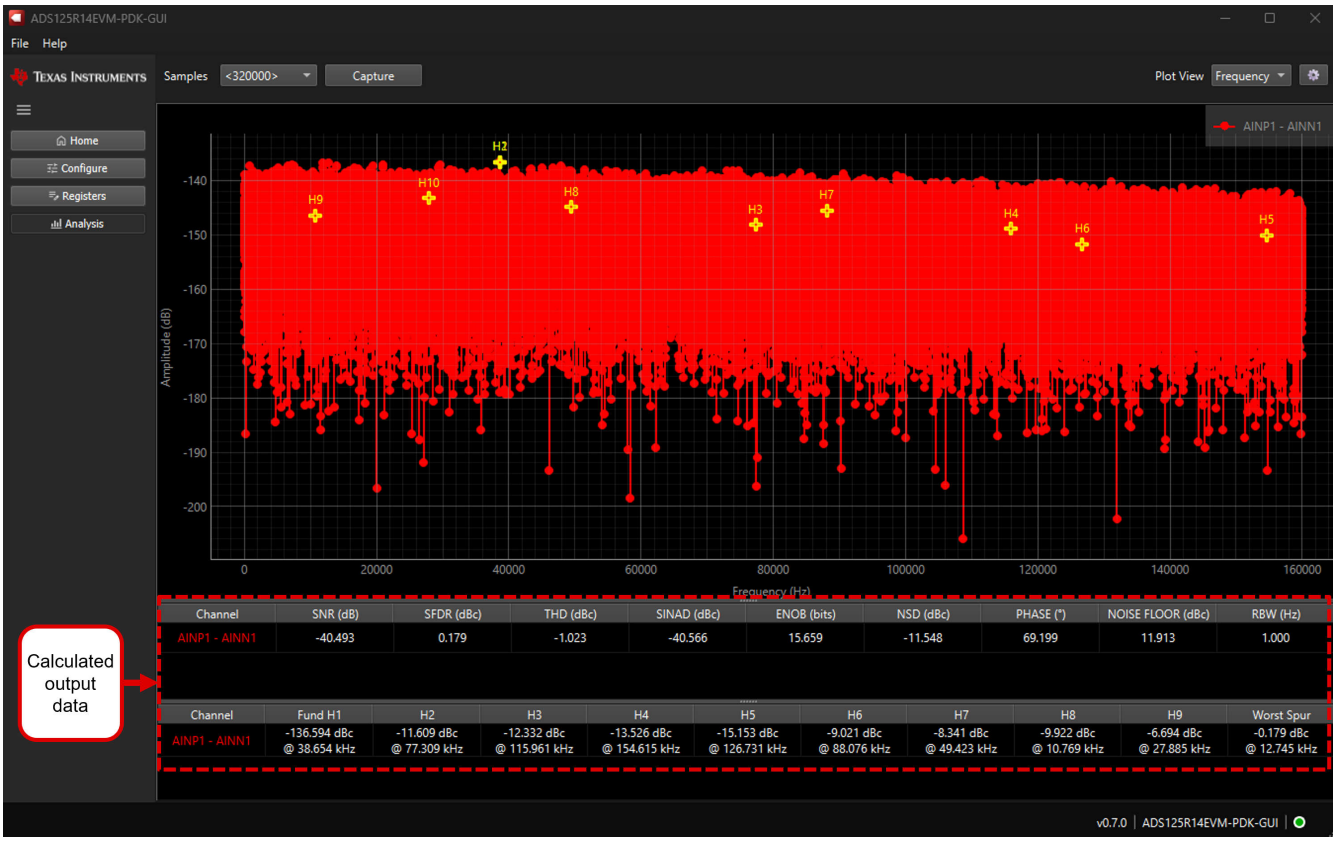


Figure 4-8. ADS125R14 EVM GUI Analysis Page - Frequency-Domain View

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5 Hardware Design Files

This section contains the ADS125R14 EVM schematics, PCB layout, and bill of materials (BOM).

5.1 Schematics

Figure 5-1 to Figure 5-6 show the complete ADS125R14 EVM schematic:

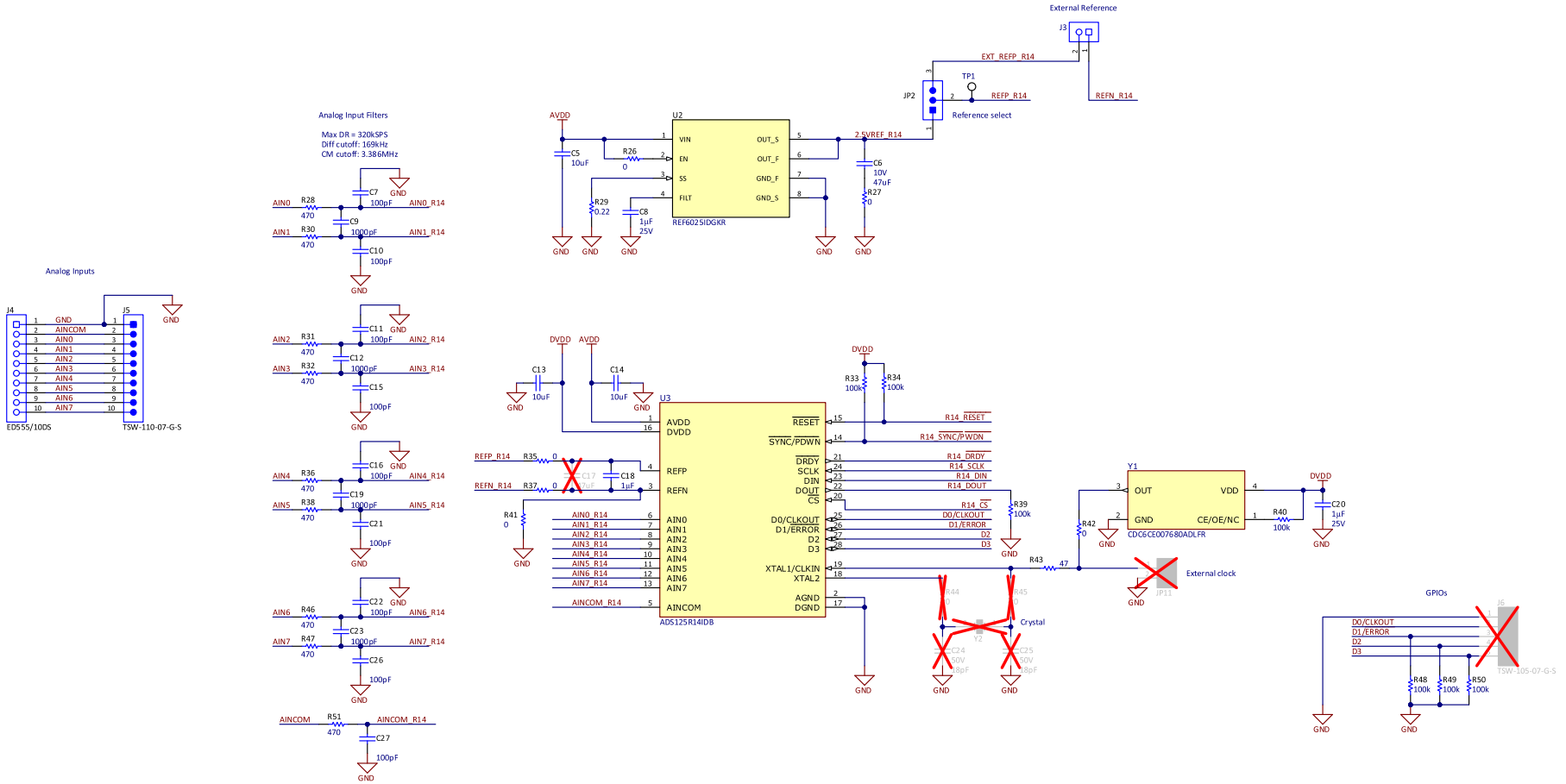


Figure 5-1. ADS125R14 EVM Schematic - ADS125R14

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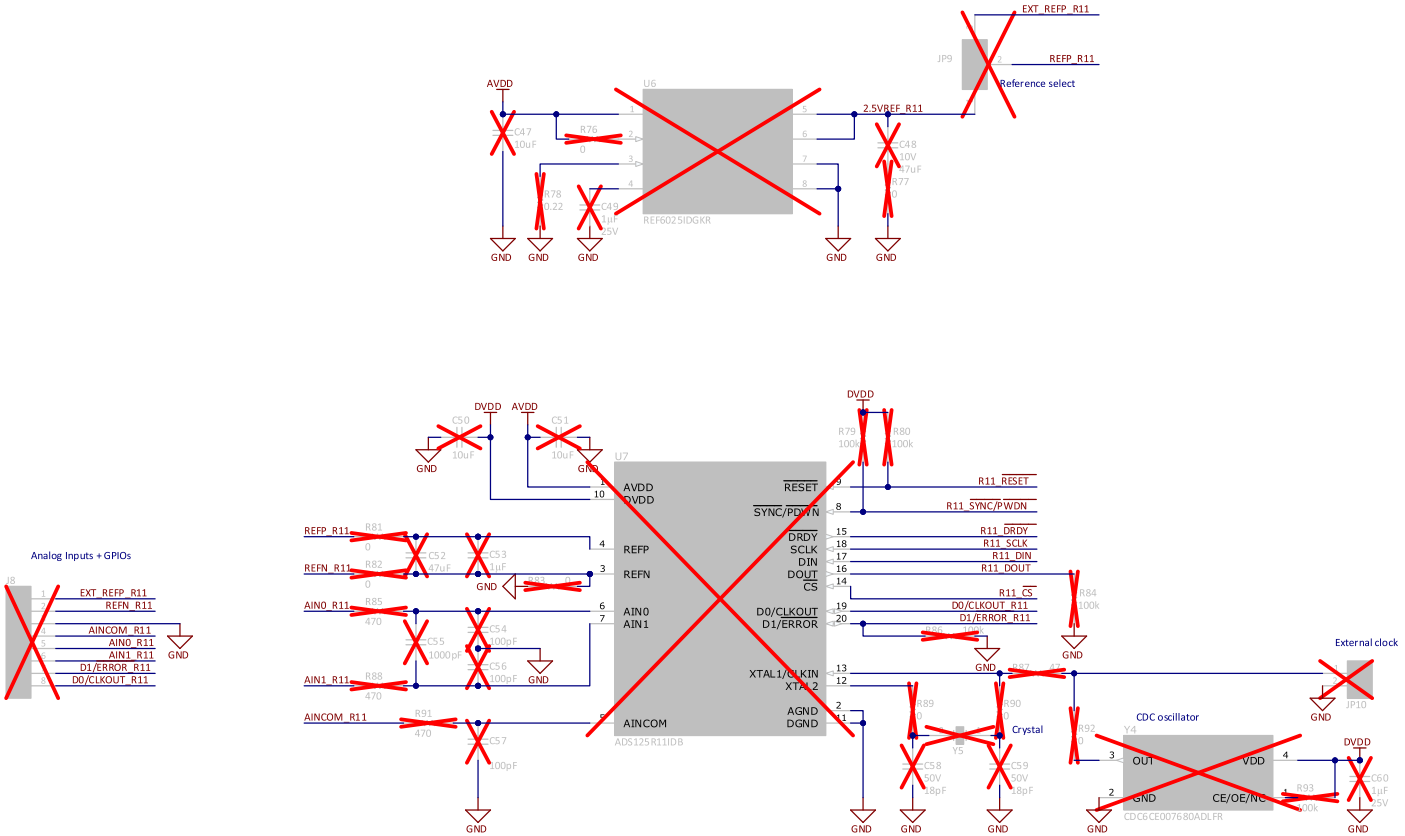


Figure 5-2. ADS125R14 EVM Schematic - ADS125R11

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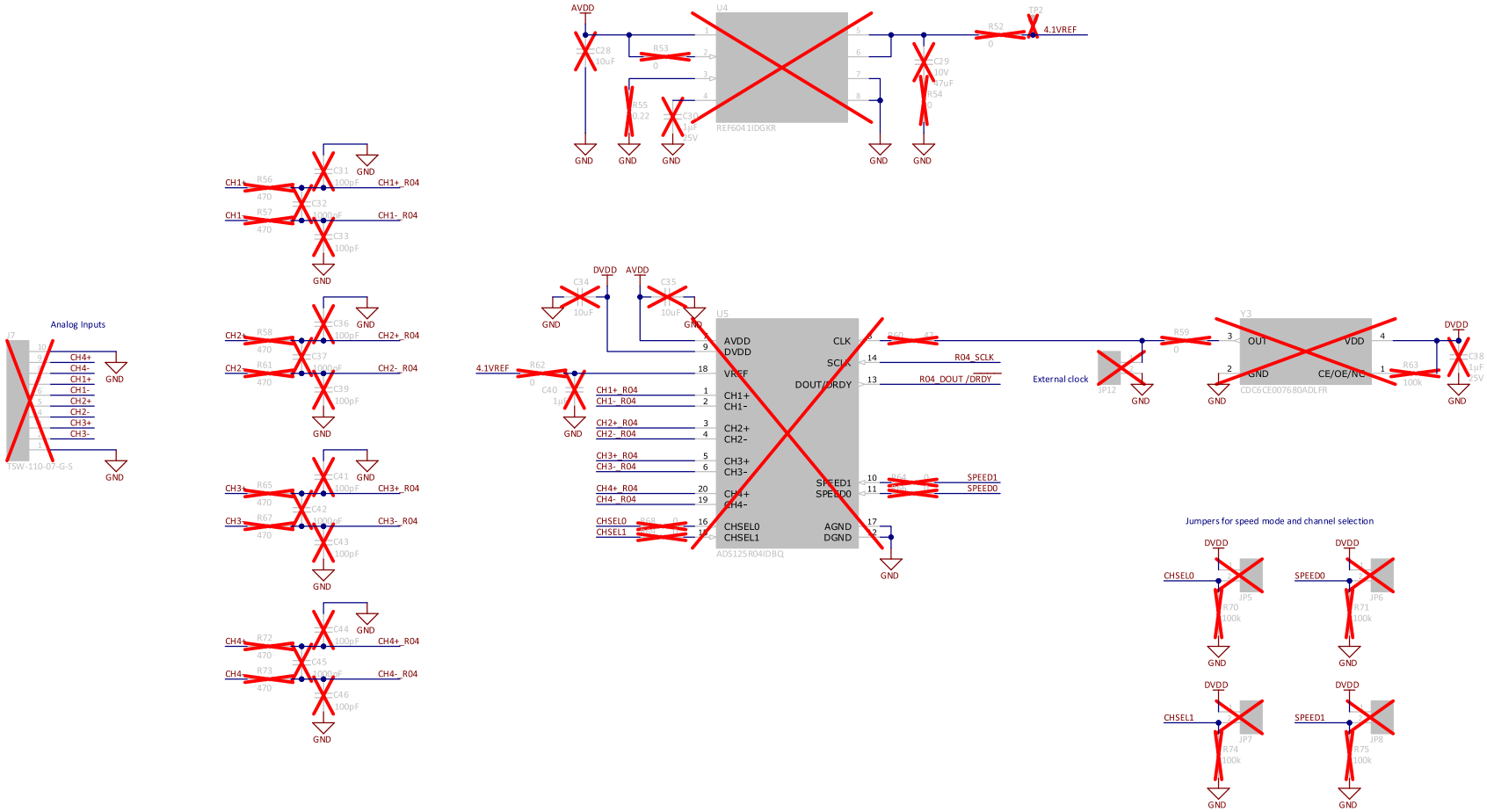


Figure 5-3. ADS125R14 EVM Schematic - ADS125R04

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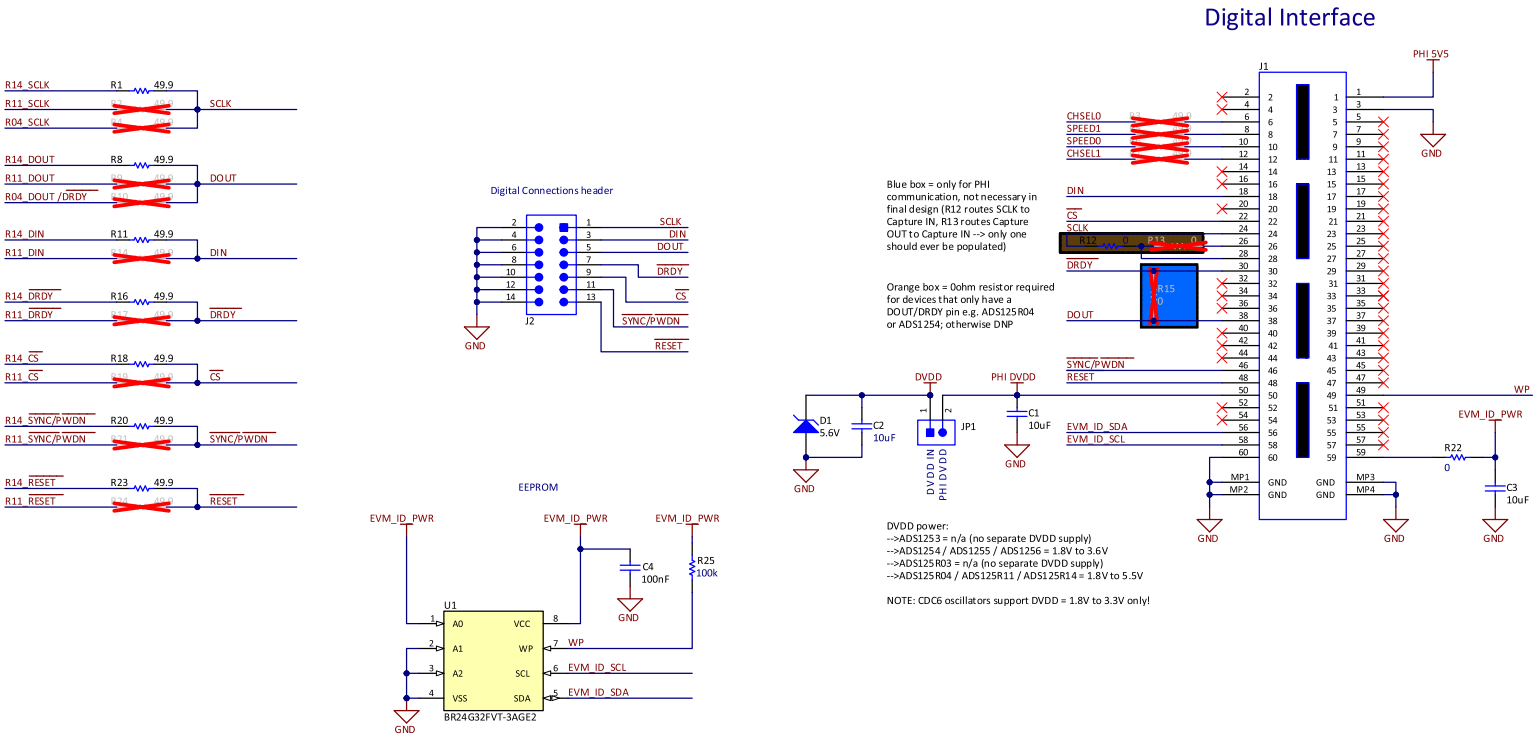


Figure 5-4. ADS125R14 EVM Schematic - Digital Connections

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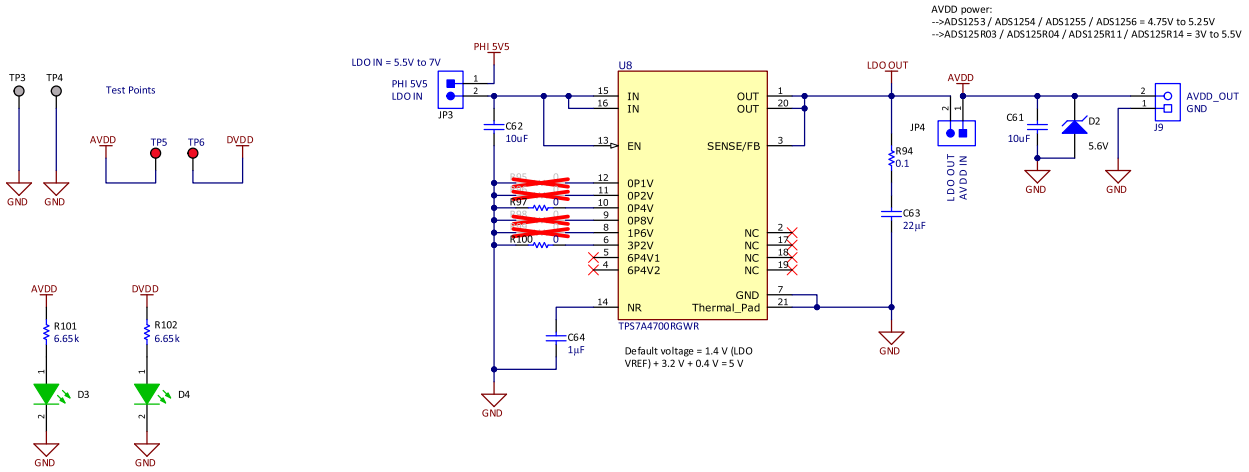


Figure 5-5. ADS125R14 EVM Schematic - Power Connections

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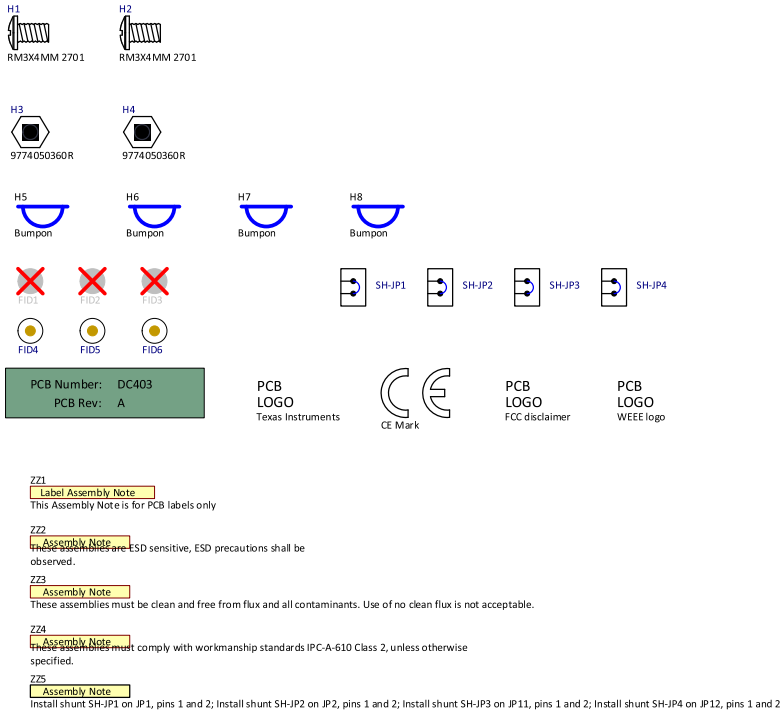


Figure 5-6. ADS125R14 EVM Schematic - Hardware

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5.2 PCB Layouts

Figure 5-7 to Figure 5-10 show the layout drawings for all ADS125R14 EVM PCB layers:

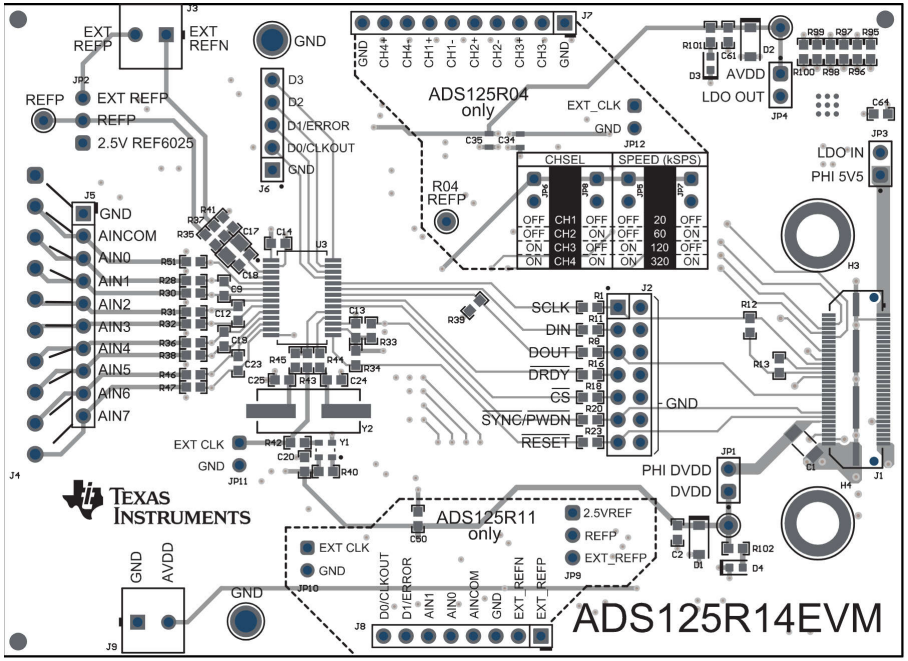


Figure 5-7. ADS125R14 EVM PCB Layout - Top Layer

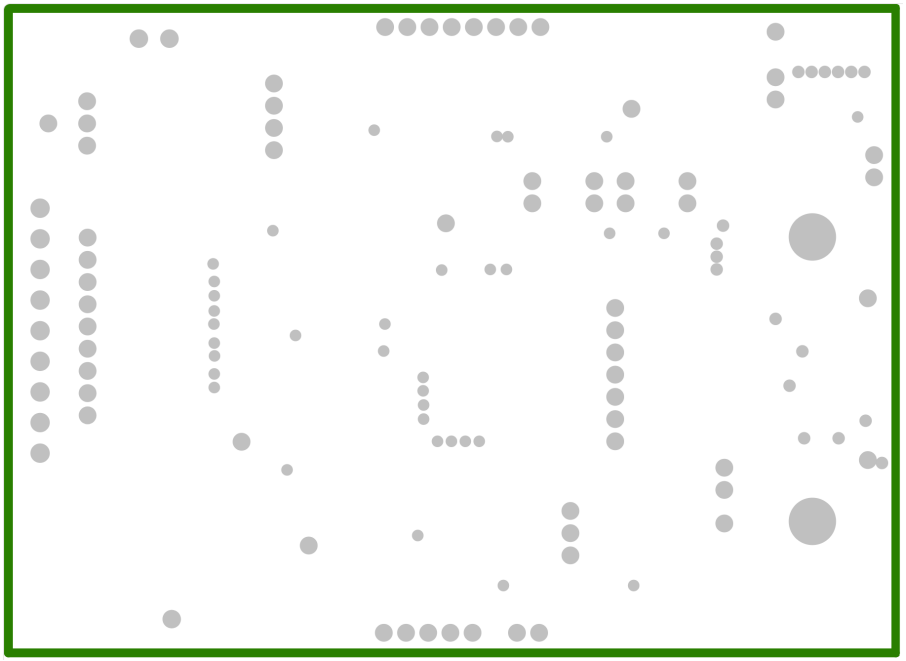


Figure 5-8. ADS125R14 EVM PCB Layout - Ground Layer 1

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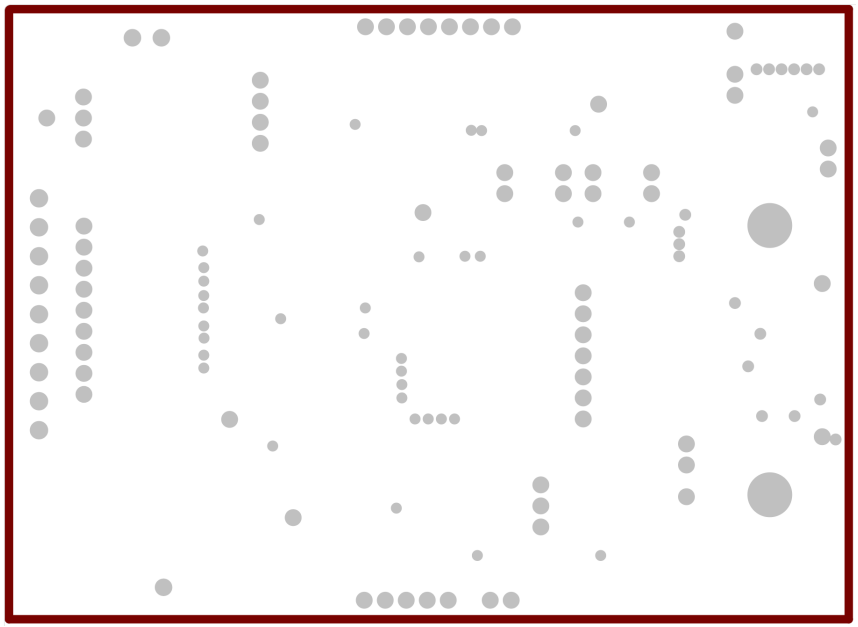


Figure 5-9. ADS125R14 EVM PCB Layout - Ground Layer 2

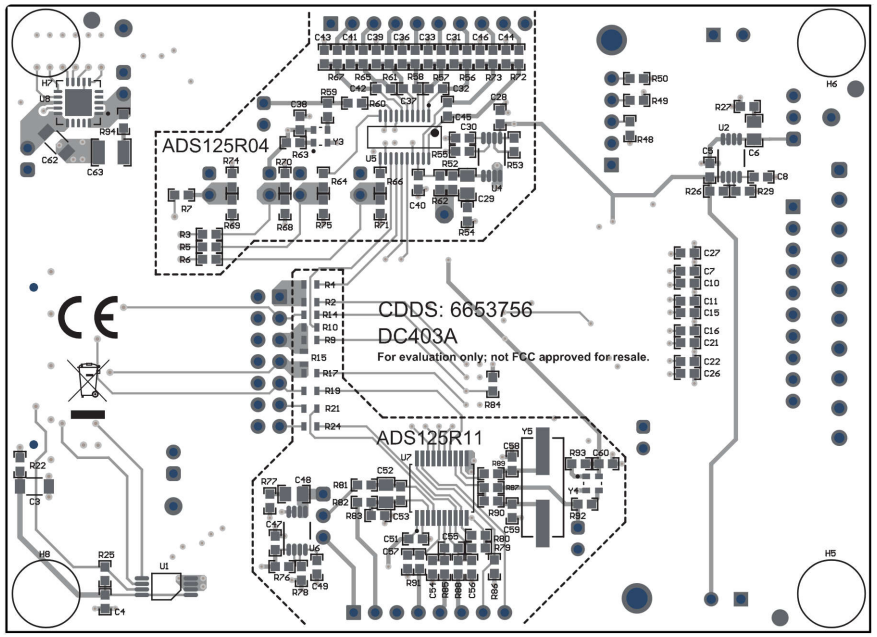


Figure 5-10. ADS125R14 EVM PCB Layout - Bottom Layer

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5.3 Bill of Materials (BOM)

Table 5-1 lists the ADS125R14 EVM bill of materials.

Table 5-1. ADS125R14 EVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C1, C3, C62	3	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
C2, C5, C13, C14, C61	5	10uF	CAP, CERM, 10 uF, 25 V, +/- 20%, X5R, 0603	0603	GRT188R61E106ME13D	MuRata
C4	1	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C104K3RACTU	Kemet
C6	1	47uF	CAP, CERM, 47 uF, 10 V, +/- 20%, X5R, 0805	0805	C2012X5R1A476M125AC	TDK
C7, C10, C11, C15, C16, C21, C22, C26, C27	9	100pF	CAP, CERM, 100 pF, 50 V,+/- 1%, C0G/NP0, 0603	0603	C0603C101F5GACTU	Kemet
C8, C18, C20, C64	4	1uF	CAP, CERM, 1 µF, 25 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1E105K080AC	TDK
C9, C12, C19, C23	4	1000pF	CAP, CERM, 1000 pF, 25 V,+/- 1%, C0G/NP0, 0603	0603	C0603C102F3GACTU	Kemet
C63	1	22uF	CAP, CERM, 22 µF, 25 V,+/- 10%, X7R, 1210	1210	CL32B226KAJNFNE	Samsung Electro-Mechanics
D1, D2	2	5.6V	Diode, Zener, 5.6 V, 500 mW, SOD-123	SOD-123	MMSZ4690-E3-08	Vishay-Semiconductor
D3, D4	2	Green	LED, Green, SMD	Body1.6x0.8mm	LTST-C193TGKT-5A	Lite-On
FID4, FID5, FID6	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
H3, H4	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
H5, H6, H7, H8	4		Bumpon, Cylindrical, 0.312 X 0.200, Black	Black Bumpon	SJ61A1	3M
J1	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
J2	1		Header, 100mil, 7x2, Gold, TH	7x2 Header	TSW-107-07-G-D	Samtec
J3, J9	2		Terminal Block, 3.5 mm, 2x1, Tin, TH	Terminal Block, 3.5 mm, 2x1, TH	0393570002	Molex
J4	1		Terminal Block, 3.5mm, 10x1, TH	Terminal Block, 3.5mm, 10x1, TH	ED555/10DS	On-Shore Technology
J5	1		Header, 100mil, 10x1, Gold, TH	10x1 Header	TSW-110-07-G-S	Samtec
JP1, JP3, JP4	3		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
JP2	1		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec

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Table 5-1. ADS125R14 EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R1, R8, R11, R16, R18, R20, R23	7	49.9	RES, 49.9, 0.5%, 0.1 W, 0603	0603	RT0603DRE0749R9L	Yageo America
R12, R22, R26, R27, R35, R37, R41, R42, R97, R100	10	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R25, R33, R34, R39, R40, R48, R49, R50	8	100k	RES, 100 k, 5%, 0.1 W, 0603	0603	CRCW0603100KJNEAC	Vishay-Dale
R28, R30, R31, R32, R36, R38, R46, R47, R51	9	470	RES, 470, 0.1%, 0.1 W, 0603	0603	RT0603BRD07470RL	Yageo America
R29	1	0.22	RES, 0.22, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3RQFR22V	Panasonic
R43	1	47	RES, 47, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060347R0JNEA	Vishay-Dale
R94	1	0.1	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	0603	ERJ-L03KF10CV	Panasonic
R101, R102	2	6.65k	RES, 6.65 k, 1%, 0.1 W, 0603	0603	RC0603FR-076K65L	Yageo
SH-JP1, SH-JP2, SH-JP3, SH-JP4	4	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1	1		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone Electronics
TP3, TP4	2		Terminal, Turret, TH, Triple	Keystone1598-2	1598-2	Keystone
TP5, TP6	2		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone Electronics
U1	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
U2	1		5ppm/C High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6025IDGKR	Texas Instruments
U3	1		ADS125R14IDB	SSOP28	ADS125R14IDB	Texas Instruments
U8	1		36-V, 1-A, 4.17-µVRMS, RF low-dropout (LDO) voltage regulator 20-VQFN -40 to 125	VQFN20	TPS7A4700RGWR	Texas Instruments
Y1	1		High-Performance BAW Oscillator	VSON4	CDC6CE007680ADLFR	Texas Instruments
C17, C29, C48, C52	0	47uF	CAP, CERM, 47 uF, 10 V, +/- 20%, X5R, 0805	0805	C2012X5R1A476M125AC	TDK
C24, C25, C58, C59	0	18pF	CAP, CERM, 18 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	06035A180JAT2A	AVX

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Table 5-1. ADS125R14 EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C28, C34, C35, C47, C50, C51	0	10uF	CAP, CERM, 10 uF, 25 V, +/- 20%, X5R, 0603	0603	GRT188R61E106ME13D	MuRata
C30, C38, C40, C49, C53, C60	0	1uF	CAP, CERM, 1 µF, 25 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1E105K080AC	TDK
C31, C33, C36, C39, C41, C43, C44, C46, C54, C56, C57	0	100pF	CAP, CERM, 100 pF, 50 V,+/- 1%, C0G/NP0, 0603	0603	C0603C101F5GACTU	Kemet
C32, C37, C42, C45, C55	0	1000pF	CAP, CERM, 1000 pF, 25 V,+/- 1%, C0G/NP0, 0603	0603	C0603C102F3GACTU	Kemet
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J6	0		Header, 100mil, 5x1, Gold, TH	5x1 Header	TSW-105-07-G-S	Samtec
J7	0		Header, 100mil, 10x1, Gold, TH	10x1 Header	TSW-110-07-G-S	Samtec
J8	0		Header, 100mil, 8x1, Gold, TH	8x1 Header	TSW-108-07-G-S	Samtec
JP5, JP6, JP7, JP8, JP10, JP11, JP12	0		Header, 2.54mm, 2x1, Tin, TH	Header, 2.54mm, 2x1, TH	TSW-102-23-T-S	Samtec
JP9	0		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
R2, R3, R4, R5, R6, R7, R9, R10, R14, R17, R19, R21, R24	0	49.9	RES, 49.9, 0.5%, 0.1 W, 0603	0603	RT0603DRE0749R9L	Yageo America
R13, R15, R44, R45, R52, R53, R54, R59, R62, R64, R66, R68, R69, R76, R77, R81, R82, R83, R89, R90, R92, R95, R96, R98, R99	0	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R55, R78	0	0.22	RES, 0.22, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3RQFR22V	Panasonic

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Table 5-1. ADS125R14 EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R56, R57, R58, R61, R65, R67, R72, R73, R85, R88, R91	0	470	RES, 470, 0.1%, 0.1 W, 0603	0603	RT0603BRD07470RL	Yageo America
R60, R87	0	47	RES, 47, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060347R0JNEA	Vishay-Dale
R63, R70, R71, R74, R75, R79, R80, R84, R86, R93	0	100k	RES, 100 k, 5%, 0.1 W, 0603	0603	CRCW0603100KJNEAC	Vishay-Dale
TP2	0		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone Electronics
U4	0		5ppm/C High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6041IDGKR	Texas Instruments
U5	0		ADS125R04IDBQ	SSOP20	ADS125R04IDBQ	Texas Instruments
U6	0		5ppm/C High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6025IDGKR	Texas Instruments
U7	0		ADS125R11IDB	SSOP20	ADS125R11IDB	Texas Instruments
Y2, Y5	0		Crystal, 7.68 MHz, 18pF, SMD	AT-Cut Crystal	HCM49-7.680MABJ-UT	Citizen Electronics
Y3, Y4	0		High-Performance BAW Oscillator	VSON4	CDC6CE007680ADLFR	Texas Instruments

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6 Additional Information

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7 References

1. Texas Instruments, ADS125R1x, 320kSPS, 24-Bit delta-sigma ADC with PGA, datasheet

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   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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