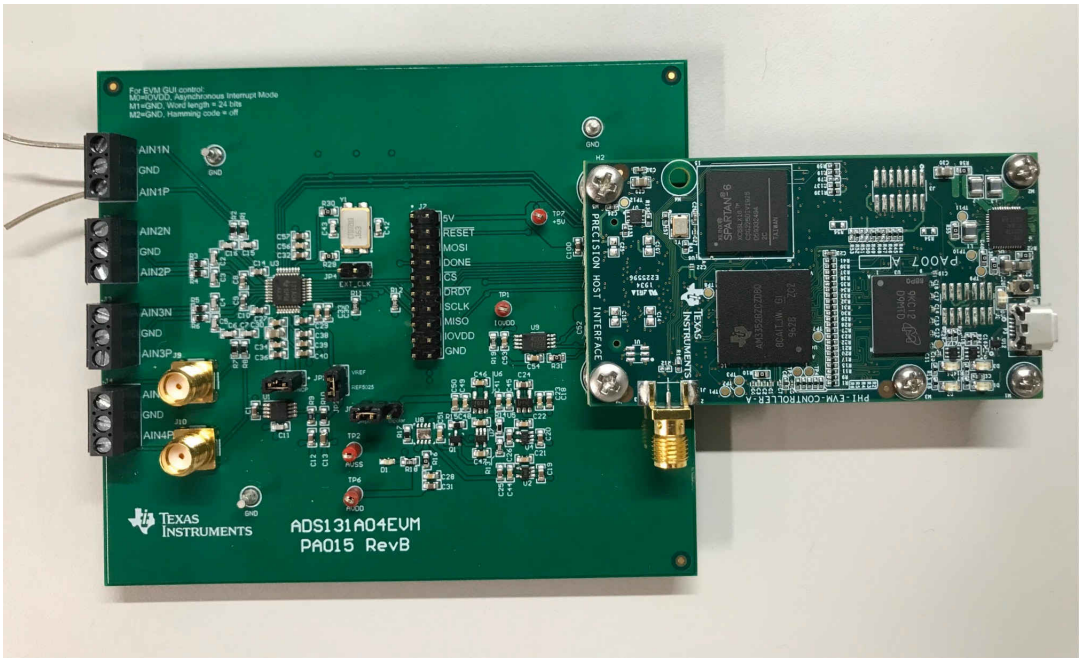
User's Guide

ADS131A04 Evaluation Module

Joseph Wu

ABSTRACT



This user's guide describes the characteristics, operation, and use of the ADS131A04 evaluation module (EVM). This kit is an evaluation platform for the ADS131A04, which is a 4-channel, simultaneously-sampling, 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADS131A04 offers wide dynamic range and internal calibration features, making the device excellent for energy metering, power quality, protection relay, and circuit breaker applications.

The ADS131A04EVM eases the evaluation of the device with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS131A04EVM. The following related documents are available through the Texas Instruments web site at www.ti.com.

Table 1-1. Related Documentation

Device	Literature Number
ADS131A04	SBAS590

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1 EVM Overview

The ADS131A04EVM is a platform for evaluating the performance of the ADS131A04, which is a 4-channel, simultaneously-sampling, 24-bit, ΔΣ ADC. The evaluation kit includes the ADS131A04EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture and analysis.

The ADS131A04EVM board includes the ADS131A04 ADC and all the peripheral analog circuits and components required to extract optimum performance from the ADC.

The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS131A04
- Supplies power to all active circuitry on the ADS131A04EVM board

1.1 ADS131A04EVM Kit

The ADS131A04 evaluation module kit includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS131A04 ADC
- USB powered—no external power supply is required
- The PHI controller that provides a convenient communication interface to the ADS131A04 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for 64-bit Microsoft Windows® 7, Windows 8, and Windows 10 operating systems
- The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a .CSV file for post-processing.

Figure 1-1 illustrates an example system setup for evaluation.

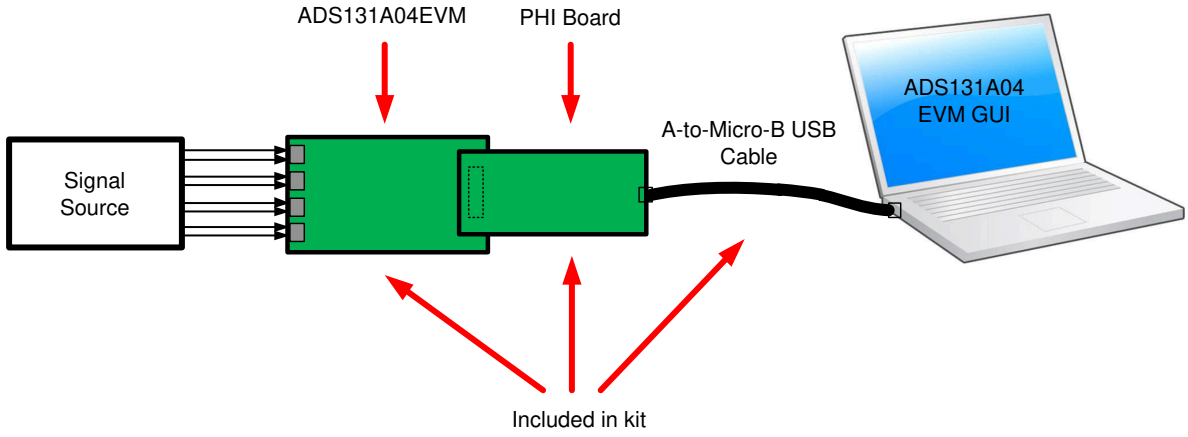

Figure 1-1. System Connection for Evaluation

1.2 ADS131A04EVM Board

The ADS131A04EVM board includes the following features:

- External signal source from differential pair headers
- Options to use external analog and digital power supplies
- Serial interface header for easy connection to the PHI controller
- Pin connections to monitor digital signals with a logic analyzer
- Onboard ultra-low noise low-dropout (LDO) regulator for excellent 3.3-V, single-supply regulation of all analog circuits

2 ADS131A04EVM Quick Start Guide

The following instructions are a step-by-step guide to connecting the ADS131A04EVM to the computer and evaluating the performance of the ADS131A04:

1. Review the default jumper settings in Section 6 and GUI software installation in Section 6.2.
2. Connect the ADS131A04EVM to the PHI. Install the two screws as indicated in Figure 2-1.
3. Use the provided USB cable to connect the PHI to the computer.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC. Figure 2-1 shows the resulting LED indicators.

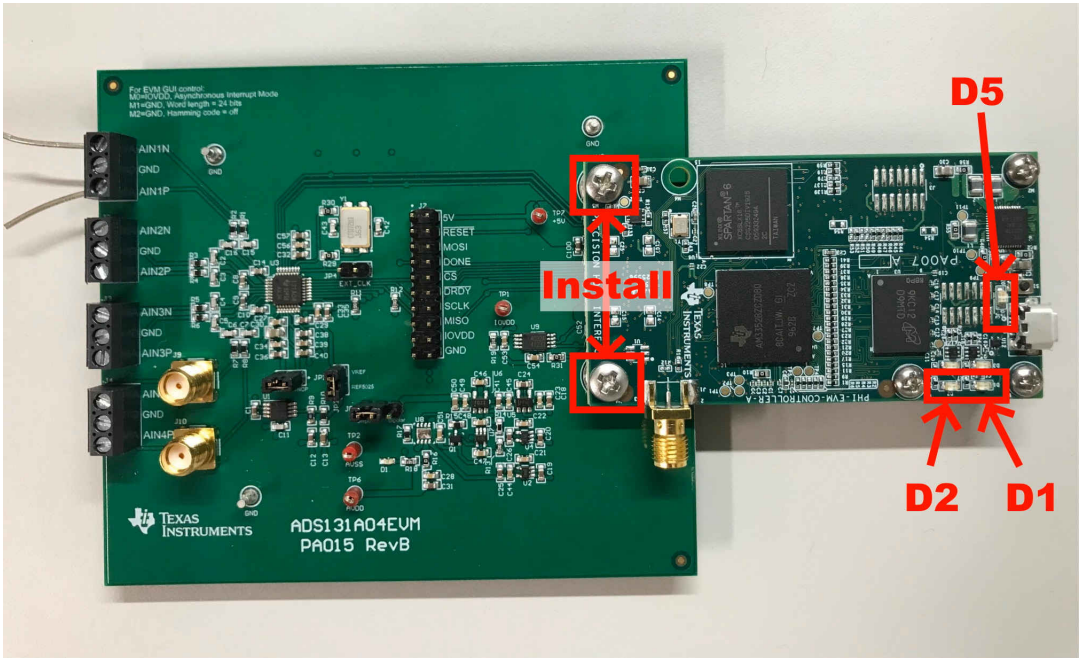

Figure 2-1. ADS131A04EVM Hardware Setup and LED Indicators

4. Launch the ADS131A04EVM GUI software as by clicking the ADS131A04EVM executable shown in Figure 2-2.

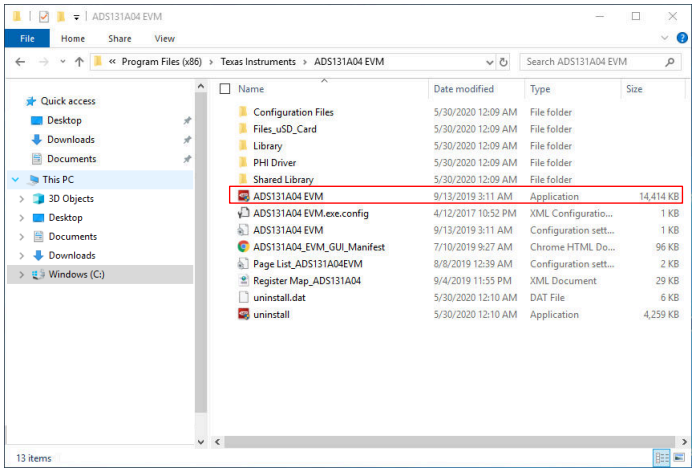

Figure 2-2. Launch the EVM GUI Software

5. Click the Wake Up and then Unlock button in the Single commands section of the GUI and start using the ADS1282EVM GUI to evaluate the EVM as shown in Figure 2-3. Learn more about EVM GUI Global Input Parameters and the various pages within the GUI in Section 7.1.

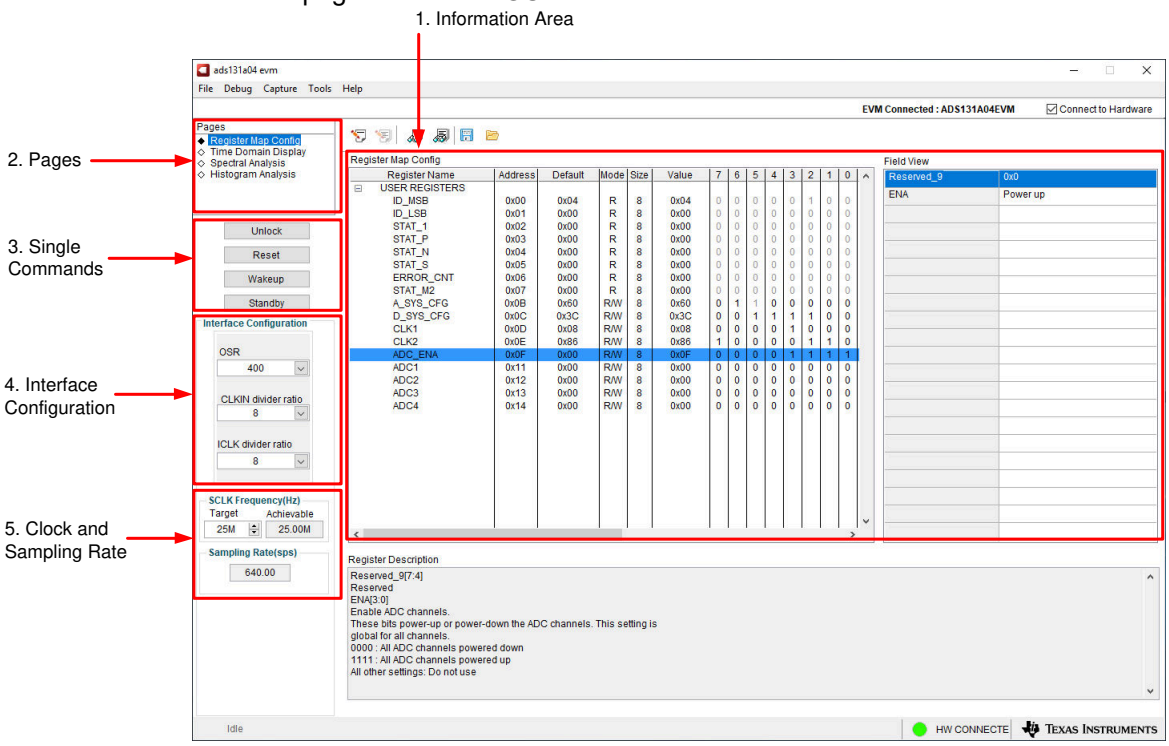

Figure 2-3. EVM GUI Global Input Parameters

3 EVM Analog Interface

The ADS131A04EVM is designed for easy interfacing with analog sources. This section covers the details of the front-end circuit including jumper configuration for different input test signals and board connectors for signal sources.

3.1 ADC Analog Input Signal Path

Analog inputs to the EVM can be connected to either the terminal blocks associated with each ADC channel. The screw terminal blocks (J1, J2, J3, and J4) can interface directly with the leads of an external sensor input. There are SMA connectors on channel 4, J9 for AIN4N and J10 for AIN4P, in addition to the terminal blocks that can be utilized as well. Figure 3-1 shows the signal chain used for all four input channels on the EVM and is used to describe the supported input options in Figure 3-1 and Figure 3-2.

An input must not be applied such that the voltage on the input pins of the ADS131A04 exceeds the absolute maximum ratings. For more details, see the *ADS131A04 4-Channel, Simultaneously-Sampling, 24-Bit, Delta-Sigma ADC Data Sheet*.

R1, R2, and C14 form a differential low-pass filter with a –3-dB cutoff frequency of 169.3 kHz for channel 1. In addition R1 and C15 with R2 and C16 form a common mode low-pass filter with a –3-dB cutoff frequency of 15.9 MHz. The series impedance is kept relatively low in order to maintain adequate total harmonic distortion (THD) performance. Similar differential and common model low pass filters are present on all inputs.

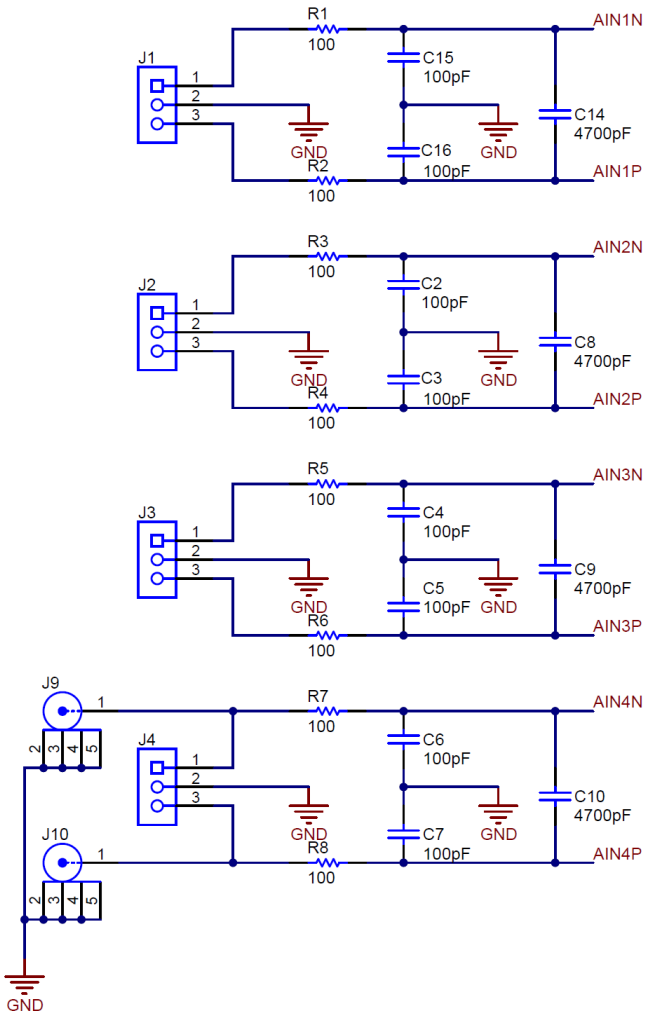

Figure 3-1. Input Terminal Blocks and Headers (Schematic)

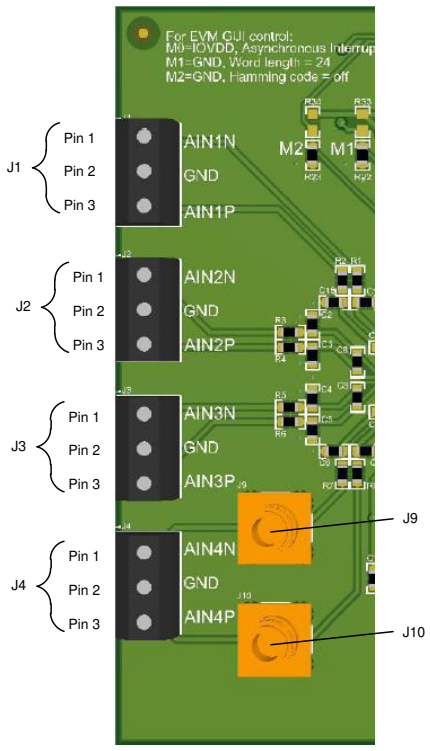

Figure 3-2. Input Terminal Blocks and Headers (PCB)

Table 3-1. Analog Input Terminal Blocks, J1–J4

Terminal Block	Pin	Function	ADS131A04 Input Pin(s)
J1	1	Channel 0 positive input	AIN0P
	2	EVM ground	AGND and DGND
	3	Channel 0 negative input	AIN0N
J2	1	Channel 1 positive input	AIN1P
	2	EVM ground	AGND and DGND
	3	Channel 1 negative input	AIN1N
J3	1	Channel 2 positive input	AIN2P
	2	EVM ground	AGND and DGND
	3	Channel 2 negative input	AIN2N
J4	1	Channel 3 positive input	AIN3P
	2	EVM ground	AGND and DGND
	3	Channel 3 negative input	AIN3N

3.2 ADC External Clock (XTAL1/CLKIN and XTAL2) Options

Multiple clocks are created from one external main clock source in the ADS131A04 to create device configuration flexibility. The ADC operates from the internal system clock, ICLK, which is provided in one of three ways.

- A crystal oscillator can be applied between XTAL1/CLKIN and XTAL2, generating a main clock to be divided down using the CLK_DIV[2:0] bits in the CLK1 register to generate ICLK.
  - The onboard crystal oscillator (Y1) provides the nominal 16.384-MHz clock frequency.
  - This is the default configuration for the EVM.
- An external main clock, CLKIN, can be applied directly to the XTAL1/CLKIN pin to be divided down to generate ICLK using the CLK_DIV[2:0] bits in the CLK1 register.
  - In this case, remove R29 and R30 to disconnect the crystal oscillator and use JP4 to provide an external clock. Pin 1 of JP4 is the CLKIN node where pin 2 of JP4 is GND.
  - Be sure to review the valid CLKIN input frequency in the datasheet when IOVDD is above 2.7 V (16.384-MHz typical) or below 2.7 V (8.192-MHz typical).
- A free-running SCLK can be internally routed to be set as ICLK. This mode is only available in synchronous peripheral SPI interface mode. Tie the CLKIN/XTAL1 pin to GND.
  - To tie the CLKIN/XTAL1 pin to GND, cover JP4 1x2, 100 mil header with a jumper.
  - Note this interface mode is not compatible with the provided EVM software.

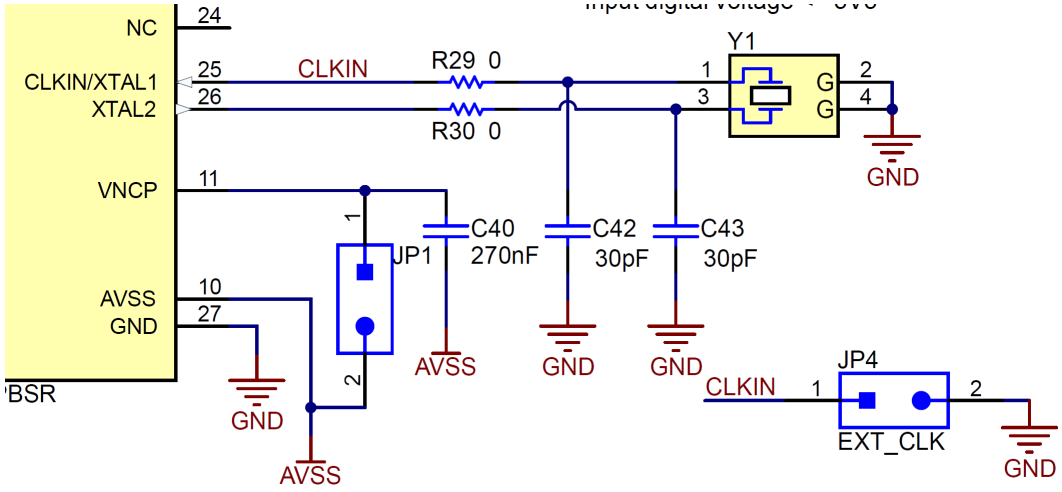

Figure 3-3. XTAL1/CLKIN and XTAL2 Clock (Schematic)

The hardware changes are described in Table 3-2.

Table 3-2. Clock Source Options for XTAL1/CLKIN and XTAL2

Clock Source Option	Hardware Description
An external main clock	Uninstall R29 and R30, use JP4 pin 1 for the CLKIN signal and JP4 pin 2 for GND
A crystal oscillator (Default)	Ensure R29, R30, and Y1 are populated
A free-running SCLK	Install jumper onto JP4 to connect XTAL1/CLKIN to GND

4 Digital Interface

As noted in Section 1, the EVM interfaces with the PHI and communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the ADS131A04 ADC (over SPI) and the EEPROM (over I^2C). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS131A04EVM platform. When the hardware is initialized, the EEPROM is no longer used.

4.1 SPI Communication

The ADS131A04EVM supports limited interface modes as detailed in the ADS131A04 data sheet. The ADS131A04 uses an SPI-compatible interface to configure the device and retrieve conversion data. SPI communication on the ADS131A04 is performed in frames. Each SPI communication frame consists of several words. The word size is configurable as either 16 bits, 24 bits (default), or 32 bits by setting the state of M1 pin to Hi-Z, GND, or IOVDD, respectively.

For this EVM not all modes and functions for this SPI communication are supported. Specifically, the EVM GUI software expects SPI words size to be 24 bits. For more information about the SPI communication, see the *ADS131A0x 2- or 4-Channel, 24-Bit, 128-kSPS, Simultaneous-Sampling, Delta-Sigma ADC Data Sheet*.

4.2 Connection to the PHI

The ADS131A04EVM board communicates with the PHI through a shrouded, 60-pin connector, J5. There are two round standoffs next to J5 with Phillips-head screws. To connect the PHI to the EVM, remove the screws, attach the PHI to the EVM, and replace the screws into the standoffs. The screws secure the EVM to the PHI and ensures the connection between the boards.

Table 4-1 lists the different PHI connection and their functions.

Table 4-1. PHI Connector Pin Functions

PHI Connector Pin Name	PHI Connector Pin	Function
EVM_RAW_5V	J5[2]	Power-supply source for the analog section of the EVM
GND	J5[3]	Ground
M0	J5[6]	SPI configuration mode select pin
M1	J5[8]	SPI word size select pin
M2	J5[10]	Hamming code enable pin
DIN	J5[18]	Serial data input for the ADS131A04
$\overline{CS}$	J5[22]	Chip-select for the ADS131A04; active-low
SCLK	J5[24]	Serial data clock for the ADS131A04
SCLK	J5[28]	Serial data clock for the ADS131A04
$\overline{DRDY}$	J5[30]	Data-ready for the ADS131A04; active-low
DOUT	J5[36]	Serial data output for the ADS131A04
$\overline{RESET}$	J5[46]	Conversion system reset for the ADS131A04; active-low
WP	J5[49]	Write protection for EEPROM
3V3_IOVDD	J5[50]	Power-supply source for the digital section of the EVM
SDA	J5[56]	I^2C serial data for the EEPROM used to identify the EVM
SCL	J5[58]	I^2C serial clock for the EEPROM used to identify the EVM
EVM_ID_PWR	J5[59]	Power-supply source for the EEPROM used to identify the EVM
GND	J5[60]	Ground

4.3 Digital Header

In addition to the PHI, the EVM has a header connected to the digital lines that can be used to connect a logic analyzer or oscilloscope. This placement allows for easy access to the digital communications. Header J7 is connected to the digital lines between the ADS131A04 and the PHI connector. Table 4-2 describes the digital header pins.

Table 4-2. Digital Header Pins

Signal Name	Digital Header Pin
EVM_RAW_5V	J7[1-2]
$\overline{\text{RESET}}$	J7[3-4]
DIN	J7[5-6]
$\overline{\text{DONE}}$	J7[7-8]
$\overline{\text{CS}}$	J7[9-10]
$\overline{\text{DRDY}}$	J7[11-12]
SCLK	J7[13-14]
DOUT	J7[15-16]
3V3_IOVDD	J7[17-18]
GND	J7[19-20]

4.4 LaunchPad™ Connectors

On the bottom side of the ADS131A04EVM board is a set of unpopulated surface-mount connectors (J6 and J8). When populated, these devices can be used to connect to a TI LaunchPad directly as a typical BoosterPack™ plug-in module.

Connectors J6 and J8 are a set of 10x2, 100 mil connectors. As shown in Table 4-3, the pin numbers for J6 and J8 map to the pin numbers for a standard 40-pin LaunchPad connector. To align pin 1 of the launch pad to J6[1], which corresponds to +3.3V, the PHI connector (J5) on the ADS131A04EVM will face towards the top of the launchpad, and the launchpad will be placed underneath the ADS131A04EVM.

Table 4-3. LaunchPad Pin Functions

ADS131A04EVM Connection	ADS131A04EVM (J6, J8)	LaunchPad Connection
3V3_IOVDD(+3.3 V)	J6[1]	Pin 1
SCLK	J6[13]	Pin 7
EVM_ID_SCL	J6[17]	Pin 9
EVM_ID_SDA	J6[19]	Pin 10
DOUT	J8[14]	Pin 17
DIN	J8[12]	Pin 18
GND	J8[2]	Pin 19
EVM_RAW_5V(+5 V)	J6[2]	Pin 21
GND	J6[4]	Pin 22
$\overline{\text{DRDY}}$	J8[7]	Pin 37
$\overline{\text{CS}}$	J8[5]	Pin 38
$\overline{\text{RESET}}$	J8[3]	Pin 39

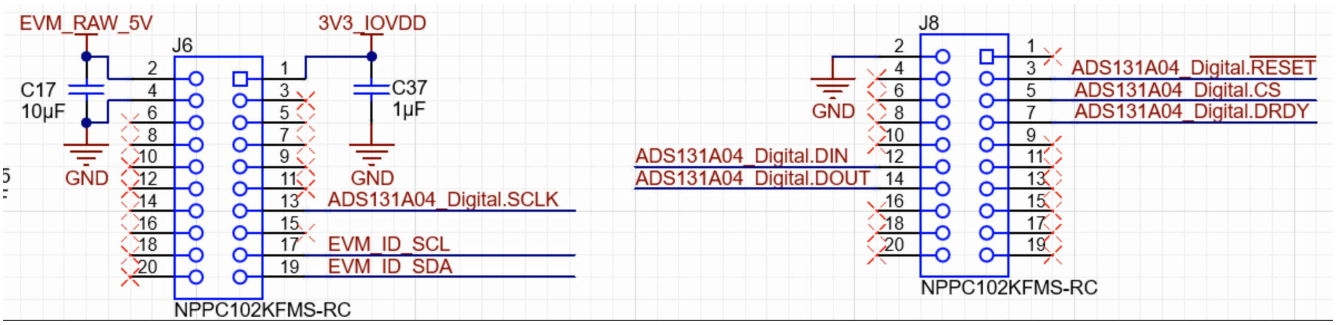

Figure 4-1. Launchpad connector (schematic)

5 Power Supplies

The PHI provides multiple power-supply options for the EVM, derived from the USB supply of the computer which is routed to EVM_RAW_5V on the ADS131A04EVM on the board.

The EEPROM on the ADS131A04EVM uses a 3.3-V power supply, EVM_ID_PWR, generated directly by the PHI. The 3.3-V supply to the digital section of the ADC, 3V3_IOVDD, is provided directly by a separate LDO on the PHI.

The analog supply of the ADC, AVDD, is powered by the TPS71733 onboard the EVM, which is a low-noise linear regulator that uses the 5-V supply on the PHI to generate a cleaner 3.3-V output. There is also an inverting charge pump regulator, TPS60403, and fixed-output LDO, TPS72325, which converts the 5-V to -2.5-V.

The user has the option to configure the EVM for unipolar supplies (AVSS = 0V and AVDD = 3.3V) by placing a jumper to cover pins 1 and 2 of JP3, or to configure the EVM for bidirectional supplies (AVSS = -2.5 V and AVDD = 2.5 V) by placing the jumper to cover pins 2 and 3 of JP3. The TPS2115 and TLV3691 work to automatically select the correct value for AVDD so that the AVDD to AVSS voltage does not go above the recommended operating conditions.

AVDD is used as the supply for the REF5025, which is a drift precision series voltage reference that outputs 2.5 V with respect to AVSS. This can be used to supply REFEXT for the ADS131A04 using JP2.

The power supply for each active component on the EVM is bypassed with a ceramic capacitor placed close to that component. Additionally, the EVM layout uses thick traces or large copper fill areas, where possible, between bypass capacitors and their loads to minimize inductance along the load current path.

As mentioned previously in Section 1, power to the EVM is supplied by the PHI through connector J5. For information about PHI pins and the power connections, see Table 4-1.

With modifications, the user may use external supplies for either AVDD or DVDD. AVDD can be driven externally by uninstalling R16. Power can then be applied through the AVDD test point at TP6. DVDD can be driven externally from the DVDD test point at TP1 if R100 is removed from the EVM.

6 ADS131A04EVM Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for properly operating the ADS131A04EVM.

6.1 Default Jumper Settings

After unpacking, the EVM is already configured with the default jumper settings. Figure 6-1 shows the locations for the default jumpers.

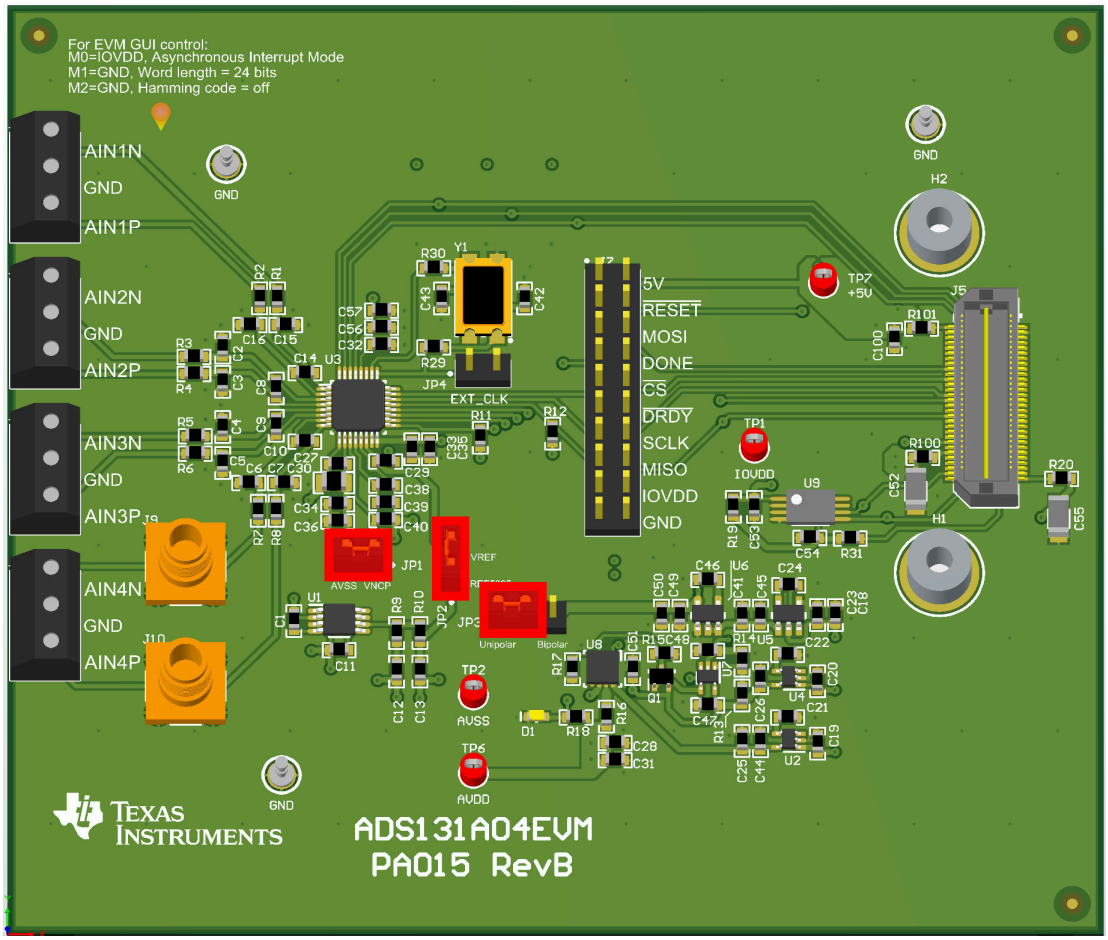

Figure 6-1. ADS131A04EVM Jumper Default Settings

The default position of the JP1 jumper ties VNCP, the negative charge pump, to AVSS to effectively disable it. The negative charge pump can also be disabled by setting VNCPEN to 0b0, which is the default value on power up. The default position of JP2 (labeled VREF in silkscreen) connects the REF5025, which outputs 2.5-V, to the REFEXT pin of the ADS131A04.

JP3 sets the EVM in unipolar supply mode by default, where AVDD = 3.3-V and AVSS = 0-V or GND. Specifically, the jumper covers pins 1 and 2 of JP3.

Table 6-1. Default Settings

Jumper	Position	Function
JP1	[1-2]	Disables negative charge pump
JP2	[1-2]	Connects 2.5-V t0 REFEXT with respect to AVSS
JP3	[1-2]	Sets AVSS to GND for unipolar supply mode
JP4	Not installed	Header to supply external clock

6.2 EVM Graphical User Interface (GUI) Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS131A04EVM and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message may appear or the installer. The exe file can be deleted.

Accept the license agreements and follow the on-screen instructions shown in Figure 6-2 to complete the installation.

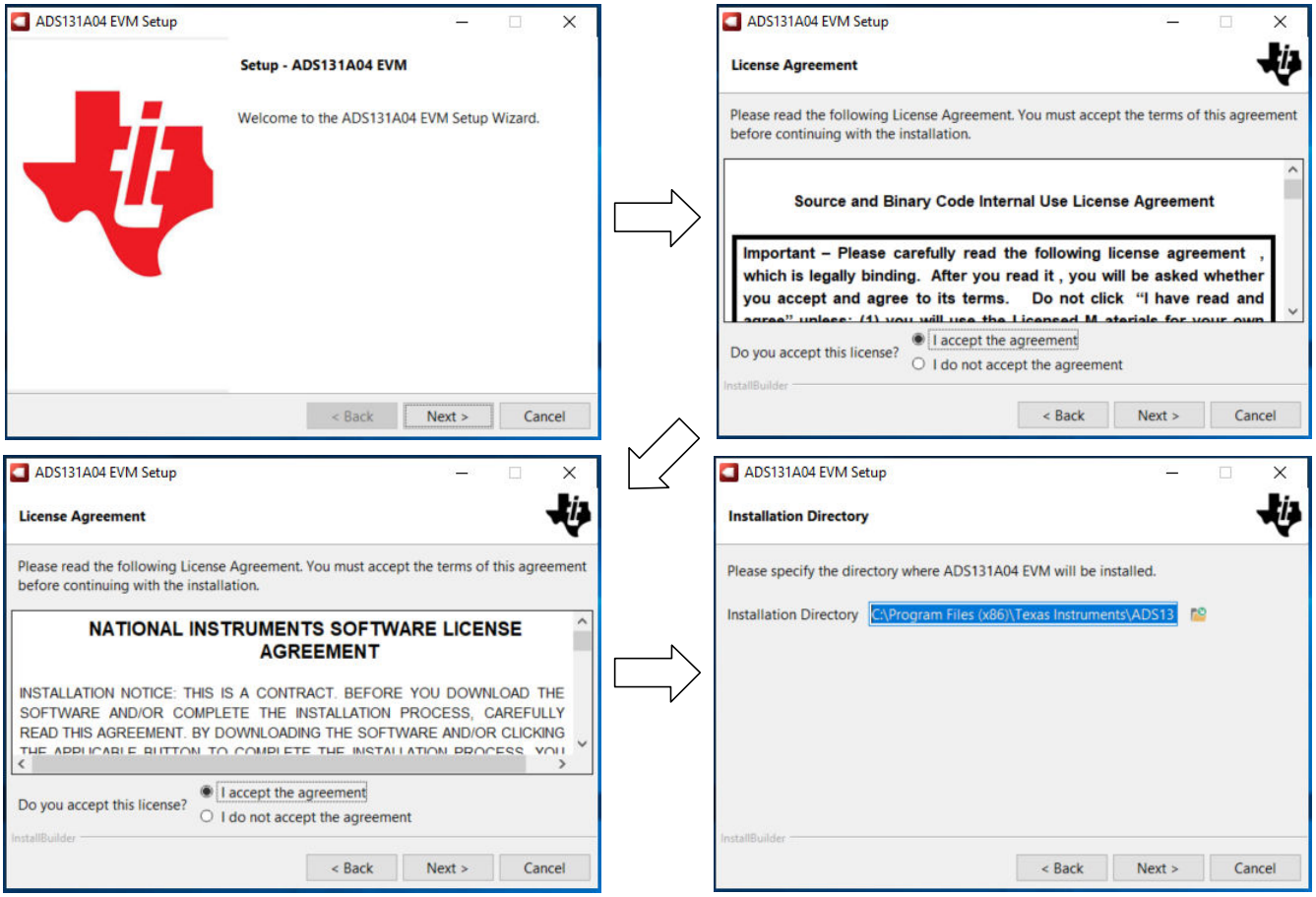

Figure 6-2. ADS131A04 Software Installation Prompts

As a part of the ADS131A04EVM GUI installation, a prompt with a Device Driver Installation (as shown in Figure 6-3) appears on the screen. Click *Next* to proceed.

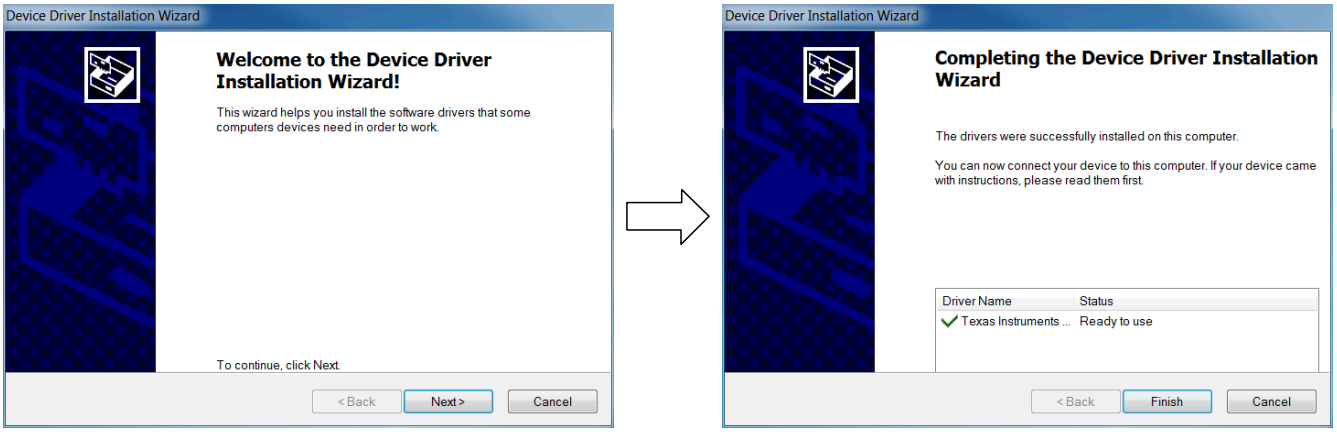

Figure 6-3. Device Driver Installation Wizard Prompts

Note

A notice may appear on the screen stating that Windows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

The ADS131A04EVM requires the LabVIEW® run-time engine and may prompt for the installation of this software, as shown in Figure 6-4, if not already installed.

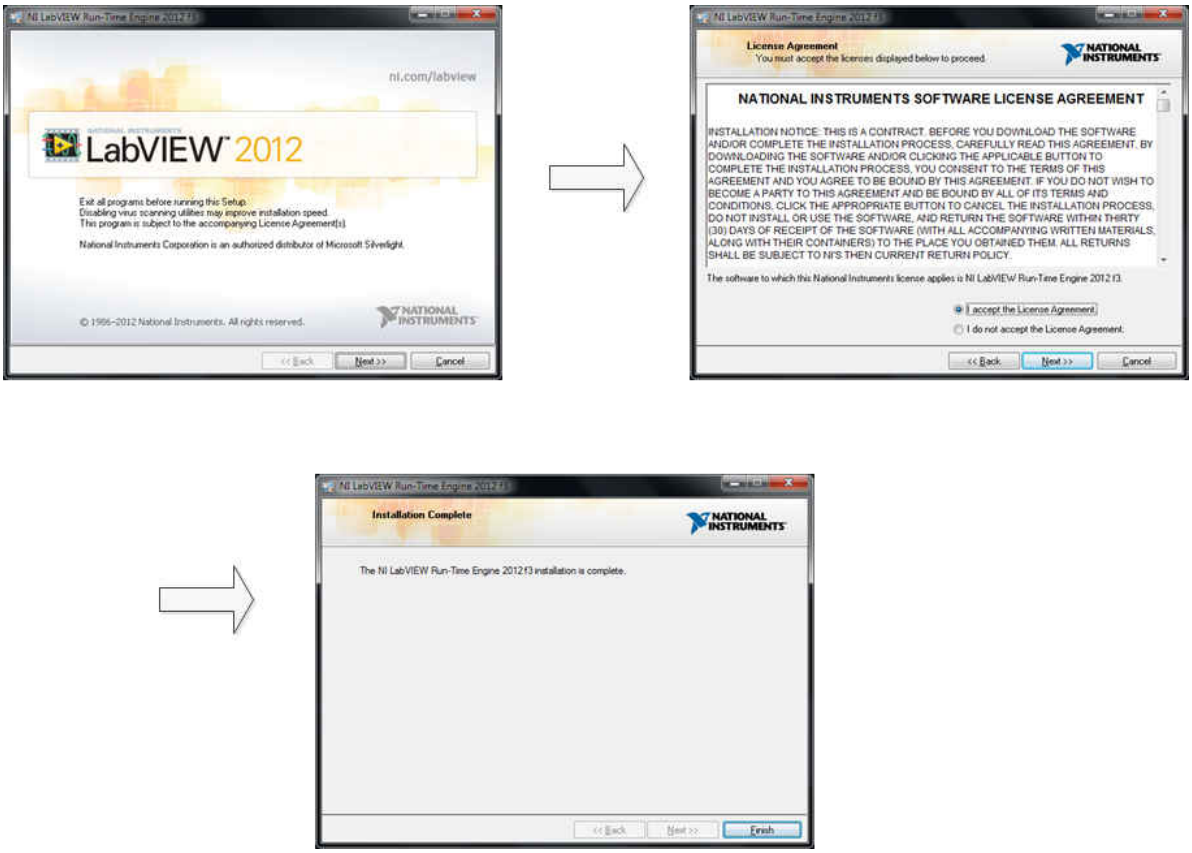

Figure 6-4. LabVIEW Run-Time Engine Installation

Verify that *C:\Program Files (x86)\Texas Instruments\ADS131A04EVM* is after these installations.

7 ADS131A04EVM Software Reference

7.1 EVM GUI Global Settings for ADC Control

Although the EVM GUI does not allow direct access to the levels and timing configuration of the ADC digital interface, the EVM GUI does give users high-level control over many other functions of the ADS131A04 including: internal clock dividers, oversampling ratio (OSR), and number of samples to be captured. Figure 7-1 identifies the input parameters of the GUI (as well as their default values) through which the various functions of the ADS131A04 can be exercised.

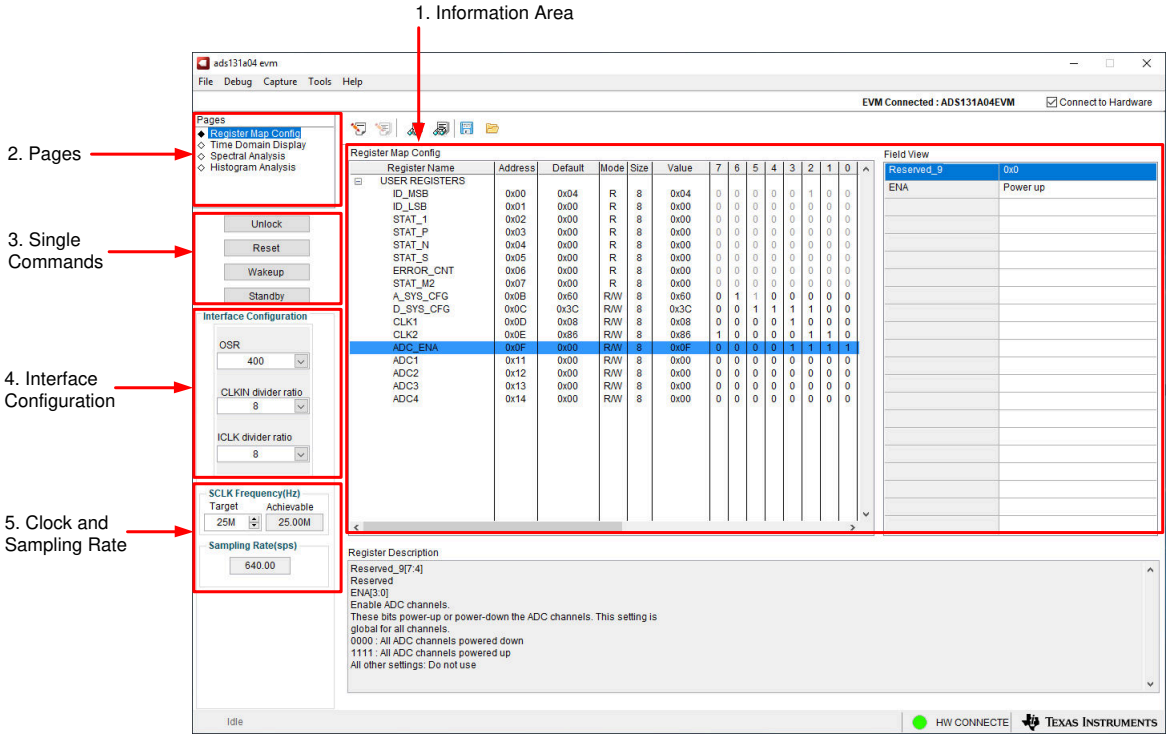

Figure 7-1. EVM GUI Global Input Parameters

There are four pages available in the ADS131A04EVM GUI. The information area displays the results of each of the pages. Each of these pages display a different control or measurement of the device. The Register Map Config page is used to read and write to the registers of the device. The Time Domain Display page is used to collect a set of data from the device and display the result. The Spectral Analysis page can compute the FFT of the collected data, and the Histogram Analysis page shows a histogram of the collected data and displays basic statistics of the result.

The Single Commands section allows for direct control of the device for three basic functions. First the *Reset* button sends a signal to the RESET pin to reset the device. The *Standby* button puts the device into a low-power state in which all channels are disabled, and the reference and other non-essential circuitry are powered down. The *Wakeup* button exits the standby mode.

The interface section also sets the data rate by setting the internal clock dividers and OSR in the ADC. Finally, this section may used to set the power modes in the registers. The ADS131A04 has two power modes (Low-Power and High-Resolution), which is configured in the A_SYS_CFG register (bit 6). This is used in conjunction with the jumper settings of JP4 for the CLKIN pin, as outlined in Table 3-2. This information is also discussed in Section 3.2.

The Clock and Sampling Rate section allows the user to specify a target SCLK frequency (in Hz) and the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings, but the achievable frequency may differ from the target value entered. This section also displays the sampling rate of the ADC as controlled by the internal clock dividers and the OSR.

The GUI is switched between hardware mode and simulation mode by checking and unchecking the *Connected to Hardware* box in the top right area of the screen at any time.

7.2 Register Map Configuration Tool

The register map configuration tool allows the user to view and modify the registers of the ADS131A04. This tool can be selected, as indicated in Figure 7-2, by clicking on the *Register Map Config* radio button at the Pages section of the left pane. On power-up, the values on this page correspond to the Host Configuration Settings that enable ADC sampling at the maximum sampling rate specified for the ADC. The register values can be edited by double-clicking the corresponding value field. If interface mode settings are affected by the change in register values, this change reflects on the left pane immediately.

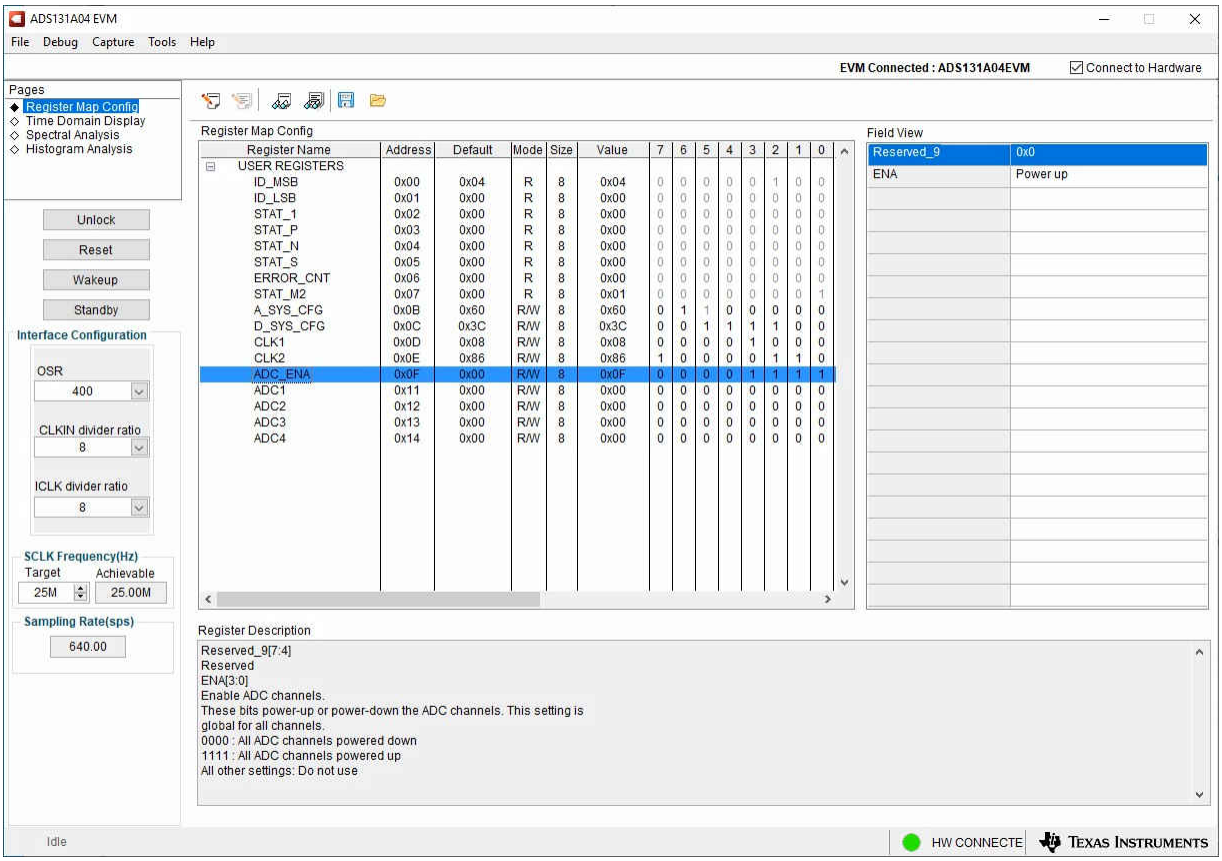

Figure 7-2. Register Map Configuration

Section 7.3 through Section 7.5 describe the data collection and analysis features of the ADS131A04EVM GUI.

7.3 Time Domain Display Tool

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits.

The user can trigger a capture of the data of the selected number of samples from the ADS131A04EVM, as per the current interface mode settings indicated in Figure 7-3 by using the *Capture* button. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the Analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

Figure 7-3. Time Domain Display Tool Options

7.4 Spectral Analysis Tool

The spectral analysis tool, shown in Figure 7-4, is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS131A04 ADC through single-tone sinusoidal signal FFT analysis using the *7-term Blackman-Harris* window setting.

Figure 7-4. Spectral Analysis Tool

The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The *7-Term Blackman Harris* window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

7.5 Histogram Tool

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a DC input applied to a given channel.

As shown in Figure 7-5, the histogram corresponding to a DC input is displayed on clicking the *Capture* button.

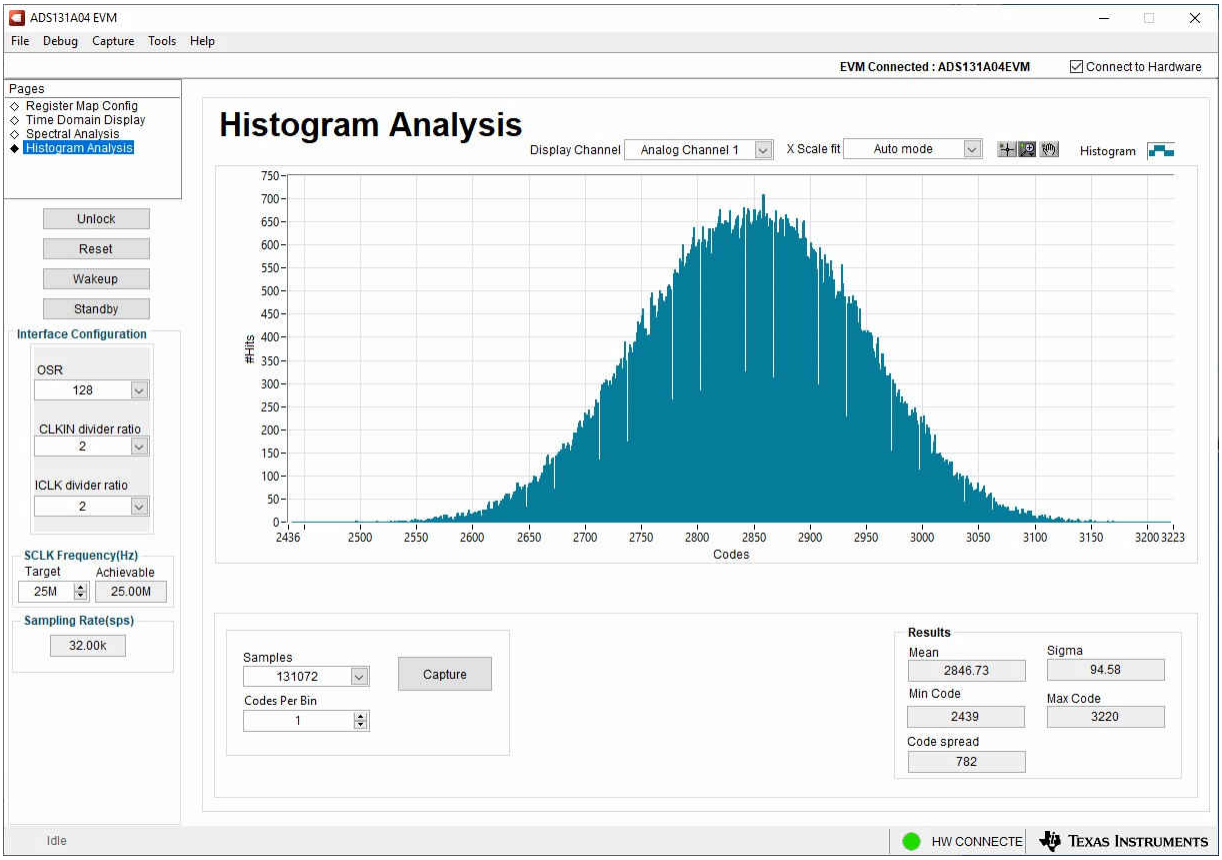

Figure 7-5. Histogram Analysis Tool

8 ADS131A04EVM Bill of Materials, PCB Layout, and Schematic

8.1 Bill of Materials

Table 8-1 lists the ADS131A04EVM bill of materials.

Table 8-1. ADS131A04EVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C1, C12, C18, C19, C20, C24, C25, C26, C29, C31, C32, C35, C36, C38, C41, C57, C100	17	1 µF	CAP, CERM, 1 µF, 25 V, ± 10%, X7R, 0603	603	06033C105KAT2A	AVX
C2, C3, C4, C5, C6, C7, C15, C16	8	100 pF	CAP, CERM, 100 pF, 50 V, ± 5%, C0G/NP0, 0603	603	885012006057.00	Wurth Elektronik
C8, C9, C10, C14	4	4700 pF	CAP, CERM, 4700 pF, 100 V, ± 5%, C0G/NP0, 0603	603	C0603C472J1GAC7867	Kemet
C11	1	1000 pF	CAP, CERM, 1000 pF, 100 V, ± 5%, X7R, 0603	603	06031C102JAT2A	AVX
C13	1	10 µF	CAP, CERM, 10 µF, 25 V, ± 20%, X5R, 0603	603	GRM188R61E106MA73D	MuRata
C21, C22, C23, C28, C33, C34, C45, C46, C49, C56	10	0.01 µF	CAP, CERM, 0.01 µF, 100 V, ± 10%, X7R, 0603	603	06031C103KAT2A	AVX
C27, C39, C53, C54	4	0.1 µF	CAP, CERM, 0.1 µF, 25 V, +/- 5%, X7R, 0603	603	06033C104JAT2A	AVX
C30	1	10 µF	CAP, CERM, 10 µF, 10 V, ± 10%, X7R, 0805	805	885012207026.00	Wurth Elektronik
C40	1	0.27µuF	CAP, CERM, 0.27 µF, 16 V, ± 10%, X7R, 0603	603	C0603C274K4RACTU	Kemet
C42, C43	2	30 pF	CAP, CERM, 30 pF, 50 V, ± 5%, C0G/NP0, 0603	603	GRM1885C1H300JA01D	MuRata
C44, C47, C48, C51	4	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ± 10%, X7R, AEC-Q200 Grade 1, 0603	603	C0603C104K5RACAUTO	Kemet
C50	1	2.2 µF	CAP, CERM, 2.2 µF, 16 V,+/- 10%, X7R, 0603	603	CC0603KRX7R7BB225	Yageo America
C52, C55	2	10 µF	CAP, CERM, 10 µF, 25 V, ± 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
D1	1	Yellow	LED, Yellow, SMD	LED, 1.3x0.65x0.8mm	LY L29K-J1K2-26-Z	OSRAM
H1, H2	2		ROUND STANDOFF M3 STEEL 5 MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
H3, H4, H5, H6	4		Bumpon, Cylindrical, 0.312 X 0.200, Black	Black Bumpon	SJ61A1	3M

Table 8-1. ADS131A04EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
H9	1		Cable, USB-A to micro USB-B, 1 m		102-1092-BL-00100	CnC Tech
J1, J2, J3, J4	4		Terminal Block, 3.5 mm Pitch, 3x1, TH	10.5x8.2x6.5mm	ED555/3DS	On-Shore Technology
J5	1		Header(Shrouded), 19.7 mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
J7	1		Header, 100 mil, 10x2, Gold, TH	10x2 Header	TSW-110-07-G-D	Samtec
J9, J10	2		SMA Straight Jack, Gold, 50 Ω, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF
JP1, JP2, JP4	3		Header, 100 mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
JP3	1		Header, 100 mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
Q1	1	-20V	MOSFET, P-CH, -20 V, -0.39 A, SOT-323	SOT-323	BSS223PWH6327	Infineon Technologies
R1, R2, R3, R4, R5, R6, R7, R8	8	100	RES, 100, 1%, 0.1 W, 0603	603	RC0603FR-07100RL	Yageo
R9	1	1	RES, 1.00, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06031R00FKEA	Vishay-Dale
R10, R17	2	100	RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW0603100RFKEA	Vishay-Dale
R11, R12	2	100k	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW0603100KJNEA	Vishay-Dale
R13	1	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW0603100KFKEA	Vishay-Dale
R14	1	66.5k	RES, 66.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060366K5FKEA	Vishay-Dale
R15	1	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060310K0FKEA	Vishay-Dale
R16, R20, R29, R30, R31, R100, R101	7	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	ERJ-3GEY0R00V	Panasonic
R18	1	681	RES, 681, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW0603681RFKEA	Vishay-Dale
R19	1	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060310K0JNEA	Vishay-Dale
SH-J1, SH-J2, SH-J3	3	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP6, TP7	4		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000.00	Keystone

Table 8-1. ADS131A04EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
TP3, TP4, TP5	3		Terminal, Turret, TH, Double	Keystone1573-2	1573-2	Keystone
U1	1		3 µVpp/V Noise, 3 ppm/°C Drift Precision Series Voltage Reference, DGK0008A (VSSOP-8)	DGK0008A	REF5025IDGKT	Texas Instruments
U2	1		150 mA, High PSRR, Low Quiescent Current, Low Noise LDO, DCK0005A (SOT-SC70-5)	DCK0005A	TPS71733DCKR	Texas Instruments
U3	1		24-Bit, 128 kSPS, 4-Ch, Simultaneous-Sampling Delta-Sigma ADC, PBS0032A (TQFP-32)	PBS0032A	ADS131A04IPBSR	Texas Instruments
U4	1		150 mA, High PSRR, Low Quiescent Current, Low Noise LDO, DCK0005A (SOT-SC70-5)	DCK0005A	TPS71725DCKR	Texas Instruments
U5	1		-1.8 to -5.25 V, Inverting Charge Pump Regulator, 60 mA, 1.8 to 5.25 V Input with 2-Cell Alkaline / Nixx Input, -40 to 85 °C, 5-pin SOT23 (DBV5), Green (RoHS and no Sb/Br)	DBV0005A	TPS60403DBVR	Texas Instruments
U6	1		Single Output High PSRR LDO, 200 mA, Fixed -2.5 V Output, -10 to -2.7 V Input, 5-pin SOT-23 (DBV), -40 to 125 °C, Green (RoHS & no Sb/Br)	DBV0005A	TPS72325DBVT	Texas Instruments
U7	1		0.9 V to 6.5 V, Nano-Power Comparator, DCK0005A (SOT-SC70-5)	DCK0005A	TLV3691IDCKR	Texas Instruments
U8	1		Dual In / Single Out Autoswitching Power Mux, 2.8 to 5.5 V, -40 to 85 °C, 8-pin SON (DRB), Green (RoHS and no Sb/Br)	DRB0008B	TPS2115ADRBR	Texas Instruments
U9	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	RΩ

Table 8-1. ADS131A04EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
Y1	1		Crystal, 16.384 MHz, 20 pF, SMD	SMD, 4-Leads, Body 7.2x5.2mm	407F35E016M3840	CTS Electrocomponents
C17	0	10 µF	CAP, CERM, 10 µF, 25 V, ± 10%, X7R, 0805	805	GRM21BZ71E106KE15L	MuRata
C37	0	1 µF	CAP, CERM, 1 µF, 25 V, ± 10%, X7R, 0603	603	06033C105KAT2A	AVX
J6, J8	0		Receptacle, 2.54 mm, 10x2, Gold, SMT	Receptacle, 2.54mm, 10x2, SMT	NPPC102KFMS-RC	Sullins Connector Solutions
R21, R22, R23, R32, R33, R34	0	499	RES, 499, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW0603499RFKEA	Vishay-Dale

8.2 PCB Layout

Figure 8-1 through Figure 8-6 illustrate the ADS131A04EVM PCB layout.

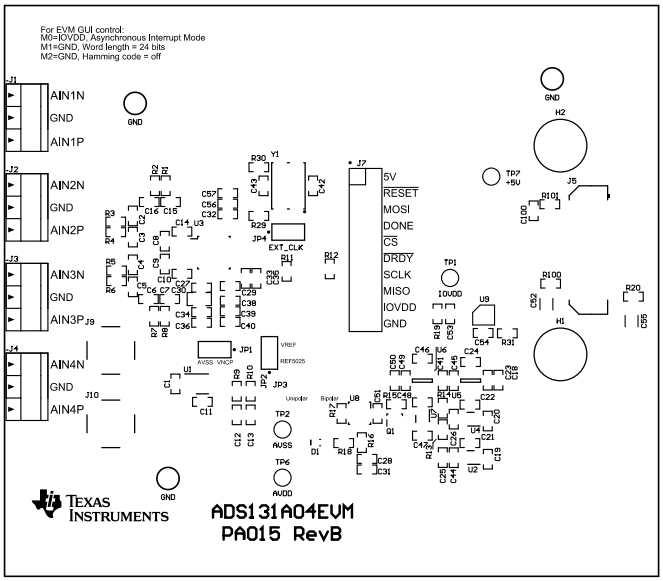

Figure 8-1. Top Silkscreen

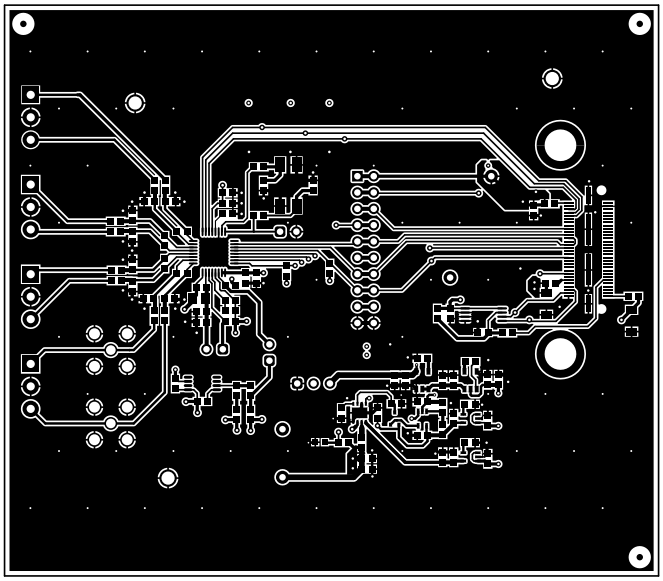

Figure 8-2. Top Layer

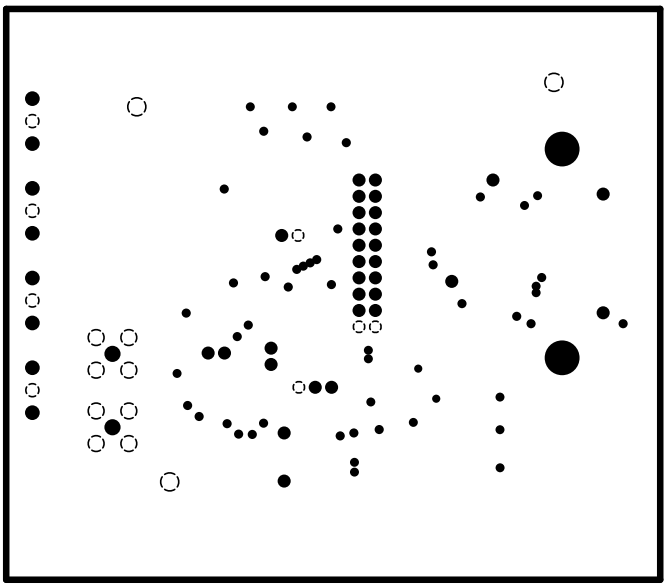

Figure 8-3. Ground Layer 1

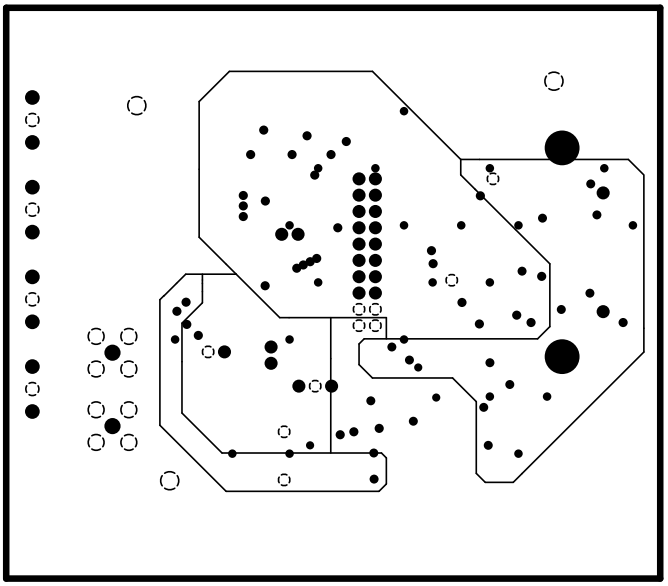

Figure 8-4. Power Layer

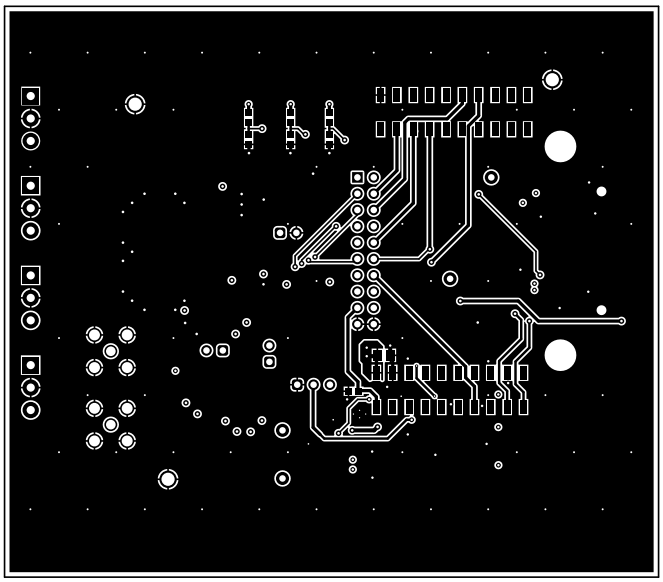

Figure 8-5. Bottom Layer

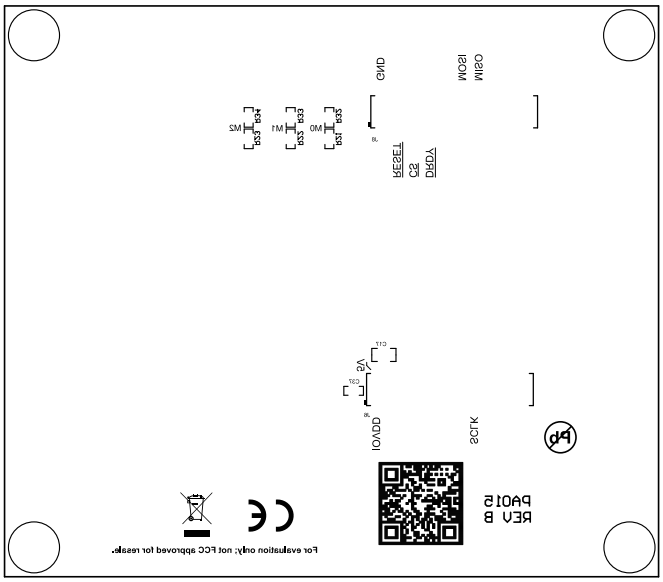

Figure 8-6. Bottom Silkscreen

8.3 Schematic

Figure 8-7 illustrate the ADS131A04EVM schematics.

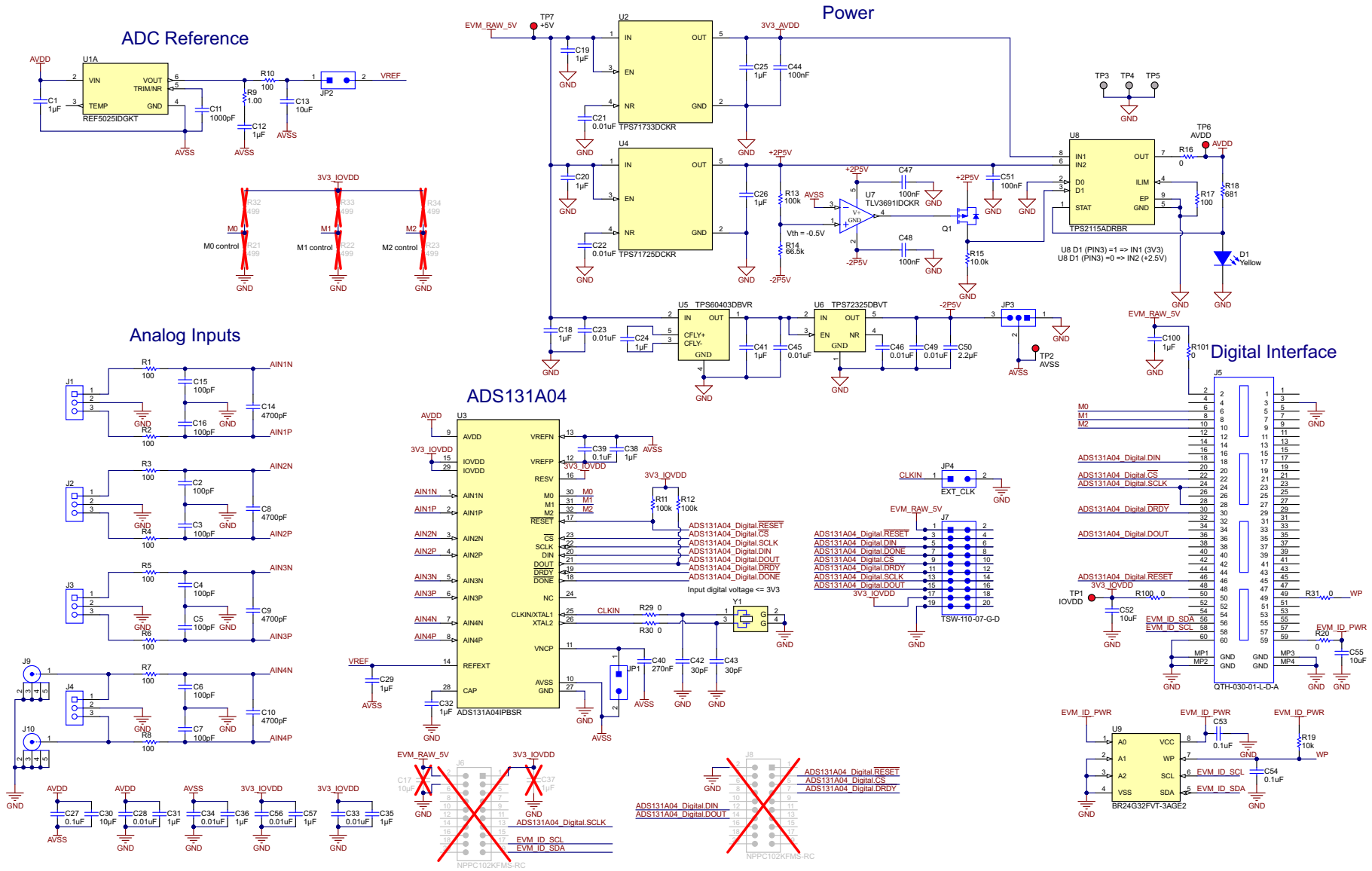

Figure 8-7. ADS131A04EVM Main Schematic

9 References

- *ADS131A04 4-Channel, Simultaneously-Sampling, 24-Bit, Delta-Sigma ADC Data Sheet*
- *ADS131A0x 2- or 4-Channel, 24-Bit, 128-kSPS, Simultaneous-Sampling, Delta-Sigma ADC Data Sheet*

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