Application Brief

Powering the Infineon TRAVEO™ T2G (CYT4DN) 1.15 V Core Rail with Pre-Bias Soft Start Using TPS62850x-Q1

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Introduction

The Infineon TRAVEO™ T2G family (for example, CYT4DN) is a high-performance automotive microcontroller targeting body control, instrument cluster, and gateway applications. Like most modern automotive SoCs, the CYT4DN integrates an internal LDO regulator to supply the 1.15V core rail during initial power-up. However, this internal LDO is thermally limited and cannot sustain the full current demand required during high-performance graphic operation modes.

To support the higher current operation, an external DC/DC buck converter is used in parallel to take over from the internal LDO. This handover creates a critical power sequencing challenge: when the external DC/DC converter is enabled, the 1.15V core rail is already at a pre-biased voltage charged by the internal LDO. A conventional synchronous buck converter with an active output discharge function tries to pull this pre-biased output voltage down before ramping up, inadvertently sinking current from that rail and potentially causing an unintended MCU reset.

Preventing this behavior by using a DC/DC converter with a pre-bias soft start capability, one that begins an output ramp only from the existing pre-bias level, without drawing reverse current from the output. Importantly, do not use any external discrete components such as a series diode, which introduces a voltage drop and power loss unacceptable in a tightly regulated 1.15V rail.

Pre-bias Soft-Start Operation

Figure 1 shows the TPS628502F0QDRLRQ1 power-on sequence when starting into a pre-biased VOUT condition.

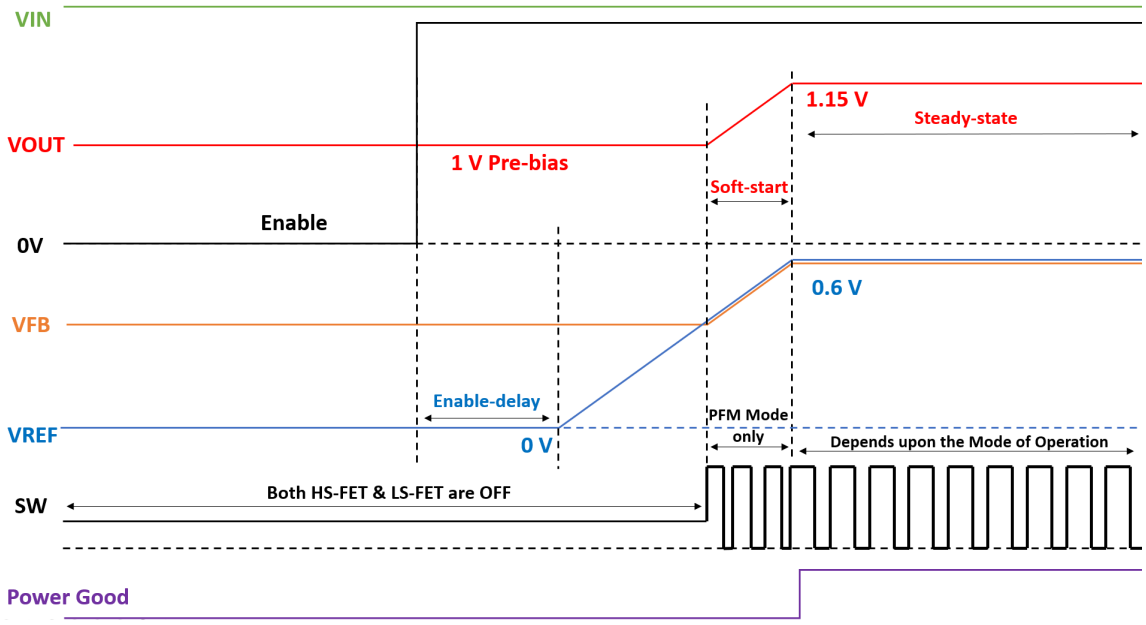

Figure 1. Start-Up Power-On Sequence with Pre-biased VOUT Condition

VIN Must Be Present Before Pre-bias Exists:

A fundamental precondition for safe pre-bias operation is that VIN must always be present whenever a pre-bias voltage exists on VOUT. This is reflected in Figure 1, where VIN is remaining high throughout the entire sequence, well before Enable is high. The reason is structural: the high-side FET of the buck converter has an inherent body diode connected between SW and VIN. If VIN is absent while VOUT is still pre-biased, this pre-bias voltage can forward-bias the HS-FET body diode, causing current to flow from VOUT back into VIN. This uncontrolled current path can exceed the body diode's safe operating current and permanently damage the HS-FET. Therefore, VIN must be established and maintained before, during, and after the pre-bias condition exists on VOUT.

Enable-Delay:

When Enable goes high, the device does not begin switching immediately. Figure 1 shows an enable-delay period between the enable rising edge and the start of the VREF ramp. This delay allows the internal circuitry — bias generators, bandgap reference, or control logic — to power up and stabilize before the converter tries to regulate. The enable-delay duration is a specified parameter listed in the TI's datasheet.

VREF Ramp and the Role of VFB Under Pre-bias:

Once the enable-delay completes, the internal reference voltage (VREF) begins ramping from 0V toward the final value of 0.6V. The rate of this ramp is set by the internal soft-start time, which is also a specified datasheet parameter. Meanwhile, VFB is not at 0V. VFB sits at a non-zero voltage determined by the feedback divider sensing the pre-biased VOUT (approximately 1V). Since VOUT is already elevated by the internal LDO, VFB reflects that pre-bias level from the very start, and it holds steady at this voltage while VREF ramps up from 0V. The device remains in a non-switching state (both HS-FET and LS-FET off, as shown on the SW waveform) throughout this period, because the control loop only begins driving switching action once VREF rises to meet the VFB level set by the pre-bias. Until that crossing point, the converter has no reason to switch, VOUT is already above the reference target, so switching is unnecessary.

PFM-Only Operation During Soft-Start:

Once VREF ramps up and reaches the VFB level, the device begins switching, and from this point on, VFB tracks VREF's continued ramp toward 0.6V, with VOUT correspondingly rising toward 1.15V. Critically, during this entire soft-start window, the converter operates in PFM (Pulse Frequency Modulation) mode regardless of the MODE pin setting (High/Low). In PFM mode, the converter includes zero-current detection circuit. This detection circuit turns off the low-side FET the instant inductor current reaches zero, preventing the inductor current from ever going negative. Since the inductor current cannot reverse, there is no mechanism by which charge can be pulled out of VOUT and sunk back through the converter. The pre-bias voltage is inherently protected by this current-direction constraint, independent of any other discharge circuitry.

Steady-State Mode of Operation:

Once VOUT reaches the 1.15V target and VREF/VFB settle at 0.6V, the soft-start sequence is complete and Power Good asserts. Beyond this point, the MODE pin configuration governs the mode of operation.

MODE Pin	Steady-State Behavior
LOW	PSM (Power Save Mode) — PFM at light load, automatically transitioning to PWM at higher load current
HIGH	FPWM (Forced PWM) — always operates in PWM, regardless of load

This means the PFM-only constraint is specific to the soft-start interval alone; once regulation is achieved, the converter follows whichever mode the MODE pin selects for normal operation.

Device Selection

The TPS62850x-Q1 family offers three output discharge configurations, which directly determine how the converter interacts with a pre-biased output rail:

- **ON**— Active discharge pulls VOUT to ground when the regulator is disabled; sinks current from a pre-biased rail.
- **OFF**— No active discharge; output floats naturally when the regulator is disabled.
- **Disconnected**— No discharge path exists at any time, including during startup and pre-bias conditions, preventing any reverse current path into the pre-biased rail under any circumstance.

For applications like the CYT4DN 1.15V core rail, where the MCU's internal LDO pre-biases the output before the external converter takes over, only disconnected discharge variants are appropriate. Table 1 lists all three OPNs in the TPS62850x-Q1 family with disconnected discharge, spanning 1A and 2A current ratings.

Device	Output Current	VOUT Discharge	Soft Start	Output Voltage
TPS628501F0QDRLRQ1	1A	Disconnected	1ms	Adjustable
TPS628501H9QDRLRQ1	1A	Disconnected	150µs	Fixed 1.15V
TPS628502F0QDRLRQ1	2A	Disconnected	1ms	Adjustable

The disconnected discharge devices offer the most robust protection because no discharge path is ever present, fully eliminating any reverse-current risk during the pre-bias-to-active handoff. Notably, TPS628501H9QDRLRQ1 provides a fixed 1.15V output with disconnected discharge and a fast 150µs soft-start, closely matching the CYT4DN core-rail voltage without needing external feedback resistors, making the device a strong option when 1A output current is sufficient. Select the OPN based on the specific current, voltage, and soft-start requirements. For this application note, TPS628502F0QDRLRQ1 (2A, adjustable, Disconnected discharge, 1ms soft-start) is used as the working example for the bench-measurement section because this device has higher graphics-mode current demand.

Bench Measurements

To validate the pre-bias soft-start behavior described in above section, TPS628502-Q1 was bench-tested with the output forced to a pre-bias condition before enable, emulating the pre-biased rail left behind by the CYT4DN's internal LDO.

Table 1. Test Conditions

Parameter	Value
VIN	6V
VOUT (forced pre-bias)	0.766V
VOUT (target)	1.8V
IOUT	0A
MODE	Low (PSM)
Temperature	25°C

Note

The 1.8V target used here is for bench validation of the pre-bias soft-start mechanism only; the same behavior applies directly to the CYT4DN 1.15V core rail application.

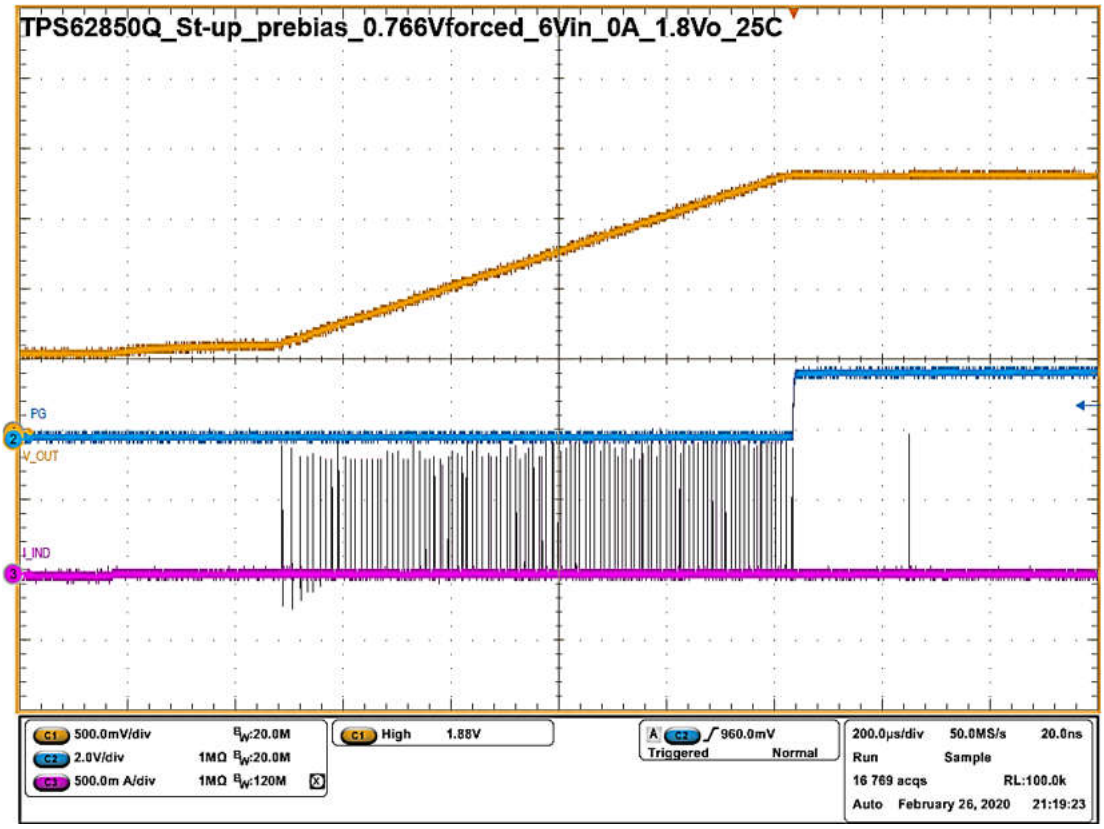

Figure 2. VOUT, PG, and Inductor Current During Pre-bias Startup

- **VOUT**ramps smoothly and monotonically from the forced pre-bias level (0.766V) up to the 1.8V target, with no dip, glitch, or discontinuity at the point where the internal soft-start ramp catches up to the pre-bias voltage.
- **Inductor current (I_IND)** shows discrete PFM switching pulses throughout the ramp, with no negative excursions at any point, confirming the zero-current detection behavior and validating that no reverse current is drawn from the pre-biased rail.
- **Power Good (PG)**remains low throughout the ramp and asserts high only once VOUT reaches the regulation target, confirming clean transition into steady-state operation.

This measurement confirms that the PFM-only soft-start and disconnected discharge function of TPS628502-Q1 prevent any reverse current path during the pre-bias-to-active handoff — directly addressing the reset risk described in the Introduction for the CYT4DN 1.15V core rail transition.

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