Application Brief

Enabling Compact Ground-Level Translation for Phased Array Satellites

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Introduction

Aerospace and defense systems have historically driven many communication innovations, including radar, GPS, and satellite links. As demand for higher bandwidth and more reliable connectivity grows, traditional mechanically steered antennas are increasingly being replaced by phased-array antennas. Unlike conventional antennas that physically rotate to steer signals, phased-array systems electronically adjust the phase of each antenna element to rapidly direct communication beams and support multiple users simultaneously.

However, modern phased-array satellites can contain hundreds or even thousands of transmit and receive paths as shown in Figure 1. Each path may include a power amplifier (PA), low-noise amplifier (LNA), phase shifter, and associated control circuitry as shown in Figure 2. This architecture dramatically improves beam steering and communication capacity, but it increases the number of required control and status signals. These control and status signals often must operate across different voltage domains

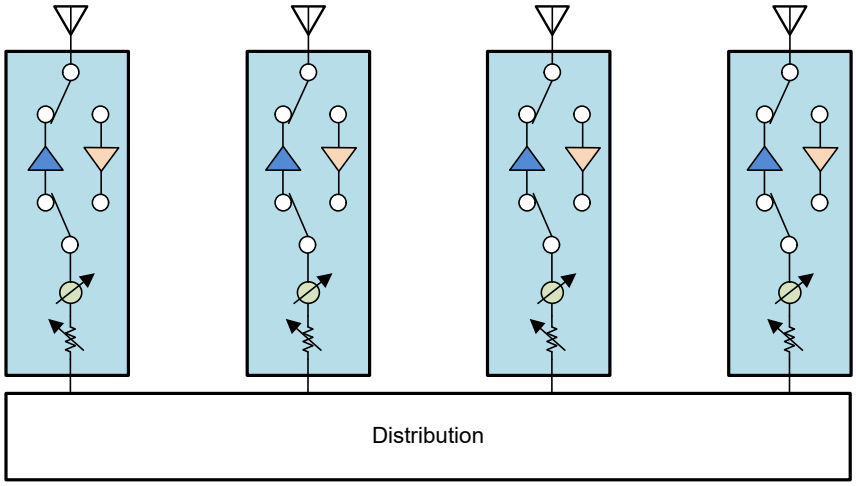

Figure 1. Antennas in an Array

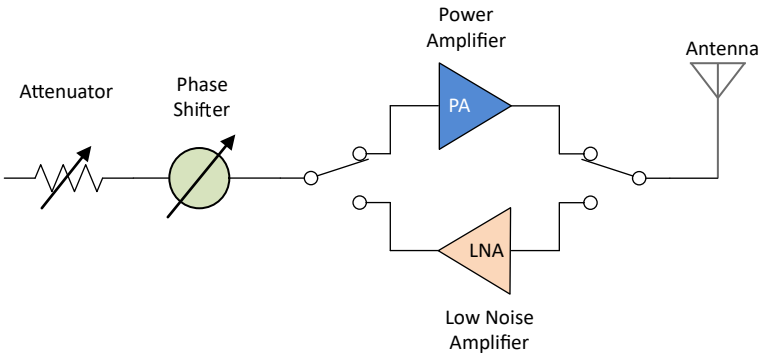

Figure 2. Phased Array Antenna

Single Supply vs Dual-Supply Power Amplifiers

One of the key benefits of power amplifiers is their ability to provide high levels of amplification with minimal output distortion. To maximize signal swing and dynamic range, phased-array systems often operate amplifiers in a dual-supply configuration, as shown in Figure 3. While enabling a power amplifier in a single-supply configuration only requires the EN voltage to exceed the minimum input high voltage (V_{IH}) referenced to ground, a dual-supply configuration shifts the EN reference from GND to V_{EE}.

For example, if an amplifier in a single-supply configuration requires >1.26V to enable and <0.54V to disable, then in a dual-supply configuration these threshold voltages are shifted by V_{EE}. Assuming −5V is used for V_{EE}, the new enable voltage becomes −3.74V and disable voltage becomes −4.46V.

This creates a challenge for modern MCUs and FPGAs, which typically cannot generate or tolerate negative voltages.

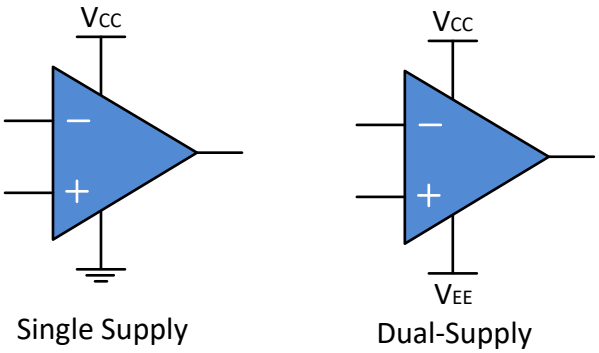

Figure 3. Operational Amplifier Single and Dual Supply Configuration

Navigating Negative Control Signals and Space Constraint

To overcome these challenges, engineers often resort to discrete based designs. Figure 4 shows a common discrete implementation used to translate a positive MCU control signal into the negative voltage domain required by a dual-supply amplifier.

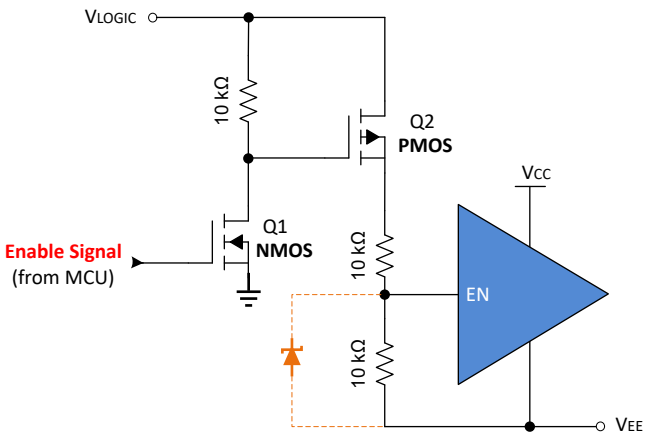

Figure 4. Enable Discrete Level-Shifting

In addition to enable pins, many amplifiers provide an alert or status output to indicate fault conditions such as over-current or over-temperature events. These outputs are typically implemented as open-drain signals that require a pull-up resistor. In single-supply systems, a fault condition pulls the alert signal low relative to ground. However, when the amplifier operates from a dual-supply rail, the alert signal becomes referenced to V_{EE} instead of ground. As a result, a fault condition can drive the alert signal to a negative voltage, which many MCUs and FPGAs cannot tolerate directly.

Figure 5 shows a common discrete implementation used to translate a negative alert signal to a positive MCU interrupt signal.

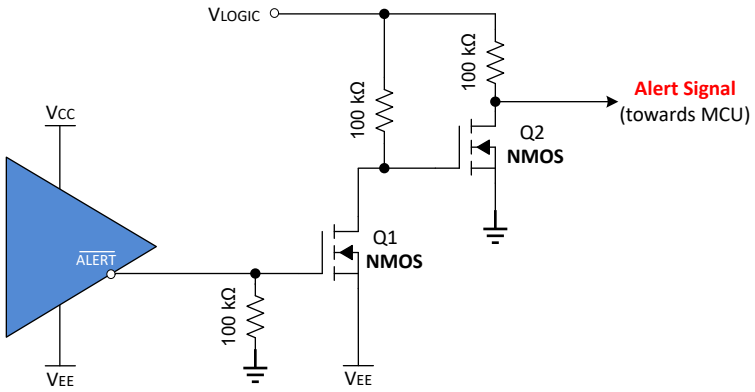

Figure 5. Alert Discrete Level-Shifting

Both enable and alert flag discrete solutions are a good way to generate or tolerate negative signals that occur from dual-supply rails. However, in a phased-array satellite containing hundreds of channels, this can translate into thousands of additional components and significant PCB area. Table 1 shows the total discrete components needed for each power amplifier pair.

Table 1. Discrete Components per PA Pair

Design	Components per Channel
Discrete Enable Translation	2 FETs + 3 resistors
Discrete Alert Translation	2 FETs + 3 resistors
Total	10+ components for one PA pair

Why Not Use Digital Isolators?

Integrated solutions such as digital isolators can address negative signals from dual-supply rails. These devices provide signal transfer across a galvanic isolation barrier, which is beneficial in safety-critical or high-voltage applications. In phased-array satellites, many communication challenges originate from ground offsets rather than safety isolation requirements. The addition of a galvanic isolation barrier also decreases timing performance (propagation delay, channel-to-channel skew, data rate) while increasing system cost and solution size.

When galvanic isolation is unnecessary, a ground-level translator provides a simpler and more efficient solution.

Using TI's TXG to Solve Ground-Level Challenges

Texas Instruments addresses these challenges with the TXG family of ground-level translators. Unlike conventional level translators, TXG devices are specifically designed to communicate between voltage domains that operate at different ground potentials. TXG devices eliminate the need for additional discrete components while providing robust signal translation, integrated ESD protection, and improved switching performance by integrating dual-ground architecture into a compact IC.

For example, replacing the enable discrete design in Figure 6 with a TXG device, the solution is simplified, as shown in Figure 6. By connecting TXG's VCCB pin to system ground and GNDB pin to V_{EE}, the output voltage on side B will swing from V_{EE} to GND. This configuration is only tolerant to V_{CC} and GND differences up to 6.5V.

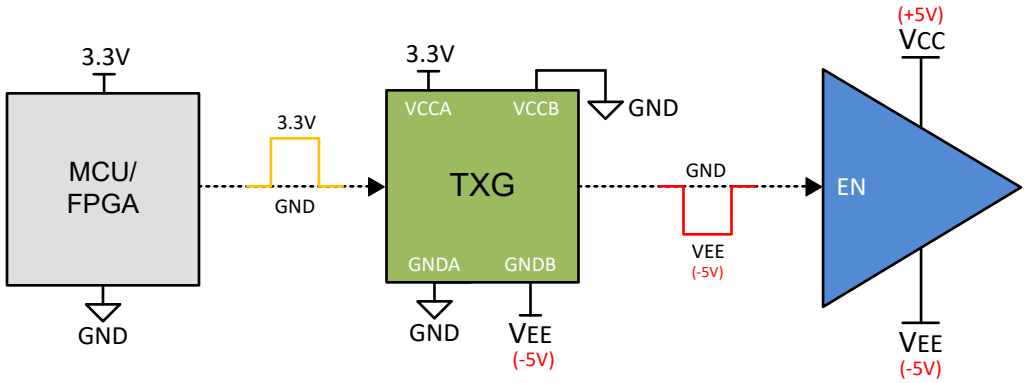

Figure 6. TXG Implementation

Although discrete circuits and digital isolators can be used to communicate across ground offsets, each approach introduces compromises in system size, cost, performance, or complexity. These tradeoffs become increasingly important as phased-array systems continue to increase channel count. Table 2 compares the most common approaches used to address negative-voltage signaling challenges.

Table 2. Comparison of Ground-Offset Communication Solutions

Feature	Discrete Circuit	Digital Isolator	TXG
Ground Offset Support	Yes	Yes	Yes
Galvanic Isolation	No	Yes	No
Component / Routing Overhead	High (10+ parts per channel)	Low	Low
PCB Area	Large	Medium	Small
Cost	Low	High	Low
Propagation Delay / Timing	Slow / RC Limited	Moderate	Fast / Low Skew
Scalability	Poor	Moderate	Excellent

Conclusion

Phased-array satellites continue to increase channel count and communication bandwidth, placing greater demands on system density and scalability. While dual-supply RF amplifiers improve signal performance, they introduce control and status signals that operate in different ground domains. Traditional discrete translation circuits solve this challenge but increase component count, board area, and design complexity. TI's TXG family of ground-level translators provides a compact and scalable alternative that simplifies implementation while maintaining high-performance communication between ground-referenced and negative-voltage domains.

Additional Resources

- Texas Instruments, *Top Design Questions about Ground-Level Translators*, application brief.
- Texas Instruments, *Not All Grounds Are 0V*, application brief.
- Texas Instruments, *Uneven grounds? Address offset challenges with novel ground-level translators*, technical article.

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