Application Note

How to Select Compensation Setting in TPS62A2xx-Q1

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ABSTRACT

This application note presents a comprehensive methodology for optimizing load-transient response and selecting compensation settings in TI's TPS62A2xx-Q1 automotive buck-converter family. It begins with a brief overview of the two transient-response phases. The passive phase is capacitor-dominated, while the active phase is controlled by the loop. Next, it identifies the parameters that affect overshoot, undershoot, and recovery time. A step-by-step design procedure guides the designer through target crossover-frequency selection, calculation of the minimum output-capacitor value for both in-regulation and loop-saturation criteria, and the integration of Transient non-synchronous Mode (TAM). The note concludes with practical recommendations for achieving fast, low-overshoot transient response while minimizing bill-of-materials, making it a ready-to-use reference for power-design engineers developing automotive buck-converter designs with TPS62A2xx-Q1 family

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1 Introduction

1.1 Load Transient Response Fundamentals

In any power supply design, the output voltage is expected to remain stable and within a specified tolerance regardless of how the load current changes. However, in real-world applications, such as automotive microcontrollers, SoCs, or DSPs, the load current can switch between light and heavy demands within microseconds or even nanoseconds. The converter's ability to maintain a regulated output voltage during these sudden changes is what we refer to as load transient response.

When the load current suddenly increases, the output voltage experiences a momentary undershoot, a dip below the regulated value. Conversely, when the load current suddenly decreases, the output voltage spikes above the regulated value, known as overshoot. The converter's control loop detects this deviation and corrects the duty cycle to restore the output voltage back to regulation. The time it takes to return within a specified tolerance band is called the settling time. These three quantities, undershoot, overshoot (ΔV) and settling time (t_s) are the primary metrics used to evaluate the quality of a converter's transient response. A well-designed converter minimizes both the peak voltage deviation and the time it takes to recover, verifying the downstream load always operates within its safe voltage range. A useful way to visualize this is through a typical transient response waveform, shown in Figure 1-1.

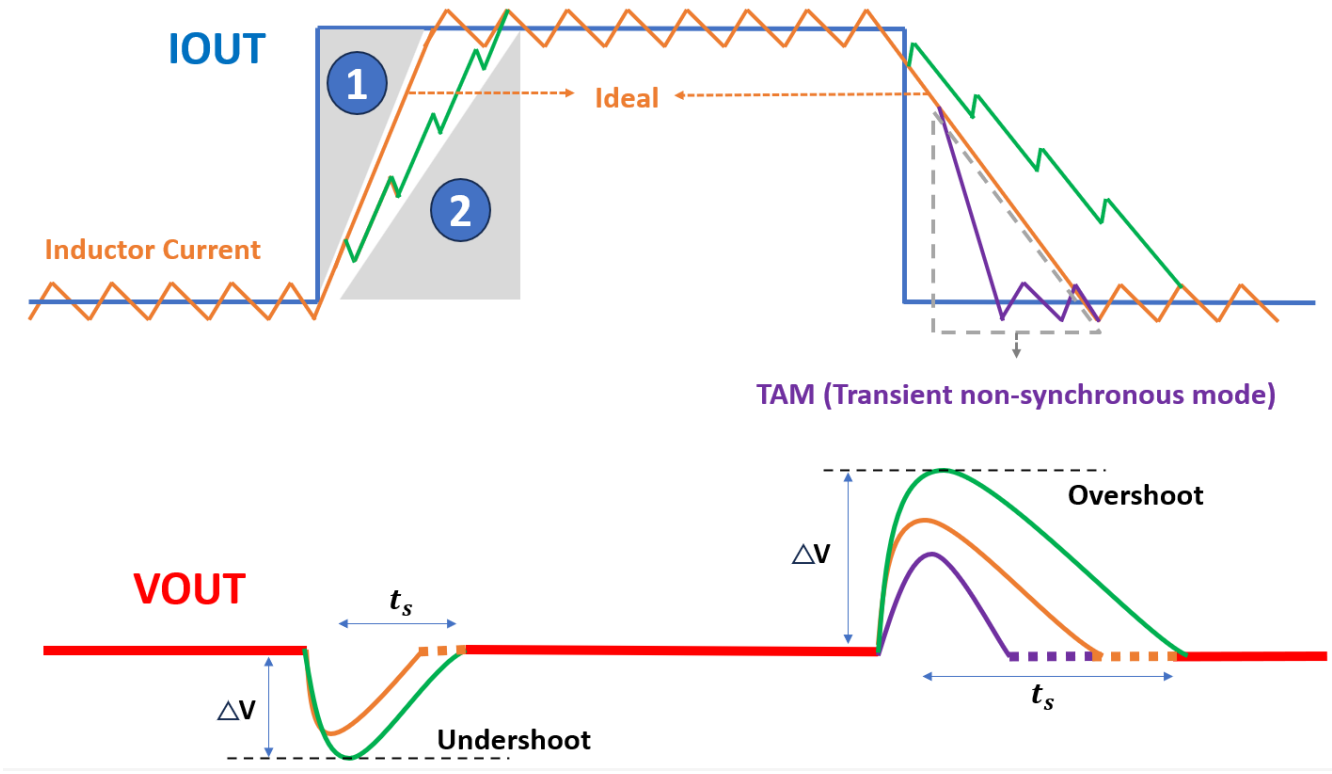


Figure 1-1. Load Transient Response

As shown in Figure 1-1, the transient response unfolds in two distinct phases, each governed by different elements of the power supply design:

1.1.1 Phase 1: Passive Response (Capacitor Dominated)

Before the control loop reacts, the output capacitor alone is responsible for supplying or absorbing the sudden change in load current. During this phase, the initial peak voltage deviation (ΔV) is determined entirely by the output capacitor's value and its parasitic impedances, primarily the equivalent series resistance (ESR) and equivalent series inductance (ESL). A larger output capacitance with lower parasitics will limit the initial voltage deviation, buying time for the control loop to respond.

1.1.2 Phase 2: Active Response (Control Loop)

Once the control loop detects the output voltage deviation, it adjusts the duty cycle and ramps the inductor current to meet the new load demand, gradually restoring the output voltage to its regulated value. The speed and smoothness of this recovery are determined by the control loop bandwidth and its compensation settings. A wider bandwidth allows the loop to react faster, reducing settling time. However, the loop must also be properly compensated to avoid excessive ringing or instability during recovery.

Understanding these two phases is the foundation for analyzing which parameters influence transient response , and how to optimize the compensation network for the best possible performance.

2 Parameters Affecting Load Transient Response

The load transient response of a buck converter is shaped by two distinct groups of parameters. Those belonging to the external passive components of the output stage, which dominate the initial passive response, and those belonging to the small-signal internal characteristics of the control loop, which govern the active recovery. Understanding each group in depth allows the designer to make targeted, informed decisions rather than relying on trial and error.

2.1 Output Stage Parameters

The output stage comprise the inductor, output capacitor, and its parasitics. These form the converter's first and immediate line of defense during a transient event. Before the control loop has had time to act, these components alone determine the peak voltage deviation seen at the output.

2.1.1 Output Capacitance

Building on the passive response phase discussed in Section 1, the output capacitor must supply or absorb the sudden change in load current during the interval before the inductor current has caught up. The peak voltage deviation during this interval is governed by: $\Delta V \approx \left(\Delta I_{Load} \times \Delta t\right) / C_{OUT}$

2.1.2 ESR and ESL of COUT

Beyond the capacitance value itself, the parasitic impedances of the output capacitor play a critical role — particularly at the moment the transient begins. The ESR introduces an immediate resistive voltage step: $\Delta V_{ESR} \approx \Delta I_{LOAD} \times ESR$

The ESL adds a further inductive spike during fast current transitions: $\Delta V_{ESL} = ESL \times \left(d\Delta I_{LOAD} / dt\right)$

In applications with high load current slew rates, ESL can in fact dominate the initial voltage spike, making capacitor selection about more than just capacitance value. Low-ESR, low-ESL ceramic capacitors (MLCCs) are generally preferred. Where higher bulk capacitance is needed, a combination of MLCCs and bulk capacitors is commonly used, placing the MLCCs physically closest to the load to minimize parasitic inductance in the current path.

2.1.3 Output Inductance

The output inductor determines how quickly the converter can ramp its current once the control loop has begun responding. The inductor current slew rate during the on-time is: $dI_L/dt = (V_{IN} - V_{OUT})/L$

A smaller inductance allows faster current ramping, which shortens the settling time and reduces the duration over which COUT must sustain the load alone. However, reducing L increases the peak-to-peak ripple current, affecting efficiency and potentially EMI performance. Inductance selection therefore involves a deliberate trade-off between transient response speed and steady-state ripple requirements.

2.2 Control Loop Parameters

Once the output stage has absorbed the initial transient, the control loop takes over to restore regulation. The quality of this active recovery is governed by the small-signal characteristics of the loop — specifically how fast it can respond and how stable it remains while doing so. Unlike the passive output stage parameters, these are internal to the control architecture and are shaped by both device-fixed characteristics and designer-controlled compensation settings.

2.2.1 Crossover Frequency, Phase Margin

The crossover frequency (f_c) is the frequency at which the open-loop gain of the system falls to unity (0 dB). It is the most direct indicator of how fast the control loop can respond to a disturbance — a higher f_c means the loop reacts faster, resulting in a shorter settling time and reduced voltage deviation during the active recovery phase.

In TPS62A2xx-Q1, f_c is determined by the product of the error amplifier transconductance (g_M) and the compensation resistor (R_{comp}). Increasing this product raises the mid-frequency loop gain, pushing f_c higher and making the loop respond faster to transient events. However, f_c cannot be increased without limit. As the crossover frequency is pushed higher, the phase margin is reduced. A system with insufficient phase margin will exhibit ringing or oscillatory behavior during transient recovery, which is equally undesirable. A phase margin of 45° is the widely accepted for stable operation, with 60° or above preferred in most practical designs. The selection of the $g_M \times R_{comp}$ product is therefore a deliberate balance:

- Too low → sluggish loop response, large settling time, excessive voltage deviation during active recovery
- Too high → fast response but reduced phase margin, risk of ringing or instability

This balance is precisely what Section 3 addresses — providing a structured approach to selecting the appropriate compensation setting in TPS62A2xx-Q1 for optimized transient performance.

2.2.2 Transient Non-Synchronous Mode

The crossover frequency and phase margin govern the loop's response to a load step-up event — how quickly the loop can detect the undershoot and command additional inductor current to restore regulation. However, the load step-down event introduces a fundamentally different challenge that the small-signal loop alone cannot fully address: overshoot.

During a load step-down event, the inductor current does not immediately drop to the new lower load level. In a conventional synchronous buck converter, the low-side FET remains active, and the inductor current ramps down at a rate governed by: $dI_L/dt = V_{OUT}/L_{OUT}$

This relatively slow ramp-down means excess inductor current continues to flow into COUT after the load has reduced, injecting surplus charge and pushing V_{OUT} above the regulation target — this is the overshoot.

How TAM Works

When the control loop detects a load step-down event, TAM forces the low-side FET off, redirecting the inductor current through the body diode of the low-side FET. The body diode has a forward voltage drop of approximately 0.6 V, which adds to V_{OUT} in opposing the inductor current. The effective voltage driving the inductor current down becomes: $\Delta V_L = V_{OUT} + V_{diode} \approx V_{OUT} + 0.6V$

This increases the inductor current slew rate during the step-down transient: $dI_L/dt = (V_{OUT} + \ \ 0.6)/L_{OUT}$

Impact on Overshoot and Output Capacitance

The faster inductor current slew rate means the inductor current returns to the new load level more quickly, reducing the excess charge injected into COUT. Since overshoot voltage is directly proportional to this excess charge, a faster current slew rate — achieved by TAM — means either a lower overshoot for the same COUT, or equivalently, a smaller COUT can be used to meet the same overshoot specification. This directly reduces the minimum output capacitance requirement during a load step-down event, as reflected in the device-specific design equations discussed in Section 3.

3 Step-by-Step Compensation Selection Procedure

Note

Compensation values are nominal and can vary by ±10%. The COMP pin resistor must be placed close to the pin to minimize parasitic capacitance and must not be left floating.

Step 1 : Define the Application Requirements

Before beginning the calculation, the following application parameters must be established:

Parameter	Symbol	Description
Target output voltage undershoot	ΔV_{OUT}	Maximum allowable voltage dip during a load step
Load step magnitude	I_{step}	The peak load current step
Output inductance	L_{OUT}	Selected inductor value
Output voltage	V_{OUT}	Determines FB_{Ratio} and V_{OUT} Range
Switching frequency	F_{SW}	Set via CONF pin (1.5, 2.25, 2.5, or 4MHz)

Step 2 : Determine FB_{Ratio}

The FB_{Ratio} accounts for the difference in internal feedback scaling across the four output voltage ranges. It is fixed by the V_{OUT} range, which is configured through the CONF pin.

Table 3-1. FB_{Ratio} Values

V_{OUT} Range	V_{OUT}(V)	FB_{Ratio}
Range 1	0.4 – 0.5875	1
Range 2	0.5 and 0.6 – 0.775	1
Range 3	0.8 – 1.55	2
Range 4	1.6 – 3.3	4

Step 3 : Calculate the Target Compensation Value

Use Equation 1to calculate the recommended (g_M × R_c):

- $$g_M \times Rc \left(\frac{V}{V}\right) = 78571.43 \times \left(\frac{I_{step}}{\Delta V_{out}}\right) \times FB_{Ratio} \times L_{out} \quad (1)$$

Where:

- Δ V_{OUT}= Target V_{OUT} undershoot (V)
- I_{step} = Load step (A)
- L_{OUT} = Output inductance (H)
- FB_{Ratio} = From Table 1 above

Step 4 : Select the Compensation Setting

From the given table, select the COMP setting whose g_M × R_c value most closely matches the calculated result:

Table 3-2. Compensation Setting

Compensation Setting	g_M × R_c
COMP 15	8.5
COMP 14	6.8
COMP 13	5.75
COMP 12	4.6
COMP 11	3.75
COMP 10	3.0
COMP 9	2.5
COMP 8	2.0
COMP 7	1.75

Table 3-2. Compensation Setting (continued)

Compensation Setting	$g_M \times R_c$
COMP 6	1.4
COMP 5	1.125
COMP 4	0.9
COMP 3	0.75
COMP 2	0.6
COMP 1	0.5
COMP 0	0.4

If the calculated value falls between two settings, choosing the higher setting provides more loop gain and tighter transient regulation. Selecting the lower setting reduces the risk of instability when output capacitance is at its minimum due to derating.

Step 5 : Set the COMP Pin Resistor

Configure the COMP pin using the corresponding resistor from given table, placed between the COMP pin and GND using E96 series values:

Table 3-3. Configuration Options for TPS62A2xx-Q1 through the COMP Pin

COMP Pin Configuration	Compensation Setting
Connected to V_IN	`COMP 15
100kΩ to GND	COMP 14
33.2kΩ to GND	COMP 13
16.9kΩ to GND	COMP 12
10kΩ to GND	COMP 11
6.3kΩ to GND	COMP 10
4.2kΩ to GND	COMP 9
2.8kΩ to GND	COMP 8
1.9kΩ to GND	COMP 7
1.3 kΩ to GND	COMP 6
887Ω to GND	COMP 5
576Ω to GND	COMP 4
365Ω to GND	COMP 3
210Ω to GND	COMP 2
100Ω to GND	COMP 1
Connected to GND	COMP 0

Important: The COMP resistor is read during device startup. Changing the resistor value during operation has no effect. In fixed-OTP devices, connect the COMP pin to AGND.

Step 6 : Verify Loop Bandwidth and Minimum Output Capacitance

The transient response of the converter depends on which operating region the control loop is in:

- In regulation: response is determined by the loop bandwidth
- Loop saturated: response is limited by the maximum inductor current slew rate

TI recommends calculating the minimum output capacitance for both criteria and selecting the larger value.

6a : Loop Bandwidth Constraint

The loop bandwidth must satisfy the following under all operating conditions, including all applicable derating factors:

$$100\text{kHz} \le \text{BW} \le \text{Minimum}\left(600\text{kHz}, \frac{f_{sw}}{5}\right) \quad (2)$$

6b : Minimum Capacitance: In-Regulation Criterion

If the converter remains in regulation, the minimum output capacitance required is:

$$C_{out(min)(reg)} = 1.59 \times 10^{-6} \times \frac{g_M \times Rc}{L_{out} \times BW \times FB\_Ratio} \quad (3)$$

6c : Minimum Capacitance: Loop Saturation with TAM Disabled

TPS62A2xx-Q1 family employs a Frequency-Regulated Constant On-Time (F-COT) control architecture, which maintains a nearly constant switching frequency while preserving the fast transient response characteristic of COT control. The control loop is configured through a single external resistor on the COMP pin, selecting one of 16 discrete internal compensation settings (COMP 0 through COMP 15). Each setting corresponds to a specific value of the internal compensation product $g_M \times R_c$, ranging from 0.4 to 8.5, which determines the crossover frequency and governs how fast the converter responds to load transients.

The design task reduces to calculating the required $g_M \times R_c$ from the application's transient requirements, selecting the closest available setting, and verifying the minimum output capacitance requirement is met.

When the load step is large enough to saturate the control loop and the TAM feature is disabled, the minimum output capacitance is:

$$C_{out(min)(sat)} = \frac{1}{\Delta V_{out}} \times \left(\left(\frac{I_{pk}^2 \times L_{out}}{2 \times \Delta V_L} \right) + \left(I_{Step} \left[T_{on} - \frac{T_t}{2} \right] \right) \right) \quad (4)$$

Where:

$$I_{pk} = I_{DC} + \frac{I_{L(PP)}}{2} \quad (5)$$

$$I_{L(PP)} = \text{Inductor current ripple} \quad (6)$$

$$\Delta V_L = \text{Voltage across the Inductor} = \text{Minimum} \left(V_{in} - V_{out}, V_{out} \right) \quad (7)$$

$$T_t = \text{Transition time of the Load Step} \quad (8)$$

$$T_{on} = \frac{V_{out}}{\eta \times V_{in}} \times \frac{1}{f_{sw}} \quad (9)$$

6d : Minimum Capacitance: Loop Saturation with TAM Enabled

When the load step saturates the control loop and the TAM feature is enabled, the minimum output capacitance is:

$$C_{out(min)(sat\_TAM)} = \frac{1}{\Delta V_{out}} \times \left(\left(I_{pk} \times (T_{sw} - T_{on}) \right) - \left(\frac{(T_{sw} - T_{on})^2}{2} \times \frac{V_{out}}{L_{out}} \right) + \left(\frac{I_{val}^2 \times L_{out}}{2 \times (V_{out} + 0.6)} \right) + \left(I_{Step} \left[T_{on} - \frac{T_t}{2} \right] \right) \right) \quad (10)$$

Where:

$$T_{sw} = \frac{1}{f_{sw}} \quad (11)$$

$$I_{val} = I_{DC} - \frac{I_{L(PP)}}{2} \quad (12)$$

Note: TAM is available only for V_{OUT} Ranges 1, 2, and 3. It is not available for V_{OUT} Range 4.

6e : Final COUT Selection

Select the minimum output capacitance based on the applicable saturation criterion for your design:

V_{OUT} Range	TAM Status	COUT(min) Selection
Range 1, 2, or 3	TAM Enabled	max(Eq. 4, Eq. 10)
Range 1, 2, or 3	TAM Disabled	max(Eq. 3, Eq. 4)
Range 4	TAM Not Available	max(Eq. 3, Eq. 4)

Always apply appropriate derating to the selected capacitor to account for DC bias voltage coefficient and temperature effects.

4 Selecting Compensation Setting in TPS62A2xx-Q1

Worked Example

The following example is taken directly from the typical application section of the TPS62A212-Q1 datasheet.

Table 4-1. Application Parameters

Parameter	Value
Output voltage (V_{OUT})	0.75V (V_{OUT} Range 2)
Input voltage (V_IN)	3.3V
Load step (I_step)	7.9A (0.1 A to 8 A)
Load step rise/fall time (t_r / t_f)	1µs
Target undershoot (ΔV_{OUT})	26.25mV
Output inductance (L_OUT)	100nH
Switching frequency (f_SW)	2.5MHz
Efficiency (η)	90%

Derived Values

- I_{DC} (maximum load current) = 8A
- I_{step}= 7.9A
- FB_{Ratio} (for V_{OUT} Range 2) = 1
- Steps 1–2: V_{OUT} = 0.75V → Range 2; FB_{Ratio} = 1
- Step 3: Calculate $g_M \times R_c$ using (Equation 13):
  - $$g_M \times Rc\left(\frac{V}{V}\right) = 78571.43 \times \left(\frac{7.9}{26.25 \times 10^{-3}}\right) \times 1 \times 100 \times 10^{-9} = 2.36 \quad (13)$$
- Step 4: Select compensation setting:
  - Closest available → COMP 9 ($g_M \times R_c$ = 2.5)
- Step 5: Set COMP pin resistor:
  - COMP 9 → 4.2kΩ to GND
- Step 6a: Verify loop bandwidth:
  - BW_max = f_SW / 5 = 2.5 MHz / 5 = 500kHz (satisfies 100 kHz ≤ BW ≤ 600kHz)
- Step 6b: COUT In-Regulation (Eq. 3):
  - COUT(min)(reg) = 75.04 µF
- Step 6c: COUT Saturation, TAM Disabled (Eq. 4):

  Calculate intermediate values:

  - $I_{L(PP)}$= 2.58A
  - $I_{(pk)}$ = 9.29A
  - ΔV_L= 0.75V
  - T_{on}= 101.01ns

  - COUT(min)(sat) = 99.008µF
- Step 6d: COUT Saturation, TAM Enabled (Eq. 5):

  Calculate intermediate values:

  - T_{sw}= 400ns
  - I_{val}= 6.71A
  - COUT(min)(sat_TAM) = 36.508µF
- Step 6e: Final COUT Selection:

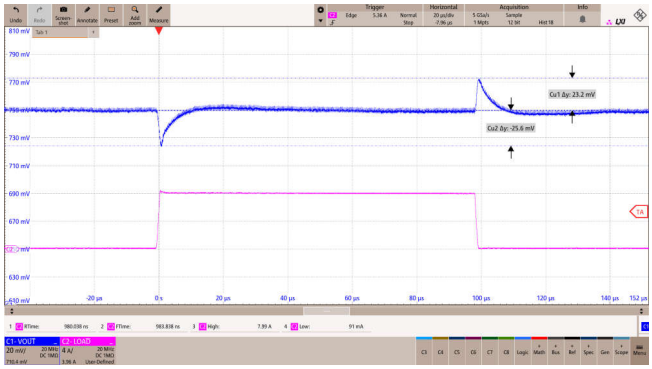
Criterion	COUT (min)
In-regulation (Eq. 15)	75.04 µF
Saturation, TAM disabled (Eq. 18)	99.008 µF ← larger, governs if TAM off
Saturation, TAM enabled (Eq. 25)	36.508 µF
Final with TAM disabled	99.008 µF
Final with TAM enabled	max(75.04, 36.508) = 75.04 µF

Enabling TAM reduces the required output capacitance from approximately 99µF to approximately 75µF in this example: a meaningful reduction that enables a more compact design.

Lab Optimization Results

Based on laboratory measurements, COMP 12 (g_M × R_c = 4.6) with 4 × 22µF output capacitors (Murata GCM31CR71A226KE02L) delivered optimized load transient performance. This illustrates an important principle: the equation-based calculation provides a well-grounded starting point, but real-world capacitor derating, PCB parasitic inductance, and PDN impedance effects mean the optimum compensation setting is best confirmed through lab validation or simulation using the actual board's PDN model and the selected capacitor stack-up.

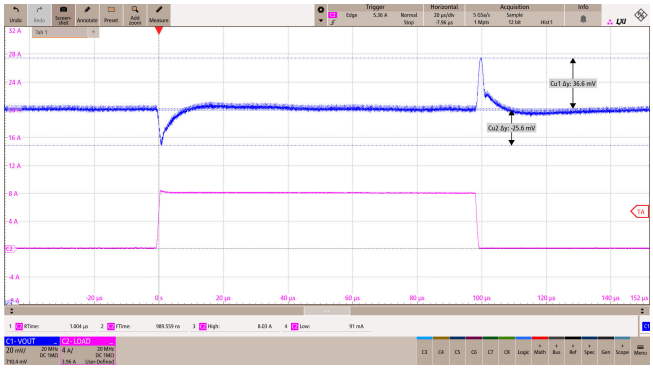
Bench Measurements



V_{OUT} = 0.75V PWM, COMP = 12, TAM enabled T_A = 25°C

V_{IN} = 3.3V I_{OUT} = 0.1A to 8A to 0.1A in 1µs

Figure 4-1. Load Transient Response



V_{OUT} = 0.75V PWM, COMP = 12, TAM disabled T_A = 25°C

V_{IN} = 3.3V I_{OUT} = 0.1A to 8A to 0.1A in 1µs

Figure 4-2. Load Transient Response

5 Summary

Optimizing load transient response in high-current automotive buck converters requires a systematic understanding of both the passive output stage and the control loop dynamics. By working through the Phase 1 (capacitor-dominated) and Phase 2 (control loop) response mechanisms, designers can make informed decisions about component selection and compensation settings.

TPS62A2xx-Q1 families simplify this process through 16 discrete internal compensation settings, allowing the designer to tailor the loop response to the application's specific transient requirements without external compensation networks. The design equations presented in this application note — validated through the worked example — provide a reliable starting point for selecting the appropriate compensation setting and minimum output capacitance.

Key takeaways:

- Phase 1 response is dominated by COUT, ESR, ESL, and inductance — minimize parasitics and choose low-ESR MLCCs
- Phase 2 response is governed by the crossover frequency, which is shaped by both the internal error amplifier gain and the external RCOMP selection
- TAM significantly reduces overshoot and minimum capacitance requirements for V_{OUT} Ranges 1–3
- Always calculate minimum COUT for both in-regulation and saturation criteria and select the larger value
- The equation-based approach provides a solid foundation, but lab validation or PDN simulation is recommended for final optimization

By following the structured design procedure in Section 3, designers can confidently select compensation settings that balance fast transient response with robust stability across all operating conditions.

6 References

Texas Instruments, *TPS62A2xx-Q1 2.7V to 6V Input, 8A, 10A, 12A Automotive Fast Transient Synchronous Step-Down Converters*, datasheet.

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