Application Note

Input Common-Mode Tolerance Modes for TAx5x1x/ TAx5x1x-Q1 Devices

Lakshmi Narasimhan Badrinarayanan, Aman Agrawal, Jeff McPherson

ABSTRACT

The TAx5x1x/TAx5x1x-Q1 family of devices include dual-channel, high-performance, analog to-digital converters for audio applications. This family of devices supports highly configurable inputs to allow the device to achieve high performance even in the presence of large common-mode signals.

Common Mode Rejection Ratio (CMRR) is an important specification in determining the performance of an audio ADC when it is placed in systems that can contain common-mode interferences on the signal lines. One example of such must be the 50-60Hz supply line interference. This application note describes how to configure the input common-mode level tolerance on the TAC5x1x/TAC5x1x-Q1 devices, along with the impact on certain performance parameters such as SNR, THD+N, and so on.

This application note is applicable for the following devices in the family:

- TAC5212, TAC5112
- TAC5111
- TAA5212
- TAC5112-Q1, TAC5111-Q1
- TAC5242, TAC5142
- TAA5242

Table of Contents

Trademarks

1 Introduction

Figure 1-1 (a) describes a differential-input amplifier, with input signals V_{IN+} and V_{IN-} on the (+) and (-) terminals respectively.

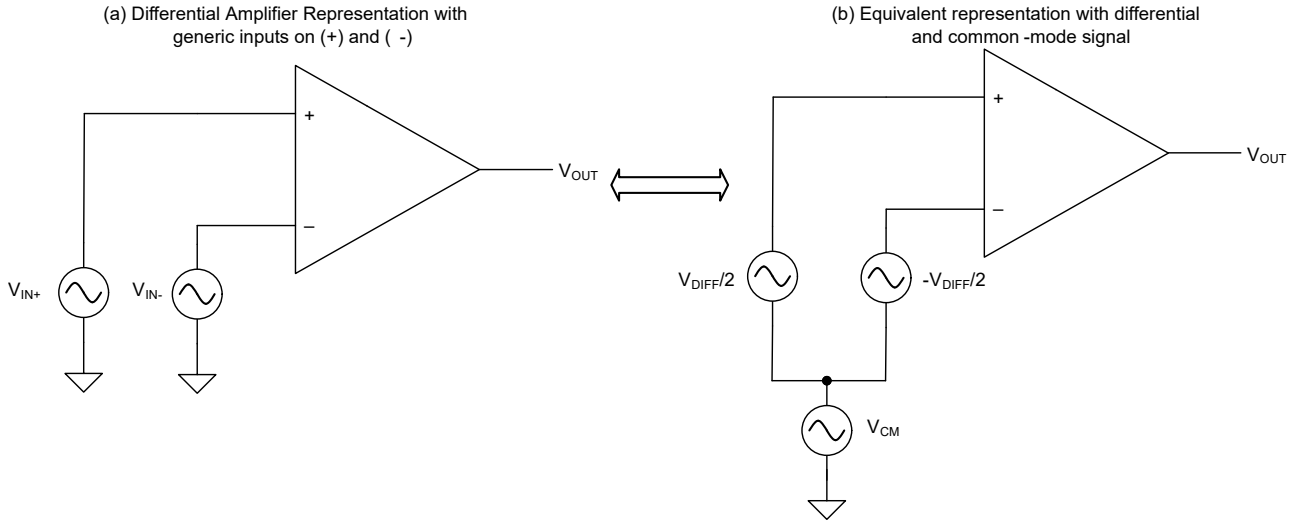

Figure 1-1. Differential-Input Amplifier

For an ideal amplifier, the output V_{OUT} is:

$$V_{OUT} = A_d*(V_{IN+} + V_{IN-}) \quad (1)$$

Where A_d is the differential gain of the amplifier.

However, in a practical amplifier, mismatches between the (+) and (-) signals paths can result in an additional component to the output signal. To compute this, the circuit in Fig 1-1 (b) can be equivalently represented as shown in Figure 1-1 (b), with a "differential signal" V_{DIFF}, and a "common-mode" signal "V_{CM}". For such an amplifier, the output is given by:

$$V_{OUT} = A_d*V_{DIFF} + A_c*V_{CM} \quad (2)$$

Where A_d is the differential gain, and A_c is called the common-mode gain of the amplifier. These signals are given by:

$$V_{DIFF} = V_{IN+} - V_{IN-} \quad (3)$$

$$V_{CM} = \frac{V_{IN+} + V_{IN-}}{2} \quad (4)$$

One of the key performance parameters for a differential input system is it's ability to "reject" such common-mode signals. This is called "Common-Mode Rejection Ratio (CMRR)", and the value of CMRR in dB is given by:

$$CMRR(dB) = 20*\log\left(\frac{1}{A_c}\right) \quad (5)$$

For an ideal differential amplifier, the CMRR is ∞ dB.

The CMRR of a non-ideal amplifier can be measured by providing the same signal V_{CM} at both the input terminals and observing the output V_{OUT}. The CMRR can then be calculated as:

$$CMRR(dB) = 20*\log\left(\frac{V_{CM}}{V_{OUT}}\right) \quad (6)$$

However, such circuits also have a specified range of common-mode swing which they can tolerate. In this document, the common-mode swing tolerance for the TAC5x1x/TAC5x1x-Q1 devices is discussed, along with how this tolerance can be programmed, and its impact on device performance.

2 Detailed Description

The TAC5x1x/TAC5x1x-Q1 family comprises of mono/stereo ADCs, which can process differential and single-ended signals. These signals can be AC-coupled or DC-coupled to the INxP/M pins.

In an audio system, these differential signals are inevitably combined with common-mode interfering signals before reaching the device pins. There are three different modes the ADCs can operate in, and each mode describes the maximum common mode swing that can be tolerated on the INxP/M pins. In each mode, the CMRR of the device is rated to the respective common-mode tolerance swing. These modes are described in detail in Common Mode Tolerance Modes.

To test the device operation with a common-mode swing, an AC signal source is connected to both INP and INM pins of the codec, as shown in Figure 2-1. All the results in this app note are measured on the respective EVMs.

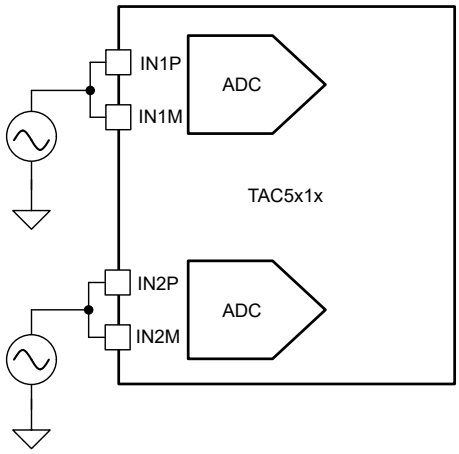

Figure 2-1. Connection for Checking Common-Mode Functions

2.1 Common Mode Tolerance Modes

The TAC5x1x/TAC5x1x-Q1 family of devices support three modes of common-mode operation for the input ADCs. This mode is selected by configuring the ADC_CHx_CM_TOL field (x is the channel number) that is present in the ADC_CHx_CFG0 register (B0_P0_R80[3:2] for IN1P/IN1M, B0_P0_R85[3:2] for IN2P/IN2M). These register fields are described in Table 2-1.

Table 2-1. Register Settings for ADC Common-Mode Tolerance

Register Field Location (Book_Page_Register[MSB:LSB])	Register Field Name	Register Field Description
B0_P0_R80[3:2]	ADC_CH1_CM_TOL[1:0]	ADC Channel 1 input common-mode tolerance (applicable for the analog input). 0d = AC-coupled input with common mode variance tolerance supported 100mV$_{pp}$ for differential configuration 1d = AC-coupled / DC-coupled input with common mode variance tolerance supported 1V$_{pp}$ for differential configuration 2d = AC-coupled / DC-coupled input with common mode variance tolerance supported rail to rail (supply to ground) (High CMRR tolerance mode) 3d = Reserved
B0_P0_R85[3:2]	ADC_CH2_CM_TOL[1:0]	ADC Channel 2 input common-mode tolerance (applicable for the analog input). 0d = AC-coupled input with common mode variance tolerance supported 100mV$_{pp}$ for differential configuration 1d = AC-coupled / DC-coupled input with common mode variance tolerance supported 1V$_{pp}$ for differential configuration 2d = AC-coupled / DC-coupled input with common mode variance tolerance supported rail to rail (supply to ground) (High CMRR tolerance mode) 3d = Reserved

Similarly, for the TAx5x42 hardware-controlled devices listed in Abstract, the common-mode tolerance can be set by configuring the MD5-MD4 pins of the device per Table 2-2.

Table 2-2. Analog Input Configurations for TAx5x42 Devices

MD5	MD4	ANALOG INPUT CONFIGURATION
Low (0)	Low (0)	Differential input; AC-Coupled only
Low (0)	High (1)	Differential input; AC or DC-Coupled with High Common Mode Tolerance
High (1)	Low (0)	Single-Ended input on INxP; AC-Coupled only
High (1)	High (1)	Single-Ended input on INxP; AC or DC-Coupled with High Common Mode Tolerance

2.2 Common-Mode Rejection

Each common-mode tolerance mode achieves good common-mode rejection up to the limits of that mode. The graphs in Figure 2-2 show FFTs of the ADC output on a on a TAC5212EVM-K, with a 1kHz AC common-mode signal given to the inputs along with a common-mode DC bias voltage. Figure 2-2 (a) is the FFT when the common-mode swing is at 50mV_{pp} which is within the tolerable limit of 100mV_{pp} (35.36mVrms, which corresponds to -35.05dBFS for a 2Vrms full-scale swing). Figure 2-2 (b) is the FFT when the common-mode swing is at tolerance limit of 100mV_{pp}. Figure 2-2 (c) is the FFT when the common-mode swing exceeds the tolerance limit of 100 mV_{pp}.

Similarly, Figure 2-3 and Figure 2-4 show the FFTs for the TAC5212 output on the TAC5212EVM-K when the device is configured in CM_TOL of 1 and 2 respectively.

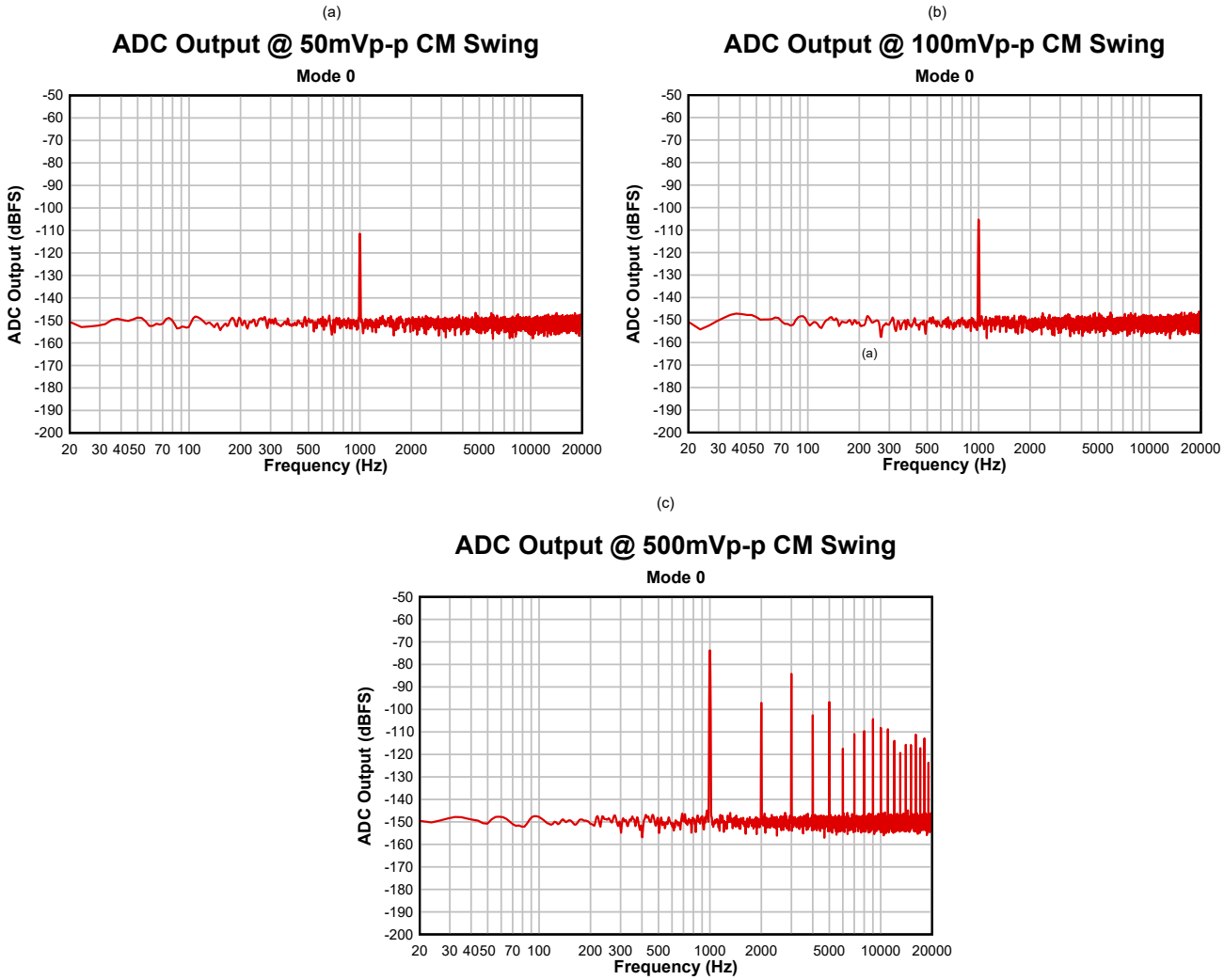

Figure 2-2. ADC Output Spectrum at CM_TOL Mode 0

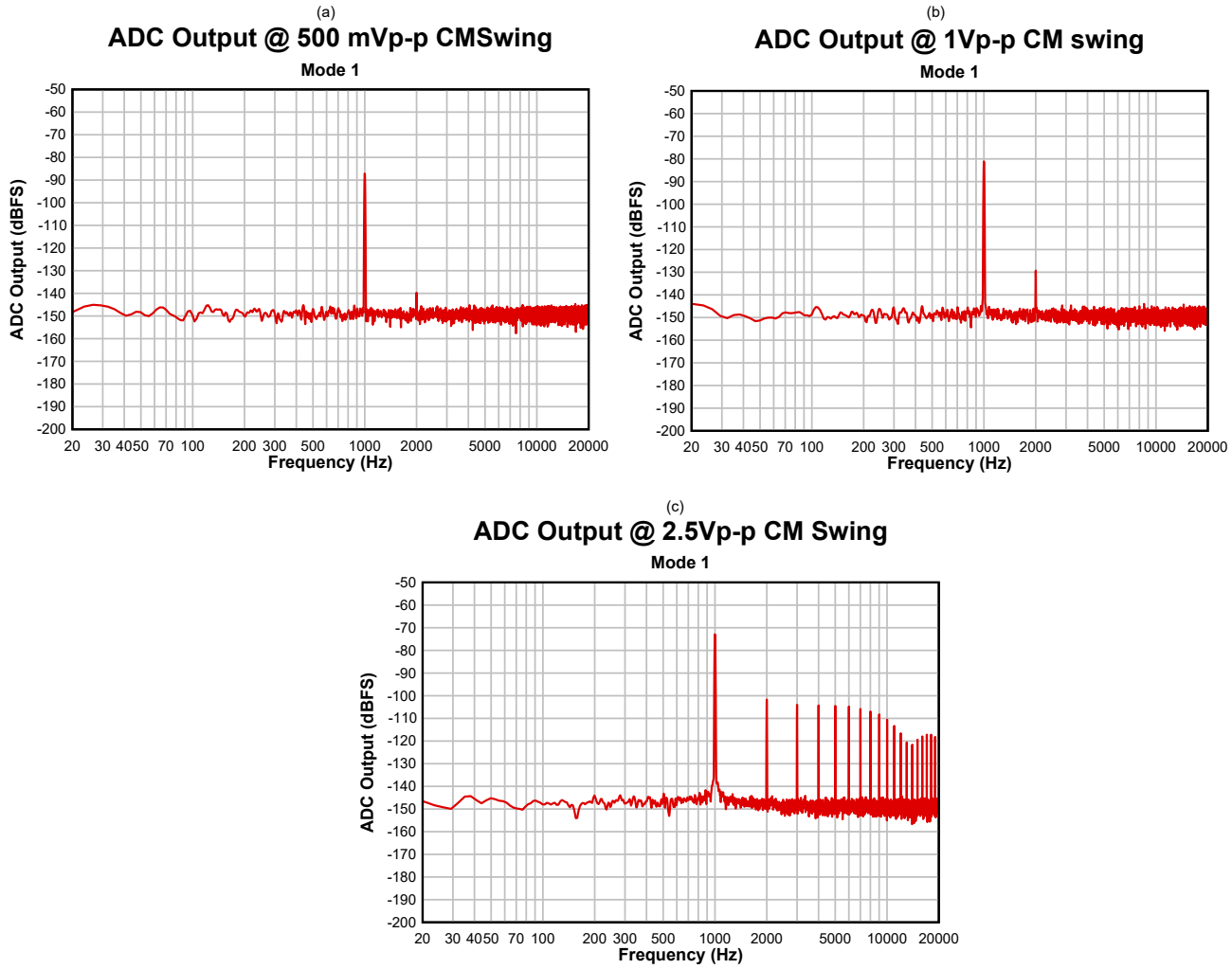

Figure 2-3. ADC Output Spectrum at CM_TOL Mode 1

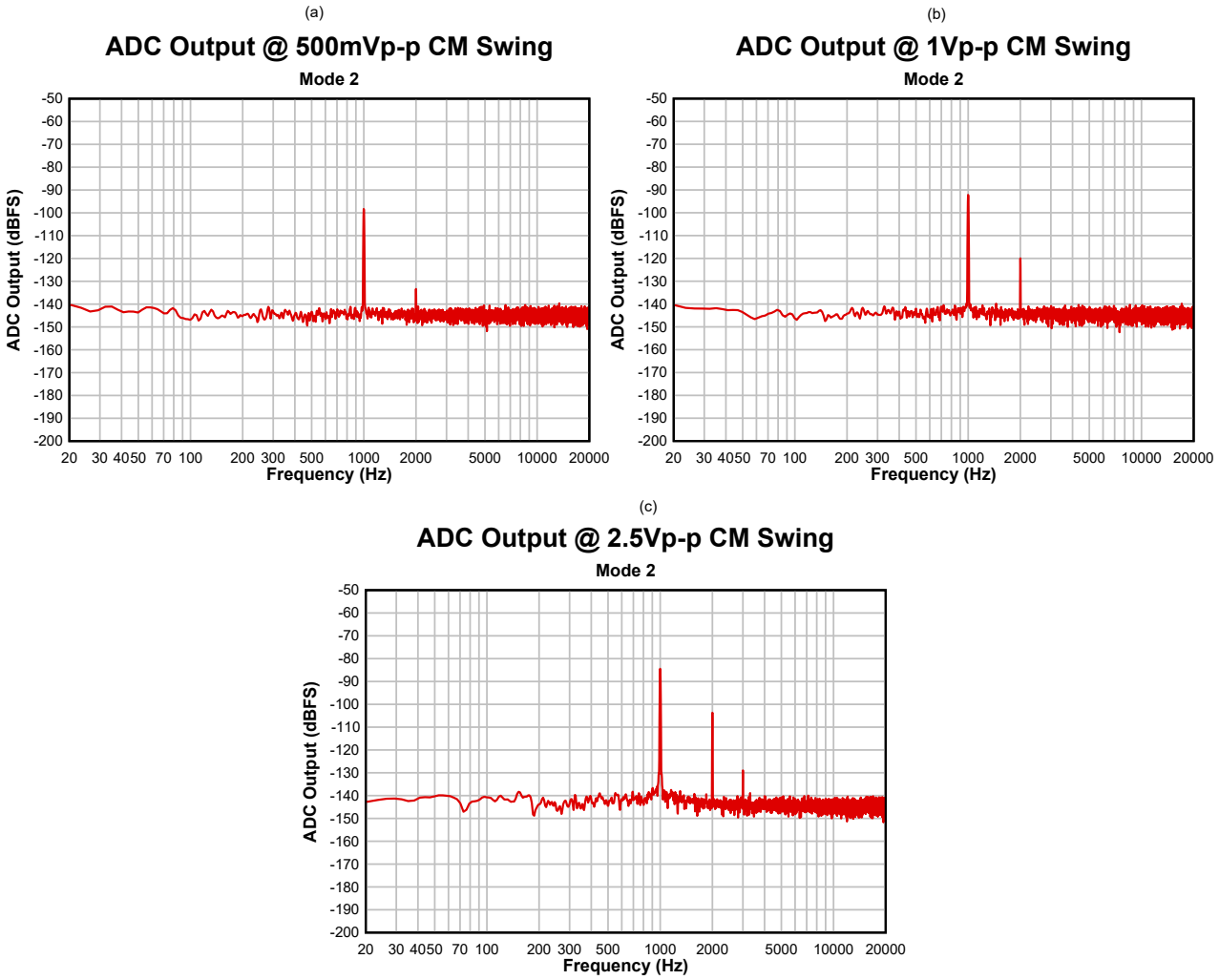

Figure 2-4. ADC Output Spectrum at CM_TOL Mode 2

CMRR for the TAx511x/TAx511x-Q1 devices in mode 0 is 60dB(typ) and typically changes by a few dB in modes 1 and 2 for an equivalent signal amplitude. The higher performance TAx521x and TAx521x-Q1 can achieve a CMRR closer to 80dB (typ) in mode 2 and is a good choice for systems that want the best performance possible in applications that require high common-mode tolerance. The variation of CMRR across different levels of input common-mode swing is plotted in Figure 2-5 for a 1kHz common-mode signal. The AC signal level is varied from 50mVpp to 2.75Vpp, with a common-mode DC bias voltage. The CMRR in Figure 2-5 is averaged across both input channels on a TAC5212EVM-K.

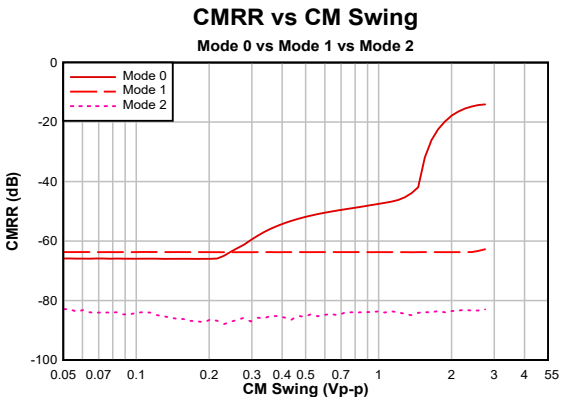

Figure 2-5. CMRR vs Swing

Note that mismatches in the external differential signal path (trace impedance, AC-coupling capacitor tolerance etc.) also contribute to the CMRR seen at the ADC output. Figure 2-6 shows the variation in CMRR across frequency on the TAC5212EVM-K when the inputs are AC-Coupled with 10µF capacitors whose tolerance is up to +/-20%, and when the inputs are DC-Coupled. The measurement was taken with a 100mV$_{p-p}$ common-mode signal level. The CMRR in Figure 2-6 is averaged across both input channels.

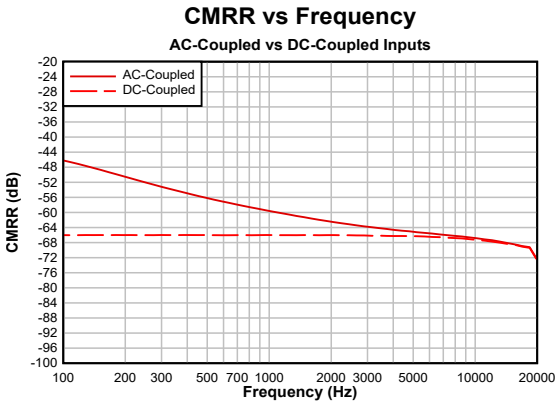

Figure 2-6. AC-Coupled vs DC-Coupled Input CMRR

2.3 Device Performance Across CM_TOL Modes

Additionally, some of the other performance parameters (like SNR) are impacted by the configured CM_TOL mode. Table 2-3 lists the SNR (A-weighted), Dynamic Range (A-weighted) and CMRR for the different modes measured on a TAC5112EVM-K and TAC5212EVM-K devices. The results are measured for a 1kHz, 100mV$_{pp}$ signal with a common-mode DC bias voltage, and averaged across both input channels.

These results indicate that if the user requires a higher common-mode tolerance at the input (and in the case of TAC5212, higher CMRR performance), it comes at the cost of performance reduction. For instance, configuring a TAC5212 device to operate at a CM_TOL mode of 2 provides a CMRR of 80dB (typ), however the SNR degrades by approximately 6-7dB (typ).

Table 2-3. Performance of TAx511x/TAx521x Across CM_TOL Modes

Device	CM_TOL Mode	Impedance Setting (kΩ)	CMRR @ 100mV$_{pp}$ (dB)	SNR (dBFS) A-Weighted	Dynamic Range (dBFS) A-Weighted	THD+N (dB)
TAC5212	0	5	66	119	119	-95
		10	61	114	114	-101
		40	48	103	103	-98
	1	5	64	117	117	-95
		10	61	113	113	-101
		40	48	102	102	-97
	2	5	84	112	112	-945
		10	73	109	109	-100
		40	78	100	100	-94
TAC5112	0	5	61	104	104	-98
		10	58	103	103	-101
		40	47	102	102	-97
	1	5	61	104	104	-98
		10	58	103	103	-100
		40	47	101	101	-97
	2	5	63	103	103	-97
		10	58	102	102	-100
		40	47	100	100	-96

3 Summary

Multiple common-mode tolerance modes are provided in the TAx5x1x/TAx5x1x-Q1 family to allow the system to perform well even in the presence of large amounts of common-mode noise. However, note that higher common-mode tolerance comes with performance reduction, hence TI recommends the lowest common-mode tolerance setting possible that still satisfies the requirements of the system.

4 References

1. Texas Instruments, *TAC5212 High-performance stereo audio codec with 119dB dynamic range ADC and 120dB dynamic range DAC*, datasheet.
2. Texas Instruments, *TAC5112 Low-power stereo audio codec with 105dB dynamic range ADC and 114dB dynamic range DAC*, datasheet.
3. Texas Instruments, *Input Common-Mode Tolerance and High CMRR Modes for TLV320ADCx120 and PCMx120-Q1 Devices*, application note.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Corrected link to Reference 2

Changes from Revision * (April 2026) to Revision A (September 2026)	Page
• Updated datasheet reference title from *"TAC5112 Low-Power, Stereo Audio Codec with 102dB Dynamic Range ADC and 106dB"* to *"TAC5112 Low-power stereo audio codec with 105dB dynamic range ADC and 114dB dynamic range DAC"* for citation accuracy	10

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025