TPS6594-Q1 Power Management IC (PMIC) with 5 BUCKs and 4 LDOs for Safety-Relevant Automotive Applications

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device operates from 3 V to 5.5 V input supply
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM classification level 2
  - Device CDM classification level C4A
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 system design up to ASIL-D
  - Documentation available to aid IEC 61508 system design up to SIL-3
  - Systematic capability up to ASIL-D
  - Hardware integrity up to ASIL-D
  - Input supply voltage monitor and over-voltage protection
  - Under/overvoltage monitors and over-current monitors on all output supply rails
  - Watchdog with selectable trigger / Q&A mode
  - Two error signal monitors (ESMs) with selectable level / PWM mode
  - Thermal monitoring with high temperature warning and thermal shutdown
  - Bit-integrity (CRC) error detection on internal configuration registers and non-volatile memory (NVM)
- Low-power consumption
  - 2 µA typical shutdown current
  - 7 µA typical in back up supply only mode
  - 20 µA typical in low power standby mode
- Five step-down switched-mode power supply (BUCK) regulators:
  - 0.3 V to 3.34 V output voltage range in 5, 10, or 20-mV steps
  - One with 4 A, three with 3.5 A, and one with 2 A output current capability
  - Flexible multi-phase capability for four BUCKs: up to 14 A output current from a single rail
  - Short-circuit and over-current protection
  - Internal soft-start for in-rush current limitation
  - 2.2 MHz / 4.4 MHz switching frequency
  - Ability to synchronize to external clock input
- Three low-dropout (LDO) linear regulators with configurable bypass mode
  - 0.6 V to 3.3 V output voltage range with 50-mV steps in linear regulation mode
  - 1.7 V to 3.3 V output voltage range in bypass mode
  - 500 mA output current capability with short-circuit and over-current protection
- One low-dropout (LDO) linear regulator with low-noise performance
  - 1.2 V to 3.3 V output voltage range in 25-mV steps
  - 300 mA output current capability with short-circuit and over-current protection
- Configurable power sequence control in non-volatile memory (NVM):
  - Configurable power-up and power-down sequences between power states
  - Digital output signals can be included in the power sequences
  - Digital input signals can be used to trigger power sequence transitions
  - Configurable handling of safety-relevant errors
- 32-kHz crystal oscillator with option to output a buffered 32-kHz clock output
- Real-time clock (RTC) with alarm and periodic wake-up mechanism
- One SPI or two I^2C control interfaces, with second I^2C interface dedicated for Q&A watchdog communication
- Package option:
  - 8-mm × 8-mm 56-pin VQFNP with 0.5-mm pitch

2 Applications

- Automotive infotainment and digital cluster, navigation systems, telematics, body electronics and lighting
- Advanced driver assistance system (ADAS)
- Industrial control and automation

3 Description

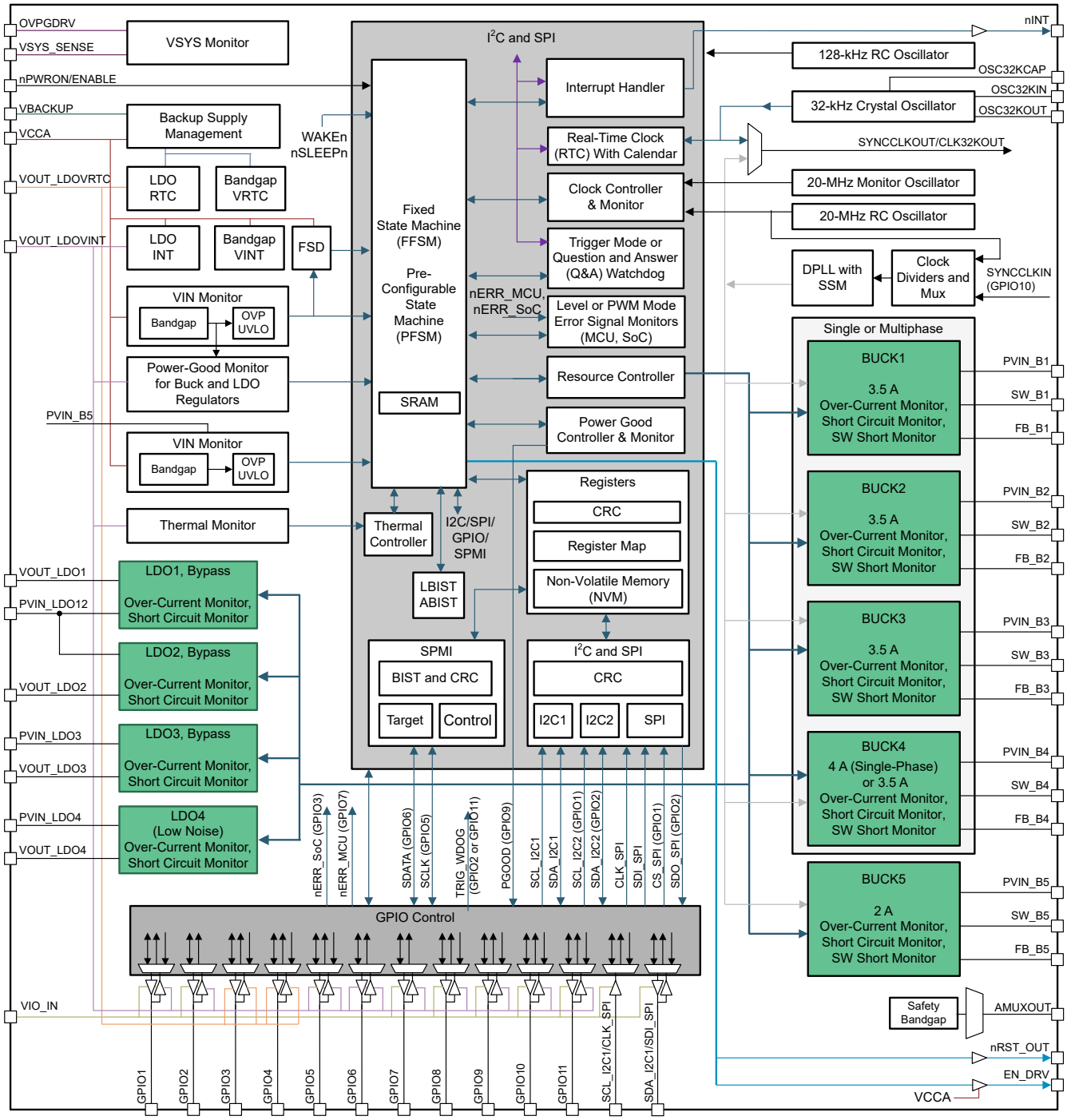
The TPS6594-Q1 device provides four flexible multi-phase configurable BUCK regulators with 3.5 A output current per phase, and one additional BUCK regulator with 2 A output current.

Table 3-1. Device Information Table

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TPS6594-Q1	VQFNP (56)	8.00 mm × 8.00 mm

(1) See the orderable addendum at the end of the data sheet for all available packages.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.



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Functional Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2021) to Revision B (February 2022) **Page**

- Section 8.8 Specifications - BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators: Change typical value for parameter 4.112 (from 300-mA to 420-mA), parameter 4.113 (from 200-mA to 100-mA), parameter 4.122 (from 250-mA to 370-mA), parameter 4.123 (from 150-mA to 30-mA), parameter 4.131 (from 400-mA to 310-mA), parameter 4.132 (from 170-mA to 290-mA), parameter 4.133 (from 230-mA to 20-mA), parameter 4.151 (from 335-mA to 290-mA), parameter 4.152 (from 150-mA to 230-mA), parameter 4.153 (from 185-mA to 50-mA) 18
- Added description about OVGDRV - VSYSSENSE relation 47
- BUCK Regulator Overview: added Current Limit and Short-to-Ground Detection on SW_Bx pins 49
- Added section: BUCK Regulator Current Limit 58
- Added section: SW_Bx Short-to-Ground Detection 58
- Added LDO1, LDO2, LDO3 Current Limit description 61
- Added LDO4 Current Limit description 62
- Added note about unmasking the UV/OV right before the release of the nRSTOUT resp. nRSTOUT_SoC pins. 65
- Added note which explains the required voltage accuracy for external supply rails (including VCCA input supply) that are monitored by the TPS6594-Q1 in order to pass the ABIST 65
- Added explanation on how to use Voltage Monitors of unused BUCK and LDO regulators 65
- Corrected Watchdog Reference Answer Calculation figure 94
- Added note which explains necessary system-software steps for using RUNTIME_BIST 121
- Added BOOT_BIST and RUNTIME_BIST 121

- Changed all instances of legacy terminology into "controller" and "target", also in all sub-sections 146
- For I2C, changed all instances of legacy terminology into "controller" and "target". For SPI, changed all instances of legacy terminology into "controller" and "peripheral". For the CRC, changed all instances of legacy terminology into "CRC on received data (R_CRC)", and "CRC on transmitted data" (T_CRC). These changes also applies to all sub-sections. 154
- Corrected figure on Calculation of 8-Bit Controller CRC (R_CRC) Output, corrected figure on Calculation of 8-Bit Target CRC (T_CRC) Input 154
- Added note about missing R_CRC after am I2C write 157
- Added note which describes a device erratum related to COMM_FRM_ERR_INT bit 159
- Added note which explains the I^2C addresses for each register map page on the I^2C bus. Added note which explains how each register map page is addressed when using SPI. 161
- Added note about writing to RESERVED bits causing a Register Map CRC error 162
- Corrected description of register DEV_REV 163
- Updated PDN example figure, and updated the table with the Local and POL Capacitors used for Buck Use Case Validation 368
- Updated the recommendations for the Digital Signal Connections 371
- Updated Layout Guidelines with respect to output capacitor on VOUT_LDOVINT pin 383
- Updated Layout Example figure 385

Changes from Revision * (December 2019) to Revision A (April 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Changed the status of the document from: *advanced information* to: *publication data* 1

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5 Description (continued)

All of the BUCK regulators can be synchronized to an internal 2.2-MHz or 4.4-MHz or an external 1-MHz, 2-MHz, or 4-MHz clock signal. To improve the EMC performance, an integrated spread-spectrum modulation can be added to the synchronized BUCK switching clock signal. This clock signal can also be made available to external devices through a GPIO output pin. The device provides four LDOs: three with 500-mA capability, which can be configured as load switches; one with 300-mA capability and low-noise performance.

Non-volatile memory (NVM) is used to control the default power sequences and default configurations, such as output voltage and GPIO configurations. The NVM is pre-programmed to allow start-up without external programming. Most static configurations, stored in the register map of the device, can be changed from the default through SPI or I^2C interfaces to configure the device to meet many different system needs. The NVM contains a bit-integrity-error detection feature (CRC) to stop the power-up sequence if an error is detected, preventing the system from starting in an unknown state.

The TPS6594-Q1 includes a 32-kHz crystal oscillator, which generates an accurate 32-kHz clock for the integrated RTC module. A backup-battery management provides power to the crystal oscillator and the real-time clock (RTC) module from a coin cell battery or a super-cap in the event of power loss from the main supply.

The TPS6594-Q1 device includes protection and diagnostic mechanisms such as voltage monitoring on the input supply, input over-voltage protection, voltage monitoring on all BUCK and LDO regulator outputs, register and interface CRC, current-limit, short-circuit protection, thermal pre-warning, and over-temperature shutdown. The device also includes a Q&A or trigger mode watchdog to monitor for MCU software lockup, and two error signal monitor (ESM) inputs with fault injection options to monitor the error signals from the attached SoC or MCU. The TPS6594-Q1 can notify the processor of these events through the interrupt handler, allowing the MCU to take action in response.

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6 Pin Configuration and Functions

Figure 6-1 shows the 56-pin RWE plastic quad-flatpack no-lead (VQFNP) pin assignments and thermal pad.

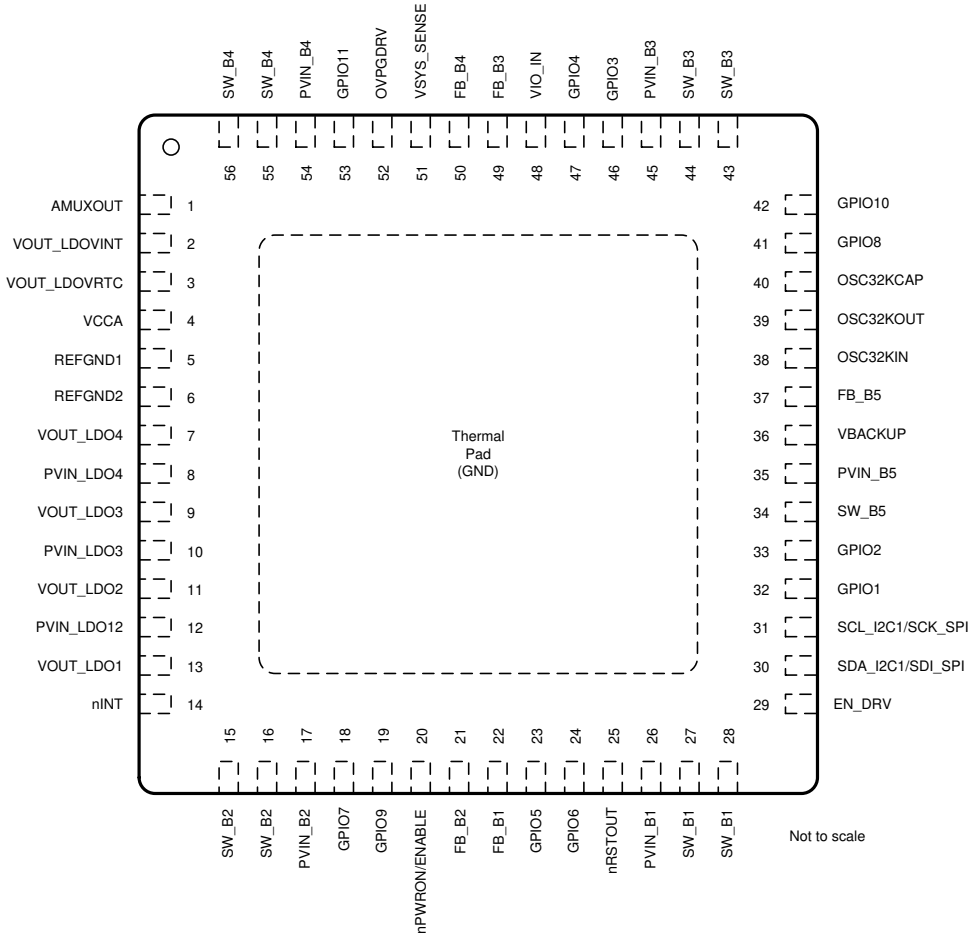

Figure 6-1. 56-Pin RWE (VQFNP) Package, 0.5-mm Pitch, With Thermal Pad (Top View)

Table 6-1. Pin Attributes

PIN		I/O	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.			
STEP-DOWN CONVERTERS (BUCKs)				
FB_B1	22	I	Output voltage-sense (feedback) input for BUCK1 or differential voltage-sense (feedback) positive input for BUCK12/123/1234 in multi-phase configuration.	Ground
FB_B2	21	I	Output voltage-sense (feedback) input for BUCK2 or differential voltage-sense (feedback) negative input for BUCK12/123/1234 in multi-phase configuration.	Ground
FB_B3	49	I	Output voltage-sense (feedback) input for BUCK3 or differential voltage-sense (feedback) positive input for BUCK34 in dual-phase configuration.	Ground
FB_B4	50	I	Output voltage-sense (feedback) input for BUCK4 or differential voltage-sense (feedback) negative input for BUCK34 in dual-phase configuration.	Ground
FB_B5	37	I	Output voltage-sense (feedback) input for BUCK5	Ground
PVIN_B1	26	I	Power input for BUCK1	VCCA
PVIN_B2	17	I	Power input for BUCK2	VCCA
PVIN_B3	45	I	Power input for BUCK3	VCCA
PVIN_B4	54	I	Power input for BUCK4	VCCA

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Table 6-1. Pin Attributes (continued)

PIN		I/O	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.			
PVIN_B5	35	I	Power input for BUCK5	VCCA
SW_B1	27	O	Switch node of BUCK1	Floating
SW_B1	28	O	Switch node of BUCK1	Floating
SW_B2	15	O	Switch node of BUCK2	Floating
SW_B2	16	O	Switch node of BUCK2	Floating
SW_B3	43	O	Switch node of BUCK3	Floating
SW_B3	44	O	Switch node of BUCK3	Floating
SW_B4	55	O	Switch node of BUCK4	Floating
SW_B4	56	O	Switch node of BUCK4	Floating
SW_B5	34	O	Switch node of BUCK5	Floating
LOW-DROPOUT REGULATORS				
PVIN_LDO3	10	I	Power input voltage for LDO3 regulator	VCCA
PVIN_LDO4	8	I	Power input voltage for LDO4 regulator	VCCA
PVIN_LDO12	12	I	Power input voltage for LDO1 and LDO2 regulator	VCCA
VOUT_LDO1	13	O	LDO1 output voltage	Floating
VOUT_LDO2	11	O	LDO2 output voltage	Floating
VOUT_LDO3	9	O	LDO3 output voltage	Floating
VOUT_LDO4	7	O	LDO4 output voltage	Floating
LOW-DROPOUT REGULATORS (INTERNAL)				
VOUT_LDOVINT	2	O	LDOVINT output for connecting to the filtering capacitor. Not for external loading.	—
VOUT_LDOVRTC	3	O	LDOVRTC output for connecting to the filtering capacitor. Not for external loading.	—
CRYSTAL OSCILLATOR				
OSC32KCAP	40	O	Filtering capacitor for the 32 KHz crystal Oscillator, connected to VRTC through an internal 100 Ω resistor.	Floating
OSC32KIN	38	I	32-KHz crystal oscillator input	Ground
OSC32KOUT	39	O	32-KHz crystal oscillator output	Floating
SYSTEM CONTROL				
AMUXOUT	1	O	Buffered bandgap output	Floating
EN_DRV	29	O	Enable Drive output pin to indicate the device entering safe state (set low when ENABLE_DRV bit is '0').	Floating
GPIO1	32	I/O	Primary function: General-purpose input[(1)] and output When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground Output: Floating
		I	Alternative function: SCL_I2C2, which is the Q&A WatchDog I^2C serial clock (external pull-up).	Ground
		I	Alternative function: CS_SPI, which is the SPI chip enable signal.	Ground
		O	Alternative function: nRSTOUT_SoC, which is the SoC reset or power on output (Active Low).	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground

Table 6-1. Pin Attributes (continued)

PIN		I/O	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.			
GPIO2	33	I/O	Primary function: General-purpose input[(1)] and output When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground Output: Floating
		I/O	Alternative function: SDA_I2C2, which is the Q&A WatchDog I^2C serial bidirectional data (external pull-up).	Ground
		O	Alternative function: SDO_SPI, which is the SPI output data signal.	Floating
		I	Alternative function: TRIG_WDOG, which is the watchdog trigger input signal for Watchdog Trigger mode.	Ground
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
GPIO3	46	I/O	Primary function: General-purpose input[(1)] and output. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground Output: Floating
		I	Alternative function: nERR_SoC, which is the system error count down input signal from the SoC (Active Low).	Floating
		O	Alternative function: CLK32KOUT, which is the output of the 32 KHz crystal oscillator clock.	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Alternative function: LP_WKUP1 or LP_WKUP2, which are capable of processing a wake-up request for the device to go to higher power states while the device is in LP STANDBY state. They can also be used as regular WKUP1 or WKUP2 pins while the device is in mission states.	Ground
GPIO4	47	I/O	Primary function: General-purpose input[(1)] and output. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground Output: Floating
		O	Alternative function: CLK32KOUT, which is the output of the 32 KHz crystal oscillator clock.	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Alternative function: LP_WKUP1 or LP_WKUP2, which are capable of processing a wake-up request for the device to go to higher power states while the device is in LP STANDBY state. They can also be used as regular WKUP1 or WKUP2 pins while the device is in mission states.	Ground
GPIO5	23	I/O	Primary function: General-purpose input[(1)] and output. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground Output: Floating
		I/O	Alternative function: SCLK_SPMI, which is the Multi-PMIC SPMI serial interface clock signal. It is an output pin for the SPMI controller device, and an input pin for the SPMI peripheral device.	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground

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Table 6-1. Pin Attributes (continued)

PIN		I/O	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.			
GPIO6	24	I/O	Primary function: General-purpose input[(1)] and output. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground Output: Floating
		I/O	Alternative function: SDATA_SPMI, which is the Multi-PMIC SPMI serial interface bidirectional data signal.	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
GPIO7	18	I/O	Primary function: General-purpose input[(1)] and output. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground Output: Floating
		I	Alternative function: nERR_MCU, which is the system error count down input signal from the MCU (Active Low).	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
GPIO8	41	I/O	Primary function: General-purpose input[(1)] and output. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground Output: Floating
		O	Alternative function: SYNCCLKOUT, which is a clock output synchronized to the switching clock signals for the bucks in the device.	Floating
		I	Alternative function: DISABLE_WDOG, which is the input to disable the watchdog monitoring function.	Floating
		O	Alternative function: CLK32KOUT, which is the output of the 32 KHz crystal oscillator clock.	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
GPIO9	19	I/O	Primary function: General-purpose input[(1)] and output. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground Output: Floating
		O	Alternative function: PGOOD, which is the indication signal for valid regulator output voltages and currents	Floating
		O	Alternative function: SYNCCLKOUT, which is the internal fallback switching clock for BUCK.	Floating
		I	Alternative function: DISABLE_WDOG, which is the input to disable the watchdog monitoring function.	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground

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Table 6-1. Pin Attributes (continued)

PIN		I/O	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.			
GPIO10	42	I/O	Primary function: General-purpose input[(1)] and output. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground Output: Floating
		I	Alternative function: SYNCCLKIN, which is the external switching clock input for BUCK.	Floating
		O	Alternative function: SYNCCLKOUT, which is the internal fallback switching clock for BUCK.	Floating
		O	Alternative function: CLK32KOUT, which is the output of the 32 KHz crystal oscillator clock.	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
GPIO11	53	I/O	Primary function: General-purpose input[(1)] and output. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground Output: Floating
		I	Alternative function: TRIG_WDOG, which is the watchdog trigger input signal for Watchdog Trigger mode.	Ground
		O	Alternative function: nRSTOUT_SoC, which is the SoC reset or power on output (Active Low).	Floating
		I	Alternative function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Alternative function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
nINT	14	O	Maskable interrupt output request to the host processor (Active Low)	Floating
nPWRON/ENABLE	20	I	NPWRON_SEL = '0': ENABLE- Level sensitive input pin to power up the device, with configurable polarity	Floating
		I	NPWRON_SEL = '1': nPWRON - Active low edge sensitive button press pin to power up the device	Ground
OVPGDRV	52	O	Gate drive output for input over voltage protection FET	Floating
nRSTOUT	25	O	MCU reset or power on reset output (Active Low)	Floating
SCL_I2C1/SCK_SPI	31	I	If SPI is the default interface: SCL_I2C1 - I^2C serial clock (external pullup)	Ground
		I	If I^2C is the default interface: CLK_SPI - SPI clock signal	Ground
SDA_I2C1/SDI_SPI	30	I/O	If SPI is the default interface: SDA_I2C1 - I^2C serial bidirectional data (external pullup)	Ground
		I	If I^2C is the default interface: SDI_SPI - SPI input data signal	Ground
POWER SUPPLIES AND REFERENCE GROUNDS				
PGND/ThermalPad	—	—	Power Ground, which is also the thermal pad of the package. Connect to PCB ground planes with multiple vias.	—
REFGND1	5	—	System reference ground	—
REFGND2	6	—	System reference ground	—
VBACKUP	36	I	Backup power source input pin	Ground
VCCA	4	I	Analog input voltage for the internal LDOs and other internal blocks	—
VIO_IN	48	I	Digital supply input for GPIOs and I/O supply voltage	—
VSYS_SENSE	51	I	Analog input sense pin	Ground

(1) Default option before NVM settings are loaded into the device.

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6.1 Digital Signal Descriptions

Table 6-2. Signal Descriptions

SIGNAL NAME	I/O	Threshold Level	INPUT TYPE SELECTION		OUTPUT TYPE SELECTION		Internal PU/ PD[2]	RECOMMENDED EXTERNAL PU/PD[2]	Control Register Bits
			Power Domain	DEGLITCH TIME[5]	Power Domain	Push-pull/ Open-drain[4]			
nPWRON (Selectable function of nPWRON/ ENABLE pin)[1]	Input	$V_{IL(VCCA)}$, $V_{IH(VCCA)}$	VRTC	50 ms			400 kΩ PU to VCCA	None	NPWRON_SEL
ENABLE (Selectable function of nPWRON/ ENABLE pin)[1]	Input	$V_{IL(VCCA)}$, $V_{IH(VCCA)}$	VRTC	8 µs			400 kΩ SPU to VCCA, or 400 kΩ SPD to GND	None	NPWRON_SEL ENABLE_POL ENABLE_DEGLITCH_EN ENABLE_PU_PD_EN ENABLE_PU_SEL
EN_DRV	Output	$V_{OL(EN_DRV)}$			VCCA/ PVIN_B1	PP	10 kΩ High-side to VCCA	None	ENABLE_DRV
SCL_I2C1 (Selectable function of SCL_I2C1/ SCK_SPI pin)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	High-speed mode: 10 ns All other modes: 50 ns			None	PU to VIO	I2C or SPI selection from NVM-configuration [6] I2C1_HS
SDA_I2C1 (Selectable function of SDA_I2C1/ SDI_SPI pin)[1]	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)_20mA}$	VINT	High-speed mode: 10 ns All other modes: 50 ns	VIO	OD	None	PU to VIO	I2C or SPI selection from NVM-configuration[6] I2C1_HS
SCL_I2C2 (Selectable function of GPIO1)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	High-speed mode: 10 ns All other modes: 50 ns			None	PU to VIO	I2C or SPI selection from NVM-configuration[6] I2C2_HS GPIO1_SEL
SDA_I2C2 (Selectable function of GPIO2)[1]	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)_20mA}$	VINT	High-speed mode: 10 ns All other modes: 50 ns	VIO	OD	None	PU to VIO	I2C or SPI selection from NVM-configuration[6] I2C2_HS GPIO2_SEL
SCK_SPI (Selectable function of SCL_I2C1/ SCK_SPI pin)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	None			None	None	I2C or SPI selection from NVM-configuration[6]

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Table 6-2. Signal Descriptions (continued)

SIGNAL NAME	I/O	Threshold Level	INPUT TYPE SELECTION		OUTPUT TYPE SELECTION		Internal PU/ PD[2]	RECOMMENDED EXTERNAL PU/PD[2]	Control Register Bits
			Power Domain	DEGLITCH TIME[5]	Power Domain	Push-pull/ Open-drain[4]			
SDI_SPI (Selectable function of SDA_I2C1/ SDI_SPI pin)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	None			None	None	I2C or SPI selection from NVM-configuration[6]
CS_SPI (Selectable function of GPIO1)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	None			None	None	I2C or SPI selection from NVM-configuration[6] GPIO1_SEL
SDO_SPI (Selectable function of GPIO2)[1]	Output	$V_{OL(VIO)_20mA}$, $V_{OH(VIO)}$			VIO	PP[3] / HiZ	None	None	I2C or SPI selection from NVM-configuration[6] GPIO2_SEL
SCLK_SPMI (Configurable function of GPIO5)[1]	Output for SPMI controller device, input for SPMI peripheral device	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)_20mA}$, $V_{OH(DIG)}$	VINT	None	VINT	PP	400 kΩ PD to GND	None	NVM-configuration[6] GPIO5_SEL GPIO5_PU_PD_EN
SDATA_SPMI (Configurable function of GPIO6)[1]	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)_20mA}$, $V_{OH(DIG)}$	VINT	None	VINT	PP / HiZ	400 kΩ PD to GND	None	NVM-configuration[6] GPIO6_SEL GPIO6_PU_PD_EN
nINT	Output	$V_{OL(nINT)}$			VCCA	OD	None	PU to VCCA	
nRSTOUT	Output	$V_{OL(nRSTOUT)}$			VCCA/ VIO	PP[3] or OD	10 kΩ Pull-Up to VIO if configured as Push-Pull	PU to VIO if Open-drain (driven low if no VINT)	NRSTOUT_OD
nRSTOUT_SoC (Configurable function of GPIO1 and GPIO11)[1]	Output	$V_{OL(nRSTOUT)}$			VCCA/ VIO	PP[3] or OD	10 kΩ Pull-Up to VIO if configured as Push-Pull	PU to VIO if Open-drain (driven low if no VINT)	GPIO1_SEL GPIO1_OD GPIO11_SEL GPIO11_OD
PGOOD (Configurable function of GPIO9)[1]	Output	$V_{OL(VIO)}$, $V_{OH(VIO)}$			VIO	PP[3] or OD	None	PU to VIO if Open-drain	GPIO9_SEL GPIO9_OD PGOOD_POL PGOOD_WINDOW PGOOD_SEL_x

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Table 6-2. Signal Descriptions (continued)

SIGNAL NAME	I/O	Threshold Level	INPUT TYPE SELECTION		OUTPUT TYPE SELECTION		Internal PU/PD[2]	RECOMMENDED EXTERNAL PU/PD[2]	Control Register Bits
			Power Domain	DEGLITCH TIME[5]	Power Domain	Push-pull/ Open-drain[4]			
nERR_MCU (Configurable function of GPIO7)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	8 µs			400 kΩ PD to GND	None	GPIO7_SEL
nERR_SoC (Configurable function of GPIO3)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VRTC	15 µs			400 kΩ PD to GND	None	GPIO3_SEL
DISABLE_WDOG (Configurable function of GPIO8 and GPIO9)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	30 µs			400 kΩ PD to GND	PU to VIO	GPIO8_SEL GPIO9_SEL
TRIG_WDOG (Configurable function of GPIO2 and GPIO11)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	30 µs			400 kΩ SPD to GND	None	GPIO2_SEL GPIO2_PU_PD_EN GPIO11_SEL GPIO11_PU_PD_EN
nSLEEP1 (Configurable function of all GPIO pins)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	GPIO3 or 4: VRTC other GPIOs: VINT	8 µs			GPIO3 or 4: 400 kΩ SPU to VRTC GPIO5 or 6: 400 kΩ SPU to VINT all other GPIOs: 400 kΩ SPU to VIO	None	GPIOn_SEL GPIOn_PU_PD_EN NSLEEP1B
nSLEEP2 (Configurable function of all GPIO pins)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	GPIO3 or 4: VRTC other GPIOs: VINT	8 µs			GPIO3 or 4: 400 kΩ SPU to VRTC GPIO5 or 6: 400 kΩ SPU to VINT all other GPIOs: 400 kΩ SPU to VIO	None	GPIOn_SEL GPIOn_PU_PD_EN NSLEEP2B

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Table 6-2. Signal Descriptions (continued)

SIGNAL NAME	I/O	Threshold Level	INPUT TYPE SELECTION		OUTPUT TYPE SELECTION		Internal PU/PD[2]	RECOMMENDED EXTERNAL PU/PD[2]	Control Register Bits
			Power Domain	DEGLITCH TIME[5]	Power Domain	Push-pull/ Open-drain[4]			
WKUP1 (Configurable function of all GPIO pins except GPIO3 and GPIO4)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	8 µs			GPIO5 or 6: 400 kΩ SPU to VINT or 400 kΩ SPD to GND all other GPIOs: 400 kΩ SPU to VIO or 400 kΩ SPD to GND	None	GPIOn_SEL GPIOn_DEGLITCH_EN GPIOn_PU_PD_EN GPIOn_PU_SEL
WKUP2 (Configurable function of all GPIO pins except GPIO3 and GPIO4)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	8 µs			GPIO5 or 6: 400 kΩ SPU to VINT or 400 kΩ SPD to GND all other GPIOs: 400 kΩ SPU to VIO or 400 kΩ SPD to GND	None	GPIOn_SEL GPIOn_DEGLITCH_EN GPIOn_PU_PD_EN GPIOn_PU_SEL
LP_WKUP1 (Configurable function of GPIO3 and GPIO4)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VRTC	8 µs, no deglitch in LP_STANDBY state			400 kΩ SPU to VRTC, or 400 kΩ SPD to GND	None	GPIO3,4_SEL GPIO3,4_DEGLITCH_EN GPIO3,4_PU_PD_EN GPIO3,4_PU_SEL
LP_WKUP2 (Configurable function of GPIO3 and GPIO4)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VRTC	8 µs, no deglitch in LP_STANDBY state			400 kΩ SPU to VRTC, or 400 kΩ SPD to GND	None	GPIO3,4_SEL GPIO3,4_DEGLITCH_EN GPIO3,4_PU_PD_EN GPIO3,4_PU_SEL
GPIO1	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)_20mA}$, $V_{OH(VIO)}$	VINT	8 µs	VIO	PP[3] or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	GPIO1_DIR Input: GPIO1_DEGLITCH_EN GPIO1_PU_PD_EN GPIO1_PU_SEL Output: GPIO1_OD

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Table 6-2. Signal Descriptions (continued)

SIGNAL NAME	I/O	Threshold Level	INPUT TYPE SELECTION		OUTPUT TYPE SELECTION		Internal PU/ PD[2]	RECOMMENDED EXTERNAL PU/PD[2]	Control Register Bits
			Power Domain	DEGLITCH TIME[5]	Power Domain	Push-pull/ Open-drain[4]			
GPIO2	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)_20mA}$, $V_{OH(VIO)}$	VINT	8 µs	VIO	PP[3] or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	GPIO2_DIR Input: GPIO2_DEGLITCH_EN GPIO2_PU_PD_EN GPIO2_PU_SEL Output: GPIO2_OD
GPIO3	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)}$, $V_{OH(DIG)}$	VRTC	8 µs	VINT	PP or OD	400 kΩ SPU to VINT, or 400 kΩ SPD to GND	PU to VIO if Open-drain	GPIO3_DIR Input: GPIO3_DEGLITCH_EN GPIO3_PU_PD_EN GPIO3_PU_SEL Output: GPIO3_OD
GPIO4	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)}$, $V_{OH(DIG)}$	VRTC	8 µs	VINT	PP or OD	400 kΩ SPU to VINT, or 400 kΩ SPD to GND	PU to VIO if Open-drain	GPIO4_DIR Input: GPIO4_DEGLITCH_EN GPIO4_PU_PD_EN GPIO4_PU_SEL Output: GPIO4_OD
GPIO5	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)_20mA}$, $V_{OH(DIG)}$	VINT	8 µs	VINT	PP or OD	400 kΩ SPU to VINT, or 400 kΩ SPD to GND	PU to VIO if Open-drain	GPIO5_DIR Input: GPIO5_DEGLITCH_EN GPIO5_PU_PD_EN GPIO5_PU_SEL Output: GPIO5_OD
GPIO6	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(DIG)_20mA}$, $V_{OH(DIG)}$	VINT	8 µs	VINT	PP or OD	400 kΩ SPU to VINT, or 400 kΩ SPD to GND	PU to VIO if Open-drain	GPIO6_DIR Input: GPIO6_DEGLITCH_EN GPIO6_PU_PD_EN GPIO6_PU_SEL Output: GPIO6_OD

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Table 6-2. Signal Descriptions (continued)

SIGNAL NAME	I/O	Threshold Level	INPUT TYPE SELECTION		OUTPUT TYPE SELECTION		Internal PU/ PD[2]	RECOMMENDED EXTERNAL PU/PD[2]	Control Register Bits
			Power Domain	DEGLITCH TIME[5]	Power Domain	Push-pull/ Open-drain[4]			
GPIO7	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)}$, $V_{OH(VIO)}$	VINT	8 µs	VIO	PP[3] or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	GPIO7_DIR Input: GPIO7_DEGLITCH_EN GPIO7_PU_PD_EN GPIO7_PU_SEL Output: GPIO7_OD
GPIO8	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)}$, $V_{OH(VIO)}$	VINT	8 µs	VIO	PP[3] or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	GPIO8_DIR Input: GPIO8_DEGLITCH_EN GPIO8_PU_PD_EN GPIO8_PU_SEL Output: GPIO8_OD
GPIO9	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)}$, $V_{OH(VIO)}$	VINT	8 µs	VIO	P[3]P or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	GPIO9_DIR Input: GPIO9_DEGLITCH_EN GPIO9_PU_PD_EN GPIO9_PU_SEL Output: GPIO9_OD
GPIO10	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)}$, $V_{OH(VIO)}$	VINT	8 µs	VIO	PP[3] or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	GPIO10_DIR Input: GPIO10_DEGLITCH_EN GPIO10_PU_PD_EN GPIO10_PU_SEL Output: GPIO10_OD
GPIO11	Input/output	$V_{IL(DIG)}$, $V_{IH(DIG)}$, $V_{OL(VIO)}$, $V_{OH(VIO)}$	VINT	8 µs	VIO	PP[3] or OD	400 kΩ SPU to VIO, or 400 kΩ SPD to GND	PU to VIO if Open-drain	GPIO11_DIR Input: GPIO11_DEGLITCH_EN GPIO11_PU_PD_EN GPIO11_PU_SEL Output: GPIO11_OD

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Table 6-2. Signal Descriptions (continued)

SIGNAL NAME	I/O	Threshold Level	INPUT TYPE SELECTION		OUTPUT TYPE SELECTION		Internal PU/ PD[2]	RECOMMENDED EXTERNAL PU/PD[2]	Control Register Bits
			Power Domain	DEGLITCH TIME[5]	Power Domain	Push-pull/ Open-drain[4]			
SYNCCLKIN (Configurable function of GPIO10)[1]	Input	$V_{IL(DIG)}$, $V_{IH(DIG)}$	VINT	None			400 kΩ SPD to GND	None	GPIO10_SEL GPIO10_PU_PD_EN
SYNCCLKOUT (Configurable function of GPIO8, GPIO9, and GPIO10)[1]	Output	$V_{OL(VIO)}$, $V_{OH(VIO)}$			VIO	PP[3]	None	None	GPIO8_SEL GPIO9_SEL GPIO10_SEL
CLK32KOUT (Configurable function of GPIO3, GPIO4, GPIO8, and GPIO10)[1]	Output	GPIO3 or 4: $V_{OL(DIG)}$, $V_{OH(DIG)}$ GPIO8 or 10: $V_{OL(VIO)}$, $V_{OH(VIO)}$			GPIO3 or 4: VRTC GPIO8 or 10: VIO	PP[3]	None	None	GPIO3_SEL GPIO4_SEL GPIO8_SEL GPIO10_SEL

(1) Configurable function through NVM register setting.
(2) PU = Pullup, PD = Pulldown, SPU = Software-configurable pullup, SPD = Software-configurable pulldown.
(3) When VIO is not available, the push-pull pin must be configured as low output to minimize current leakage from the IO cell.
(4) PP = Push-pull, OD = Open-drain.
(5) Deglitch time is only applicable when option is enabled.
(6) NVM-configuration for I2C/SPI and SPMI cannot be overwritten during operation.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). Voltage level is with reference to the thermal/ground pad of the device.(1)

POS			MIN	MAX	UNIT
M1.1	Voltage on power supply sense pin	VSYS_SENSE	–0.3	12.5	V
M1.2	Voltage on overvoltage (OV) gate drive	OVPGDRV(2)	–0.3	12.5	V
M1.3	Voltage on OV protected supply input pin	VCCA(3)	–0.3	6	V
M1.4	Voltage on all buck supply voltage input pins	PVIN_Bx(3)	–0.3	6	V
M1.4a	Voltage difference between supply input pins	Between VCCA and each PVIN_Bx	–0.5	0.5	V
M1.5a	Voltage on all buck switch nodes	SW_Bx pins	–0.3	PVIN_Bx + 0.3 V, up to 6 V	V
M1.5b		SW_Bx pins, 10-ns transient	–2	10	V
M1.6	Voltage on all buck voltage sense nodes	FB_Bx	–0.3	4	V
M1.7	Voltage on all LDO supply voltage input pins	PVIN_LDOx(3)	–0.3	6	V
M1.8	Voltage on all LDO output pins	VOUT_LDOx	–0.3	PVIN_LDOx + 0.3 V, up to 6 V	V
M1.9	Voltage on internal LDO output pins	VOUT_LDOVINT, VOUT_LDOVRTC	–0.3	2	V
M1.10	Voltage on I/O supply pin	VIO_IN with respect to ground pad	–0.3	VCCA + 0.3 V, up to 6 V	V
M1.11	Voltage on logic pins (input or output) in VIO domain	I^2C and SPI pins, nRSTOUT, and nINT pins, and all GPIO output buffers except GPIO5 & GPIO6	–0.3	6	V
M1.12	Voltage on logic pins (input or output) in LDOVINT domain	GPIO5 & GPIO6, and all GPIO input buffers except GPIO3 & GPIO4	–0.3	6	V
M1.13	Voltage on logic pins (input) in LDOVRTC domain	GPIO3 & GPIO4	–0.3	6	V
M1.14	Voltage on logic pins (input or output) in VCCA domain	nPWRON/ENABLE & EN_DRV	–0.3	6	V
M1.15	Voltage on analog mux output pin	AMUXOUT	–0.3	VCCA + 0.3 V, up to 6 V	V
M1.16	Voltage on back-up power supply input	VBACKUP	–0.3	6	V
M1.17	Voltage on crystal oscillator pins	OSC32KIN, OSC32KOUT, & OSC32KCAP	–0.3	2	V
M1.18	Voltage on REFGND pins	REFGND1 & REFGND2	–0.3	0.3	V
M2.1a	Voltage rise slew-rate on input supply pins	VCCA, PVIN_Bx (voltage below 2.7 V)		60	mV/µs
M2.1b		VIO (only when VCCA < 2 V)		60	mV/µs
M2.2	Current through input protection FET	Between VSYS_SENSE & VCCA		15	A
M2.3a	Peak output current	All pins other than power resources		20	mA
M2.3b		Buck1/2/3/4 regulators: PVIN_Bx and SW_Bx per phase		5	A
M2.3c		Buck5 regulator: PVIN_B5 and SW_B5		3	A
M2.4a	Average output current, 100 k hour, T_J = 125℃	GPIOx pins, source current		3	mA
M2.4b		GPIO1/2/5/6, SDA_I2C1/SDI_SPI, EN_DRV, nINT, and nRSTOUT pins, sink current		8	mA
M2.4c		GPIO3/4/7/8/9/10/11 pins, sink current		3	mA
M2.4d		LDO1/2/3 regulators		350	mA
M2.4e		LDO4 regulators		210	mA
M3	Junction temperature, T_J		–45	160	°C
M4	Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) The voltage at OVPGDRV can exceed the 12 V absolute max condition for a short period of time in the case of steep rising of the voltage at the VSYS_SENSE pin, but must remain less than 14 V.

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(3) The voltage at VCCA and PVIN pins can exceed the 6 V absolute max condition for a short period of time, but must remain less than 8 V. VCCA at 8 V for a 100 ms duration is equivalent to approximately 8 hours of aging for the device at room temperature.

7.2 ESD Ratings

POS				VALUE	UNIT
M5	$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]	±2000	V
M6	$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011	±500	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device.

POS			MIN	NOM	MAX	UNIT
R1.1	Voltage on power supply sense pin	VSYS_SENSE	VCCA_UV		5.5	V
R1.2	Voltage on OV gate drive	OVPGDRV	0		12	V
R1.3	Voltage on OV protected supply input pin	VCCA	VCCA_UV		5.5	V
R1.4	Voltage on all buck supply input pins	PVIN_Bx	2.8		5.5	V
R1.4a	Voltage difference between supply input pins	Between VCCA and each PVIN_Bx	–0.2		0.2	V
R1.5	Voltage on all buck switch nodes	SW_Bx pins		3.3	5.5	V
R1.6	Voltage on all buck voltage sense nodes[(1)]	FB_Bx	0		$V_{OUT_Bn,max}$	V
R1.7a	Voltage on all LDO supply voltage input pins	PVIN_LDO12, PVIN_LDO3	1.2	3.3	VCCA	V
R1.7b		PVIN_LDO4	2.2	3.3	VCCA	V
R1.8	Voltage on all LDO output pins[(1)]	VOUT_LDOx	0		3.3	V
R1.9	Voltage on internal LDO output pins	VOUT_LDOVINT, VOUT_LDOVRTC	1.65		1.95	V
R1.10	Voltage on reference ground pins	REFGNDx	–0.3		0.3	V
R1.11	Voltage on I/O supply pin	V_{VIO_IN} = 1.8 V	1.7	1.8	1.9	V
R1.12		V_{VIO_IN} = 3.3 V	3.135	3.3	VCCA, up to 3.465V	
R1.13	Voltage on logic pins (input or output) in VIO domain	I^2C and SPI pins, nRSTOUT & nRSTOUT_SoC pins, GPIO1, GPIO2, GPIO7, GPIO8, GPIO9, GPIO10, and GPIO11 pins	0	V_{VIO_IN}	$V_{VIO_IN,max}$	V
R1.14	Voltage on backup supply pin	VBACKUP	0		Full Battery, up to 5.5V	V
R1.15	Voltage on crystal oscillator pins	OSC32KIN, OSC32KOUT, OSC32KCAP	0		$V_{OUT_LDOVRTC,max}$	V
R1.16	Voltage on logic pins (input or output) in LDOVRTC domain	With fail-safe[(3)]: GPIO3 & GPIO4	0	1.8	$V_{OUT_LDOVRTC,max}$	V
R1.17	Voltage on logic pins (input or output) in LDOVINT domain	With fail-safe[(3)]: GPIO5 & GPIO6	0	1.8	$V_{OUT_LDOVINT,max}$	V
R1.18	Voltage on logic pins (input or output) in VCCA domain	nPWRON/ENABLE, EN_DRV	0		V_{VCCA}	V
R1.19	Operating free-air temperature[(2)]		–40	25	125	°C
R1.20	Junction temperature, T_J	Operational	–40	25	150	°C

(1) The maximum output voltage of BUCK1 to BUCK5 and LDO1 to LDO4 can be reduced by an NVM setting to adopt the maximum voltage to the requirements (or maximum ratings) of the load. This protects the processor from exceeding the maximum ratings of the core voltage. The default value is defined in the nonvolatile memory (NVM) and can be updated by software through I2C/SPI interface after device start-up.
(2) Additional cooling strategies may be necessary to keep junction temperature at recommended limits.
(3) The input buffer of a fail-safe GPIO pin is isolated from its input signal. Therefore, the input voltage to a fail-safe pin can be as high as 5.5 V.

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7.4 Thermal Information

THERMAL METRIC[1]		TPS6594-Q1 RWE (VQFNP) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.

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7.5 General Purpose Low Drop-Out Regulators (LDO1, LDO2, LDO3)

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
1.1a	$C_{IN(LDOn)}$	Input filtering capacitance[1]	Connected from PVIN_LDOn to GND, Shared input tank capacitance (depending on platform requirements)	1	2.2		µF
1.1b	$C_{OUT(LDOn)}$	Output filtering effective capacitance[2]	Connected from VOUT_LDOn to GND	1	2.2	4	µF
1.1c	C_{ESR} (LDOn)	Filtering capacitor ESR[3]	1 MHz ≤ f ≤ 10 MHz			20	mΩ
1.1d	C_{OUT_TOTAL} (LDOn)	Total capacitance at output (Local + POL)[5]	1 MHz ≤ f ≤ 10 MHz			20	µF
1.2a	$V_{IN(LDOn)}$	LDO Input voltage	LDO mode	1.2		VCCA	V
1.2b	$V_{IN(LDOn)_bypass}$	LDO Input voltage in bypass mode	Bypass mode	1.7		VCCA, up to 3.6 V	V
1.3	$V_{OUT(LDOn)}$	LDO output voltage configurable range	LDO mode, with 50-mV steps	0.6		3.3	V
1.4a	$T_{DCOV(LDOn)}$	Total DC output voltage accuracy, including voltage references, DC load and line regulations, process and temperature variations	LDO mode, $V_{IN(LDOn)}$ - $V_{OUT(LDOn)}$ > 300 mV, $V_{OUT(LDOn)}$ ≥ 1V	–1%		1%	
1.4b			LDO mode, $V_{IN(LDOn)}$ - $V_{OUT(LDOn)}$ > 300 mV, $V_{OUT(LDOn)}$ < 1V	–10		10	mV
1.6	$I_{OUT(LDOn)}$	Output current	$V_{IN(LDOn)min}$ ≤ $V_{IN(LDOn)}$ ≤ $V_{IN(LDOn)max}$			500	mA
1.7	$I_{SHORT(LDOn)}$	LDO current limitation	LDO mode and bypass mode	700		1800	mA
1.8a	$I_{IN_RUSH(LDOn)}$	LDO inrush current	LDOn_BYPASS = 0			1500	mA
			LDOx_BYPASS = 1, with maximum 50-µF load connected to VOUT_LDOn			1500	
1.11a	$R_{DIS(LDOn)}$	Pulldown discharge resistance at LDO output	Active only when converter is disabled. Also applies to bypass mode. LDOn_PLDN = '00'	35	50	65	kΩ
1.11b	$R_{DIS(LDOn)}$	Pulldown discharge resistance at LDO output	Active only when converter is disabled. Also applies to bypass mode. LDOn_PLDN = '01'	60	125	200	Ω
1.11c	$R_{DIS(LDOn)}$	Pulldown discharge resistance at LDO output	Active only when converter is disabled. Also applies to bypass mode. LDOn_PLDN = '10'	120	250	400	Ω
1.11d	$R_{DIS(LDOn)}$	Pulldown discharge resistance at LDO output	Active only when converter is disabled. Also applies to bypass mode. LDOn_PLDN = '11'	240	500	800	Ω
1.12a	$PSRR_{VIN(LDOn)}$	Power supply ripple rejection from $V_{IN(LDOn)}$	f = 1 kHz, $V_{IN(LDOx)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 500 mA		60		dB
1.12b			f = 10 kHz, $V_{IN(LDOx)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 500 mA		50		
1.12c			f = 100 kHz, $V_{IN(LDOx)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 500 mA		35		
1.12d			f = 1 MHz, $V_{IN(LDOx)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 500 mA		24		
1.13	$I_{Qoff(LDOn)}$	Quiescent current, off mode	For LDO1, LDO2, & LDO3, VCCA = $V_{IN(LDOn)}$ = 3.3 V, T_J = 25°C			2	µA
1.14a	$I_{Qon(LDOn)}$	Quiescent current, on mode	LDOn_BYPASS = 0, I_{LOAD} = 0 mA , T_J = 25°C			78	µA
1.14b			LDOn_BYPASS = 1, I_{LOAD} = 0 mA , T_J = 25°C			68	
1.15	$T_{LDR(LDOn)}$	Transient load regulation, ΔV_{OUT} [4]	LDOn_BYPASS = 0, I_{OUT} = 20% to 80% of I_{OUTmax}, t_r = t_f = 1 µs		25		mV
1.16	$T_{BYPASS_to_LDO(LDOn)}$	Transient regulation due to Bypass Mode to Linear Mode Transition	$V_{IN(LDOn)}$ = 3.3V, I_{OUT}=$I_{OUT(LDOn)max}$, LDOn_BYPASS bit switches between 1 and 0		-2		mV
1.17	$V_{NOISE(LDOn)}$	RMS Noise	100 Hz < f ≤ 100 kHz, V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 300 mA		250		$µV_{RMS}$
1.18		Ripple	From the internal charge pump			5	mV_{PP}
1.19a	$R_{BYPASS(LDOn)}$	Bypass resistance	3.1 V ≤ $V_{IN(LDOn)}$ ≤ 3.5 V, PVIN_LDOx ≤ VCCA, I_{OUT} = 500 mA, LDOx_BYPASS = 1			200	mΩ
1.19c			1.7 V ≤ $V_{IN(LDOn)}$ ≤ 1.9 V, I_{OUT} = 500 mA, LDOn_BYPASS = 1			250	

7.5 General Purpose Low Drop-Out Regulators (LDO1, LDO2, LDO3) (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.20	$V_{TH_SC_RV(LDOn)}$	Threshold voltage for Short Circuit and Residual Voltage Detection	LDOn_EN = 0 and LDOn_RV_SEL = 1	140	150	160	mV
Timing Requirements							
19.1	$t_{on(LDOn)}$	Turn-on time	Time between enable of the LDOn to within OV/UV monitor level			500	µs
19.2a	$t_{ramp(LDOn)}$	Ramp-up slew rate	VOUT from 0.3 V to 90% of LDOn_VSET. LDOn_SLOW_RAMP = 0			25	mV/µs
19.2b			VOUT from 0.3 V to 90% of LDOn_VSET. LDOn_SLOW_RAMP = 1			3	mV/µs
19.3a	$t_{delay_OC(LDOn)}$	Over-current detection delay	Detection signal delay when I_{OUT} > ILIM			35	µs
19.3b	$t_{deglitch_OC(LDOn)}$	Over-current detection signal deglitch time	Digital deglitch time for the over-current detection signal	38		44	µs
19.4	$t_{latency_OC(LDOn)}$	Over-current signal total latency time	Total delay from I_{out} > ILIM to interrupt or PFSM trigger			79	µs

(1) Input capacitors must be placed as close as possible to the device pins.
(2) When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as CAPACITANCE. In order to meet the minimum capacitance requirement, the nominal value of the capacitor may have to be scaled accordingly to take the drop of capacitance into account for a given dc voltage at the outputs of regulators.
(3) Ceramic capacitors recommended
(4) Load transient voltage must be considered when selecting UV/OV threshold levels for the LDO output
(5) Additional capacitance, including local and POL, beyond the specified value can cause the LDO to become unstable

7.6 Low Noise Low Drop-Out Regulator (LDO4)

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
2.1a	$C_{IN(LDO4)}$	Input filtering capacitance(1)	Connected from PVIN_LDO4 to GND, Shared input tank capacitance (depending on platform requirements)	1	2.2		µF
2.1b	$C_{OUT(LDO4)}$	Output filtering capacitance(2)	Connected from VOUT_LDO4 to GND	1	2.2	4	µF
2.1c	$C_{ESR(LDO4)}$	Input and output capacitor ESR(3)	1 MHz ≤ f ≤ 10 MHz			20	mΩ
2.1d	$C_{OUT_TOTAL(LDO4)}$	Total capacitance at output (Local + POL)(4)	1 MHz ≤ f ≤ 10 MHz, fast ramp			15	µF
2.1e			1 MHz ≤ f ≤ 10 MHz, slow ramp			30	µF
2.2	$V_{IN(LDO4)}$	LDO Input voltage		2.2		5.5	V
2.3	$V_{OUT(LDO4)}$	LDO output voltage configurable range	with 25-mV steps	1.2		3.3	V
2.5	$T_{DCOV(LDO4)}$	Total DC output voltage accuracy, including voltage references, DC load and line regulations, process and temperature	$V_{IN(LDO4)}$ - $V_{OUT(LDO4)}$ > 300 mV	–1%		1%	
2.7	$I_{OUT(LDO4)}$	Output current	$V_{IN(LDO4)min}$ ≤ $V_{IN(LDO4)}$ ≤ $V_{IN(LDO4)max}$			300	mA
2.8	$I_{SHORT(LDO4)}$	LDO current limit		400		900	mA
2.9	$I_{IN_RUSH(LDO4)}$	LDO inrush current	V_{IN} = 3.3V when LDO is enabled			650	mA
2.13a	$PSRR_{(LDO4)}$	Power supply ripple rejection	f = 1 kHz, $V_{IN(LDO4)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 300 mA		70		dB
2.13b			f = 10 kHz, $V_{IN(LDO4)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 300 mA		70		
2.13c			f = 100 kHz, $V_{IN(LDO4)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 300 mA		62		
2.13d			f = 1 MHz, $V_{IN(LDO4)}$ = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 300 mA		15		

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7.6 Low Noise Low Drop-Out Regulator (LDO4) (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
2.12a	$R_{DIS(LDO4)}$	Pulldown discharge resistance at LDO output	Active only when converter is disabled, LDO4_PLDN = '00'	35	50	65	kΩ
2.12b			Active only when converter is disabled, LDO4_PLDN = '01'	60	125	200	Ω
2.12c			Active only when converter is disabled, LDO4_PLDN = '10'	120	250	400	Ω
2.12d			Active only when converter is disabled, LDO4_PLDN= '11'	240	500	800	Ω
2.14	$I_{Qoff(LDO4)}$	Leakage current in off mode	For all LDO regulators, VCCA = $V_{IN(LDO4)}$ = 3.8 V, T_J = 25°C			2	µA
2.15	$I_{Qon(LDO4)}$	Quiescent current	I_{LOAD} = 0 mA ,LDO4 under valid operating condition, T_J = 25°C			40	µA
2.16	$T_{LDR(LDO4)}$	Transient load regulation, ΔV_{OUT}	$V_{IN(LDO4)}$ = 3.3V, $V_{OUT(LDO4)}$ = 2.80V, I_{OUT} = 20% of I_{OUT_MAX} to 80% of I_{OUT_MAX} in 1us, $C_{OUT(LDO4)}$ = 2.2uF	–25		25	mV
2.17	$T_{LNR(LDO4)}$	Transient line regulation, ΔV_{OUT} / V_{OUT}	On mode, not under dropout condition, V_{IN} step = 600 mV_{PP}, t_r = t_f = 10 µs	-25		25	mV
2.18	$V_{NOISE(LDO4)}$	RMS Noise	100 Hz < f ≤ 100 kHz, V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 300 mA		15		$µV_{RMS}$
2.19	$V_{TH_SC_RV(LDO4)}$	Threshold voltage for Short Circuit and Residual Voltage Detection	LDO4_EN = 0 and LDO4_RV_SEL = 1	140	150	160	mV
Timing Requirements							
19.11a	$t_{START(LDO4)}$	Start Time	Time from completion of enable command to output voltage at 0.5 V			150	µs
19.12 a1	$t_{RAMP(LDO4)}$	Ramp Time	Measured from 0.5 V to 90% of LDO4_VSET. LDO4_SLOW_RAMP = 0			350	µs
19.12 a2			Measured from 0.5 V to 90% of LDO4_VSET. LDO4_SLOW_RAMP = 1			2.3	ms
19.12 b	$t_{RAMP_SLEW(LDO4)}$	Ramp up slew rate	VOUT from 0.5 V to 90% of LDO4_VSET. LDO4_SLOW_RAMP = 0			27	mV/µs
19.12c			VOUT from 0.5 V to 90% of LDO4_VSET. LDO4_SLOW_RAMP = 1			3	mV/µs
19.13 a	$t_{delay_OC(LDO4)}$	Over-current detection delay	Detection signal delay when I_{OUT} > ILIM			35	µs
19.13 b	$t_{deglitch_OC(LDO4)}$	Over-current detection signal deglitch time	Digital deglitch time for the over-current detection signal	38		44	µs
19.14	$t_{latency_OC(LDO4)}$	Over-current signal total latency time	Total delay from I_{out} > ILIM to interrupt or PFSM trigger			79	µs

(1) Input capacitors must be placed as close as possible to the device pins.
(2) When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as CAPACITANCE. In order to meet the minimum capacitance requirement, the nominal value of the capacitor may have to be scaled accordingly to take the drop of capacitance into account for a given dc voltage at the outputs of regulators.
(3) Ceramic capacitors recommended
(4) Additional capacitance, including local and POL, beyond the specified value can cause the LDO to become unstable

7.7 Internal Low Drop-Out Regulators (LDOVRTC, LDOVINT)

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
3.1	$C_{OUT(LDOinternal)}$	Output filtering capacitance(1)	Connected from VOUT_LDOx to GND	1	2.2	4	µF
3.3a	$V_{OUT(LDOVRTC)}$	LDO output voltage	LDOVRTC		1.8		V
3.3b	$V_{OUT(LDOVINT)}$		LDOVINT		1.8		V

7.7 Internal Low Drop-Out Regulators (LDOVRTC, LDOVINT) (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.7a	$I_{Qoff(LDOinternal)}$	Leakage current, off mode	LDOVRTC, VCCA = 3.3 V, T_J = 25℃			2	µA
3.7b			LDOVINT, VCCA = 3.3 V, T_J = 25℃			2	
3.8a	$I_{Qon(LDOinternal)}$	Quiescent current, on mode	LDOVRTC under valid operating condition, I_{LOAD} = 0 mA		3	10	µA
3.8b			LDOVINT under valid operating condition, I_{LOAD} = 0 mA		3	10	
3.9	$R_{DIS(LDOinterna;)}$	Pulldown discharge resistance at LDO output	LDOx disabled	60	125	190	Ω

(1) When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as CAPACITANCE. In order to meet the minimum capacitance requirement, the nominal value of the capacitor may have to be scaled accordingly to take the drop of capacitance into account for a given DC voltage at the outputs of regulators.

7.8 BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators

Over operating free-air temperature range (unless otherwise noted). Voltage level are referenced to the thermal/ground pad of the device except for V_{OUT_Bn} in multiphase configurations, in which case, the voltage level is referenced to the negative FB_Bn pin of the differential pair.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics - Output Voltage							
4.1a	V_{VOUT_Bn}	Output voltage configurable range	1-phase output	0.3		3.34	V
4.1b			Multi-phase output	0.3		1.9	V
4.2a	$V_{VOUT_Bn_Step}$	Output voltage configurable step size	0.3 V ≤ V_{VOUT_Bn} < 0.6 V		20		mV
4.2b			0.6 V ≤ V_{VOUT_Bn} < 1.1 V		5		mV
4.2c			1.1 V ≤ V_{VOUT_Bn} < 1.66 V		10		mV
4.2d			1.66 V ≤ V_{VOUT_Bn} < 3.34 V		20		mV
4.4	$V_{DROPOUT_Bn}$	Input and output voltage difference	Minimum voltage between PVIN_Bn and VOUT_Bn to fulfill the electrical characteristics	0.7			V
4.5a	$V_{OUT_SR_Bn}$	Output voltage slew-rate configurable range(5) (8)	BUCKn_SLEW_RATE[2:0] = 000b	26.6	33.3	36.6	mV/µs
4.5b			BUCKn_SLEW_RATE[2:0] = 001b	17	20	22	mV/µs
4.5c			BUCKn_SLEW_RATE[2:0] = 010b	9	10	11	mV/µs
4.5d			BUCKn_SLEW_RATE[2:0] = 011b	4.5	5	5.5	mV/µs
4.5e			BUCKn_SLEW_RATE[2:0] = 100b	2.25	2.5	2.75	mV/µs
4.5f			BUCKn_SLEW_RATE[2:0] = 101b	1.12	1.25	1.38	mV/µs
4.5g			BUCKn_SLEW_RATE[2:0] = 110b	0.56	0.625	0.69	mV/µs
4.5h			BUCKn_SLEW_RATE[2:0] = 111b	0.281	0.3125	0.344	mV/µs
Electrical Characteristics - Output Current, Limits and Thresholds							
4.7a	I_{OUT_Bn}	Output current(3) (4)	1-phase, BUCK5			2	A
4.7b			1-phase, BUCK4			4	A
4.7c			1-phase, BUCK1, BUCK2, BUCK3			3.5	A
4.7d			2-phase			7	A
4.7e			3-phase			10.5	A
4.7f			4-phase			14	A
4.8a	$I_{OUT_MP_Bal}$	Current balancing for multi-phase output	Mismatch between phase current and average phase current, 1A/phase < I_{OUT_Bn} ≤ 2A / phase			20%	
4.8b			Mismatch between phase current and average phase current, I_{OUT_Bn} > 2 A / phase			10%	
4.9a	$I_{LIM_FWD_PEAK_Range}$	Forward current limit (peak during each switching cycle) configurable range	BUCK5	2.5		3.5	A
4.9b			BUCK1, BUCK2, BUCK3, BUCK4	2.5		5.5	A
4.10	$I_{LIM_FWD_PEAK_Step}$	Forward current limit step Size			1		A

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7.8 BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level are referenced to the thermal/ground pad of the device except for V_{OUT_Bn} in multiphase configurations, in which case, the voltage level is referenced to the negative FB_Bn pin of the differential pair.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.11a	$I_{LIM_FWD_PEAK_Accuracy}$	Forward current limit accuracy	I_{LIM_FWD} = 2.5 A or 3.5 A, 3.0 V ≤ V_{PVIN_Bn} ≤ 5.5 V	-0.55		0.55	A
4.11b			I_{LIM_FWD} = 4.5 A, 3.0 V ≤ V_{PVIN_Bn} ≤ 5.5 V, BUCK1, BUCK2, BUCK3, BUCK4	-0.55		0.55	A
4.11c			I_{LIM_FWD} = 5.5 A, 3.0 V ≤ V_{PVIN_Bn} ≤ 4.5 V, BUCK1, BUCK2, BUCK3, BUCK4	–15%		10%	
4.11d			I_{LIM_FWD} = 5.5 A, 4.5 V ≤ V_{PVIN_Bn} ≤ 5.5 V, BUCK1, BUCK2, BUCK3, BUCK4	–10%		10%	
4.12	I_{LIM_NEG}	Negative current limit (peak during each switching cycle)		1.5	2	2.8	A
4.15a	I_{ADD}	Phase adding level (multi-phase rails)	From 1-phase to 2-phase		2.0		A
4.15b			From 2-phase to 3-phase		4.0		A
4.15c			From 3-phase to 4-phase		6.0		A
4.16a	I_{SHED}	Phase shedding level (multi-phase rails)	From 2-phase to 1-phase		1.3		A
4.16b			From 3-phase to 2-phase		2.7		A
4.16c			From 4-phase to 3-phase		3.5		A
4.16d	I_{SHED_Hyst}	Phase shedding hysteresis (multi-phase rails)	Hysteresis from 2-phase to 1-phase		0.7		A
4.16e			Hysteresis from 3-phase to 2-phase		1.3		A
4.16f			Hysteresis from 4-phase to 3-phase		2.5		A
Electrical Characteristics - Current Consumption, On-Resistance, and Output Pulldown Resistance							
4.17	I_{off}	Shutdown current, BUCKn disabled	VCCA = V_{PVIN_Bn} = 3.3 V. T_J = 25°C		1		µA
4.18a	I_{Q_AUTO}	Auto mode quiescent current	I_{OUT_Bn} = 0 mA, not switching, first single phase or primary phase in multi-phase configuration, T_J = 25°C		80		µA
4.18b			I_{OUT_Bn} = 0 mA, not switching, additional single phase or primary phase in multi-phase configuration, T_J = 25°C		60		µA
4.18c			I_{OUT_Bn} = 0 mA, not switching, secondary/ tertiary/quaternary phase in multi-phase configuration, T_J = 25°C		30		µA
4.19a	$R_{DS(ON)\ HS\ FET}$	On-resistance, high-side FET	I_{OUT_Bn} = 1 A, BUCK5		55	110	mΩ
4.19b			I_{OUT_Bn} = 1 A, BUCK1, BUCK2, BUCK3, BUCK4		52	100	mΩ
4.20a	$R_{DS(ON)\ LS\ FET}$	On-resistance, low-side FET	I_{OUT_Bn} = 1 A, BUCK5		41	70	mΩ
4.20b			I_{OUT_Bn} = 1 A, BUCK1, BUCK2, BUCK3, BUCK4		30	55	mΩ
4.21	R_{DIS_Bn}	Output pulldown discharge resistance	Regulator disabled, per phase, BUCKn_PLDN = 1	50	100	150	Ω
4.22	R_{SW_SC}	Short circuit detection resistance threshold at the SW pin		2	4.5	20	Ω
Electrical Characteristics - 4.4 MHz V_{OUT} Less than 1.9 V, Multiphase or High C_{OUT} Single Phase							
4.31	V_{PVIN_Bn}	Input voltage range		3.0	3.3	5.5	V
4.32	V_{VOUT_Bn}	Output voltage configurable range		0.3		1.9	V
4.33a	C_{IN_Bn}	Input filtering capacitance(1)		3	22		µF
4.33b	$C_{OUT\text{-}Local(Buckn)}$	Output capacitance, local(2)	Per phase	10	22		µF
4.33c	$C_{OUT\text{-}TOTAL_Bn}$	Output capacitance, total (local and POL)(2)	Per phase	70		250	µF
4.34a	L_{Bn}	Power inductor	Inductance	154	220	286	nH
4.34b			DCR		10		mΩ
4.35	I_{Q_PWM}	PWM mode Quiescent current	Per phase, I_{OUT_Bn} = 0 mA		19		mA

7.8 BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level are referenced to the thermal/ground pad of the device except for V_{OUT_Bn} in multiphase configurations, in which case, the voltage level is referenced to the negative FB_Bn pin of the differential pair.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.160a	$V_{OUT_DC_Bx}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations and temperature	V_{VOUT_Bx} < 1 V, PWM mode	–10		10	mV
4.160b			V_{VOUT_Bx} ≥ 1 V, PWM mode	–1%		1%	
4.160c			V_{VOUT_Bx} < 1 V, PFM mode	–20		25	mV
4.160d			V_{VOUT_Bx} ≥ 1 V, PFM mode	-1% - 10 mV		1% + 15 mV	
4.37a	T_{LDSR_MP}	Transient load step response[7]	0.3 V ≤ V_{VOUT_Bn} < 0.6 V, I_{OUT_Bn} = 1 mA to 400 mA / phase, t_r = t_f = 1 µs, PWM mode		10		mV
4.37ba			0.6 V ≤ V_{VOUT_Bn} < 1.5 V, I_{OUT_Bn} = 1 mA to 1.75A / phase, t_r = t_f = 1 µs, PWM mode, BUCK1, BUCK2, BUCK3, BUCK4		15		mV
4.37bb			0.6 V ≤ V_{VOUT_Bn} < 1.5 V, I_{OUT_Bn} = 1 mA to 1 A / phase, t_r = t_f = 1 µs, PWM mode, BUCK5		15		mV
4.37ca			1.5 V ≤ V_{VOUT_Bn} ≤ 1.9 V, I_{OUT_Bn} = 1 mA to 1.75 A / phase, t_r = t_f = 1 µs, PWM mode, BUCK1, BUCK2, BUCK3, BUCK4		1.2%		
4.37cb			1.5 V ≤ V_{VOUT_Bn} ≤ 1.9 V, I_{OUT_Bn} = 1 mA to 1 A / phase, t_r = t_f = 1 µs, PWM mode, BUCK5		1.0%		
4.38	T_{LNSR}	Transient line response	V_{PVIN_Bn} stepping from 3 V to 3.5 V, t_r = t_f = 10 µs, I_{OUT_Bn} = $I_{OUT(max)}$	-20	±5	20	mV
4.39a	V_{OUT_Ripple}	Ripple voltage[7]	PWM mode, 1-phase		3		mV_{PP}
4.39b			PFM mode		15	25	mV_{PP}
4.40	$V_{TH_SC_RV(Bn)}$	Threshold voltage for Short Circuit and Residual Voltage Detection	Bn_EN = 0 and BUCKn_RV_SEL = 1	140	150	160	mV
4.102	$I_{PWM-PFM}$	PWM to PFM switch current threshold[6]	Auto mode, V_{PVIN_Bn} = 3.3 V, V_{VOUT_Bn} = 1.0 V		400		mA
4.101	$I_{PFM-PWM}$	PFM to PWM switch current threshold[6]	Auto mode, V_{PVIN_Bn} = 3.3 V, V_{VOUT_Bn} = 1.0 V		500		mA
4.103	$I_{PWM-PFM_HYST}$	PWM to PFM switch current hysteresis	Auto mode, V_{PVIN_Bn} = 3.3 V, V_{VOUT_Bn} = 1.0 V		100		mA
Electrical Characteristics - DDR VTT Termination, 2.2 MHz Single Phase Only							
4.41	V_{PVIN_Bn}	Input voltage range		2.8	3.3	5.5	V
4.42	$I_{OUT_Bn_SINK}$	Current sink		–1			A
4.43	V_{VOUT_Bn}	Output voltage programmable range		0.5		0.7	V
4.44a	C_{IN_Bn}	Input filtering capacitance[1]		3	22		µF
4.44b	$C_{OUT-TOTAL_Bn}$	Output capacitance, local[2]		10	22		µF
4.44c	$C_{OUT-TOTAL_Bn}$	Output capacitance, total (local and POL)[2]		35		65	µF
4.45a	L_{Bn}	Power inductor	Inductance	329	470	611	nH
4.45b			DCR		10		mΩ
4.46a	I_{Q_PWM}	PWM mode Quiescent current	I_{OUT_Bn} = 0 mA		19		mA
4.161a	$V_{OUT_DC_Bx}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations and temperature	V_{VOUT_Bx} < 1 V, PWM mode	–10		10	mV
4.161b			V_{VOUT_Bx} ≥ 1 V, PWM mode	–1%		1%	
4.48	T_{LDSR_MP}	Transient load step response[7]	0.5 V ≤ V_{VOUT_Bn} ≤ 0.7 V, I_{OUT_Bn} = -1 mA to -1000 mA, t_r = t_f = 1 µs, PWM mode		15		mV
4.49	T_{LNSR}	Transient line response	V_{PVIN_Bn} stepping from 3 V to 3.5 V, t_r = t_f = 10 µs, I_{OUT_Bn} = $I_{OUT_Bn(max)}$	-20	±5	20	mV
4.50	V_{OUT_Ripple}	Ripple voltage[7]	PWM mode		3	6	mV_{PP}
Electrical Characteristics - 4.4 MHz V_{OUT} Less than 1.9 V, Low C_{OUT}, Single Phase Only							
4.51	V_{PVIN_Bn}	Input voltage range		3.0	3.3	5.5	V
4.52	V_{VOUT_Bn}	Output voltage configurable range		0.3		1.9	V
4.53a	C_{IN_Bn}	Input filtering capacitance[1]		3	22		µF
4.53b	$C_{OUT-Local_Bn}$	Output capacitance, local[2]		10	22		µF

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7.8 BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level are referenced to the thermal/ground pad of the device except for V_{OUT_Bn} in multiphase configurations, in which case, the voltage level is referenced to the negative FB_Bn pin of the differential pair.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.53c	$C_{OUT\text{-}TOTAL_Bn}$	Output capacitance, total (local and POL)[2]		25		100	µF
4.54a	L_{Bn}	Power inductor	Inductance	154	220	286	nH
4.54b			DCR		10		mΩ
4.55a	I_{Q_PWM}	PWM mode Quiescent current	I_{OUT_Bn} = 0 mA, BUCK1, BUCK2, BUCK3, BUCK4		19		mA
4.55b			I_{OUT_Bn} = 0 mA, BUCK5		19		mA
4.162a	$V_{OUT_DC_Bx}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations and temperature	V_{VOUT_Bx} < 1 V, PWM mode	–10		10	mV
4.162b			V_{VOUT_Bx} ≥ 1 V, PWM mode	–1%		1%	
4.162c			V_{VOUT_Bx} < 1 V, PFM mode	–20		35	mV
4.162d			V_{VOUT_Bx} ≥ 1 V, PFM mode	-1% - 10 mV		1% + 25 mV	
4.57a	T_{LDSR_MP}	Transient load step response[7]	0.3 V ≤ V_{VOUT_Bn} < 0.6 V, I_{OUT_Bn} = 1 mA to 200 mA / phase, t_r = t_f = 1 µs, PWM mode		15		mV
4.57b			0.6 V ≤ V_{VOUT_Bn} < 1.5 V, I_{OUT_Bn} = 1 mA to 1 A / phase, t_r = t_f = 1 µs, PWM mode		15		mV
4.57c			1.5 V ≤ V_{VOUT_Bn} ≤ 1.9 V, I_{OUT_Bn} = 1 mA to 1 A / phase, t_r = t_f = 1 µs, PWM mode		1.5%		
4.58	T_{LNSR}	Transient line response	V_{PVIN_Bn} stepping from 3 V to 3.5 V, t_r = t_f = 10 µs, I_{OUT_Bn}= $I_{OUT_Bn(max)}$	-20	±5	20	mV
4.59a	V_{OUT_Ripple}	Ripple voltage[7]	PWM mode		5	8	mV_{PP}
4.59b			PFM mode		15	50	mV_{PP}
4.111	$I_{PFM\text{-}PWM}$	PFM to PWM switch current threshold[6]	Auto mode, V_{PVIN_Bn} = 3.3 V, V_{VOUT_Bn} = 1.0 V		500		mA
4.112	$I_{PWM\text{-}PFM}$	PWM to PFM switch current threshold[6]	Auto mode, V_{PVIN_Bn} = 3.3 V, V_{VOUT_Bn} = 1.0 V		420		mA
4.113	$I_{PWM\text{-}PFM_HYST}$	PWM to PFM switch current hysteresis	Auto mode, V_{PVIN_Bn} = 3.3 V, V_{VOUT_Bn} = 1.0 V		100		mA
Electrical Characteristics - 4.4 MHz V_{OUT} Greater than 1.7 V, Single Phase Only							
4.61	V_{PVIN_Bn}	Input voltage range		4.5	5	5.5	V
4.62	$I_{OUT_Bn_4.4_HV_OUT}$	Output current				2.5	A
4.63	V_{VOUT_Bn}	Output voltage configurable range		1.7		3.34	V
4.64a	C_{IN_Bn}	Input filtering capacitance[1]		3	22		µF
4.64b	$C_{OUT\text{-}Local_Bn}$	Output capacitance, local[2]		10	22		µF
4.64c	$C_{OUT\text{-}TOTAL_Bn}$	Output capacitance, total (local and POL)[2]		50		150	µF
4.65a	L_{Bn}	Power inductor	Inductance	329	470	611	nH
4.65b			DCR		10		mΩ
4.66a	I_{Q_PWM}	PWM mode Quiescent current	I_{OUT_Bn} = 0 mA		19		mA
4.163a	$V_{OUT_DC_Bx}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations and temperature	V_{VOUT_Bx} < 1 V, PWM mode	–10		10	mV
4.163b			V_{VOUT_Bx} ≥ 1 V, PWM mode	–1%		1%	
4.163c			V_{VOUT_Bx} < 1 V, PFM mode	–20		25	mV
4.163d			V_{VOUT_Bx} ≥ 1 V, PFM mode	-1% - 10 mV		1% + 15 mV	
4.68	T_{LDSR_SP}	Transient load step response[7]	1.7 V ≤ V_{VOUT_Bn} ≤ 3.34 V, I_{OUT_Bn} = 1 mA to 1 A/phase, t_r = t_f = 1 µs, PWM mode		1.5%		
4.69	T_{LNSR}	Transient line response	V_{PVIN_Bn} stepping from 4.7 V to 5.2 V, t_r = t_f = 10 µs, I_{OUT_Bn} = $I_{OUT_Bn(max)}$	-20	±5	20	mV
4.70a	V_{OUT_Ripple}	Ripple voltage[7]	PWM mode		3	7	mV_{PP}
4.70b			PFM mode		15	25	mV_{PP}

7.8 BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level are referenced to the thermal/ground pad of the device except for V_{OUT_Bn} in multiphase configurations, in which case, the voltage level is referenced to the negative FB_Bn pin of the differential pair.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.121	$I_{PFM-PWM}$	PFM to PWM switch current threshold(6)	Auto mode, V_{PVIN_Bn} = 5 V, V_{VOUT_Bn} = 1.8 V		400		mA
4.122	$I_{PWM-PFM}$	PWM to PFM switch current threshold(6)	Auto mode, V_{PVIN_Bn} = 5 V, V_{VOUT_Bn} = 1.8 V		370		mA
4.123	$I_{PWM-PFM_HYST}$	PWM to PFM switch current hysteresis	Auto mode, V_{PVIN_Bn} = 5 V, V_{VOUT_Bn} = 1.8 V		30		mA
Electrical Characteristics - 2.2 MHz Full V_{OUT} Range and V_{IN} Greater than 4.5 V, Single Phase Only							
4.71	V_{PVIN_Bn}	Input voltage range		4.5	5	5.5	V
4.72	V_{VOUT_Bn}	Output voltage configurable range		0.3		3.34	V
4.73a	C_{IN_Bn}	Input filtering capacitance(1)		3	22		µF
4.73b	$C_{OUT-Local_Bn}$	Output capacitance, local(2)		10	22		µF
4.73c	$C_{OUT-TOTAL_Bn}$	Output capacitance, total (local and POL)(2)		100		1000	µF
4.74a	L_{Bn}	Power inductor	Inductance	700	1000	1300	nH
4.74b			DCR		10		mΩ
4.75	I_{Q_PWM}	PWM mode Quiescent current	I_{OUT_Bn} = 0 mA		13		mA
4.164a	$V_{OUT_DC_Bx}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations and temperature	V_{VOUT_Bx} < 1 V, PWM mode	–10		10	mV
4.164b			V_{VOUT_Bx} ≥ 1 V, PWM mode	–1%		1%	
4.164c			V_{VOUT_Bx} < 1 V, PFM mode	–20		25	mV
4.164d			V_{VOUT_Bx} ≥ 1 V, PFM mode	-1% - 10 mV		1% + 15 mV	
4.77a	T_{LDSR_MP}	Transient load step response(7)	0.3 V ≤ V_{VOUT_Bn} < 0.6 V, I_{OUT_Bn} = 1 mA to 400 mA / phase, t_r = t_f = 1 µs, PWM mode		15		mV
4.77b			0.6 V ≤ V_{VOUT_Bn} < 1.5 V, I_{OUT_Bn} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		15		mV
4.77c			1.5 V ≤ V_{VOUT_Bn} ≤ 3.34 V, I_{OUT_Bn} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		1.5%		
4.78	T_{LNSR}	Transient line response	V_{PVIN_Bn} stepping from 4.7 V to 5.2 V, t_r = t_f = 10 µs, I_{OUT_Bn}= $I_{OUT_Bn(max)}$	-20	±5	20	mV
4.79a	V_{OUT_Ripple}	Ripple voltage(7)	PWM mode		3	7.5	mV_{PP}
4.79b			PFM mode		15	25	mV_{PP}
4.131	$I_{PFM-PWM}$	PFM to PWM switch current threshold(6)	Auto mode, V_{PVIN_Bn} = 5 V, V_{VOUT_Bn} = 1.0V		310		mA
4.132	$I_{PWM-PFM}$	PWM to PFM switch current threshold(6)	Auto mode, V_{PVIN_Bn} = 5 V, V_{VOUT_Bn} = 1.0V		290		mA
4.133	$I_{PWM-PFM_HYST}$	PWM to PFM switch current hysteresis	Auto mode, V_{PVIN_Bn} = 5 V, V_{VOUT_Bn} = 1.0V		20		mA
Electrical Characteristics - 2.2 MHz V_{OUT} Less than 1.9 V Multiphase or Single Phase							
4.81	V_{PVIN_Bn}	Input voltage range		3.0	3.3	5.5	V
4.82	V_{VOUT_Bn}	Output voltage configurable range		0.3		1.9	V
4.83a	C_{IN_Bn}	Input filtering capacitance(1)		3	22		µF
4.83b	$C_{OUT-Local_Bn}$	Output capacitance, local(2)	Per phase	10	22		µF
4.83c	$C_{OUT-TOTAL_Bn}$	Output capacitance, total (local and POL)(2)	Per phase	100		1000	µF
4.84a	L_{Bn}	Power inductor	Inductance	329	470	611	nH
4.84b			DCR		10		mΩ
4.85	I_{Q_PWM}	PWM mode Quiescent current	I_{OUT_Bn} = 0 mA		13		mA
4.165a	$V_{OUT_DC_Bx}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations and temperature	V_{VOUT_Bx} < 1 V, PWM mode	–10		10	mV
4.165b			V_{VOUT_Bx} ≥ 1 V, PWM mode	–1%		1%	
4.165c			V_{VOUT_Bx} < 1 V, PFM mode	–20		25	mV
4.165d			V_{VOUT_Bx} ≥ 1 V, PFM mode	-1% - 10 mV		1% + 15 mV	

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7.8 BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level are referenced to the thermal/ground pad of the device except for V_{OUT_Bn} in multiphase configurations, in which case, the voltage level is referenced to the negative FB_Bn pin of the differential pair.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.87a	T_{LDSR_MP}	Transient load step response[7]	0.3 V ≤ V_{VOUT_Bn} < 0.6 V, I_{OUT_Bn} = 1 mA to 400 mA / phase, t_r = t_f = 1 µs, PWM mode		5		mV
4.87b			0.6 V ≤ V_{VOUT_Bn} < 1.5 V, I_{OUT_Bn} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		15		mV
4.87c			1.5 V ≤ V_{VOUT_Bn} ≤ 1.9 V, I_{OUT_Bn} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		1.0%		
4.88	T_{LNSR}	Transient line response	V_{PVIN_Bn} stepping from 4.7 V to 5.2 V, t_r = t_f = 10 µs, I_{OUT_Bn}= $I_{OUT_Bn(max)}$	-20	±5	20	mV
4.89a	V_{OUT_Ripple}	Ripple voltage[7]	PWM mode, 1-phase		3	5	mV_{PP}
4.89b			PFM mode		15	25	mV_{PP}
4.141	$I_{PFM-PWM}$	PFM to PWM switch current threshold[6]	Auto mode, V_{PVIN_Bn} = 3.3 V, V_{VOUT_Bn} = 1.0V		500		mA
4.142	$I_{PWM-PFM}$	PWM to PFM switch current threshold[6]	Auto mode, V_{PVIN_Bn} = 3.3 V, V_{VOUT_Bn} = 1.0V		400		mA
4.143	$I_{PWM-PFM_HYST}$	PWM to PFM switch current hysteresis	Auto mode, V_{PVIN_Bn} = 3.3 V, V_{VOUT_Bn} = 1.0V		100		mA
Electrical Characteristics - 2.2 MHz Full V_{OUT} and Full V_{IN} Range, Single Phase Only							
4.91	V_{PVIN_Bn}	Input voltage range		2.8	3.3	5.5	V
4.92	V_{VOUT_Bn}	Output voltage configurable range		0.3		3.34	V
4.93a	C_{IN_Bn}	Input filtering capacitance[1]		3	22		µF
4.93b	$C_{OUT-Local_Bn}$	Output capacitance, local[2]		10	22		µF
4.93c	$C_{OUT-TOTAL_Bn}$	Output capacitance, total (local and POL)[2]		100		500	µF
4.94a	L_{Bn}	Power inductor	Inductance	700	1000	1300	nH
4.94b			DCR		10		mΩ
4.95	I_{Q_PWM}	PWM mode Quiescent current	I_{OUT_Bn} = 0 mA, BUCK1, BUCK2, BUCK3, BUCK4		13		mA
4.166a	$V_{OUT_DC_Bx}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations and temperature	V_{VOUT_Bx} < 1 V, PWM mode	–10		10	mV
4.166b			V_{VOUT_Bx} ≥ 1 V, PWM mode	–1%		1%	
4.166d			V_{VOUT_Bx} ≥ 1 V, PFM mode	-1% - 10 mV		1% + 15 mV	
4.166c			V_{VOUT_Bx} < 1 V, PFM mode	–20		25	mV
4.97a	T_{LDSR_SP}	Transient load step response[7]	0.3 V ≤ V_{VOUT_Bn} < 0.6 V, I_{OUT_Bn} = 1 mA to 400 mA / phase, t_r = t_f = 1 µs, PWM mode		35		mV
4.97b			0.6 V ≤ V_{VOUT_Bn} < 1.0 V, I_{OUT_Bn} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		17		mV
4.97c			1.0 V ≤ V_{VOUT_Bn} ≤ 3.34 V, I_{OUT_Bn} = 1 mA to 2 A / phase, t_r = t_f = 1 µs, PWM mode		3.5%		
4.98	T_{LNSR}	Transient line response	V_{PVIN_Bn} stepping from 3 V to 3.5 V, t_r = t_f = 10 µs, I_{OUT_Bn} = $I_{OUT_Bn(max)}$	-20	±5	20	mV
4.99a	V_{OUT_Ripple}	Ripple voltage[7]	PWM mode		3	7.5	mV_{PP}
4.99b			PFM mode		15	25	mV_{PP}
4.151	$I_{PFM-PWM}$	PFM to PWM switch current threshold[6]	Auto mode, V_{PVIN_Bn} = 3.3 V, V_{VOUT_Bn} = 1.0V		290		mA
4.152	$I_{PWM-PFM}$	PWM to PFM switch current threshold[6]	Auto mode, V_{PVIN_Bn} = 3.3 V, V_{VOUT_Bn} = 1.0V		230		mA
4.153	$I_{PWM-PFM_HYST}$	PWM to PFM switch current hysteresis	Auto mode, V_{PVIN_Bn} = 3.3 V, V_{VOUT_Bn} = 1.0V		50		mA
Switching Characteristics							

7.8 BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level are referenced to the thermal/ground pad of the device except for V_{OUT_Bn} in multiphase configurations, in which case, the voltage level is referenced to the negative FB_Bn pin of the differential pair.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
20.1a	f_{SW}	Steady state switching frequency in PWM mode (NVM configurable)	2.2 MHz setting, internal clock	2	2.2	2.4	MHz
20.1b			4.4 MHz setting, internal clock	4	4.4	4.8	MHz
20.1d			2.2 MHz setting, internal clock, spread spectrum	1.76	2.2	2.64	MHz
20.1e			4.4 MHz setting, internal clock, spread spectrum	3.5	4.4	5.3	MHz
20.1f			2.2 MHz setting, synchronized to external clock	1.76	2.2	2.64	MHz
20.1g			4.4 MHz setting, synchronized to external clock	3.5	4.4	5.3	MHz
20.2a	f_{SW_max}	Automatic maximum switching frequency scaling in PWM mode	0.6 V ≤ V_{VOUT_Bn}		4.4		MHz
20.2b			0.3 V ≤ V_{VOUT_Bn} < 0.6 V		2.2		MHz
Timing Requirements							
20.3	t_{settle_Bn}	Settling time after voltage scaling	From end of voltage ramp to within 15mV from target $V_{OUT_DC_Bx}$			105	µs
20.4	$t_{startup_Bn}$	Start-up delay	From enable to start of output voltage rise	100	150	218	µs
20.5a	t_{delay_OC}	Over-current detection delay	Peak current limit triggering during every switching cycle			7	µs
20.5b	$t_{deglitch_OC}$	Over-current detection signal deglitch time	Digital deglitch time for detected signal. Time duration to filter out short positive and negative pulses	19		23	µs
20.6	$t_{latency_OC}$	Over-current signal latency time from detection	Total delay from over-current detection to interrupt or PFSM trigger			30	µs

(1) Input capacitors must be placed as close as possible to the device pins.
(2) When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as CAPACITANCE. In order to meet the minimum capacitance requirement, the nominal value of the capacitor may have to be scaled accordingly to take the drop of capacitance into account for a given DC voltage at the outputs of regulators.
(3) The maximum output current can be limited by the forward current limit. The maximum output current is also limited by the junction temperature and maximum average current over lifetime. The power dissipation inside the die increases the junction temperature and limits the maximum current depending on the length of the current pulse, efficiency, board and ambient temperature.
(4) Additional cooling strategies may be necessary to keep the device junction temperature at recommended limits with large output current.
(5) SLEW_RATEx[2:0] register default comes from NVM memory, and can be re-configured by the MCU. Output capacitance, forward and negative current limits and load current may limit the maximum and minimum slew rates.
(6) The final PFM-to-PWM and PWM-to-PFM switchover current varies slightly and is dependent on the output voltage, input voltage, and the inductor current level. The BUCK Regulator does not switch over from PWM to PFM for Fsw=2.2MHz and VOUT < 0.5V
(7) Please refer to the applications section of the datasheet regarding the power delivery network (PDN) used for the transient load step and output ripple test conditions. All ripple specs are defined across POL capacitor in the described PDN.
(8) The 33.3 mV/µs slew-rate setting is not recommended for L_{Bx} ≥ 1 µH, as this can trigger OV detection due to larger overshoot at the buck output.

7.9 Reference Generator (BandGap)

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
5.1		Max capacitance at AMUX pin	Capacitance between AMUXOUT pin and thermal/ ground pad			100	pF
5.2		Output voltage	Measured at the AMUXOUT pin	1.17	1.2	1.23	V
Timing Requirements							
21.1	t_{SU_REF}	Start-up time	From AMUXOUT_EN=1 to the time bandgap voltage settles		30		µs

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7.10 Monitoring Functions

Over operating free-air temperature range (unless otherwise noted). Voltage level is measured with reference to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics: BUCK REGULATORS OUTPUT							
7.1a	$V_{BUCK_OV_TH}$	Overvoltage monitoring for BUCK output, threshold accuracy, $V_{OUT_Bn} \geq 1$ V(1)	BUCKn_OV_THR = 0x0	2%	3%	4%	
7.1b			BUCKn_OV_THR = 0x1	2.5%	3.5%	4.5%	
7.1c			BUCKn_OV_THR = 0x2	3%	4%	5%	
7.1d			BUCKn_OV_THR = 0x3	4%	5%	6%	
7.1e			BUCKn_OV_THR = 0x4	5%	6%	7%	
7.1f			BUCKn_OV_THR = 0x5	6%	7%	8%	
7.1g			BUCKn_OV_THR = 0x6	7%	8%	9%	
7.1h			BUCKn_OV_THR = 0x7	9%	10%	11%	
7.2a	$V_{BUCK_OV_TH_mv}$	Overvoltage monitoring for BUCK output, threshold accuracy, $V_{OUT_Bn} < 1$ V(1)	BUCKn_OV_THR = 0x0	20	30	40	mV
7.2b			BUCKn_OV_THR = 0x1	25	35	45	
7.2c			BUCKn_OV_THR = 0x2	30	40	50	
7.2d			BUCKn_OV_THR = 0x3	40	50	60	
7.2e			BUCKn_OV_THR = 0x4	50	60	70	
7.2f			BUCKn_OV_THR = 0x5	60	70	80	
7.2g			BUCKn_OV_THR = 0x6	70	80	90	
7.2h			BUCKn_OV_THR = 0x7	90	100	110	
7.3a	$V_{BUCK_UV_TH}$	Undervoltage monitoring for buck output, threshold accuracy, $V_{OUT_Bn} \geq 1$ V(1)	BUCKn_UV_THR = 0x0	–4%	–3%	–2%	
7.3b			BUCKn_UV_THR = 0x1	–4.5%	–3.5%	–2.5%	
7.3c			BUCKn_UV_THR = 0x2	–5%	–4%	–3%	
7.3d			BUCKn_UV_THR = 0x3	–6%	–5%	–4%	
7.3e			BUCKn_UV_THR = 0x4	–7%	–6%	–5%	
7.3f			BUCKn_UV_THR = 0x5	–8%	–7%	–6%	
7.3g			BUCKn_UV_THR = 0x6	–9%	–8%	–7%	
7.3h			BUCKn_UV_THR = 0x7	–11%	–10%	–9%	
7.4a	$V_{BUCK_UV_TH_mv}$	Undervoltage monitoring for buck output, threshold accuracy, $V_{OUT_Bn} < 1$ V(1)	BUCKn_UV_THR = 0x0	–40	–30	–20	mV
7.4b			BUCKn_UV_THR = 0x1	–45	–35	–25	
7.4c			BUCKn_UV_THR = 0x2	–50	–40	–30	
7.4d			BUCKn_UV_THR = 0x3	–60	–50	–40	
7.4e			BUCKn_UV_THR = 0x4	–70	–60	–50	
7.4f			BUCKn_UV_THR = 0x5	–80	–70	–60	
7.4g			BUCKn_UV_THR = 0x6	–90	–80	–70	
7.4h			BUCKn_UV_THR = 0x7	–110	–100	–90	
Electrical Characteristics: LDO REGULATOR OUTPUTS							
7.5a	$V_{LDO_OV_TH}$	Overvoltage monitoring for LDO output, threshold accuracy, $V_{OUT_LDOn} \geq 1$ V(2)	LDOn_OV_THR = 0x0	2%	3%	4%	
7.5b			LDOn_OV_THR = 0x1	2.5%	3.5%	4.5%	
7.5c			LDOn_OV_THR = 0x2	3%	4%	5%	
7.5d			LDOn_OV_THR = 0x3	4%	5%	6%	
7.5e			LDOn_OV_THR = 0x4	5%	6%	7%	
7.5f			LDOn_OV_THR = 0x5	6%	7%	8%	
7.5g			LDOn_OV_THR = 0x6	7%	8%	9%	
7.5h			LDOn_OV_THR = 0x7	9%	10%	11%	

7.10 Monitoring Functions (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level is measured with reference to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
7.6a	$V_{LDO_OV_TH_mv}$	Overvoltage monitoring for LDO output, threshold accuracy, V_{OUT_LDOn} < 1 V(2)	LDOn_OV_THR = 0x0	20	30	40	mV
7.6b			LDOn_OV_THR = 0x1	25	35	45	
7.6c			LDOn_OV_THR = 0x2	30	40	50	
7.6d			LDOn_OV_THR = 0x3	40	50	60	
7.6e			LDOn_OV_THR = 0x4	50	60	70	
7.6f			LDOn_OV_THR = 0x5	60	70	80	
7.6g			LDOn_OV_THR = 0x6	70	80	90	
7.6h			LDOn_OV_THR = 0x7	90	100	110	
7.7a	$V_{LDO_UV_TH}$	Undervoltage monitoring for LDO output, threshold accuracy, V_{OUT_LDOn} ≥ 1 V(2)	LDOn_UV_THR = 0x0	–4%	–3%	–2%	
7.7b			LDOn_UV_THR = 0x1	–4.5%	–3.5%	–2.5%	
7.7c			LDOn_UV_THR = 0x2	–5%	–4%	–3%	
7.7d			LDOn_UV_THR = 0x3	–6%	–5%	–4%	
7.7e			LDOn_UV_THR = 0x4	–7%	–6%	–5%	
7.7f			LDOn_UV_THR = 0x5	–8%	–7%	–6%	
7.7g			LDOn_UV_THR = 0x6	–9%	–8%	–7%	
7.7h			LDOn_UV_THR = 0x7	–11%	–10%	–9%	
7.8a	$V_{LDO_UV_TH_mv}$	Undervoltage monitoring for LDO output, threshold accuracy, V_{OUT_LDOn} < 1 V(2)	LDOn_UV_THR = 0x0	–40	–30	–20	mV
7.8b			LDOn_UV_THR = 0x1	–45	–35	–25	
7.8c			LDOn_UV_THR = 0x2	–50	–40	–30	
7.8d			LDOn_UV_THR = 0x3	–60	–50	–40	
7.8e			LDOn_UV_THR = 0x4	–70	–60	–50	
7.8f			LDOn_UV_THR = 0x5	–80	–70	–60	
7.8g			LDOn_UV_THR = 0x6	–90	–80	–70	
7.8h			LDOn_UV_THR = 0x7	–110	–100	–90	
Electrical Characteristics: VCCA INPUT							
7.9a	$VCCA_{OV_TH}$	Overvoltage monitoring for VCCA input, threshold accuracy(3)	VCCA_OV_THR = 0x0	2%	3%	4%	
7.9b			VCCA_OV_THR = 0x1	2.5%	3.5%	4.5%	
7.9c			VCCA_OV_THR = 0x2	3%	4%	5%	
7.9d			VCCA_OV_THR = 0x3	4%	5%	6%	
7.9e			VCCA_OV_THR = 0x4	5%	6%	7%	
7.9f			VCCA_OV_THR = 0x5	6%	7%	8%	
7.9g			VCCA_OV_THR = 0x6	7%	8%	9%	
7.9h			VCCA_OV_THR = 0x7	9%	10%	11%	
7.10a	$VCCA_{UV_TH}$	Undervoltage monitoring for VCCA input, threshold accuracy(3)	VCCA_UV_THR = 0x0	-4%	-3%	-2%	
7.10b			VCCA_UV_THR = 0x1	-4.5%	-3.5%	-2.5%	
7.10c			VCCA_UV_THR = 0x2	-5%	-4%	-3%	
7.10d			VCCA_UV_THR = 0x3	-6%	-5%	-4%	
7.10e			VCCA_UV_THR = 0x4	-7%	-6%	-5%	
7.10f			VCCA_UV_THR = 0x5	-8%	-7%	-6%	
7.10g			VCCA_UV_THR = 0x6	-9%	-8%	-7%	
7.10h			VCCA_UV_THR = 0x7	-11%	-10%	-9%	
Timing Requirements							
26.30a	$t_{delay_OV_UV}$	BUCK and LDO OV/UV detection delay	Detection delay with 5 mV (V_{in} < 1 V) or 0.5% (V_{in} ≥ 1 V) over/underdrive			8	µs
26.30b	$t_{delay_OV_UV}$	VCCA OV/UV detection delay	Detection delay with 30 mV over/underdrive			12	µs
26.31a	$t_{deglitch1_OV_UV}$	VCCA, BUCK and LDO OV/UV signal deglitch time	VMON_DEGLITCH_SEL = 0: Digital deglitch time for detected signal	3.4	3.8	4.2	µs
26.31b	$t_{deglitch2_OV_UV}$		VMON_DEGLITCH_SEL = 1: Digital deglitch time for detected signal	18	20	22	µs

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7.10 Monitoring Functions (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level is measured with reference to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
26.32a	$t_{latency1_OV_UV}$	BUCK and LDO OV/UV signal latency time	VMON_DEGLITCH_SEL = 0: Total delay from 5mV (V_{in} < 1 V) or 0.5% (V_{in} ≥ 1 V) over/underdrive to interrupt or PFSM trigger			13	µs
26.32b	$t_{latency2_OV_UV}$		VMON_DEGLITCH_SEL = 1: Total delay from 5mV (V_{in} < 1 V) or 0.5% (V_{in} ≥ 1 V) over/underdrive to interrupt or PFSM trigger			30	µs
26.32b	$t_{latency1_VCCA_OV_UV}$	VCCA OV/UV signal latency time	VMON_DEGLITCH_SEL = 0: Total delay from 30 mV over/underdrive to interrupt or PFSM trigger			13	µs
26.32b	$t_{latency2_VCCA_OV_UV}$		VMON_DEGLITCH_SEL = 1: Total delay from 30 mV over/underdrive to interrupt or PFSM trigger			30	µs
26.33a	$t_{deglitch_PGOOD_rise}$	PGOOD signal deglitch time	Internal logic signal transitions from invalid to valid(4)	9.5		10.5	µs
26.33b	$t_{deglitch_PGOOD_fall}$		Internal logic signal transitions from valid to invalid(4)		0		µs

(1) The default values of BUCKn_OV_THR & BUCKn_UV_THR registers come from the NVM memory, and can be re-configured by software.
(2) The default values of LDOn_OV_THR & LDOn_UV_THR registers come from the NVM memory, and can be re-configured by software.
(3) The default values of VCCA_OV_THR & VCCA_UV_THR registers come from the NVM memory, and can be re-configured by software.
(4) Interrupt status signal is input signal for PGOOD deglitch logic.

7.11 Clocks, Oscillators, and PLL

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics: CRYSTAL							
6.1		Crystal frequency			32768		Hz
6.2		Crystal frequency tolerance	Parameter of crystal, T_J = 25°C	–20		20	ppm
6.4		Crystal series resistance	At fundamental frequency			90	kΩ
6.5		Oscillator drive power	The power dissipated in the crystal during oscillator operation		0.1	0.5	µW
6.6		Crystal Load capacitance(1)	Corresponding to crystal frequency, including parasitic capacitances	6		12.5	pF
6.7		Crystal shunt capacitance	Parameter of crystal		1.4	2.6	pF
Electrical Characteristics: 32-kHz CRYSTAL OSCILLATOR EXTERNAL COMPONENTS							
6.7a		Load capacitance on OSC32KIN and OSC32KOUT (parallel mode, including parasitic of PCB for external capacitor)(2)	External Capacitors	0		13	pF
6.7b			Internal Capacitors	9.5	12	14.5	pF
Switching Characteristics: 32-kHz CRYSTAL OSCILLATOR CLOCK							
23.1		Crystal Oscillator output frequency	Typical with specified load capacitors		32768		Hz
23.2		Crystal Oscillator Output duty cycle	Parameter of crystal, T_J = 25°C	40%	50%	60%	
23.3		Crystal Oscillator rise and fall time	10% to 90%, with 10 pF load capacitance		10	20	ns
23.4		Crystal Oscillator Settling time	From Oscillator enable to reaching ±1% of final output frequency			200	ms
Switching Characteristics: 20-MHz and 128-kHz RC OSCILLATOR CLOCK							
23.10		20 MHz RC Oscillator output frequency		19	20	21	MHz
23.12		128 kHz RC Oscillator output frequency		121	128	135	kHz
Switching Characteristics: DPLL, SYNCCLKIN, and SYNCCLKOUT							

7.11 Clocks, Oscillators, and PLL (continued)

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
22.1a		External input clock nominal frequency	EXT_CLK_FREQ = 0x0		1.1		MHz
22.1b			EXT_CLK_FREQ = 0x1		2.2		
22.1c			EXT_CLK_FREQ = 0x2		4.4		
22.2a		External input clock required accuracy from nominal frequency	SS_DEPTH = 0x0	–18%		18%	
22.2b			SS_DEPTH = 0x1	–12%		12%	
22.2c			SS_DEPTH = 0x2	–10%		10%	
22.13 a		Logic low time for SYNCCLKIN clock		40			ns
22.13 b		Logic high time for SYNCCLKIN clock		40			ns
22.3		External clock detection delay for missing clock detection				1.8	µs
22.4		External clock input debounce time for clock detection				20	µs
22.5		Clock change delay (internal to external)	From valid clock detection to use of external clock		600		µs
22.7a		SYNCCLKOUT clock nominal frequency	SYNCCLKOUT_FREQ_SEL = 0x1		1.1		MHz
22.7b			SYNCCLKOUT_FREQ_SEL = 0x2		2.2		MHz
22.7c			SYNCCLKOUT_FREQ_SEL = 0x3		4.4		MHz
22.8		SYNCCLKOUT duty-cycle	Cycle-to-cycle	40%	50%	60%	
22.9		SYNCCLKOUT output buffer external load		5	35	50	pF
22.11a		Spread spectrum variation for nominal switching frequency	SS_DEPTH = 0x1		6.3%		
22.11b			SS_DEPTH = 0x2		8.4%		
Timing Requirements: Clock Monitors							
26.7a	$t_{latency_CLKfail}$	Clock Monitor Failure signal latency from occurrence of error	Failure on 20MHz system clock			10	µs
26.7b			Failure on 128KHz monitoring clock			40	µs
26.8	$t_{latency_CLKdrift}$	Clock Monitor Drift signal latency from detection				115	µs
26.9	f_{sysclk}	Internal system clock		19	20	21	MHz
26.10	CLKdrift_TH	Threshold for internal system clock frequency drift detection		-20%		20%	
26.11	CLKfail_TH	Threshold for internal system clock stuck at high or stuck at low detection				10	MHz

(1) Customer must use the XTAL_SEL bit to select the corresponding crystal based on its load capacitance.
(2) External capacitors must be used if crystal load capacitance > 6 pF.

7.12 Thermal Monitoring and Shutdown

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
8.1a	T_{WARN_0}	TWARN_INT thermal warning threshold (no hysteresis)	TWARN_LEVEL = 0	120	130	140	°C
8.1b	T_{WARN_1}		TWARN_LEVEL = 1	130	140	150	°C
8.2a	$T_{SD_orderly_0}$	TSD_ORD_INT thermal shutdown rising threshold	TSD_ORD_LEVEL = 0	130	140	150	°C
8.2b	$T_{SD_orderly_1}$		TSD_ORD_LEVEL = 1	135	145	155	°C
8.2c	$T_{SD_orderly_hys_0}$	TSD_ORD_INT thermal shutdown hysteresis	TSD_ORD_LEVEL = 0		10		°C
8.2d	$T_{SD_orderly_hys_1}$		TSD_ORD_LEVEL = 1		5		°C
8.3a	T_{SD_imm}	TSD_IMM_INT thermal shutdown rising threshold		140	150	160	°C

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7.12 Thermal Monitoring and Shutdown (continued)

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
8.3b	$T_{SD_imm_hys}$	TSD_IMM_INT thermal shutdown hysteresis			5		°C
Timing Requirements							
26.6	$t_{latency_TSD}$	TSD signal latency from detection				425	µs

7.13 System Control Thresholds

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
9.1	$V_{POR_Falling}$	VCCA UVLO/POR falling threshold	Measured on VCCA pin	2.7	2.75	2.8	V
9.2	V_{POR_Rising}	VCCA UVLO/POR rising threshold	Measured on VCCA pin	2.7		3	V
9.3	V_{POR_Hyst}	VCCA UVLO/POR hysteresis			100		mV
9.5aa	$V_{VCCA_OVP_Rising}$	VCCA OVP rising threshold	Measured on VCCA pin. VCCA_PG_SET = 0b	3.9	4.0	4.1	V
9.5ab			Measured on VCCA pin. VCCA_PG_SET = 1b	5.6	5.7	5.8	V
9.5b	$V_{VCCA_OVP_Hyst}$	VCCA OVP hysteresis			50		mV
9.7	$V_{VSYS_OVP_Rising}$	VSYS OVP rising threshold	Measured on VSYS_SENSE pin, untrimmed	5.6	5.9	6.2	V
9.8	$V_{VSYS_OVP_Rising_Trim}$	VSYS OVP rising threshold, trimmed	Measured on VSYS_SENSE pin, trimmed	5.8	5.9	6	V
9.9	$V_{OVPGDRV_OFF}$	Output voltage at OVPGDRV pin when external FET is switched off	Measured after OVPGDRV pin has reached steady state voltage			0.4	V
9.10	$V_{OVPGDRV_On}$	Output voltage at OVPGDRV pin when external FET is switched on	Measured after OVPGDRV pin has reached steady state voltage			12	V
9.11	C_{iss_extFET}	Gate capacitance of external NMOS FET	External NMOS FET: V_{DS} = 12V, V_{GS} = 0V			4	nF
9.12	$V_{OVPGDRV_OV_TH}$	Over-voltage threshold level at OVPGDRV pin when external FET is switched on				12.5	V
9.13	$R_{VCCA_OVP_PD}$	Active pull down resistance between VCCA and GND in case of VSYS OVP detection		50	100	140	Ω
9.14	V_{VSYS_SR}	Input slew rate of VSYS supply	Measured at VSYS_SENSE pin as voltage rises from 0V to V_{POR_Rising}			30	mV/µs
9.15	$V_{VCCA_PVIN_SR}$	Input slew rate of VCCA and PVIN_x supplies	Measured at VCCA and PVIN_x pins as voltage rises from 0V to V_{POR_Rising}			60	mV/µs
9.16	V_{VIO_SR}	Input slew rate of VIO supply	Measured at VIO pin as voltage rises from 0V to V_{POR_Rising}			60	mV/µs
9.17	$V_{VBACKUP_SR}$	Input slew rate of VBACKUP supply	Measured at VBACKUP pin			60	mV/µs
9.18	$V_{VSYS_RC_TH}$	VSYS reset recovery threshold	Measured on VSYS_SENSE pin			50	mV
9.19	$V_{VSYS_UVLO_Rising_TH}$	VSYS UVLO recovery threshold	Measured on VSYS_SENSE pin	2.4		2.7	V
9.20	$V_{OVP_FET_Short_TH}$	VSYS OVP FET-fail short test threshold	Measured on VCCA pin	0.3		0.42	V
9.21	$V_{OVP_FET_Short_Hyst}$	VSYS OVP FET fail-short test hysteresis	Measured on VCCA pin	30		60	mV
Timing Requirements							
26.1	$t_{VSYS_RC_TH}$	VSYS reset recovery time	Minimum time VSYS_SENSE stays below $V_{VSYS_RC_TH}$ before device recovers from VSYS power cycle	5			ms

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7.13 System Control Thresholds (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
26.20	$t_{VSYSOVP_INIT}$	Startup time for OVPGDRV output	Total startup time for OVPDGRV to rise from 0V to V_{VSYS_SENSE}, including OVP circuit startup, FET fault detection, and OVPGDRV ramp time. 200 µF capacitance at VCCA		6	20	ms
26.2	$t_{latency_VSYSOVP}$	OVPGDRV latency from VSYS OVP detection	Voltage at VSYS_SENSE pin rises from 6 V to 8 V in 7 µs. Measured from the time VSYS_SENSE = 6 V to the time OVPGDRV = VCCA			15	µs
26.3a	$t_{latency_VCCAOVP}$	OVPGDRV latency from VCCA OVP detection	VCCA_PG_SEL = 0b. Voltage at VSYS_SENSE pin rises from 4 V to 8 V in 7 µs. Measured from the time VCCA = $V_{VCCA_OVP_Rising}$ to the time OVPGDRV = VCCA			10	µs
26.3b			VCCA_PG_SEL = 1b. Voltage at VSYS_SENSE pin rises from 6 V to 8 V in 7 µs. Measured from the time VCCA = $V_{VCCA_OVP_Rising}$ to the time OVPGDRV = VCCA			10	µs
26.4	$t_{latency_VCCAUVLO}$	VCCA_UVLO signal latency from detection	Measured time between V_{VCCA} falling from 3.3 V to 2.7 V with ≤ 100mv/µs slope, to the detection of VCCA_UVLO signal			10	µs
26.5	$t_{latency_VINT}$	LDOVINT OVP and UVLO signal latency from detection	With 25-mV overdrive			12	µs
26.14	$t_{ABISTrun}$	Run time for ABIST				0.25	ms
26.15	$t_{LBISTrun}$	Run time for LBIST				1.8	ms
26.16	$t_{INIT_NVM_ANALOG}$	Device initialization time to load default values for NVM registers, and start-up analog circuits				2	ms
26.17	$t_{INIT_REF_CLK_LDO}$	Device initialization time for reference bandgaps, system clock, and internal LDOs				1	ms

7.14 Current Consumption

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
10.2	I_{BACKUP_RTC}	Backup current consumption, regulators disabled	From VBACKUP pin. PWRON/ENABLE deactivated. Device powered by the backup battery source. VSYS_SENSE = VCCA = 0V. VIO = 0V. VBACKUP = 3.3V. Only 32-kHz crystal oscillator and RTC counters are functioning. T_J = 25℃. VSYS_OVP function deactivated.		7	10	µA
10.3a	$I_{LP_STANDBY}$	Low Power Standby current consumption, regulators disabled	Combined current from VCCA and PVIN_x pins. VSYS_SENSE is grounded. VCCA = PVIN_Bx = PVIN_LDOx = 3.3 V. VIO = 0V. 32-kHz crystal oscillator and RTC digital is functioning. GPIO pins in LDOVRTC domain are active. All monitors are off. T_J = 25℃. VSYS OVP function deactivated		11	24	µA
10.3b	$I_{LP_STANDBY_OVP}$	Low Power Standby current consumption, OVP activated	Combined current from VSYS_SENSE, VCCA and PVIN_x pins, with protection FET in place connecting the VSYS_SENSE pin with VCCA pin. VSYS_SENSE = VCCA = PVIN_Bx = PVIN_LDOx = 3.3 V. VIO = 0V. 32-kHz crystal oscillator and RTC digital is functioning. GPI pins in LDOVRTC domain are active. All Monitors are off. T_J = 25℃. VSYS_OVP function activated		26	34	µA
10.5a	$I_{STANDBY}$	Standby current consumption	Combined current from VCCA, and PVIN_x. VSYS_SENSE is grounded. VCCA = PVIN_Bx = PVIN_LDOx = 3.3 V. VIO = 0V. T_J = 25℃. VCCA_VMON_EN=0. VSYS_OVP function deactivated		50	62	µA

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7.14 Current Consumption (continued)

Over operating free-air temperature range (unless otherwise noted).

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
10.5b	$I_{STANDBY_OVP}$	Standby current consumption, OVP activated	Combined current from VSYS_SENSE, VCCA and PVIN_x pins, with protection FET in place connecting the VSYS_SENSE pin with VCCA pin. VSYS_SENSE = VCCA = PVIN_Bx = PVIN_LDOx = 3.3 V. VIO = 0V. T_J = 25℃. VCCA_VMON_EN=0. VSYS_OVP function activated		66	83	µA
10.5c	$I_{STANDBY_OVP_VCCAmon}$	Standby current consumption	Combined current from VSYS_SENSE, VCCA and PVIN_x pins, with protection FET in place connecting the VSYS_SENSE pin with VCCA pin. VSYS_SENSE = VCCA = PVIN_Bx = PVIN_LDOx = 3.3 V. VIO = 0V. T_J = 25℃. VCCA_VMON_EN=1. VSYS_OVP function activated		250	315	µA
10.6a	I_{SLEEP_3V3}	Sleep current consumption	Combined current from VSYS_SENSE, VCCA and PVIN_x pins, with protection FET in place connecting the VSYS_SENSE pin with VCCA pin. VSYS_SENSE = VCCA = PVIN_Bx = PVIN_LDOx = 3.3 V. VIO = 0V. T_J = 25℃. One buck regulator enabled in PFS/PWM mode, no load. Buck and VCCA OV/UV monitoring enabled. VSYS_OVP function activated		290	363	µA
10.6b	I_{SLEEP_5V}	Sleep current consumption	Combined current from VSYS_SENSE, VCCA and PVIN_x pins, with protection FET in place connecting the VSYS_SENSE pin with VCCA pin. VSYS_SENSE = VCCA = PVIN_Bx = PVIN_LDOx = 5 V. VIO = 0V. T_J = 25℃. One buck regulator enabled in PFS/PWM mode, no load. Buck and VCCA OV/UV monitoring enabled. VSYS_OVP function activated		300	375	µA

7.15 Backup Battery Charger

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
27.1a	I_{charge}	Charging current	VBACKUP = 1 V, BB_ICHR = 0x0		100		µA
27.1b			VBACKUP = 1 V, BB_ICHR = 0x1		500		
27.2a	V_{EOC}	End of charge voltage(1)	BB_VEOC = 0x0	2.4	2.5	2.6	V
27.2b			BB_VEOC = 0x1	2.7	2.8	2.9	
27.2c			BB_VEOC = 0x2	2.9	3	3.1	
27.2d			BB_VEOC = 0x3	3.2	3.3	3.4	
27.3	I_{q_CHGR}	Quiescent current of backup battery charger	End of charge, charger enabled, VCCA - VBACKUP > 200 mV. Measured from VCCA pin		5	9	µA
27.4a	$I_{q_CHGR_OFF}$	Off current of backup battery charger	VCCA - VBACKUP > 200 mV. Charger disabled. Device not in BACKUP state. Tj < 125°C		10	100	nA
27.4b			VCCA - VBACKUP > 200 mV. Charger disabled. Device not in BACKUP state. 125°C < Tj < 150°C			250	
27.5	C_{BKUP}	Backup battery capacitance with additional capacitor	Additional capacitor added when backup battery ESR > 20 Ω	1	2.2	4	µF
27.6a	R_{BKUP_ESR}	Backup battery series resistance	Without additional capacitor in parallel			20	Ω
27.6b			With additional capacitor in parallel			1000	

(1) End of charge (EOC) voltage measured when VCCA-VBACKUP > 200mV. When VCCA-VBACKUP is ≤ 200mV, the charger remains fully functional, although the EOC voltage measurement is not based on final voltage, but on charger dropout.

7.16 Digital Input Signal Parameters

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device. VIO refers to the VIO_IN pin, VCCA refers to the VCCA pin.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics: nPWRON/ENABLE							
11.1	$V_{IL(VCCA)}$	Low-level input voltage		-0.3	0	0.54	V
11.2	$V_{IH(VCCA)}$	High-level input voltage		1.26			V
11.3		Hysteresis		150			mV
Electrical Characteristics: I2C/SPI Pins and Input Signals through all GPIO pins							
11.4	$V_{IL(DIG)}$	Low-level input voltage		-0.3	0	0.54	V
11.5	$V_{IH(DIG)}$	High-level input voltage		1.26			V
11.6		Hysteresis		150			mV
Timing Requirements: nPWRON/ENABLE							
24.1a	t_{LPK_TIME}	nPWRON Long Press Key time			8		s
24.1b	t_{degl_PWRON}	nPWRON button deglitch time	ENABLE_DEGLITCH_EN = 1	48	50	52	ms
24.2	t_{degl_ENABLE}	ENABLE signal deglitch time(1)	ENABLE_EGLITCH_EN = 1, exclude when activated under LP_STANDBY state while the system clock is not available	6	8	10	µs
Timing Requirements: GPIx, nSLEEPx, nERRx, and other digital input signals							
24.3a	t_{WKUP_LP}	Time from valid GPIx assertion until device wakes up from LP_STANDBY state to ACTIVE or MCU ONLY states	FAST_BOOT_BIST=0			10	ms
24.3b			FAST_BOOT_BIST=1			5	ms
25.1a	t_{degl_GPIx}	GPIx and nSLEEPx signal deglitch time	GPIOn_DEGLITCH_EN = 1	6	8	10	µs
25.1b	t_{degl_ESMx}	nERRn signal deglitch time	GPIOn_DEGLITCH_EN = 1	12	15	18	µs
25.2a	$t_{STARTUP}$	Time from receiving nPWRON/ ENABLE trigger in STANDBY state to nRSTOUT assertion				5	ms
25.2b		Time from a valid GPIx assertion until device starts power-up sequence from a low power state	LDOVINT = 1.8V			1.5	ms
25.3	t_{SLEEP}	Time from nSLEEPx assertion until device starts power-down sequence to enter a low power state	LDOVINT = 1.8V			1.5	ms
25.4a	$t_{WK_PW_MIN}$	Minimum valid input pulse width for the WKUP input signals	input through LP_WKUP1 and LP_WKUP2 (GPIO3 or GPIO4) pins while the device is in LP_STANDBY state	40			ns
25.4b			input through WKUP1, WKUP2, LP_WKUP1 and LP_WKUP2 pins while the device is in mission states	200			ns
25.5a	t_{WD_DIS}	DISABLE_WDOG input signal deglitch time		24	30	36	µs
25.5b	t_{WD_pulse}	TRIG_WDOG input signal deglitch time		24	30	36	µs

(1) ENABLE signal deglitch is not available when device is activated from the LP_STANDBY state while the deglitching clock is not available.

7.17 Digital Output Signal Parameters

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device. VIO refers to the VIO_IN pin, VCCA refers to the VCCA pin.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics: SDA_I2C1, and Output Signals through GPO1 and GPO2 pins							
12.11	$V_{OL(VIO)_20mA}$	Low-level output voltage, push-pull and open-drain	I_{OL} = 20 mA			0.4	V
12.12	$V_{OH(VIO)}$	High-level output voltage, push-pull	I_{OH} = 3 mA	VIO – 0.4			V
Electrical Characteristics: Output Signals through GPO3 and GPO4 pins							

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7.17 Digital Output Signal Parameters (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level is in reference to the thermal/ground pad of the device. VIO refers to the VIO_IN pin, VCCA refers to the VCCA pin.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
12.13	$V_{OL(DIG)}$	Low-level output voltage, push-pull	I_{OL} = 3 mA			0.4	V
12.14	$V_{OH(DIG)}$	High-level output voltage, push-pull	I_{OH} = 3 mA	1.4			V
Electrical Characteristics: Output Signals through GPO5 and GPO6 pins							
12.4	$V_{OL(DIG)_20mA}$	Low-level output voltage, push-pull	I_{OL} = 20 mA			0.4	V
12.5	$V_{OH(DIG)}$	High-level output voltage, push-pull	I_{OH} = 3 mA	1.4			V
Electrical Characteristics: Output Signals through GPO7, GPO8, GPO9, GPO10, and GPO11 pins							
12.1	$V_{OL(VIO)}$	Low-level output voltage, push-pull and open-drain	I_{OL} = 3 mA			0.4	V
12.2	$V_{OH(VIO)}$	High-level output voltage, push-pull	I_{OH} = 3 mA	VIO – 0.4			V
12.3		Supply for external pullup resistor, open drain				VIO	V
Electrical Characteristics: EN_DRV, nINT, nRSTOUT							
12.6	$V_{OL(EN_DRV)}$	Low-level output voltage for EN_DRV pin	I_{OL} =20 mA			0.4	V
12.7	$V_{OL(nINT)}$	Low-level output voltage for nINT pin	I_{OL} = 20 mA			0.4	V
12.8	$V_{OL(nRSTOUT)}$	Low-level output voltage for nRSTOUT and nRSTOUT_SoC pin	I_{OL} = 20 mA			0.4	V
Timing Requirements							
12.10	$t_{gate_readback}$	Gating time for readback monitor	Signal level change or GPIO selection (GPIOn_SEL)	8.8		9.6	µs

7.18 I/O Pullup and Pulldown Resistance

Over operating free-air temperature range, VIO refers to the VIO_IN pin, VCCA refers the VCCA pin.

POS	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics						
13.1a	nPWRON pullup resistance	nPWRON IO buffer internal pull up to VCCA supply	280	400	520	kΩ
13.1b	ENABLE pullup and pulldown resistance	ENABLE IO buffer internal pull up to VCCA supply and pull down to ground	280	400	520	kΩ
13.2	GPIO pullup resistance	GPIO1 -11 pins configured as input with internal pullup	280	400	520	kΩ
13.3	GPIO pulldown resistance	GPIO1 - 11 pins configured as inputs with internal pulldown	280	400	520	kΩ
13.4	nRSTOUT and nRSTOUT_SoC pullup resistance	Internal pullup to VIO supply when output driven high	8	10	12	kΩ
13.5	EN_DRV pullup resistance	Internal pullup to VCCA supply when output driven high	8	10	12	kΩ

7.19 I²C Interface

Over operating free-air temperature range (unless otherwise noted). Device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode+ (1 MHz) when VIO is 3.3 V or 1.8 V, and high-speed mode (3.4 MHz) only when VIO is 1.8 V.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
14.1	C_B	Capacitive load for SDA and SCL				400	pF
Timing Requirements							

7.19 I²C Interface (continued)

Over operating free-air temperature range (unless otherwise noted). Device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode+ (1 MHz) when VIO is 3.3 V or 1.8 V, and high-speed mode (3.4 MHz) only when VIO is 1.8 V.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
16.1a	f_{SCL}	Serial clock frequency	Standard mode			100	kHz
16.1b			Fast mode			400	
16.1c			Fast mode+			1	MHz
16.1d			High-speed mode, C_b = 100 pF			3.4	
16.1e			High-speed mode, C_b = 400 pF			1.7	
16.2a	t_{LOW}	SCL low time	Standard mode	4.7			µs
16.2b			Fast mode	1.3			
16.2c			Fast mode+	0.5			
16.2d			High-speed mode, C_b = 100 pF	160			ns
16.2e			High-speed mode, C_b = 400 pF	320			
16.3a	t_{HIGH}	SCL high time	Standard mode	4			µs
16.3b			Fast mode	0.6			
16.3c			Fast mode+	0.26			
16.3d			High-speed mode, C_b = 100 pF	60			ns
16.3e			High-speed mode, C_b = 400 pF	120			
16.4a	$t_{SU;DAT}$	Data setup time	Standard mode	250			ns
16.4b			Fast mode	100			
16.4c			Fast mode+	50			
16.4d			High-speed mode	10			
16.5a	$t_{HD;DAT}$	Data hold time	Standard mode	10		3450	ns
16.5b			Fast mode	10		900	
16.5c			Fast mode+	10			
16.5d			High-speed mode, C_b = 100 pF	10		70	ns
16.5e			High-speed mode, C_b = 400 pF	10		150	
16.6a	$t_{SU;STA}$	Setup time for a start or a REPEATED START condition	Standard mode	4.7			µs
16.6b			Fast mode	0.6			
16.6c			Fast mode+	0.26			
16.6d			High-speed mode	160			ns
16.7a	$t_{HD;STA}$	Hold time for a start or a REPEATED START condition	Standard mode	4			µs
16.7b			Fast mode	0.6			
16.7c			Fast mode+	0.26			
16.7d			High-speed mode	160			ns
16.8a	t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
16.8b			Fast mode	1.3			
16.8c			Fast mode+	0.5			
16.9a	$t_{SU;STO}$	Setup time for a STOP condition	Standard mode	4			µs
16.9b			Fast mode	0.6			
16.9c			Fast mode+	0.26			
16.9d			High-speed mode	160			ns
16.10a	t_{rDA}	Rise time of SDA signal	Standard mode			1000	ns
16.10b			Fast mode	20		300	
16.10c			Fast mode+			120	
16.10d			High-speed mode, C_b = 100 pF	10		80	
16.10e			High-speed mode, C_b = 400 pF	20		160	

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7.19 I²C Interface (continued)

Over operating free-air temperature range (unless otherwise noted). Device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode+ (1 MHz) when VIO is 3.3 V or 1.8 V, and high-speed mode (3.4 MHz) only when VIO is 1.8 V.

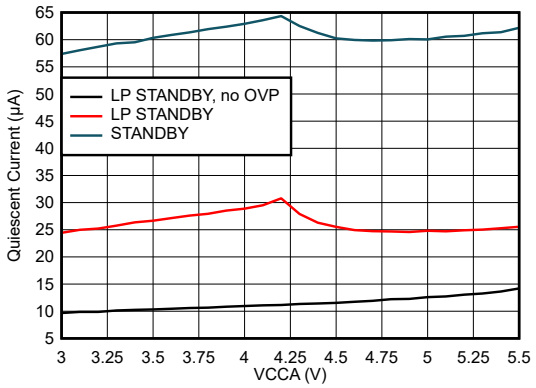
POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
16.11a	t_{fDA}	Fall time of SDA signal	Standard mode			300	ns
16.11b			Fast mode	6.5		300	
16.11c			Fast mode+	6.5		120	
16.11d			High-speed mode, C_b = 100 pF	10		80	
16.11e			High-speed mode, C_b = 400 pF	13		160	
16.12a	t_{rCL}	Rise time of SCL signal	Standard mode			1000	ns
16.12b			Fast mode	20		300	
16.12c			Fast mode+			120	
16.12d			High-speed mode, C_b = 100 pF	10		40	
16.12e			High-speed mode, C_b = 400 pF	20		80	
16.13a	t_{rCL1}	Rise time of SCL signal after a repeated start condition and after an acknowledge bit	High-speed mode, C_b = 100 pF	10		80	ns
16.13b			High-speed mode, C_b = 400 pF	20		160	
16.14a	t_{fCL}	Fall time of SCL signal	Standard mode			300	ns
16.14b			Fast mode	6.5		300	
16.14c			Fast mode+	6.5		120	
16.14d			High-speed mode, C_b = 100 pF	10		40	
16.14e			High-speed mode, C_b = 400 pF	20		80	
16.15a	t_{SP}	Pulse width of spike suppressed (SCL and SDA spikes that are less than the indicated width are suppressed)	Standard mode, fast mode, and fast mode+			50	ns
16.15b			High-speed mode			10	

7.20 Serial Peripheral Interface (SPI)

These specifications are ensured by design, VIO = 1.8 V or 3.3V (unless otherwise noted).

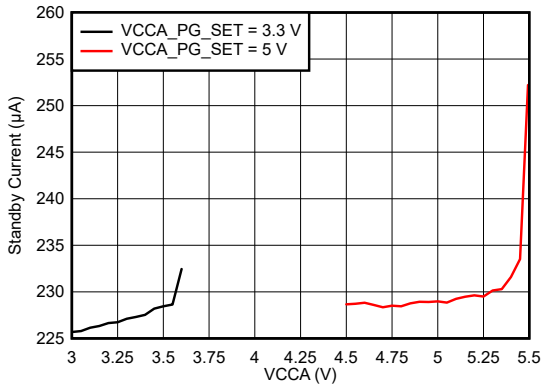
POS	PARAMETERS		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Electrical Characteristics							
15.1		Capacitive load on pin SDO				30	pF
Timing Requirements							
17.1	1	Cycle time		200			ns
17.2	2	Enable lead time		150			ns
17.3	3	Enable lag time		150			ns
17.4	4	Clock low time		60			ns
17.5	5	Clock high time		60			ns
17.6	6	Data setup time		15			ns
17.7	7	Data hold time		15			ns
17.8	8	Output data valid after SCLK falling		4			ns
17.9	9	New output data valid after SCLK falling				60	ns
17.10	10	Disable time				30	ns
17.11	11	CS inactive time		100			ns

7.21 Typical Characteristics



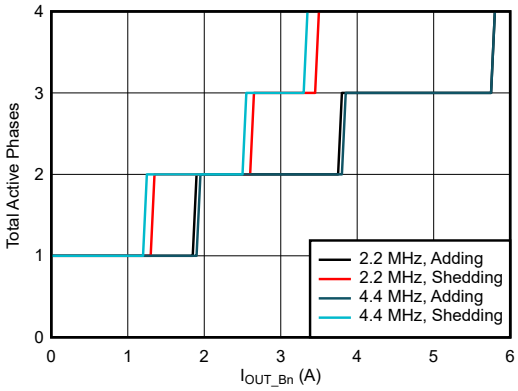
TA = 25°C

Figure 7-1. Quiescent Current vs Input Voltage



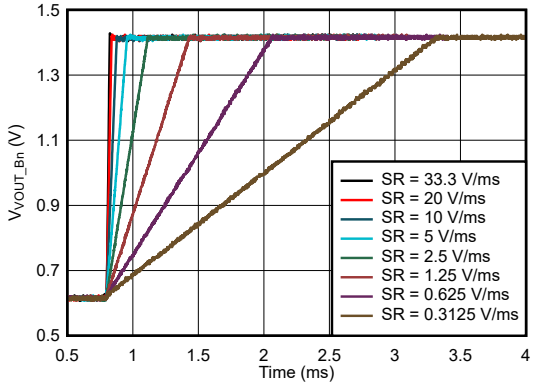
TA = 25°C

Figure 7-2. Standby Current with VCCA Monitor



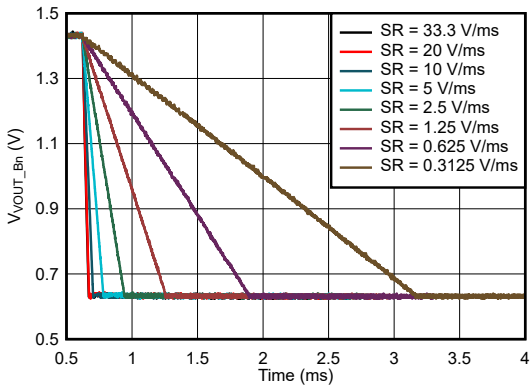
V_{PVIN_Bn} = 3.3 V Buck VSET = 1.0 V TA = 25°C

Figure 7-3. Buck Phase Adding and Shedding



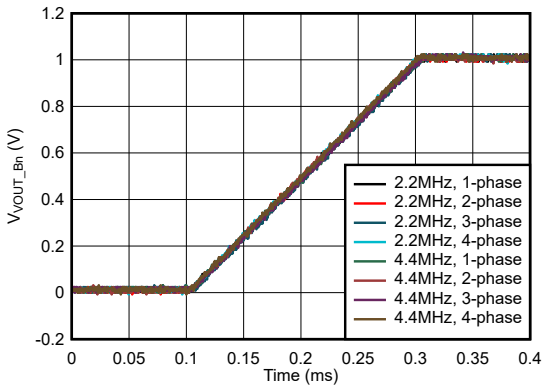
V_{PVIN_Bn} = 3.3 V Buck VSET = 0.6 V to 1.4 V TA = 25°C

Figure 7-4. Buck Ramp-up Slew Rate



V_{PVIN_Bn} = 3.3 V Buck VSET = 1.4 V to 0.6 V TA = 25°C

Figure 7-5. Buck Ramp-down Slew Rate



V_{PVIN_Bn} = 3.3 V Buck VSET = 1 V Slew Rate = 5 V/ms

Figure 7-6. Buck Start-up with no Load, Auto Mode

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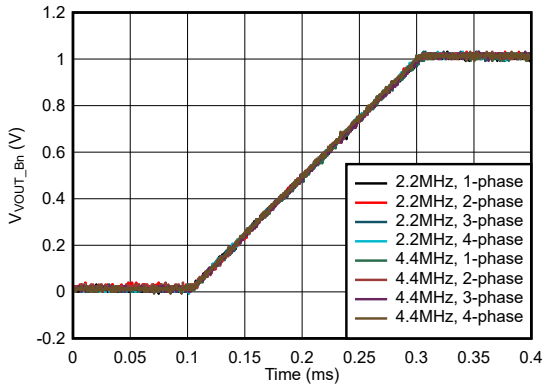
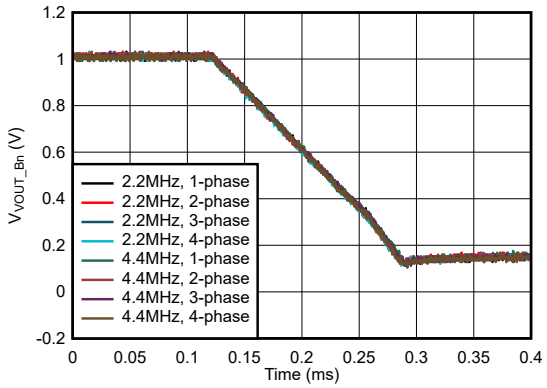
7.21 Typical Characteristics (continued)



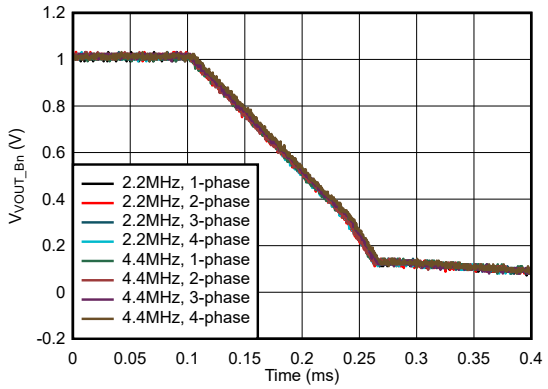
V_{PVIN_Bn} = 3.3 V Buck VSET = 1 V Slew Rate = 5 V/ms

Figure 7-7. Buck Start-up with 1A Load, Auto Mode



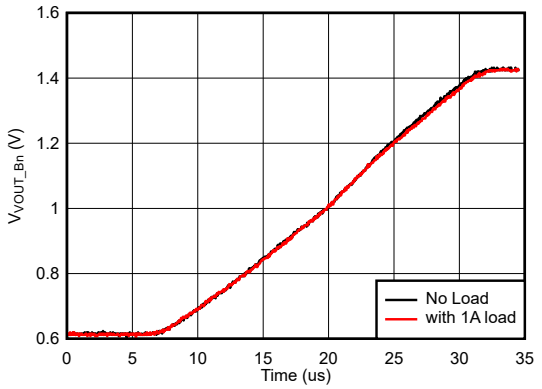
V_{PVIN_Bn} = 3.3 V Buck VSET = 1 V Slew Rate = 5 V/ms

Figure 7-8. Buck Shutdown with no Load, Auto Mode



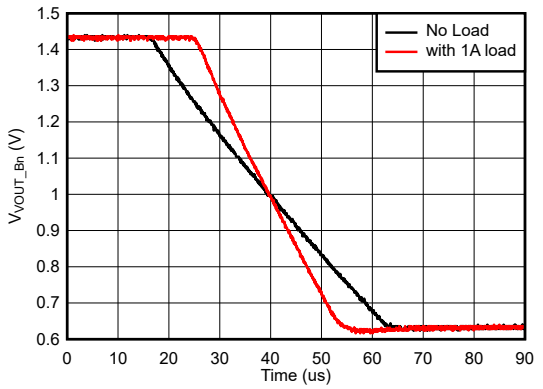
V_{PVIN_Bn} = 3.3 V Buck VSET = 1 V Slew Rate = 5 V/ms

Figure 7-9. Buck Shutdown with 1A Load, Auto Mode



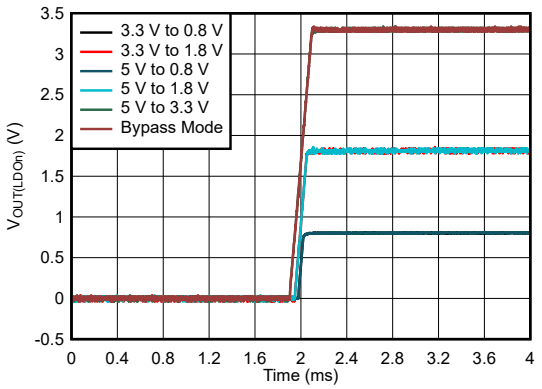
V_{PVIN_Bn} = 3.3 V Buck VSET = 0.6 V to 1.4 V Slew Rate = 33.3 V/ms

Figure 7-10. Buck Ramp-up with and without Load



V_{PVIN_Bn} = 3.3 V Buck VSET = 1.4 V to 0.6 V Slew Rate = 33.3 V/ms

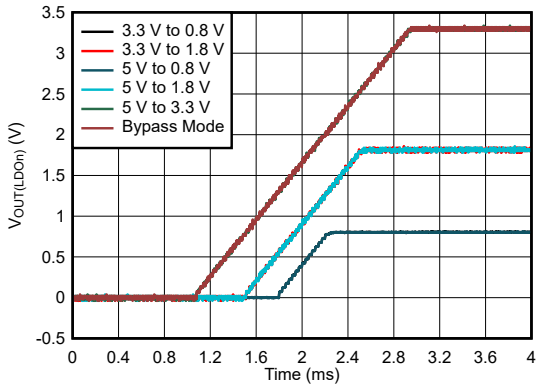
Figure 7-11. Buck Ramp-down with and without Load



$V_{IN(LDOn)}$ = 3.3 V or 5 V TA = 25°C

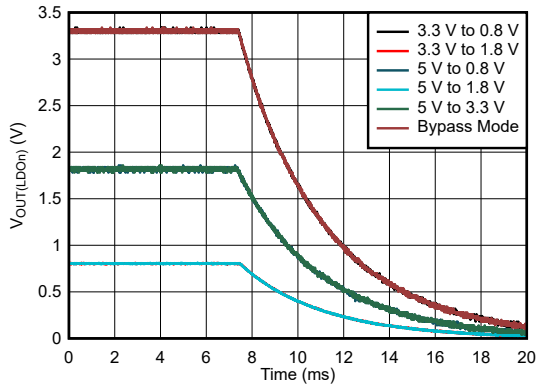
Figure 7-12. GPLDO Start-up with LDOn_SLOW_RAMP = 0

7.21 Typical Characteristics (continued)



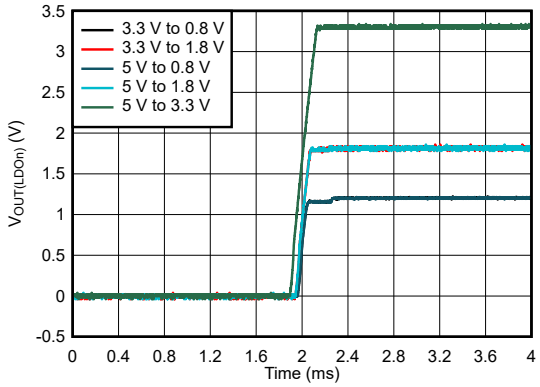
$V_{IN(LDOn)}$ = 3.3 V or 5 V TA = 25°C

Figure 7-13. GPLDO Start-up with LDOn_SLOW_RAMP = 1



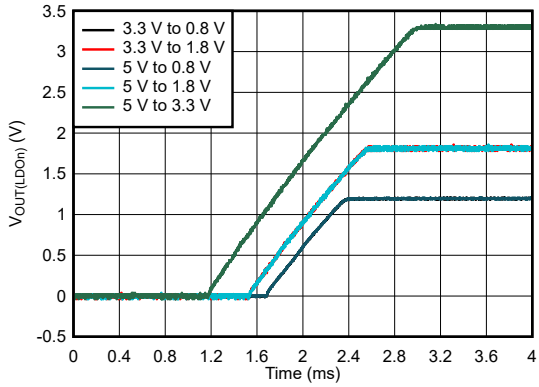
$V_{IN(LDOn)}$ = 3.3 V or 5 V LDOn_PLDN = 500 Ω TA = 25°C

Figure 7-14. GPLDO Shutdown



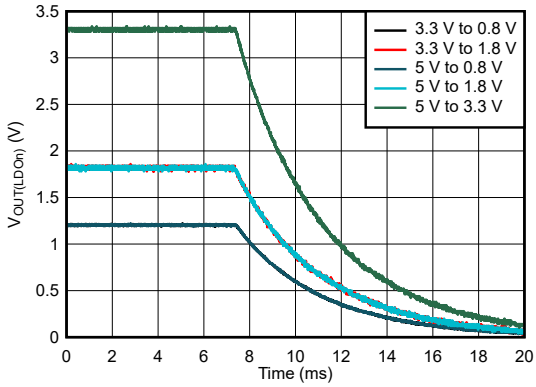
$V_{IN(LDOn)}$ = 3.3 V or 5 V TA = 25°C

Figure 7-15. LNLDO Start-up with LDOn_SLOW_RAMP = 0



$V_{IN(LDOn)}$ = 3.3 V or 5 V TA = 25°C

Figure 7-16. LNLDO Start-up with LDOn_SLOW_RAMP = 1



$V_{IN(LDOn)}$ = 3.3 V or 5 V LDOn_PLDN = 500 Ω TA = 25°C

Figure 7-17. LNLDO Shutdown

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8 Detailed Description

8.1 Overview

The TPS6594-Q1 device is a Power-Management Integrated Circuit (PMIC), available in a 56-pin, 0.5-mm pitch, 8-mm × 8-mm QFN package. It is designed for powering embedded systems or System on Chip (SoC) in automotive or industrial applications. It provides five configurable BUCK regulators, of which four rails have the ability to combine outputs in multi-phase mode. BUCK4 has the ability to supply up to 4 A output current in single-phase mode, while BUCK1, BUCK2, and BUCK3 have the ability to supply up to 3.5 A output current in single-phase mode. When working in multi-phase mode, each BUCK1, BUCK2, BUCK3, and BUCK4 can supply up to 3.5 A output current per phase, adding up to 14 A output current in four-phase configuration. BUCK5 is a single-phase only BUCK regulator, which supports up to 2 A output current. All five of the BUCK regulators have the capability to sink a current up to 1 A, and support dynamic voltage scaling. Double-buffered voltage scaling registers enable each BUCK regulator to transition to a different voltage during operation by SPI or I^2C. A digital PLL enables the BUCK regulators to synchronize to an external clock input, with phase delays between the output rails.

The TPS6594-Q1 device also provides three LDO rails, which can supply up to 500 mA output current per rail and can be configured in bypass mode and used as a load switch. One additional low-noise LDO rail can supply up to 300 mA output current. The 500-mA LDOs support 0.6 V to 3.3 V output voltage with 50-mV step. The 300-mA low-noise LDO supports 1.2 V to 3.3 V output voltage with 25-mV step. The output voltages of the LDOs can be pre-configured through the SPI or I^2C interfaces, which are used to configure the power rails and the power states of the TPS6594-Q1 device.

I^2C channel 1 (I2C1) is the main channel with access to the registers, which control the configurable power sequencer, the states and the outputs of power rails, the device operating states, the RTC registers and the Error Signal Monitors. I^2C channel 2 (I2C2), which is available through the GPIO1 and GPIO2 pins, is dedicated for accessing the Q&A Watchdog communication registers. If GPIO1 and GPIO2 are not configured as I2C2 pins, I2C1 can access all of the registers, including the Q&A Watchdog registers. Alternatively, depending on the NVM-configuration of the orderable part number, SPI is the selected interface for the device and can be used to access all registers.

The TPS6594-Q1 device includes an internal RC-oscillator to sequence all resources during power up and power down. Two internal LDOs (LDOVINT and LDOVRTC) generate the supply for the entire digital circuitry of the device as soon as the external input supply is available through the VCCA input. A backup battery supply input can also be used to power the RTC block and a 32-kHz Crystal Oscillator clock generator in the event of main supply power loss.

TPS6594-Q1 device has eleven GPIO pins each with multiple functions and configurable features. All of the GPIO pins, when configured as general-purpose output pins, can be included in the power-up and power-down sequence and used as enable signals for external resources. In addition, each GPIO can be configured as a wake-up input or a sleep-mode trigger. The default configuration of the GPIO pins comes from the non-volatile memory (NVM), and can be re-programmed by system software if the external connection permits.

The TPS6594-Q1 device includes a watchdog with selectable trigger or Q&A modes to monitor MCU software lockup, and two error signal monitor (ESM) inputs with fault injection options to monitor the lock-step signal of the attached SoC or MCU. TPS6594-Q1 includes protection and diagnostic mechanisms such as voltage monitoring on the input supply, input over-voltage protection, voltage monitoring on all BUCK and LDO regulator outputs, CRC on configuration registers, CRC on non-volatile memory, CRC on communication interfaces, current-limit and short-circuit protection on all output rails, thermal pre-warning, and over-temperature shutdown. The device also includes a Q&A or trigger mode watchdog to monitor for MCU software lockup, and two Error Signal Monitor inputs with selectable level mode or PWM mode, and with fault injection options to monitor the error signals from the attached SoC or MCU. The TPS6594-Q1 can notify the processor of these events through the interrupt handler, allowing the MCU to take action in response.

An SPMI interface is included in the TPS6594-Q1 device to distribute power state information to at most five satellite PMICs on the same network, thus enabling synchronous power state transition across multiple PMICs in the application system. This feature allows the consolidation of IO control signals from up to six PMICs powering the system into one primary TPS6594-Q1 PMIC.

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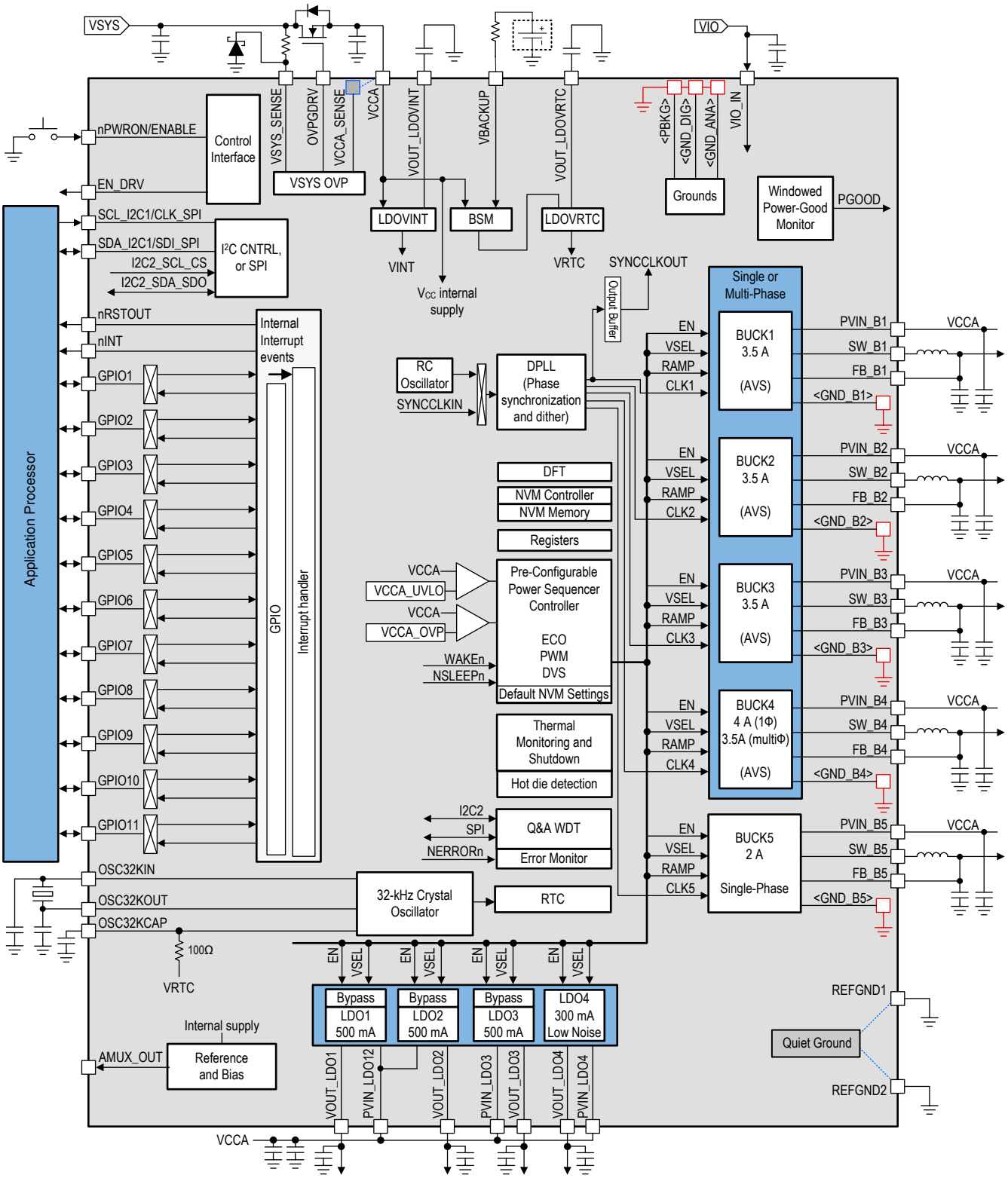
8.2 Functional Block Diagram



* These red squares are internal pads for down-bonds to the package thermal/ground pad.

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8.3 Feature Description

8.3.1 System Supply Voltage Monitor and Over-Voltage Protection

The TPS6594-Q1 device includes an over-voltage protection mechanism through a 12-V compliant input monitor at the VSYS_SENSE pin. When an over-voltage is detected at the VSYS_SENSE pin, OVPGDRV pin is pulled low to disable the external high voltage load switch, which connects the VSYS supply to the VCCA pin. After the over-voltage condition is cleared, the voltage at the OVPGDRV pin recovers after the voltage at the VSYS_SENSE pin stays below $V_{VSYS_RC_TH}$ for at least $_{VSYS_RC_TH}$.

The voltage at the OVPDRV has following relation with the voltage at the VSYS-SENSE pin:

- For VSYS_SENSE < 2.7V: OVPGDRV = 0V
- For 2.7V ≤ VSYS_SENSE ≤ 4.5V: OVPGDRV ≈ 0.9 * 3 * VSYS_SENSE
- For 4.5V < VSYS_SENSE ≤ 6V: OVPGDRV = 12V (in case of a fault in the regulation loop of the internal charge pump, OVPGDRV is limited to 12.5V)
- For VSYS_SENSE > 6V: OVPGDRV = 0V

TI recommends connecting a 10-V zener diode to ground at the VSYS_SENSE pin and one or more series resistors between the VSYS_SENSE pin and the pre-regulator output to limit the current surge and protect the VSYS_SENSE pin from an over-voltage condition due to possible short at the pre-regulator output. The voltage slew rate at the VSYS_SENSE pin must be limited to ≤ V_{VSYS_SR} to prevent possible damage to the device.

After the TPS6594-Q1 device has detected a VCCA over voltage condition, the VCCA domain is unpowered and does not signal the over voltage condition to the VSYS over-voltage protection module. Therefore, a dead-lock mechanism is implemented in the VSYS domain by setting a latch to keep the external high voltage load switch (between VSYS and VCCA) open once the TPS6594-Q1 device has detected a VCCA over voltage condition.

The TPS6594-Q1 first checks for possible fail-short condition of the external FET at initial power up. The diagnostic mechanism pulls the OVPDGRV pin low when VCCA reaches $V_{OVP_FET_Short_TH}$, and waits until the voltage on the VCCA pin decreases by $V_{OVP_FET_Short_Hyst}$ before it pulls the OVPGDRV pin high again. This mechanism effectively disconnects the VCCA pin from VSYS in case of a FET fail-short condition; with the addition of the diagnostic comparator, however, it also causes a non-monotonic power up behavior with an RC delay at the VCCA pin. The RC-delay is associated with the input capacitance at the VCCA pin and the internal pull-down resistor value $R_{VCCA_OVP_PD}$.

The comparator module in TPS6594-Q1, which monitors the voltage on the VCCA pins, controls the power state machine of the device. VCCA voltage detection outputs determine the power states of the device as follows:

VCCA_UVLO The TPS6594-Q1 returns to the BACKUP state. LDOVRTC is powered by the output of the Backup Supply Management (BSM) module during the BACKUP state. The device returns to the NO SUPPLY state and is completely shut down when the input supply of the LDOVRTC falls below the operating range. The device cannot return to the BACKUP state from the NO SUPPLY state.

VCCA_UV The TPS6594-Q1 transitions from the NO SUPPLY state to the INIT state when the voltage on the VCCA pin rises above VCCA_UV during initial power-up.

VCCA_OVP If the voltage on VCCA pin rises above the VCCA_OVP threshold while TPS6594-Q1 is in operation , despite the OVPGDRV mechanism, then the device clears the ENABLE_DRV bit and starts the immediate shutdown sequence.

A separate voltage comparator monitors whether or not the VCCA voltage is within the expected PGOOD range when VCCA is expected to be 5-V or 3.3-V. This voltage comparator checks at device power-up whether the voltage on the VCCA supply pin is above the VCCA_UV threshold. Refer to Section 8.3.4 for additional detail on the operation of the PGOOD monitor function.

LDOVINT, which is the internal supply to the digital core of the device, may attempt to restart the device when the input voltage at VCCA pin falls or stays between VCCA_UVLO and VCCA_UV voltage levels; the voltage at the VCCA pin, however, must be above the VCCA_UV voltage level for the device to power up properly.

Figure 8-1 shows a block diagram of the system input monitoring and over-voltage protection mechanism, and the generation of the VCCA_UVLO and VCCA_OVP power state control signals.

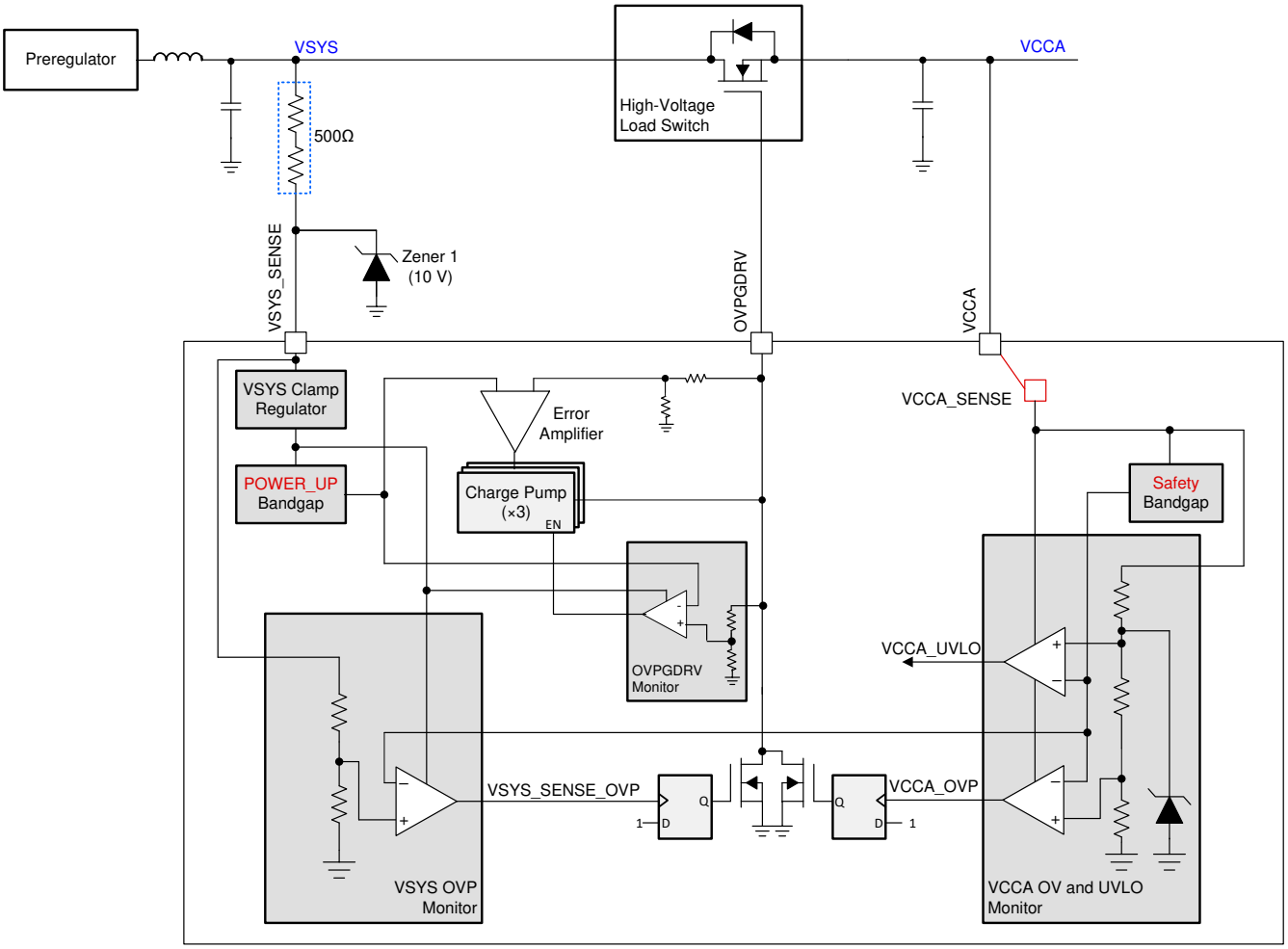

Figure 8-1. VSYS Monitor and OVPGDRV Output Generation

8.3.2 Power Resources (Bucks and LDOs)

The power resources provided by the TPS6594-Q1 device includes synchronous, current mode control bucks and linear LDOs. These supply resources provide power to the external processors, components, and modules inside the TPS6594-Q1 device. The supply of the bucks, the PVIN_Bx pins, must connect to the VCCA pin externally. The supply of the LDOs, the PVIN_LDOx pins, may connect to the VCCA pin or a buck output which is at a lower voltage level than the VCCA.

The voltage output of each power resource is continuously monitored by a dedicated analog monitor on an independent reference voltage domain. An unused regulator can also be used as a voltage monitor for an external rail by connecting the external rail to the FB_Bn the VOUT_LDOn pin. A residual voltage checking option is also available for each power resource to ensure the output voltage has dropped below 150 mV before it can be powered up again.

Table 8-1 lists the power resources provided by the TPS6594-Q1 device.

Table 8-1. Power Resources

RESOURCE	TYPE	VOLTAGE	CURRENT CAPABILITY	COMMENTS
BUCK1, BUCK2, BUCK3	BUCK	0.3 V to 0.6 V, 20-mV steps 0.6 V to 1.1 V, 5-mV steps 1.1 V to 1.66 V, 10-mV steps 1.66 V to 3.34 V, 20-mV steps	3.5 A	Can be configured in multi-phase mode or stand-alone in single-phase mode

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Table 8-1. Power Resources (continued)

RESOURCE	TYPE	VOLTAGE	CURRENT CAPABILITY	COMMENTS
BUCK4	BUCK	0.3 V to 0.6 V, 20-mV steps 0.6 V to 1.1 V, 5-mV steps 1.1 V to 1.66 V, 10 mV steps 1.66 V to 3.34 V, 20-mV steps	4 A in single-phase mode 3.5 A in multi-phase mode	Can be configured in multi-phase mode or stand-alone in single-phase mode
BUCK5	BUCK	0.3 to 0.6 V, 20-mV steps 0.6 V to 1.1 V, 5-mV steps 1.1 V to 1.66 V, 10-mV steps 1.66 V to 3.34 V , 20-mV steps	2 A	Only in single-phase mode
LDO1, LDO2, LDO3	LDO	0.6 V to 3.3 V, 50-mV steps	500 mA	Bypass mode configurable
LDO4	LDO	1.2 V to 3.3 V, 25-mV steps	300 mA	Low-noise

8.3.2.1 Buck Regulators

8.3.2.1.1 BUCK Regulator Overview

The TPS6594-Q1 includes five synchronous buck converters, of which four can be combined in multi-phase configuration. All of the buck converters support the following features:

- Automatic mode control based on the loading (PFM or PWM mode) or Forced-PWM mode operation
- External clock synchronization option to minimize crosstalk
- Optional spread spectrum technique to reduce EMI
- Soft start
- AVS support with configurable slew-rate
- Windowed undervoltage and overvoltage monitors with configurable threshold
- Windowed voltage monitor for external supply when the buck converter is disabled
- Output Current Limit
- Short-to-Ground Detection on SW_Bx pins at start-up of the buck regulator

When the outputs of these buck converters are combined in multi-phase configuration, it also supports the following features:

- Current balancing between the phases of the converter
- Differential voltage sensing from point of the load
- Phase shifted outputs for EMI reduction
- Optional dynamic phase shedding or adding

There are two modes of operation for the buck converter, depending on the required output current: pulse-width modulation (PWM) and pulse-frequency modulation (PFM). The converter operates in PWM mode at high load currents of approximately 600 mA or higher. Lighter output current loads cause the converter to automatically switch into PFM mode for reduced current consumption. The device avoids pulse skipping and allows easy filtering of the switch noise by external filter components when forced-PWM mode is selected (BUCKn_FPWM = 1). The forced-PWM mode is the recommended mode of operation for the buck converter to achieve better ripple and transient performance. The drawback of this forced-PWM mode is the higher quiescent current at low output current levels.

When operating in PWM mode the phases of a multi-phase regulator are automatically added or shed based on the load current level. The forced multi-phase mode can be enabled for lower ripple at the output.

Figure 8-2 shows a block diagram of a single core.

Figure 8-3 shows the interleaving switching action of the multi-phase converters.

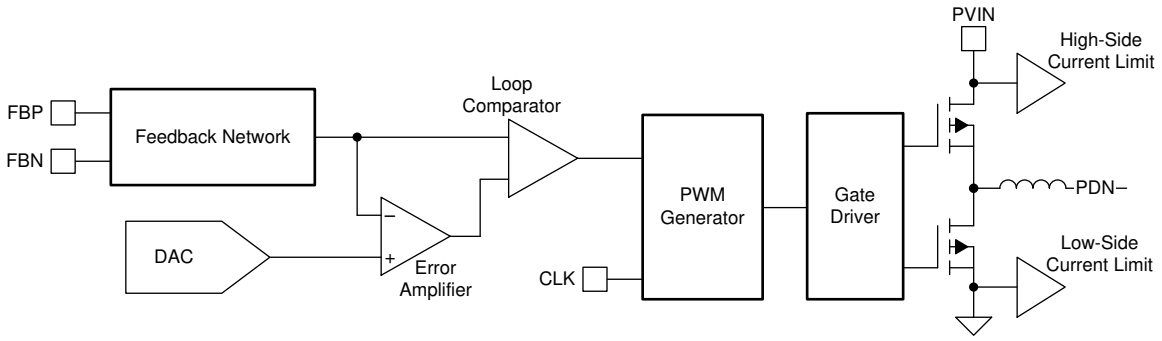

Figure 8-2. BUCK Core Block Diagram

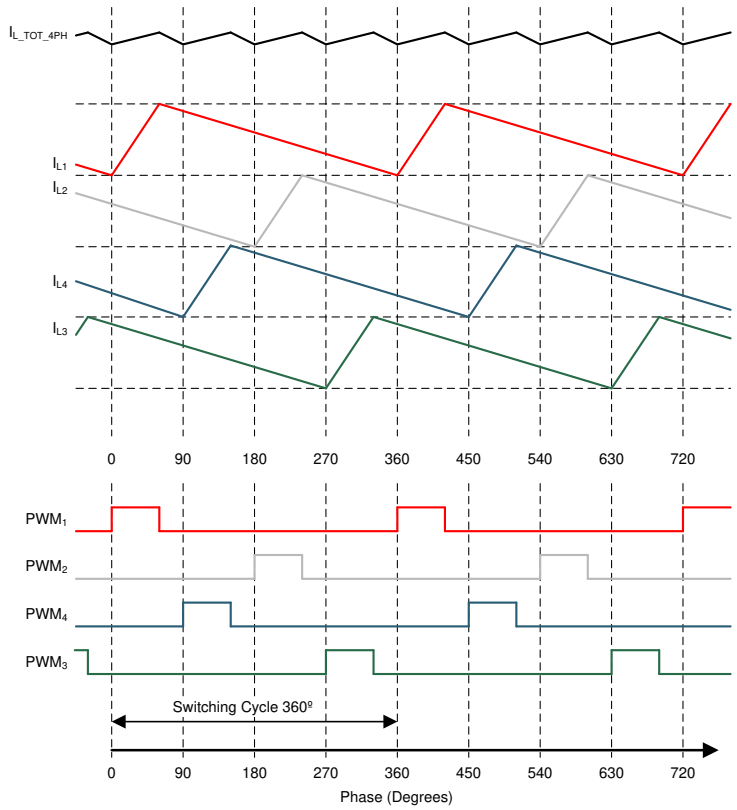

Figure 8-3. Example of PWM Timings, Inductor Current Waveforms, and Total Output Current in 4-Phase Configuration. [1]

8.3.2.1.2 Multi-Phase Operation and Phase-Adding or Shedding

The 4-phase converters (BUCK1, BUCK2, BUCK3, and BUCK4) switches each channel 90° apart under heavy load conditions. As a result, the 4-phase converter has an effective ripple frequency four times greater than the switching frequency of any one phase. In the same way, 3-phase converter has an effective ripple frequency three times greater and 2-phase converter has an effective ripple frequency two times greater than the switching frequency of any one phase; the parallel operation, however, decreases the efficiency at light load conditions. The TPS6594-Q1 can change the number of active phases to optimize efficiency for the variations of the load in order to overcome this operational inefficiency. The process in which the multi-phase buck regulator in case of increasing load current automatically increases the number of active phases is called phase adding. The process in which the multi-phase buck regulator in case of decreasing load current automatically decreases the number of active phases is called phase shedding. The concept is shown in Figure 8-4.

[1] Graph is not in scale and is for illustrative purposes only.

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The converter can be forced to multi-phase operation by the BUCKn_FPWM_MP bit in BUCKn_CTRL1 register. If the regulator operates in forced multi-phase mode , each phase automatically operates in the forced-PWM mode. If the multi-phase operation is not forced, the number of phases are added and shed automatically to follow the required output current.

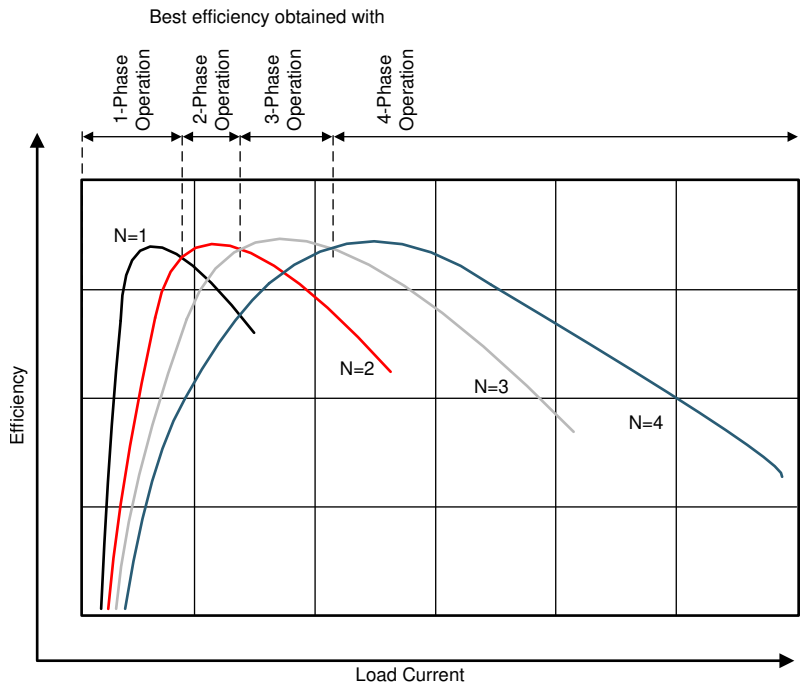

Figure 8-4. Multiphase BUCK Converter Efficiency vs Number of Phases (Converters in PWM Mode) [2]

8.3.2.1.3 Transition Between PWM and PFM Modes

The forced-PWM mode operation with phase-adding or shedding optimizes efficiency at mid-to-full load. TheTPS6594-Q1 converter operates in PWM mode at load current of about 600 mA or higher. The device automatically switches into PFM mode for reduced current consumption when forced-PWM mode is disabled (BUCKn_FPWM = 0) at lighter load-current levels. A high efficiency is achieved over a wide output-load-current range by combining the PFM and the PWM modes.

8.3.2.1.4 Multi-Phase BUCK Regulator Configurations

The control of the multi-phase regulator settings is done using the control registers of the primary BUCK regulator in the multi-phase configuration. The TPS6594-Q1 ignores settings in the following registers of the secondary/tertiary/quatenary BUCK regulators :

- BUCKn_CTRL register, except BUCKn_VMON_EN and BUCKn_RV_SEL
- BUCKn_CONF register
- BUCKn_VOUT_1 and BUCKn_VOUT_2 registers
- BUCKn_PG_WINDOW register
- Interrupt bits related to the secondary/tertiary/quatenary BUCK regulator, except BUCKn_ILIM_INT, BUCKn_ILIM_MASK and BUCKn_ILIM_STAT

Table 8-2 shows the supported Multi-Phase BUCK regulator configurations and the assigned primary BUCK regulator in each configuration.

Table 8-2. Primary BUCK Assignment for Supported Multi-phase Configuration

Supported Multi-Phase BUCK Regulator Configuration	Primary BUCK Assignment
4-Phase: BUCK1 + BUCK2 + BUCK3 + BUCK4	BUCK1
3-Phase: BUCK1 + BUCK2 + BUCK3	BUCK1

[2] Graph is not in scale and is for illustrative purposes only.

Table 8-2. Primary BUCK Assignment for Supported Multi-phase Configuration (continued)

Supported Multi-Phase BUCK Regulator Configuration	Primary BUCK Assignment
2-Phase: BUCK1 + BUCK2	BUCK1
2-Phase: BUCK3 + BUCK4	BUCK3

When the BUCK regulators are configured in 3-phase or 4-phase configurations, there are exceptions to the above list of registers that the TPS6594-Q1 ignores. The configuration registers are user-configurable for the voltage monitor function on BUCK3 and BUCK4 in a 4-phase configuration and BUCK3 in a 3-phase configuration. The UV/OV voltage monitors of these BUCK3 and BUCK4 regulators can be used to monitor external supply rails, by connecting these external rails to the FB_Bn pins of these BUCK3 and BUCK4 regulators. The following list of registers and register bits for BUCK3 and BUCK4 can be used to enable and set the target voltage for the external voltage monitoring function under such configuration:

- BUCKn_VMON_EN bit
- BUCKn_RV_SEL bit
- BUCKn_VSEL bit
- BUCKn_SLEW_RATE
- BUCKn_VOUT_1 and BUCKn_VOUT_2 registers
- BUCKn_PG_WINDOW register

Customers are responsible for the values set in these registers when using BUCK3 or BUCK4 to monitor an external supply under the 3-phase or 4-phase configuration. If the voltage monitor function is not used under such a scenario, the FB_Bn pins must be connected to the reference ground, and the BUCKn_VMON_EN and BUCKn_RV_SEL bits must be set to '0'.

8.3.2.1.5 Spread-Spectrum Mode

The TPS6594-Q1 device supports spread-spectrum modulation of the switching clock signal used by the BUCK regulators. Three factory-selectable modulation modes are available: the first mode is modulation from external input clock at the SYNCCLKIN pin; the second mode is modulating the input clock at the SYNCCLKIN pin using the DPLL; the third mode is modulating the internal 20-MHz RC-Oscillator clock using the DPLL.

The spread-spectrum modulation mode is pre-configured in NVM. Changing this modulation mode during operation is not supported.

The modulation frequency range is limited by the DPLL bandwidth. The max frequency spread for the input clock to the DPLL is ±18% to secure parametric compliance of the BUCK output performance.

The internal modulation is disabled by default and can be enabled and configured after power up. Internal modulation is activated by setting the SS_EN control bit. The internal modulation must be disabled (SS_EN = 0) when changing the following parameter:

- SS_DEPTH[1:0] – Spread Spectrum modulation depth

When internal modulation is enabled and configured, it can be disabled by the system MCU during operation. The device transition to different mission states does not impact internal modulation when it is enabled and configured.

8.3.2.1.6 Adaptive Voltage Scaling (AVS) and Dynamic Voltage Scaling (DVS) Support

An AVS or a DVS voltage value can be configured by the attached MCU after the BUCK regulator is powered up to the default output voltage selected in register BUCKn_VSET1, which loads its default value from NVM. The purpose of the AVS/DVS voltage is to set the BUCK output voltage to enable optimal efficiency and performance of the attached SoC.

All of BUCK regulators in the TPS6594-Q1 device support AVS and DVS voltage scaling changes. Once the AVS/DVS voltage value is written into the BUCKn_VSET1 or BUCKn_VSET2 register, and the MCU sets the BUCKn_VSEL register to select the AVS/DVS voltage, the output of the BUCK regulator remains at the AVS/DVS voltage level instead of the default voltage from NVM until one of the following events occur:

- Error that causes the device to re-initialize itself through a power cycle after reaching the SAFE RECOVERY state

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- Error that causes the device to execute warm reset
- MCU configures the device to enter the LP STANDBY state

Figure 8-5 shows the arbitration scheme for loading the output level of the BUCK regulator from the AVS register using the BUCKn_VSET control registers.

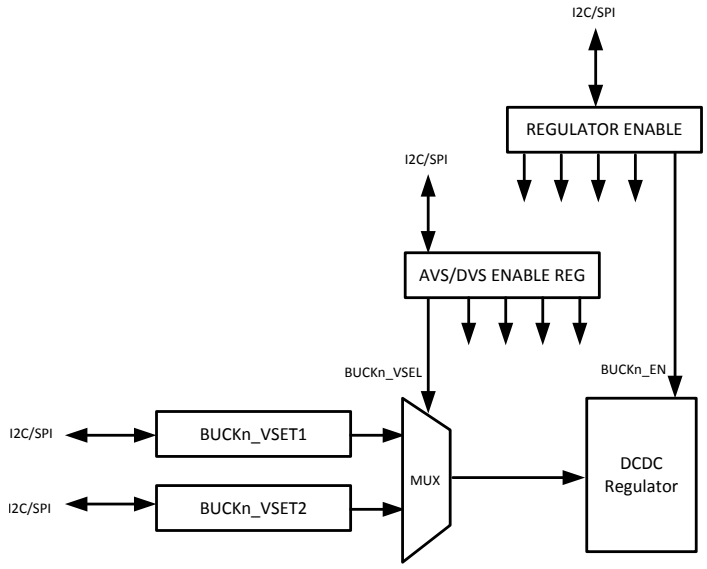

Figure 8-5. AVS/DVS Configuration Register Arbitration Diagram

The digital control block automatically updates the OV and UV threshold of the BUCK output voltage monitor during the AVS or DVS voltage change. When the output voltage is increased, the OV threshold is updated at the same time the BUCKn_VSETx is updated to the AVS voltage level, while the UV threshold is updated after a delay calculated by Equation 1.

When the output voltage is decreased, the UV threshold is updated at the same time the BUCKn_VSETx is updated to the AVS voltage level, while the OV threshold is updated after a delay calculated by Equation 1.

$$t_{PG_OV_UV_DELAY} = (dV / BUCKn_SLEW_RATE) + t_{settle_Bx} \quad (1)$$

In order to prevent erroneous voltage monitoring, the digital block also temporarily masks the results of the OV and UV monitor from the regulator output when the BUCK regulator is enabled and the voltage is rising to the BUCKn_VSETx level. The duration of the mask starts from the time the BUCK regulator is enabled. The BUCK OV monitor output is masked for a fixed delay time of $t_{PG_OV_GATE}$, which is approximately 115 µs – 128 µs. The UV monitor output is masked for the time duration calculated by Equation 2. The 370-µs additional delay time in the formula includes the start-up delay of the BUCK regulator, the fixed delay after the ramp, and the time for the BIST operation of the OV and UV monitors.

$$t_{PG_UV_GATE} = (BUCKn_VSET / BUCKn_SLEW_RATE) + 370\ \mu s \quad (2)$$

Note

Because output capacitance, forward and negative current limits and load current of the BUCK regulator may affect the slew rate of the BUCK regulator output voltage, the delay time of $t_{PG_UV_GATE}$ may not be sufficient long for the slower slew rate setting when the target BUCK regulator output voltage is higher. Please refer to the PMIC User's Guide for detail information about the supported voltage level and slew rate setting combinations of a particular orderable part number.

Figure 8-6 and Figure 8-7 are timing diagrams illustrating the voltage change for AVS and DVS enabled BUCK regulators and the corresponding OV and UV monitor threshold changes.

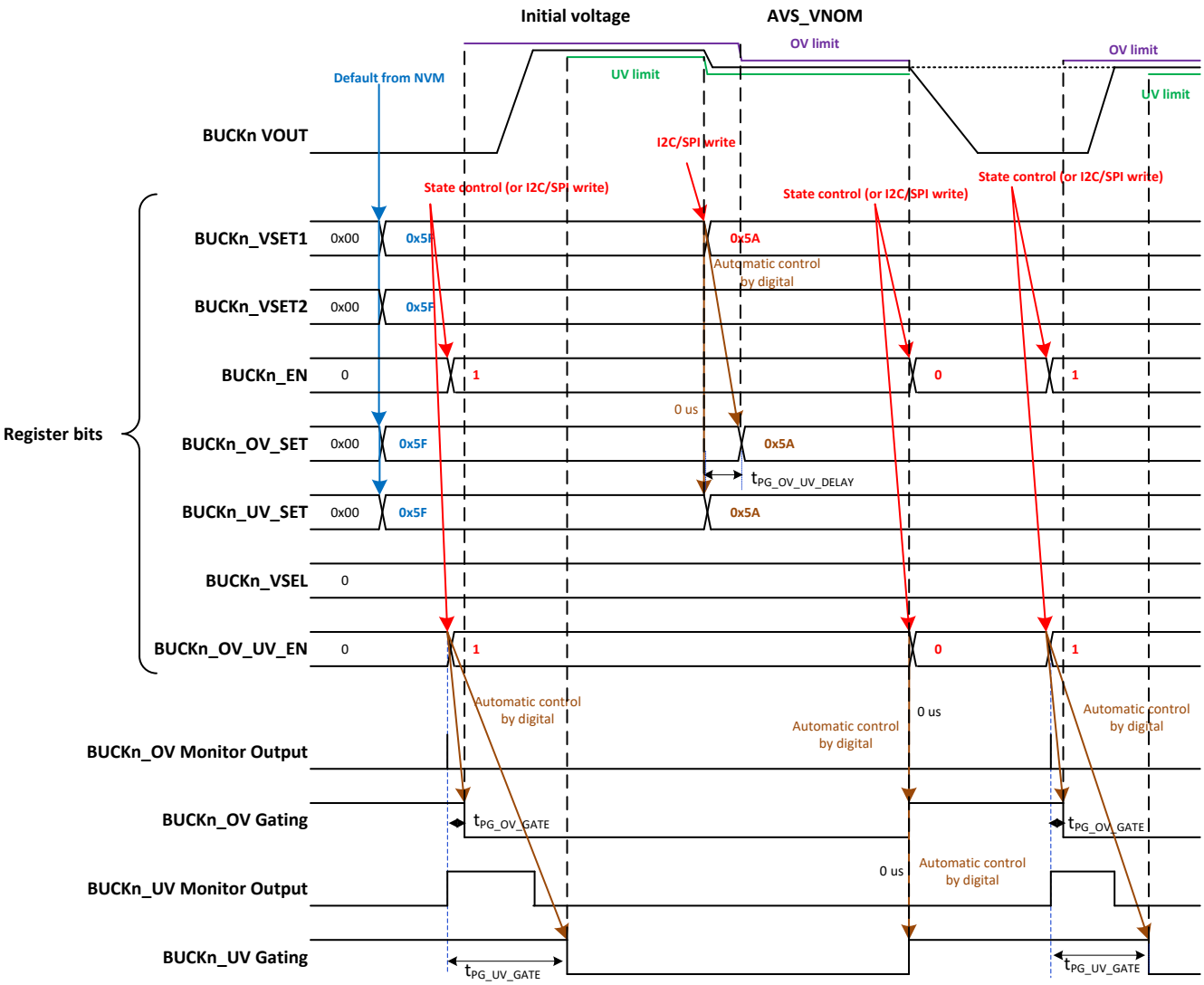

Figure 8-6. AVS Voltage and OV UV Threshold Level Change Timing Diagram

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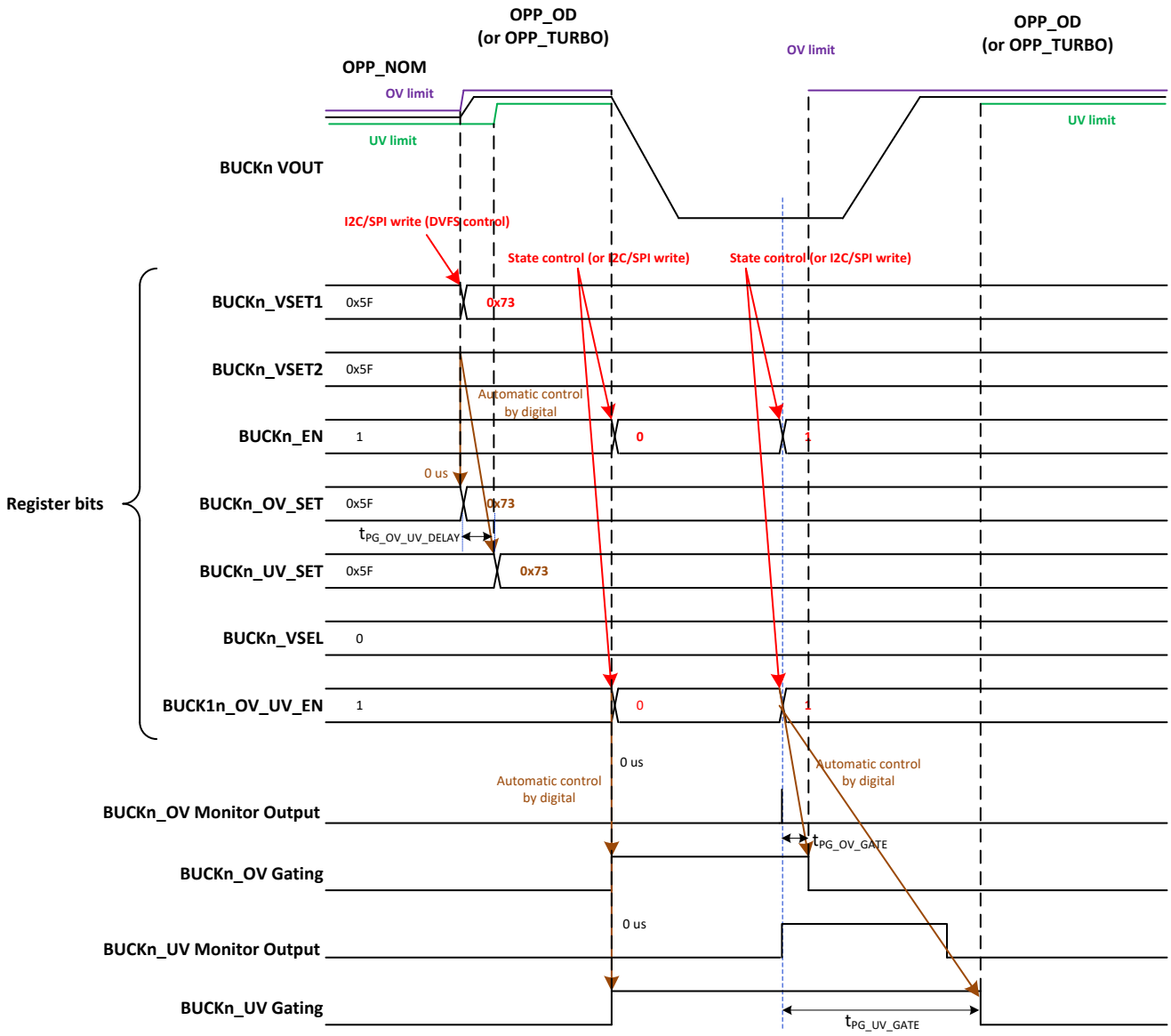

Figure 8-7. DVS Voltage and OV UV Threshold Level Change Timing Diagram

8.3.2.1.7 BUCK Output Voltage Setting

Table 8-3 shows the coding used to select the BUCK regulator output voltage.

Table 8-3. Output Voltage Selection for BUCK Regulators

BUCKn_VSE Tn	Output Voltage [V] 20 mV steps	BUCKn_VSE Tn	Output Voltage [V] 5 mV steps	BUCKn_VSE Tn	Output Voltage [V] 5 mV steps	BUCKn_VSE Tn	Output Voltage [V] 10 mV steps	BUCKn_VSE Tn	Output Voltage [V] 20 mV steps	BUCKn_VSE Tn	Output Voltage [V] 20 mV steps
0x00	0.3	0x0F	0.6	0x41	0.85	0x73	1.1	0xAB	1.66	0xD6	2.52
0x01	0.32	0x10	0.605	0x42	0.855	0x74	1.11	0xAC	1.68	0xD7	2.54
0x02	0.34	0x11	0.61	0x43	0.86	0x75	1.12	0xAD	1.7	0xD8	2.56
0x03	0.36	0x12	0.615	0x44	0.865	0x76	1.13	0xAE	1.72	0xD9	2.58
0x04	0.38	0x13	0.62	0x45	0.87	0x77	1.14	0xAF	1.74	0xDA	2.6
0x05	0.4	0x14	0.625	0x46	0.875	0x78	1.15	0xB0	1.76	0xDB	2.62
0x06	0.42	0x15	0.63	0x47	0.88	0x79	1.16	0xB1	1.78	0xDC	2.64
0x07	0.44	0x16	0.635	0x48	0.885	0x7A	1.17	0xB2	1.8	0xDD	2.66
0x08	0.46	0x17	0.64	0x49	0.89	0x7B	1.18	0xB3	1.82	0xDE	2.68
0x09	0.48	0x18	0.645	0x4A	0.895	0x7C	1.19	0xB4	1.84	0xDF	2.7
0x0A	0.5	0x19	0.65	0x4B	0.9	0x7D	1.2	0xB5	1.86	0xE0	2.72
0x0B	0.52	0x1A	0.655	0x4C	0.905	0x7E	1.21	0xB6	1.88	0xE1	2.74
0x0C	0.54	0x1B	0.66	0x4D	0.91	0x7F	1.22	0xB7	1.9	0xE2	2.76
0x0D	0.56	0x1C	0.665	0x4E	0.915	0x80	1.23	0xB8	1.92	0xE3	2.78
0x0E	0.58	0x1D	0.67	0x4F	0.92	0x81	1.24	0xB9	1.94	0xE4	2.8
		0x1E	0.675	0x50	0.925	0x82	1.25	0xBA	1.96	0xE5	2.82
		0x1F	0.68	0x51	0.93	0x83	1.26	0xBB	1.98	0xE6	2.84
		0x20	0.685	0x52	0.935	0x84	1.27	0xBC	2	0xE7	2.86
		0x21	0.69	0x53	0.94	0x85	1.28	0xBD	2.02	0xE8	2.88
		0x22	0.695	0x54	0.945	0x86	1.29	0xBE	2.04	0xE9	2.9
		0x23	0.7	0x55	0.95	0x87	1.3	0xBF	2.06	0xEA	2.92
		0x24	0.705	0x56	0.955	0x88	1.31	0xC0	2.08	0xEB	2.94
		0x25	0.71	0x57	0.96	0x89	1.32	0xC1	2.1	0xEC	2.96
		0x26	0.715	0x58	0.965	0x8A	1.33	0xC2	2.12	0xED	2.98
		0x27	0.72	0x59	0.97	0x8B	1.34	0xC3	2.14	0xEE	3.0
		0x28	0.725	0x5A	0.975	0x8C	1.35	0xC4	2.16	0xEF	3.02
		0x29	0.73	0x5B	0.98	0x8D	1.36	0xC5	2.18	0xF0	3.04
		0x2A	0.735	0x5C	0.985	0x8E	1.37	0xC6	2.2	0xF1	3.06

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Table 8-3. Output Voltage Selection for BUCK Regulators (continued)

BUCKn_VSE Tn	Output Voltage [V] 20 mV steps	BUCKn_VSE Tn	Output Voltage [V] 5 mV steps	BUCKn_VSE Tn	Output Voltage [V] 5 mV steps	BUCKn_VSE Tn	Output Voltage [V] 10 mV steps	BUCKn_VSE Tn	Output Voltage [V] 20 mV steps	BUCKn_VSE Tn	Output Voltage [V] 20 mV steps
		0x2B	0.74	0x5D	0.99	0x8F	1.38	0xC7	2.22	0xF2	3.08
		0x2C	0.745	0x5E	0.995	0x90	1.39	0xC8	2.24	0xF3	3.1
		0x2D	0.75	0x5F	1.0	0x91	1.4	0xC9	2.26	0xF4	3.12
		0x2E	0.755	0x60	1.005	0x92	1.41	0xCA	2.28	0xF5	3.14
		0x2F	0.76	0x61	1.01	0x93	1.42	0xCB	2.3	0xF6	3.16
		0x30	0.765	0x62	1.015	0x94	1.43	0xCC	2.32	0xF7	3.18
		0x31	0.77	0x63	1.02	0x95	1.44	0xCD	2.34	0xF8	3.2
		0x32	0.775	0x64	1.025	0x96	1.45	0xCE	2.36	0xF9	3.22
		0x33	0.78	0x65	1.03	0x97	1.46	0xCF	2.38	0xFA	3.24
		0x34	0.785	0x66	1.035	0x98	1.47	0xD0	2.4	0xFB	3.26
		0x35	0.79	0x67	1.04	0x99	1.48	0xD1	2.42	0xFC	3.28
		0x36	0.795	0x68	1.045	0x9A	1.49	0xD2	2.44	0xFD	3.3
		0x37	0.8	0x69	1.05	0x9B	1.5	0xD3	2.46	0xFE	3.32
		0x38	0.805	0x6A	1.055	0x9C	1.51	0xD4	2.48	0xFF	3.34
		0x39	0.81	0x6B	1.06	0x9D	1.52	0xD5	2.5		
		0x3A	0.815	0x6C	1.065	0x9E	1.53				
		0x3B	0.82	0x6D	1.07	0x9F	1.54				
		0x3C	0.825	0x6E	1.075	0xA0	1.55				
		0x3D	0.83	0x6F	1.08	0xA1	1.56				
		0x3E	0.835	0x70	1.085	0xA2	1.57				
		0x3F	0.84	0x71	1.09	0xA3	1.58				
		0x40	0.845	0x72	1.095	0xA4	1.59				
						0xA5	1.6				
						0xA6	1.61				
						0xA7	1.62				
						0xA8	1.63				
						0xA9	1.64				
						0xAA	1.65				

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8.3.2.1.8 BUCK Regulator Current Limit

Each BUCK regulator includes a Current Limit to protect the internal High-Side and Low-Side Power-FETs against over-current. The High-Side Current Limit, also referred to as Forward Current Limit, is for BUCK1..4 adjustable between 2.5 A and 5.5 A with 1-A steps with register bits BUCKx_ILIM[3:0]. For BUCK5, this Forward Current Limit has selectable levels 2.5 A and 3.5 A with register bits BUCK5_ILIM[3:0].

The Low-Side Current Limit, also referred to as Negative Current Limit, has a fixed value of typical 2 A.

8.3.2.1.9 SW_Bx Short-to-Ground Detection

Each BUCK regulator includes a SW_Bx Short-to-Ground Detection. This SW_Bx Short-to-Ground Detection monitors whether the SW_B1...SW_B5 pins have a short-to-ground condition, either caused by external short on these pins or caused by a short in the low-side power-FET of the BUCK regulator. This SW_Bx Short to Ground Detection is activated before the power-up of the BUCK regulator. When this function detects a short-to-ground condition on the SW_B1...SW_B5 pins, the TPS6594-Q1 aborts the power-up sequence and sets the corresponding interrupt bits BUCKx_SC_INT (x=1...5). After this, the TPS6594-Q1 transitions to the SAFE RECOVERY state, after which it performs an attempt to restart as described in Section 8.4.1.1.

8.3.2.1.10 Sync Clock Functionality

The TPS6594-Q1 device contains a SYNCCLKIN (GPIO10) input to synchronize switching clock of the BUCK regulator with the external clock. The block diagram of the clocking and PLL module is shown in Figure 8-8. The external clock is selected when the external clock is available, and SEL_EXT_CLK = '1'. The nominal frequency of the external input clock is set by EXT_CLK_FREQ[1:0] bits in the NVM and it can be 1.1 MHz, 2.2 MHz, or 4.4 MHz. The external SYNCCLKIN clock must be inside accuracy limits (–18%/+18%) of the typical input frequency for valid clock detection.

The EXT_CLK_INT interrupt is generated in case the external clock is expected (SEL_EXT_CLK = 1), but it is not available or the clock frequency is not within the valid range.

The TPS6594-Q1 device can also generate a clock signal, SYNCCLKOUT, for external device use. The SYNCCLKOUT_FREQ_SEL[1:0] selects the frequency of the SYNCCLKOUT. Note: SYNCCLKOUT_FREQ_SEL[1:0] must stay static while SYNCCLKOUT is used, as changing the output frequency selection can cause glitches on the clock output. The SYNCCLKOUT is available through GPIO8, GPIO9, or GPIO10.

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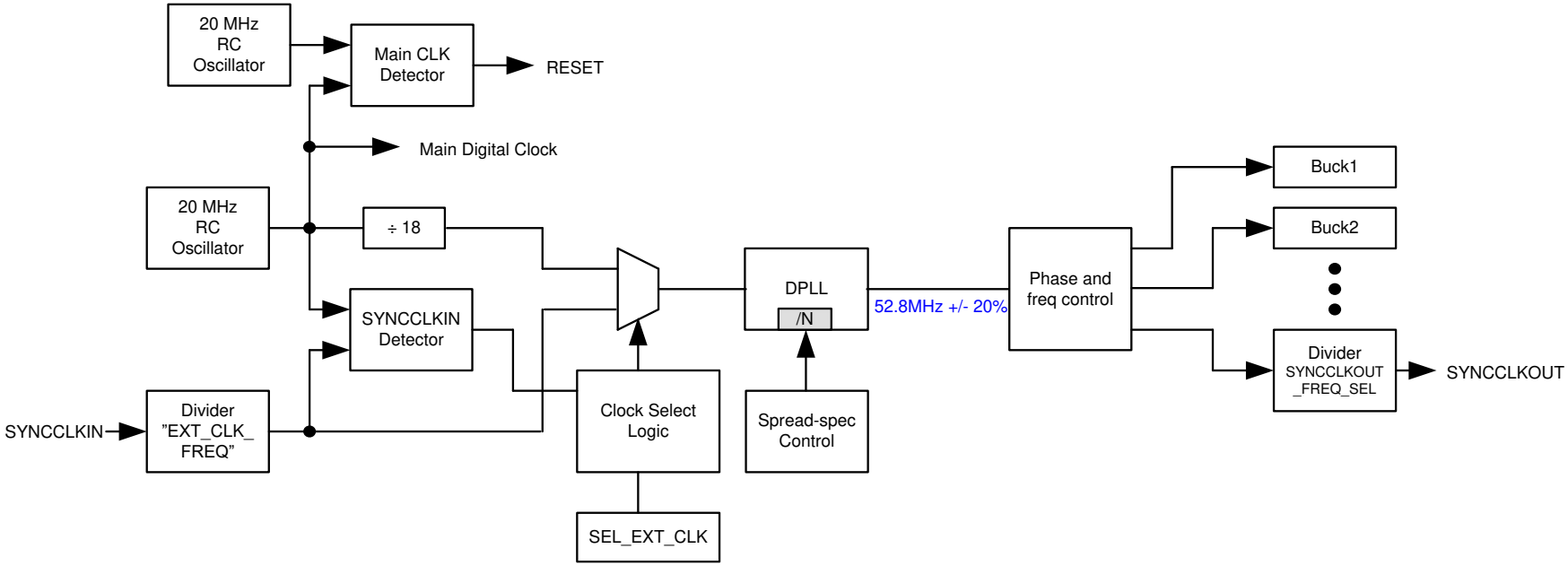

Figure 8-8. Sync Clock and DPLL Module

8.3.2.2 Low Dropout Regulators (LDOs)

All of the LDO regulators in the TPS6594-Q1 device can be supplied by the system supply or another pre-regulated voltage source which are within the specified VIN range. The PVIN_LDOn voltage level must be equal or less than the VCCA voltage level to ensure proper operation of the LDOs. The default output voltages of all LDOs are loaded from the NVM memory and can be configured by the LDOn_VSET[7:0]. There is no hardware protection to prevent software from selecting an improper output voltage if the minimum level of PVIN_LDOn is lower than the dropout voltage of the LDO regulator in addition to the configured LDO output voltage. In such conditions, the output voltage droops to near the PVIN_LDOn level.

Note

Writing a *RESERVED* value to the LDOn_VSET[7:0] register bits causes a LDOn_OV_INT or LDOn_UV_INT interrupt.

The LDO regulators do not have slew rate control for voltage ramp; by setting the LDOn_SLOW_RAMP bit to '1', however, the ramp up speed of the regulator output voltage is < 3 V/ms.

If an LDO is not needed, its associated UV/OV Voltage Monitor can be used to monitor an external voltage rail by connecting the external rail to the VOUT_LDOn pin. The voltage level of the monitored external rail must be within the PGOOD monitor range of the LDOn_VSET[7:0] of the LDO. If an external resistor divider is necessary in this case, the user must take into account the input impedance at the VOUT_LDOn pin (as shown in Figure 8-9), and adjust the resistor values to compensate for the voltage shift.

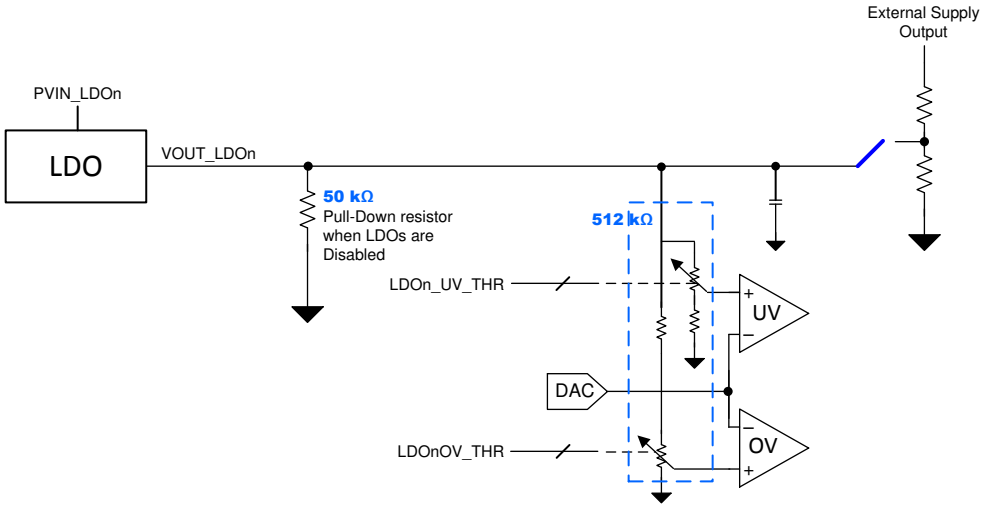

Figure 8-9. Impedance at the VOUT_LDOn Pins

8.3.2.2.1 LDOVINT

The LDOVINT voltage regulator is dedicated to supply the digital and analog functions of the TPS6594-Q1 device, which are not required to be always-on and can be turned-off when the device is in low power states. The LDOVINT voltage regulator is automatically enabled and disabled as needed if LP_STANDBY_SEL = '1'. The automatic control optimizes the overall current consumption when the device is in low power LP_STANDBY state.

The LDOVINT voltage regulator is dedicated for internal use only, and cannot be used to support external loads. An output filtering capacitor must be connected at the VOUT_LDOVINT pin. Do not connect any other components or external loads to this VOUT_LDOVINT pin.

8.3.2.2.2 LDOVRTC

The LDOVRTC voltage regulator supplies always-on functions, such as wake-up functions. This power resource is active as soon as a valid VCCA is present. The LDOVRTC voltage regulator is dedicated for internal use

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only, and cannot be used to support external loads. An output filtering capacitor must be connected at the VOUT_LDOVRTC pin. Do not connect any other components or external loads to this VOUT_LDOVRTC pin.

This voltage regulator is enabled in normal mode or backup mode. The LDOVRTC voltage regulator functions in normal mode when supplied from the main system power rail and is able to supply the input buffers of GPIO3 and GPIO4, the digital components, the crystal, and the RTC calendar module of the TPS6594-Q1 device. The LDOVRTC voltage regulator remains on in BACKUP state when VCCA is below the VCCA_UVLO level, and the backup power source is above the LDOVRTC_UVLO level.

Only the 32 kHz crystal and the RTC counter are activated in the BACKUP state. The RTC calendar function remains active in the LP_STANDBY state, but the interrupt functions are reduced to maintaining the wake up functions only. The RTC calendar and interrupt functions are fully activated in the mission states.

The customer has the option to enable the *shelf mode* by setting the LDORTC_DIS bit to 1 while the device is in the MISSION state and the I2C bus is in operation and ramp down VCCA to 0 V immediately after the I2C write has completed. This *shelf mode* forces the device to skip the BACKUP state and enters the NO SUPPLY state under VCCA_UVLO condition. This mode is useful to prevent the continual draining of the backup power source when the 32 KHz crystal and RTC counter functions are no longer needed.

8.3.2.2.3 LDO1, LDO2, and LDO3

The LDO1, LDO2 and LDO3 regulators can deliver up to 500 mA of current, with a configurable output range of 0.6 V to 3.3 V in 50-mV steps. These 3 LDO regulators also support bypass mode, which allows an input voltage at the PVIN_LDOn to show up at the VOUT_LDOn pin. This feature allows the LDOs to be configured as load switches with power sequencing control. Similar to the buck regulators mentioned in Section 8.3.2.1.4, the UV/OV Voltage Monitor of an un-used LDO regulator can also be used to monitor an external voltage rail by connecting the external rail to the VOUT_LDOn pin.

The bypass capability to connect the input voltage to the output in bypass mode is supported when the input voltage is within the 1.7 V to 3.5 V range. This bypass capability also allows the LDO to switch from 3.3 V in bypass mode to 1.8 V in LDO mode or from 1.8 V in LDO mode to 3.3 V in bypass mode for an SD card I/O supply.

The LDO1, LDO2 and LDO3 regulator include a Current-Limit to protect the internal Power-FET against overcurrent. This Current-Limit has a fixed value between 700 mA and 1800 mA.

It is important to wait until the LDO has settled on the target voltage from the previous change when changing the LDO output voltage setting. The worst-case voltage scaling time for LDO1, LDO2, and LDO3 is 63 µs x (7 + the number of 50-mV steps to the new target voltage).

Table 8-4 shows the coding used to select the output voltage for LDO1, LDO2, and LDO3.

Table 8-4. Output Voltage Selection for LDO1, LDO2, and LDO3

LDOx_VSET	Output Voltage [V]	LDOx_VSET	Output Voltage [V]	LDOx_VSET	Output Voltage [V]	LDOx_VSET	Output Voltage [V]
0x00	Reserved	0x10	1.20	0x20	2.00	0x30	2.80
0x01	Reserved	0x11	1.25	0x21	2.05	0x31	2.85
0x02	Reserved	0x12	1.30	0x22	2.10	0x32	2.90
0x03	Reserved	0x13	1.35	0x23	2.15	0x33	2.95
0x04	0.60	0x14	1.40	0x24	2.20	0x34	3.00
0x05	0.65	0x15	1.45	0x25	2.25	0x35	3.05
0x06	0.70	0x16	1.50	0x26	2.30	0x36	3.10
0x07	0.75	0x17	1.55	0x27	2.35	0x37	3.15
0x08	0.80	0x18	1.60	0x28	2.40	0x38	3.20
0x09	0.85	0x19	1.65	0x29	2.45	0x39	3.25
0x0A	0.90	0x1A	1.70	0x2A	2.50	0x3A	3.30
0x0B	0.95	0x1B	1.75	0x2B	2.55	0x3B	Reserved
0x0C	1.00	0x1C	1.80	0x2C	2.60	0x3C	Reserved

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Table 8-4. Output Voltage Selection for LDO1, LDO2, and LDO3 (continued)

LDOx_VSET	Output Voltage [V]	LDOx_VSET	Output Voltage [V]	LDOx_VSET	Output Voltage [V]	LDOx_VSET	Output Voltage [V]
0x0D	1.05	0x1D	1.85	0x2D	2.65	0x3D	Reserved
0x0E	1.10	0x1E	1.90	0x2E	2.70	0x3E	Reserved
0x0F	1.15	0x1F	1.95	0x2F	2.75	0x3F	Reserved

8.3.2.2.4 Low-Noise LDO (LDO4)

The LDO4 regulator can deliver up to 300 mA of current, with a configurable output range of 1.2 V to 3.3 V in 25-mV steps. This LDO is specifically designed to supply noise sensitive circuits. This supply can be used to power circuits such as PLLs, oscillators, or other analog modules that require low noise on the supply. LDO4 does not support bypass mode. However, if the LDO4 output voltage is not used, the associated UV/OV Voltage Monitor of this regulator can be used as to monitor an external voltage rail by connecting this external voltage rail to the VOUT_LDO4 pin.

The LDO4 regulator includes a Current-Limit to protect the internal Power-FET against overcurrent. This Current-Limit has a fixed value between 400 mA and 900 mA.

Table 8-5 shows the coding used to select the output voltage for LDO4.

Table 8-5. Output Voltage Selection for LDO4

LDO4_VSET	Output Voltage [V]	LDO4_VSET	Output Voltage [V]	LDO4_VSET	Output Voltage [V]	LDO4_VSET	Output Voltage [V]
0x00	Reserved	0x20	1.200	0x40	2.000	0x60	2.800
0x01	Reserved	0x21	1.225	0x41	2.025	0x61	2.825
0x02	Reserved	0x22	1.250	0x42	2.050	0x62	2.850
0x03	Reserved	0x23	1.275	0x43	2.075	0x63	2.875
0x04	Reserved	0x24	1.300	0x44	2.100	0x64	2.900
0x05	Reserved	0x25	1.325	0x45	2.125	0x65	2.925
0x06	Reserved	0x26	1.350	0x46	2.150	0x66	2.950
0x07	Reserved	0x27	1.375	0x47	2.175	0x67	2.975
0x08	Reserved	0x28	1.400	0x48	2.200	0x68	3.000
0x09	Reserved	0x29	1.425	0x49	2.225	0x69	3.025
0x0A	Reserved	0x2A	1.450	0x4A	2.250	0x6A	3.050
0x0B	Reserved	0x2B	1.475	0x4B	2.275	0x6B	3.075
0x0C	Reserved	0x2C	1.500	0x4C	2.300	0x6C	3.100
0x0D	Reserved	0x2D	1.525	0x4D	2.325	0x6D	3.125
0x0E	Reserved	0x2E	1.550	0x4E	2.350	0x6E	3.150
0x0F	Reserved	0x2F	1.575	0x4F	2.375	0x6F	3.175
0x10	Reserved	0x30	1.600	0x50	2.400	0x70	3.200
0x11	Reserved	0x31	1.625	0x51	2.425	0x71	3.225
0x12	Reserved	0x32	1.650	0x52	2.450	0x72	3.250
0x13	Reserved	0x33	1.675	0x53	2.475	0x73	3.275
0x14	Reserved	0x34	1.700	0x54	2.500	0x74	3.300
0x15	Reserved	0x35	1.725	0x55	2.525	0x75	Reserved
0x16	Reserved	0x36	1.750	0x56	2.550	0x76	Reserved
0x17	Reserved	0x37	1.775	0x57	2.575	0x77	Reserved
0x18	Reserved	0x38	1.800	0x58	2.600	0x78	Reserved
0x19	Reserved	0x39	1.825	0x59	2.625	0x79	Reserved
0x1A	Reserved	0x3A	1.850	0x5A	2.650	0x7A	Reserved
0x1B	Reserved	0x3B	1.875	0x5B	2.675	0x7B	Reserved

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Table 8-5. Output Voltage Selection for LDO4 (continued)

LDO4_VSET	Output Voltage [V]	LDO4_VSET	Output Voltage [V]	LDO4_VSET	Output Voltage [V]	LDO4_VSET	Output Voltage [V]
0x1C	Reserved	0x3C	1.900	0x5C	2.700	0x7C	Reserved
0x1D	Reserved	0x3D	1.925	0x5D	2.725	0x7D	Reserved
0x1E	Reserved	0x3E	1.950	0x5E	2.750	0x7E	Reserved
0x1F	Reserved	0x3F	1.975	0x5F	2.775	0x7F	Reserved

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8.3.3 Residual Voltage Checking

The residual voltage (RV) checking feature ensures the voltage level at the buck or LDO regulators is below $V_{TH_SC_RV}$ before it can be ramped up to the target output voltage. If BUCKn/LDOn_RV_SEL=1 by default, then the residual voltage is also checked before the device enters the BOOT_BIST state. If the residual voltage at the output of the regulators is greater than $V_{TH_SC_RV}$, then the device waits until voltage goes below $V_{TH_SC_RV}$ before starting BOOT_BIST or the voltage ramp up.

This feature is enabled by the BUCKn_VMON_EN and BUCKn_RV_SEL bits for each buck regulator, and by the LDOn_VMON_EN and LDOn_RV_SEL bits for each LDO regulator. The Voltage Monitor (VMON) of the corresponding regulator remains on after the regulator is disabled and for the RV_TIMEOUT period when the RV checking feature is enabled. After the RV_TIMEOUT period elapses, the Voltage Monitor (VMON) compares the output voltage of the regulator with the short circuit (SC) threshold of $V_{TH_SC_RV}$ and assert the corresponding BUCKn_SC_INT or LDOn_SC_INT interrupt bits, if the residual voltage is still higher than the threshold voltage. The RV_TIMEOUT period for the BUCK regulators is automatically calculated by the digital controller inside the device by Equation 3. The RV timeout period of the LDO regulator is configured by the LDOn_RV_TIMEOUT[3:0].

$$t_{BUCK_RV_TIMEOUT} = BUCKn_VSET / BUCKn_SLEW_RATE + 100\ \mu s \quad (3)$$

The residual voltage check can also be performed on external rails when they are connected to the VOUT_LDOn pins of unused LDO regulator outputs, or connected to FB_Bn pins of unused buck regulators, or connected to FB_Bn pins of BUCK3 or BUCK4 regulators in Multi-Phase operation.

Figure 8-10 shows the timing diagram of the residual voltage checking operation which results in pass or fail results.

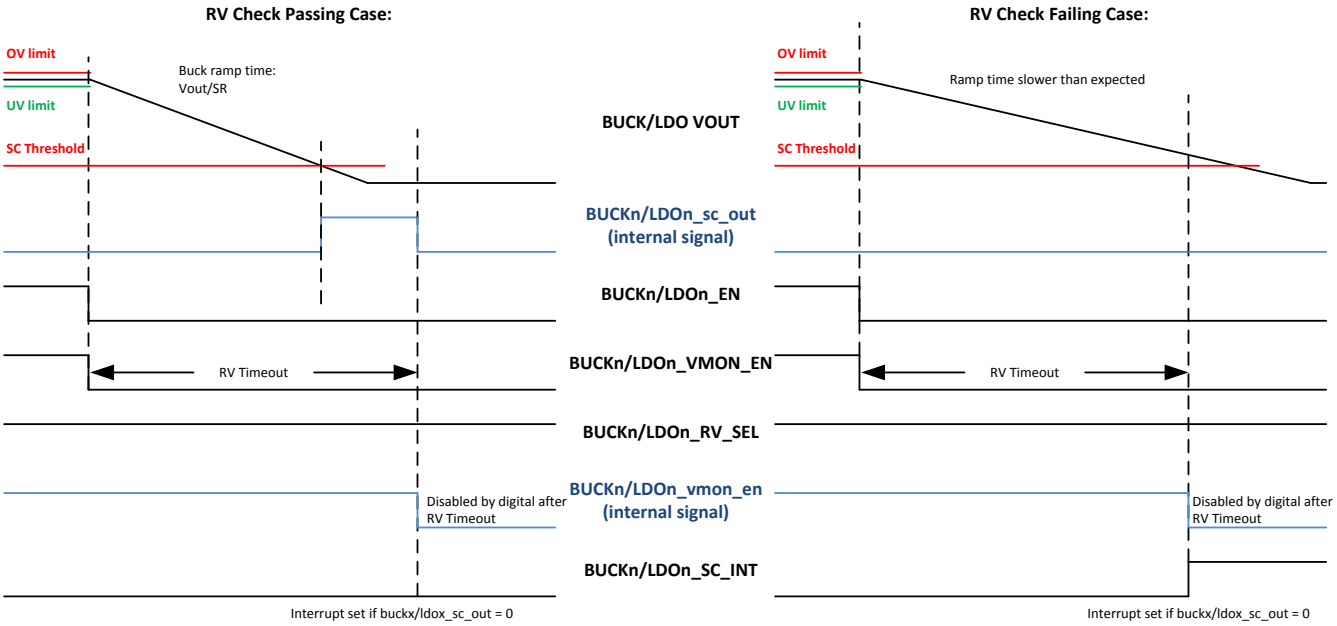

Figure 8-10. Residual Voltage Check Timing Diagram

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8.3.4 Output Voltage Monitor and PGOOD Generation

The TPS6594-Q1 device monitors the undervoltage (UV) and overvoltage (OV) conditions on the output voltages of the BUCK and LDO, regulators and VCCA (when it is expected to be 5 V or 3.3 V), and has the option to indicate the result with a PGOOD signal. Thermal warning can also be included in the result of the PGOOD monitor if it is not masked. Either voltage and current monitoring or only voltage monitoring can be selected for PGOOD indication. This selection is set by the PGOOD_SEL_BUCKn register bits for each BUCK regulator (select primary phase for multi-phase regulator), and is set by the PGOOD_SEL_LDOn register bits for each LDO regulator. When voltage and current are monitored, an active PGOOD signal active indicates that the regulator output is inside the Power-Good voltage window and that load current is below the current limit. If only voltage is monitored, then the current monitoring is ignored for the PGOOD signal.

The BUCKn_VMON_EN bit enables the overvoltage (OV) , undervoltage (UV), short-circuit (SC) and current limit (ILIM) comparators. For LDO regulators, the LDOn_VMON_EN bit enables the OV and UV, Short-circuit and current limit comparators. When a BUCK or an LDO is not needed as a regulated output, it can be used as a voltage monitor for an external rail. For BUCK converters, if the BUCKn_VMON_EN bit remains '1' while the BUCKn_EN bit is '0', it can be used as a voltage monitor for an external rail which is connected to the FB_Bn pin of the BUCK regulator. For LDO regulators, if the LDOn_VMON_EN bit remains '1' while the LDOn_EN bit is '0', it can be used as a voltage monitor for an external rail which is connected to the VOUT_LDOn pin.

When the voltage monitor for a BUCK or LDO regulator is disabled, the output of the corresponding monitor is automatically masked to prevent it from forcing PGOOD inactive. This allows PGOOD to be connected to other open-drain power good signals in the system.

The VCCA_VMON_EN bit enables the monitoring of the VCCA input voltage. It can be enabled as an NVM default setting, which starts the monitoring of the VCCA voltage after the voltage monitor passes ABIST during the BOOT BIST state. The reference voltage for the VCCA monitor can be set by the VCCA_PG_SET bit to either 3.3 V or 5 V. The PGOOD_SEL_VCCA register bit selects whether or not the result of the VCCA monitor is included in the PGOOD monitor output signal.

An NVM option is available to gate the PGOOD output with the nRSTOUT and the nRSTOUT_SoC signals, the intended reset signals for the safety MCU and the SoC respectively. When PGOOD_SEL_NRSTOUT = '1', the PGOOD pin is gated by the nRSTOUT signal. When PGOOD_SEL_NRSTOUT_SOC = '1', the PGOOD pin is gated by the nRSTOUT_SoC signal. This option allows the PGOOD output to be used as an enable signal for external peripherals.

The outputs of the voltage monitors from all the output rails are combined, and PGOOD is active only if all the sources shows active status.

The type of output voltage monitoring for PGOOD signal is selected by PGOOD_WINDOW bit. If the bit is 0, only undervoltage is monitored; if the bit is 1, then undervoltage and overvoltage are monitored.

The polarity and the output type (push-pull or open-drain) are selected by PGOOD_POL and GPIO9_OD bits.

Figure 8-11 shows the Power-Good generation block diagram, and Figure 8-12 shows the Power-Good waveforms.

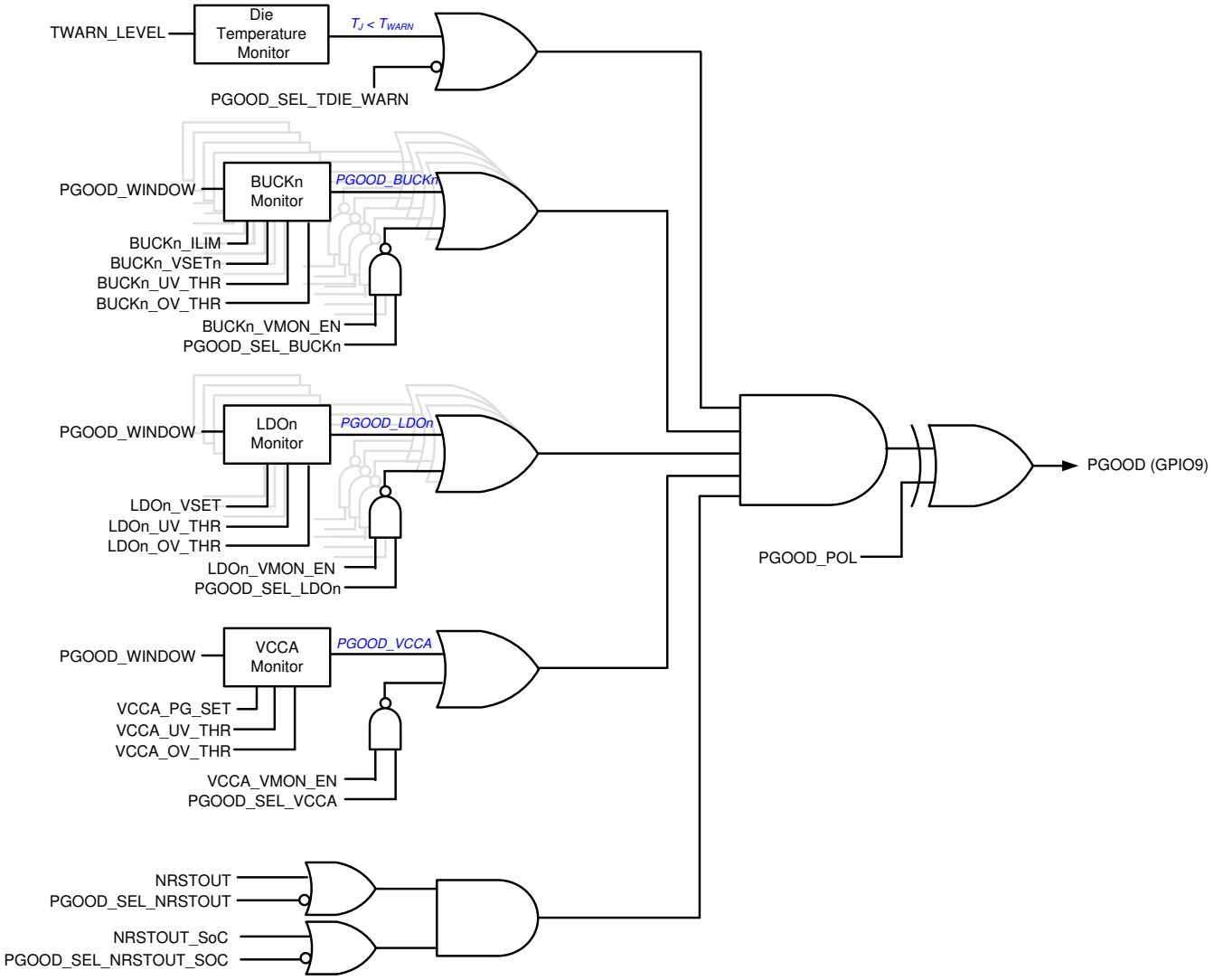

Figure 8-11. PGOOD Block Diagram

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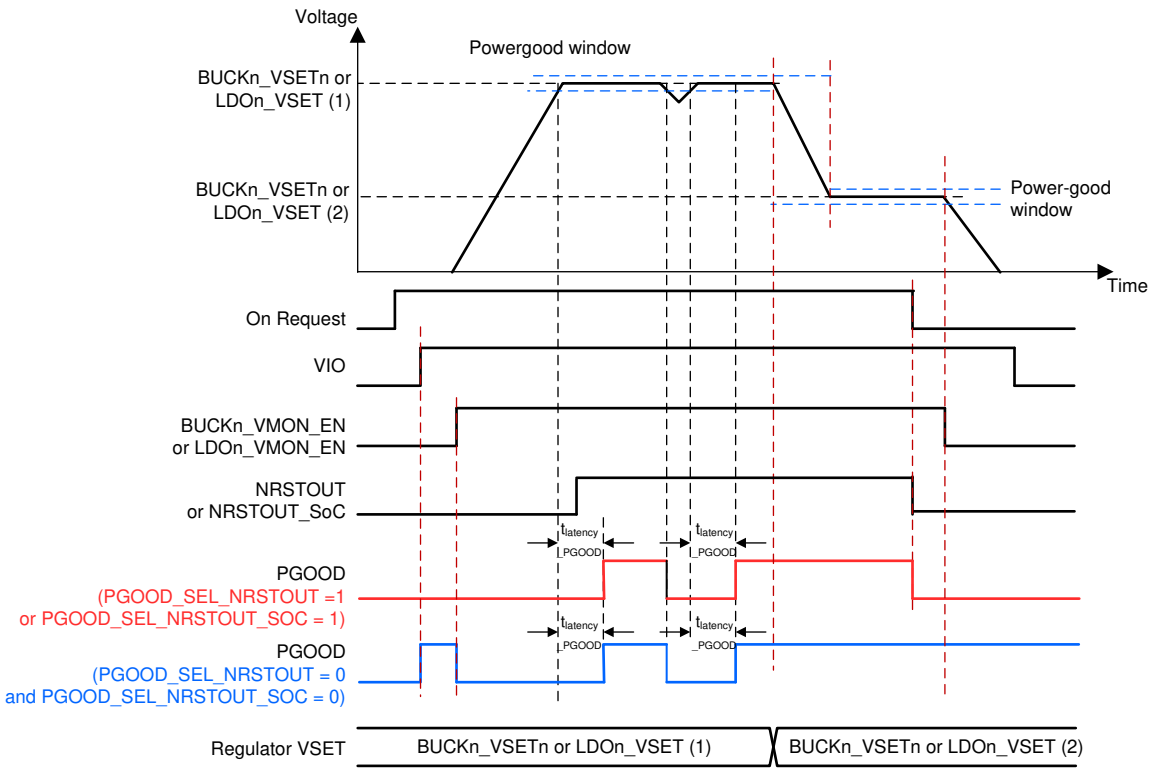

Figure 8-12. PGOOD Waveforms

The OV and UV threshold of the voltage monitors of the BUCK regulators and the LDO regulators are updated automatically by the digital control block when the output voltage setting changes. When the output voltage of the regulator is increased, the OV threshold is updated at the same time the _VSET of the regulator is changed. The UV threshold is updated after a delay calculated by the delta voltage change and the slew rate setting. When the output voltage is decreased, the UV threshold is updated at the same time the _VSET of the regulator is changed. The OV threshold is updated after a delay calculated by the delta voltage change and the slew rate setting. The OV and UV threshold of the BUCK and LDO output voltage monitors are calculated based on the target output voltage set by the corresponding BUCKn_VSET1, BUCKn_VSET2, or LDOn_VSET registers, and the deviation from the target output voltage set (the voltage window) by the corresponding BUCKn_UV_THR, BUCKn_OV_THR, LDOn_UV_THR, and the LDOn_OV_THR registers. For the OV and UV threshold of BUCK and LDO output monitors to update with the correct timing, the following operating procedures must be followed when updating the _VSET values of the regulators to avoid detection of OV/UV fault:

- BUCK and LDO regulators must be enabled at the same time as or earlier than as their VMON, such that the voltage reaches its target value before OV/UV self-test (BIST) is done
- New voltage level must not be set before the start-up has finished and OV/UV self-test (BIST) is completed
- New voltage level must not be set before the previous voltage change (ramp plus settling time) has completed

It is important to note: when a regulator is enabled, a voltage monitor self-test is performed to ensure proper operation. The monitoring function is disabled and gated during this time. Figure 8-13 shows the timing diagram of the BUCK regulator UV/OV self-test. Figure 8-14 shows the timing diagram of the LDO UV/OV self-test. The monitoring function is activated after the gating period.

The self-test for VCCA, BUCK and LDO voltage monitors is done every time when the monitoring function is enabled and VMON_ABIST_EN=1. The self-test checks that OV and UV comparators are changing their output when the input thresholds are swapped. The self-test assumes that the input voltage is inside OV/UV threshold limits. If the voltage is outside the limits, the self-test fails and BIST_FAIL_INT interrupt is set. In addition, a failed self-test for over-voltage comparator sets the over-voltage interrupt.

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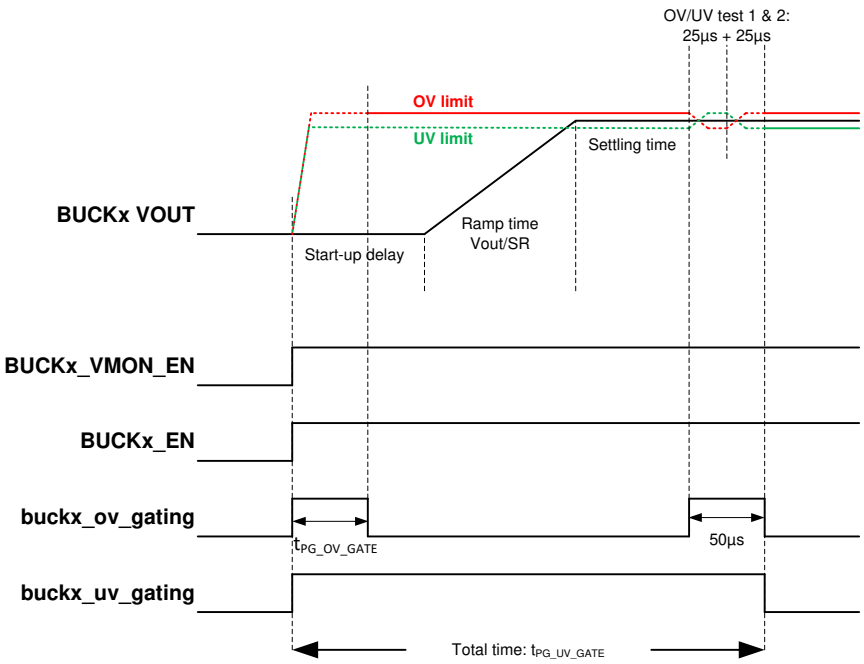

Figure 8-13. Timing of BUCK Regulator UV/OV Self Test

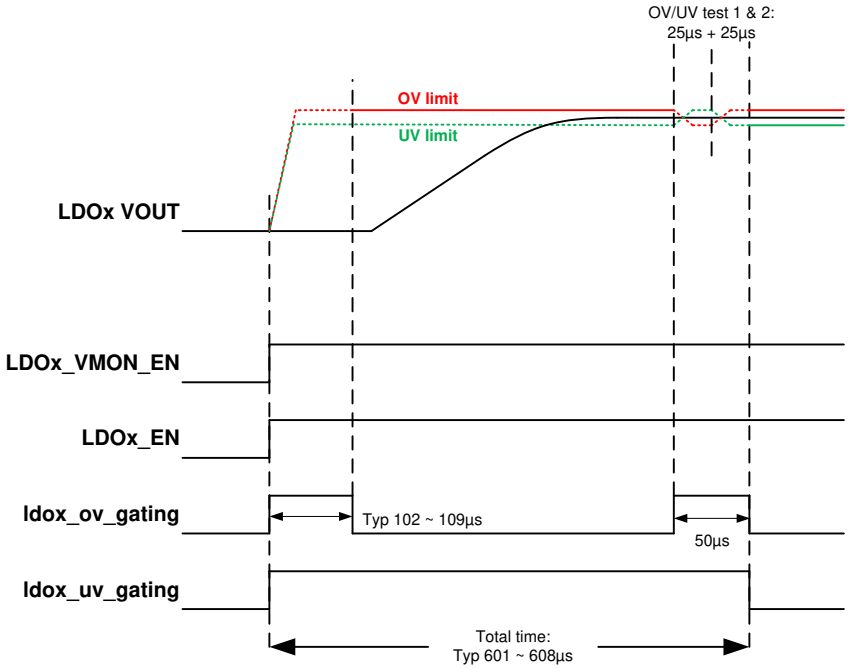

Figure 8-14. Timing of LDO Regulator UV/OV Self-Test

It is possible to use voltage monitors of unused BUCK or LDO regulators for monitoring external supply rails. In three-phase configuration, the Voltage Monitor of BUCK3 (on FB_B3 pin) becomes a free available resource for monitoring an external supply voltage. In four-phase configuration, the Voltage Monitor of both BUCK3 (on FB_B3 pin) and BUCK4 (on FB_B4 pin) become free available resources for monitoring two external supply voltages.. The target output voltage is set by the corresponding BUCKn_VSET1, BUCKn_VSET2, or LDOn_VSET registers, and the deviation from the target output voltage set (the voltage window) by the corresponding BUCKn_UV_THR, BUCKn_OV_THR, LDOn_UV_THR, and the LDOn_OV_THR registers. Following aspects need to be taken into account if Voltage Monitors of unused BUCK or LDO regulators are used for monitoring external supply rails:

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- For voltage monitors of unused LDO regulators: the voltage level applied at the VOUT_LDOx pin, inclusive expected tolerances, must be below the supply voltage applied at the PVIN_LDOx pin
- For voltage monitors of unused BUCK and LDO regulators: the maximum nominal supply voltage of the monitored supply rail is 3.3V
- For voltage monitors of unused BUCK regulators and for voltage monitors of BUCK3 and/or BUCK4 regulators if used in a three-phase or four-phase configuration: the configured values for the BUCKn_VSET and the BUCKn_SLEW_RATE determine the delay-time for the voltage monitoring to become active after the corresponding BUCKn_VMON_EN bit is set. See equation (2) in Section 8.3.2.1.6. If BUCK3 and/or BUCK4 regulators are used in a three-phase or four-phase configuration: even though the values for the BUCK1_VSET and BUCK1_SLEW_RATE bits determine the output voltage and slew-rate of the three-phase or four-phase output rail, the values for BUCK3_VSET respectively BUCK4_VSET and BUCK3_SLEW_RATE respectively BUCK4_SLEW_RATE bits determine the power-good level and the voltage monitoring delay time for the BUCK3 respectively BUCK4 Voltage Monitors.
- For voltage monitors of unused LDO regulators: the delay-time for the voltage monitoring to become active after the corresponding LDOn_VMON_EN bit is set it 601..606µs.

Note

Unless mentioned otherwise in the User's Guide for the orderable part number, for automatically sequenced Voltage Monitors (either as part of automatic sequencing of BUCK and LDO regulators, or as stand-alone Voltage Monitor), the TPS6594-Q1 unmasks the UV/OV right before the release of the nRSTOUT resp. nRSTOUT_SoC pins. For Voltage Monitors which are enabled through system software (either as associated Voltage Monitor for BUCK and LDO regulators, or as stand-alone Voltage Monitor), please refer to the User's Guide for the orderable part number.

Note

For Voltage Monitors that are used to monitor external supply voltages, in order to not have a failing self-test or a false-positive UV/OV detection after completion of the self-test, the actual voltage level of the external supply must satisfy following conditions:

- For VOUT > 1V: VOUT_actual = VOUT_typical +/- (75% * Typical UV/OV Threshold – 1%)
- For VOUT ≤ 1V: VOUT_actual = VOUT_typical +/- (Typical UV/OV Threshold – 15mV)

, in which VOUT_typical is the configured power-good voltage level for the used Voltage Monitor in registers BUCKn_VOUT1/2 and LDOn_VOUT. This requirement also applies to the voltage on the VCCA pin in case the VCCA UV/OV Monitor is used.

8.3.5 Thermal Monitoring

The TPS6594-Q1 device includes several thermal monitoring functions for internal thermal protection of the PMIC.

The TPS6594-Q1 device integrates thermal detection modules to monitor the temperature of the die. These modules are placed on opposite sides of the device and close to the LDO and BUCK modules. An over-temperature condition at either module first generates a warning to the system, and if the temperature continues to rise, then a switch-off of the PMIC device can occur before damage to the die.

Three thermal protection levels are available. One of these protections is a thermal warning function described in Section 8.3.5.1, which sends an interrupt to software. Software is expected to close any noncritical running tasks to reduce power. The second and third protections are the thermal shutdown (TS) function described in Section 8.3.5.2, which begins device shutdown orderly or immediately.

Thermal monitoring is automatically enabled when any one of the BUCK or LDO outputs is enabled within the mission states. It is disabled in low power states, including the LP_STANDBY state, when only the internal regulators are enabled, to minimize the device power consumption. Indication of a thermal warning event is written to the TWARN_INT register.

The current consumption of the thermal monitoring can be decreased in the mission states when the low power dissipation is important. If LPM_EN bit is set and the temperature is below thermal warning level in all thermal detection modules, only one thermal detection module is monitored. If the temperature rises in this module, monitoring in all thermal detection modules is started.

If the die temperature of the TPS6594-Q1 device continues to rise while the device is in mission state, an TSD_ORD_INT or TSD_IMM_INT interrupt is generated, causing a SEVERE or MODERATE error trigger (respectively) in the state machine. While the sequencing and error handling is NVM memory dependent, TI recommends a sequenced shutdown for MODERATE errors, and an immediate shutdown, using resistive discharging, for SEVERE errors to prevent damage to the device. The system cannot restart until the temperature falls below the thermal warning threshold.

8.3.5.1 Thermal Warning Function

The thermal monitor provides a warning to the host processor through the interrupt system when the temperature reaches within a cautionary range. The threshold value must be set to less than the thermal shutdown threshold.

The integrated thermal warning function provides the MCU an early warning of over-temperature condition. This monitoring system is connected to the interrupt controller and can send an TWARN_INT interrupt when the temperature is higher than the preset threshold. The TPS6594-Q1 device uses the TWARN_LEVEL register bit to set the thermal warning threshold temperature at 130°C or 140°C. There is no hysteresis for the thermal warning level.

When the power-management software triggers an interrupt, immediate action must be taken to reduce the amount of power drawn from the PMIC device (for example, noncritical applications must be closed).

8.3.5.2 Thermal Shutdown

The thermal shutdown detector monitors the temperature on the die. If the junction reaches a temperature at which damage can occur, a switch-off transition is initiated and a thermal shutdown event is written into a status register. There are two levels of thermal shutdown threshold. When the die temperature reaches the $T_{SD_orderly}$ level, the TPS6594-Q1 device performs an orderly shutdown of all output power rails. If the die temperature raises rapidly and reaches the T_{SD_imm} level before the orderly shutdown process completes, the TPS6594-Q1 device performs an immediate shutdown to turn off all of the output power rails as rapidly as possible. After the thermal shutdown takes place, the system cannot restart until the die temperature is below the thermal warning threshold.

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8.3.6 Backup Supply Power-Path

The LDOVRTC is supplied from either the VBACKUP (backup supply from either coin-cell or super-cap) input or VCCA. The power-path is designed to prioritize VCCA to maximize the life of the backup supply.

When VCCA drops below the VCCA_UVLO threshold, the device shuts down all rails except the LDOVRTC, and enters the BACKUP mode. At this point, the Backup Supply Power-Path switches to the VBACKUP as the input of LDOVRTC. When the voltage of VCCA returns to level above the VCCA_UVLO threshold level, the power-path switches the input of LDOVRTC back to VCCA.

When both the VCCA voltage drop below the VCCA_UVLO threshold, and the VBACKUP voltage drops below 1.7V (RTC_LDO_UVLO threshold), the LDOVRTC is turned OFF and the digital core is reset, which forces the device into the NO SUPPLY state.

Note: a backup supply is not required for the device to operate. The device skips the BACKUP state if the VBACKUP pin is grounded.

8.3.7 General-Purpose I/Os (GPIO Pins)

The TPS6594-Q1 device integrates eleven configurable general-purpose I/Os that are multiplexed with alternative features as listed in Section 6

For GPIOs characteristics, refer to Electrical Characteristics tables for Digital Input Signal Parameters and Digital Output Signal Parameters.

When configured as primary functions, all GPIOs are controlled through the following set of registers bits under the individual GPIOn_CONF register.

- GPIOn_DEGLITCH_EN: Enables the 8 µs deglitch time for each GPIO pin (input)
- GPIOn_PU_PD_EN: Enables the internal pull up or pull down resistor connected to each GPIO pin
- GPIOn_PU_SEL: Selects the pull up or the pull down resistor to be connected when GPIOn_PU_PD_EN = '1'. '1' = pull-up resistor selected, '0' = pull-down resistor selected
- GPIOn_OD: Configures the GPIO pin (output) as: '1' = open drain, '0' = push-pull
- GPIOn_DIR: Configures the input or output direction of each GPIO pin

Each GPIO event can generate an interrupt on a rising edge, falling edge, or both, configured through the GPIOn_FALL_MASK and the GPIOn_RISE_MASK register bits. A GPIO-interrupt applies when the primary function (general-purpose I/O) has been selected and also for the following alternative functions:

- nRSTOUT_SOC
- PGOOD
- nERR_MCU
- nERR_SoC
- TRIG_WDOG
- DISABLE_WDOG
- NSLEEP1, NSLEEP2
- WKUP1, WKUP2
- LP_WKUP1, LP_WKUP2

The GPIOn_SEL[2:0] register bits under the GPIOn_CONF registers control the selection between a primary and an alternative function. When a pre-defined function is selected, some predetermined IO characteristics (such as pullup, pulldown, push-pull or open drain) for the pin are enforced regardless of the settings of the associated GPIO configuration register. Please note that if the GPIOn_SEL[2:0] is changed during device operation, a signal glitch may occur which may cause digital malfunction, especially if it involves a clock signal such as SCL_I2C2, CLK32KOUT, SCL_SPMI, SYNCCLKIN, or SYNCCLKOUT. Please refer to Section 6.1 for more detail on the predetermined IO characteristics for each pre-defined digital interface function.

All GPIOs can be configured as a wake-up input when it is configured as a WKUP1 or a WKUP2 signal. Only GPIO3 and GPIO4 can be configured as LP_WKUP1 or LP_WKUP2 signal so that they can be used to wake-up the device from LP_STANDBY state. All GPIOs can also be configured as a NSLEEP1 or a NSLEEP2 input. For more information regarding the usage of the NSLEEPx pins and the WKUPx pins, please refer to Section 8.4.1.2.4.3 and Section 8.4.1.2.4.4.

Any of the GPIO pin can also be configured as part of the power-up sequence to enable external devices such as external BUCKs when it is configured as a general-purpose output port.

The nINT pin, the EN_DRV pin, the nRSTOUT pin and the GPIO pin assigned as nRSTOUT_SOC have readback monitoring to detect errors on the signals. The monitoring of the EN_DRV pin checks for mismatch in both low and high levels. For the nINT pin, the nRSTOUT pin and the GPIO pin assigned as nRSTOUT_SOC, the readback monitoring only checks for mismatches in the low level, therefore it is allowed to combine these signals with other external pull-down sources. The readback mismatch is continuously monitored without deglitch circuitry during operation, and the monitoring is gated for $t_{gate_readback}$ period when the signal state is changed or when a new function is selected for the GPIO pin with the GPIOn_SEL bits. NINT_READBACK_INT, EN_DRV_READBACK_INT, NRSTOUT_READBACK_INT, and NRSTOUT_SOC_READBACK_INT are the interrupt bits which are set in an event of a readback mismatch for these pins, respectively.

Note

All GPIO pin are set to generic input pins with resistive pull-down before NVM memory is loaded during device power up. Therefore, if any GPIOs has external pull-up resistors connecting to a voltage domain which is energized before the NVM memory is loaded, the GPIO pin is pulled high before the configuration for the pin is loaded from the NVM.

Note

For GPIO pins with internal pull down enabled, additional leakage current flows into the GPIO pin if this pin is pulled-up to a voltage higher than the voltage level of its output power domain. If the internal pull down must be enabled, please use a resistor divider to divide down the input voltage, or use a series resistor to connect to the input source and ensure the voltage level at the GPIO pin is below the voltage level of its output power domain.

8.3.8 nINT, EN_DRV, and nRSTOUT Pins

The nINT, EN_DRV and nRSTOUT pin, and the GPIO pin assigned as nRSTOUT_SoC are IO pins with dedicated functions.

The nINT pin is the open drain interrupt output pin. More description regarding the function of this pin can be found under Section 1.

The nRSTOUT pin, together with the GPIO pin assigned as nRSTOUT_SoC, are the system reset pins which can be configured as open-drain or push-pull outputs. These pins stay in the default low state until the PFSM of the TPS6594-Q1 sets the associated control bits NRSTOUT and NRSTOUT_SOC in the register map. These control bits NRSTOUT and NRSTOUT_SOC are set by the PFSM typically after the end of a power-up sequence. At the beginning of a power-down sequence, the PFSM clears these control bits NRSTOUT and NRSTOUT_SOC in order to pull-down the nRSTOUT and nRSTOUT_SoC pins before the ramp-down of the voltage rails.

The purpose of the EN_DRV pin is to indicate that the TPS6594-Q1 has entered a safe state. The EN_DRV pin has an internal 10kΩ high-side pull-up to the VCCA supply. The TPS6594-Q1 pulls this EN_DRV pin to the default low state, and releases the pull-down when the MCU sets the ENABLE_DRV bit to '1'.

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8.3.9 Interrupts

The interrupt registers in the device are organized in hierarchical fashion. The interrupts are grouped into the following categories:

BUCK ERROR	These interrupts indicate over-voltage (OV), under-voltage (UV), short-circuit (SC), residual voltage (SC) and over-current (ILIM) error conditions found on the BUCK regulators .
LDO ERROR	These interrupts indicate OV, UV, and SC error conditions found on the LDO regulators, as well as OV and UV error conditions found on the VCCA supply.
VMON ERROR	These interrupts indicate OV and UV error conditions found on the VCCA supply.
SEVERE ERROR	These errors indicate severe device error conditions, such as thermal shutdown, PFSM sequencing and execution error and pre-regulator over-voltage failure, which causes the device to trigger the PFSM to execute immediate shutdown of all digital outputs, external voltage rails and monitors, and proceed to the Safe Recovery State.
MODERATE ERROR	These interrupts provide warnings to the system to indicate detection of multiple WDOG Errors or ESM errors exceeding the allowed recovery count, detection of long press nPWRON button, SPMI communication error, register CRC error, BIST failure, or thermal reaching orderly shutdown level. These warning causes the device to trigger the PFSM to execute orderly shutdown of all digital outputs, external voltage rails and monitors, and proceed to the Safe Recovery State.[3]
MISCELLANEOUS WARNING	These interrupts provide information to the system to indicate detection of WDOG or ESM errors, die temperature crossing thermal warning threshold, device passing BIST test, or external sync clock availability.
START-UP SOURCE	These interrupts provide information to the system on the mechanism which caused the device to start up, which includes FSD, RTC alarm or timer interrupts, the activation of the ENABLE pin or the nPRWON pin button detection.
GPIO DETECTION	These interrupts indicate the High/Rising-Edge or the Low/Falling-Edge detection at the GPIO1 through GPIO11 pins.
FSM ERROR INTERRUPT	These interrupts indicate the detection of an error which causes the device mission state changes.

All interrupts are logically combined on a single output pin, nINT (active low). The host processor can read the INT_TOP register to find the interrupt registers to find out the source of the interrupt, and write '1' to the corresponding interrupt register bit to clear the interrupt. This mechanism ensures when a new interrupt occurs while the nINT pin is still active, all of the corresponding interrupt register bits retain the interrupt source information until it is cleared by the host.

Any interrupt source can be masked by setting the corresponding mask register to '1'. When an interrupt is masked, the interrupt bit is not updated when the associated event occurs, the nINT line is not affected, and the event is not recorded. If an interrupt is masked after the event occurred, the interrupt register bit reflects the event until the bit is cleared. While the event is masked, the interrupt register bit is not over-written when a new event occurs.

Figure 8-15 shows the hierarchical structure of the interrupt registers according to the categories described above. The purpose of this register structure is to reduce the number of interrupt register read cycles the host has to perform in order to identify the source of the interrupt. Table 8-6 summarizes the trigger and the clearing mechanism for all of the interrupt signals. More detail descriptions of each interrupt registers can be found in Section 8.7.

[3] The SEVERE ERROR and the MODERATE ERROR are handled in NVM memory but TI requires that the NVM pre-configurable finite state machine (PFSM) settings always follow this described error handling to meet device specifications.

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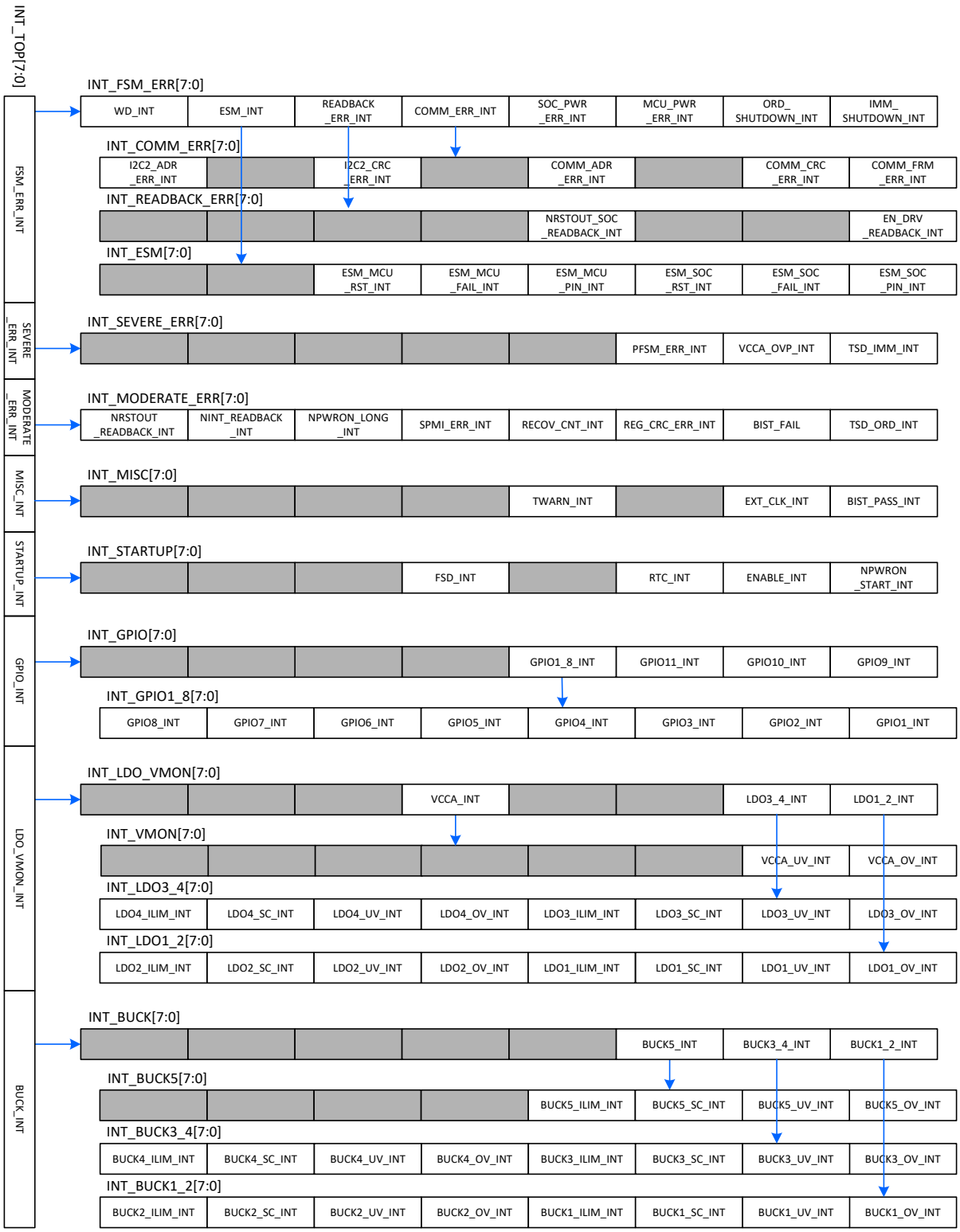

Figure 8-15. Hierarchical Structure of Interrupt Registers

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Table 8-6. Summary of Interrupt Signals

EVENT	TRIGGER FOR FSM	RESULT [1]	RECOVERY	INTERRUPT BIT	MASK FOR INTERRUPT	LIVE STATUS BIT	INTERRUPT CLEAR
BUCK regulator forward current limit triggered	**EN_ILIM_FSM_CTRL=1:** According to BUCKn_GRP_SEL and x_RAIL_TRIG bits **EN_ILIM_FSM_CTRL=0:** N/A	**EN_ILIM_FSM_CTRL=1:** Transition according to FSM trigger and interrupt **EN_ILIM_FSM_CTRL=0:** Interrupt only	Depends on PFSM configuration, see PFSM transition diagram	BUCKn_ILIM_INT = 1	BUCKn_ILIM_MASK	BUCKn_ILIM_STAT	Write 1 to BUCKn_ILIM_INT bit Interrupt is not cleared if current limit violation is active
LDO regulator current limit triggered	**EN_ILIM_FSM_CTRL=1:** According to LDOn_GRP_SEL and x_RAIL_TRIG bits **EN_ILIM_FSM_CTRL=0:** N/A	**EN_ILIM_FSM_CTRL=1:** Transition according to FSM trigger and interrupt **EN_ILIM_FSM_CTRL=0:** Interrupt only	Depends on PFSM configuration, see PFSM transition diagram	LDOn_ILIM_INT = 1	LDOn_ILIM_MASK	LDOn_ILIM_STAT	Write 1 to LDOn_ILIM_INT bit Interrupt is not cleared if current limit violation is active
BUCK output or switch short circuit detected	According to BUCKn_GRP_SEL and x_RAIL_TRIG bits	Regulator disable and transition according to FSM trigger and interrupt	Depends on PFSM configuration, see PFSM transition diagram	BUCKn_SC_INT = 1	N/A	N/A	Write 1 to BUCKn_SC_INT bit
LDO output short circuit detected	According to LDOn_GRP_SEL and x_RAIL_TRIG bits	Regulator disable and transition according to FSM trigger and interrupt	Depends on PFSM configuration, see PFSM transition diagram	LDOn_SC_INT = 1	N/A	N/A	Write 1 to LDOn_SC_INT bit
BUCK output residual voltage violation	**BUCKn_RV_SEL = 1** According to BUCKn_GRP_SEL and x_RAIL_TRIG bits **BUCKn_RV_SEL = 0** N/A	**BUCKn_RV_SEL = 1** Regulator disable and transition according to FSM trigger and interrupt **BUCKn_RV_SEL = 0** N/A	Depends on PFSM configuration, see PFSM transition diagram	BUCKn_SC_INT = 1	N/A	N/A	Write 1 to BUCKn_SC_INT bit
LDO output residual voltage violation	**LDOn_RV_SEL = 1** According to LDOn_GRP_SEL and x_RAIL_TRIG bits **LDOn_RV_SEL = 0** N/A	**LDOn_RV_SEL = 1** Regulator disable and transition according to FSM trigger and interrupt **LDOn_RV_SEL = 0** N/A	Depends on PFSM configuration, see PFSM transition diagram	LDOn_SC_INT = 1	N/A	N/A	Write 1 to LDOn_SC_INT bit
BUCK regulator overvoltage	According to BUCKn_GRP_SEL and x_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on PFSM configuration, see PFSM transition diagram	BUCKn_OV_INT = 1	BUCKn_OV_MASK	BUCKn_OV_STAT	Write 1 to BUCKn_OV_INT bit Interrupt is not cleared if it is active
BUCK regulator undervoltage	According to BUCKn_GRP_SEL and x_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on PFSM configuration, see PFSM transition diagram	BUCKn_UV_INT = 1	BUCKn_UV_MASK	BUCKn_UV_STAT	Write 1 to BUCKn_UV_INT bit Interrupt is not cleared if it is active
LDO regulator overvoltage	According to LDOn_GRP_SEL and x_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on PFSM configuration, see PFSM transition diagram	LDOn_OV_INT = 1	LDOn_OV_MASK	LDOn_OV_STAT	Write 1 to LDOn_OV_INT bit Interrupt is not cleared if it is active
LDO regulator undervoltage	According to LDOn_GRP_SEL and x_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on PFSM configuration, see PFSM transition diagram	LDOn_UV_INT = 1	LDOn_UV_MASK	LDOn_UV_STAT	Write 1 to LDOn_UV_INT bit Interrupt is not cleared if it is active
VCCA input overvoltage monitoring	According to VCCA_GRP_SEL and x_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on PFSM configuration, see PFSM transition diagram	VCCA_OV_INT = 1	VCCA_OV_MASK	VCCA_OV_STAT	Write 1 to VCCA_OV_INT bit Interrupt is not cleared if it is active
VCCA input undervoltage monitoring	According to VCCA_GRP_SEL and x_RAIL_TRIG bits	Transition according to FSM trigger and interrupt	Depends on PFSM configuration, see PFSM transition diagram	VCCA_UV_INT = 1	VCCA_UV_MASK	VCCA_UV_STAT	Write 1 to VCCA_UV_INT bit Interrupt is not cleared if it is active
Thermal warning	N/A	Interrupt only	Not valid	TWARN_INT = 1	TWARN_MASK	TWARN_STAT	Write 1 to TWARN_INT bit Interrupt is not cleared if temperature is above thermal warning level

Table 8-6. Summary of Interrupt Signals (continued)

EVENT	TRIGGER FOR FSM	RESULT [1]	RECOVERY	INTERRUPT BIT	MASK FOR INTERRUPT	LIVE STATUS BIT	INTERRUPT CLEAR
Thermal shutdown, orderly sequenced	ORDERLY_SHUTDOWN (MODERATE_ERR_INT)	All regulators disabled and Output GPIOx set to low in a sequence and interrupt[1]	Automatic start-up to STARTUP_DEST[1:0] state after temperature is below TWARN level	TSD_ORD_INT = 1	N/A	TSD_ORD_STAT	Write 1 to TSD_ORD_INT bit Interrupt is not cleared if temperature is above thermal shutdown level
Thermal shutdown, immediate	IMMEDIATE_SHUTDOWN (SEVERE_ERR_INT)	All regulators disabled with pull-down resistors and Output GPIOx set to low immediately and interrupt[1]	Automatic start-up to STARTUP_DEST[1:0] state after temperature is below TWARN level	TSD_IMM_INT = 1	N/A	TSD_IMM_STAT	Write 1 to TSD_IMM_INT bit Interrupt is not cleared if temperature is above thermal shutdown level
BIST error	ORDERLY_SHUTDOWN (MODERATE_ERR_INT)	All regulators disabled and Output GPIOx set to low immediately and interrupt[1]	Automatic start-up to STARTUP_DEST[1:0] state	BIST_FAIL_INT = 1	BIST_FAIL_MASK	N/A	Write 1 to BIST_FAIL_INT bit
Register CRC error	ORDERLY_SHUTDOWN (MODERATE_ERR_INT)	All regulators disabled and Output GPIOx set to low immediately and interrupt[1]	Automatic start-up to STARTUP_DEST[1:0] state	REG_CRC_ERR_INT = 1	REG_CRC_ERR_MASK	N/A	Write 1 to REG_CRC_ERR_INT bit
SPMI communication error	ORDERLY_SHUTDOWN (MODERATE_ERR_INT)	All regulators disabled and Output GPIOx set to low immediately and interrupt[1]	Automatic start-up to STARTUP_DEST[1:0] state	SPMI_ERR_INT = 1	SPMI_ERR_MASK	N/A	Write 1 to SPMI_ERR_INT bit
SPI frame error	N/A	Interrupt only	Not valid	COMM_FRM_ERR_INT = 1[4]	COMM_FRM_ERR_MASK	N/A	Write 1 to COMM_FRM_ERR_INT bit
I2C1 or SPI CRC error	N/A	Interrupt only	Not valid	COMM_CRC_ERR_INT = 1	COMM_CRC_ERR_MASK	N/A	Write 1 to COMM_CRC_ERR_INT bit
I2C1 or SPI address error[5]	N/A	Interrupt only	Not valid	COMM_ADR_ERR_INT = 1	COMM_ADR_ERR_MASK	N/A	Write 1 to COMM_ADR_ERR_INT bit
I2C2 CRC error	N/A	Interrupt only	Not valid	I2C2_CRC_ERR_INT = 1	I2C2_CRC_ERR_MASK	N/A	Write 1 to I2C2_CRC_ERR_INT bit
I2C2 address error[5]	N/A	Interrupt only	Not valid	I2C2_ADR_ERR_INT = 1	I2C2_ADR_ERR_MASK	N/A	Write 1 to I2C2_ADR_ERR_INT bit
PFSM error	IMMEDIATE_SHUTDOWN (SEVERE_ERR_INT)	All regulators disabled with pull-down resistors and Output GPIOx set to low immediately and interrupt[1]	Automatic start-up to STARTUP_DEST[1:0] state. If previous PFSM_ERR_INT is pending, VCCA power cycle needed for recovery.	PFSM_ERR_INT = 1		N/A	Write 1 to PFSM_ERR_INT bit
EN_DRV pin readback error (monitoring high and low states)	N/A	Interrupt only	Not valid	EN_DRV_READBACK_INT = 1	EN_DRV_READBACK_MASK	EN_DRV_READBACK_STAT	Write 1 to EN_DRV_READBACK_INT bit Interrupt is not cleared if it is active
NINT pin readback error (monitoring low state)	ORDERLY_SHUTDOWN (MODERATE_ERR_INT)	All regulators disabled with pull-down resistors and Output GPIOx set to low immediately and interrupt[1]	Automatic start-up to STARTUP_DEST[1:0] state	NINT_READBACK_INT = 1	NINT_READBACK_MASK	NINT_READBACK_STAT	Write 1 to NINT_READBACK_INT bit Interrupt is not cleared if it is active
NRSTOUT pin readback error (monitoring low state)	ORDERLY_SHUTDOWN (MODERATE_ERR_INT)	All regulators disabled with pull-down resistors and Output GPIOx set to low immediately and interrupt[1]	Automatic start-up to STARTUP_DEST[1:0] state	NRSTOUT_READBACK_INT = 1	NRSTOUT_READBACK_MASK	NRSTOUT_READBACK_STAT	Write 1 to NRSTOUT_READBACK_INT bit Interrupt is not cleared if it is active
NRSTOUT_SOC pin readback error (monitoring low state)	N/A	Interrupt only	Not valid	NRSTOUT_SOC_READBACK_INT = 1	NRSTOUT_SOC_READBACK_MASK	NRSTOUT_SOC_READBACK_STAT	Write 1 to NRSTOUT_SOC_READBACK_INT bit Interrupt is not cleared if it is active

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Table 8-6. Summary of Interrupt Signals (continued)

EVENT	TRIGGER FOR FSM	RESULT [1]	RECOVERY	INTERRUPT BIT	MASK FOR INTERRUPT	LIVE STATUS BIT	INTERRUPT CLEAR
Fault detected by SOC ESM (level mode: low level detected, PWM mode: PWM signal timing violation)	N/A	Interrupt only	Not valid	ESM_SOC_PIN_INT = 1	ESM_SOC_PIN_MASK	N/A	Write 1 to ESM_SOC_PIN_INT bit
Fault detected by SOC ESM (level mode: low level longer than DELAY1 time, PWM mode: ESM error counter > FAIL_THR longer than DELAY1time)	N/A	Interrupt and EN_DRV = 0 (configurable)	Not valid	ESM_SOC_FAIL_INT = 1	ESM_SOC_FAIL_MASK	N/A	Write 1 to ESM_SOC_FAIL_INT bit
Fault detected by SOC ESM (level mode: low level longer than DELAY1+DELAY2 time, PWM mode: ESM error counter > FAIL_THR longer than DELAY1+DELAY2 time)	ESM_SOC_RST	Interrupt, and NRSTOUT_SOC toggle[1]	Automatically returns to the current operating state after the completion of SoC warm reset	ESM_SOC_RST_INT = 1	ESM_SOC_RST_MASK	N/A	Write 1 to ESM_SOC_RST_INT bit
Fault detected by MCU ESM (level mode: low level detected, PWM mode: PWM signal timing violation	N/A	Interrupt only	Not valid	ESM_MCU_PIN_INT = 1	ESM_MCU_PIN_MASK	N/A	Write 1 to ESM_MCU_PIN_INT bit
Fault detected by MCU ESM (level mode: low level longer than DELAY1 time, PWM mode: ESM error counter > FAIL_THR longer than DELAY1 time)	N/A	Interrupt and EN_DRV = 0 (configurable)	Not valid	ESM_MCU_FAIL_INT = 1	ESM_MCU_FAIL_MASK	N/A	Write 1 to ESM_MCU_FAIL_INT bit
Fault detected by MCU ESM (level mode: low level longer than DELAY1+DELAY2 time, PWM mode: ESM error counter > FAIL_THR longer than DELAY1+DELAY2 time)	ESM_MCU_RST	Interrupt and Warm Reset (EN_DRV = 0 and NRSTOUT and NRSTOUT_SOC toggle)[1]	Automatically returns to the current operating state after the completion of warm reset	ESM_MCU_RST_INT = 1	ESM_MCU_RST_MASK	N/A	Write 1 to ESM_MCU_RST_INT bit
External clock is expected, but it is not available or the frequency is not in the valid range	N/A	Interrupt only	Not valid	EXT_CLK_INT = 1[2]	EXT_CLK_MASK	EXT_CLK_STAT	Write 1 to EXT_CLK_INT bit
BIST completed successfully	N/A	Interrupt only	Not valid	BIST_PASS_INT = 1	BIST_PASS_MASK	N/A	Write 1 to BIST_PASS_INT bit
Watchdog fail counter above fail threshold	N/A	Interrupt and EN_DRV = 0	Clear interrupt and WD_FAIL_CNT < WD_FAIL_TH	WD_FAIL_INT = 1	N/A	N/A	Write 1 to WD_FAIL_INT bit
Watchdog fail counter above reset threshold	WD_RST (if WD_RST_EN = 1)	Interrupt and Warm Reset if WD_RST_EN = 1 (EN_DRV = 0 and NRSTOUT and NRSTOUT_SOC toggle)[1]	Automatically returns to the current operating state after the completion of warm reset	WD_RST_INT = 1	N/A	N/A	Write 1 to WD_RST_INT bit
Watchdog long window timeout	WD_RST	Interrupt and Warm Reset (EN_DRV = 0 and NRSTOUT and NRSTOUT_SOC toggle)[1]	Automatically returns to the current operating state after the completion of warm reset	WD_LONGWIN_TIMEOUT_INT = 1	N/A	N/A	Write 1 to WD_LONGWIN_TIMEOUT_INT bit
RTC alarm wake-up	TRIGGER_SU_x	Start-up to STARTUP_DEST[1:0] state and interrupt[1]	Not valid	ALARM = 1	IT_ALARM = 0	N/A	Write 1 to ALARM bit
RTC timer wake-up	TRIGGER_SU_x	Start-up to STARTUP_DEST[1:0] state and interrupt[1]	Not valid	TIMER = 1	IT_TIMER = 0	N/A	Write 1 to TIMER bit

Table 8-6. Summary of Interrupt Signals (continued)

EVENT	TRIGGER FOR FSM	RESULT [1]	RECOVERY	INTERRUPT BIT	MASK FOR INTERRUPT	LIVE STATUS BIT	INTERRUPT CLEAR
Low state in NPWRON pin	TRIGGER_SU_x	Start-up to STARTUP_DEST[1:0] state and interrupt[1]	Not valid	NPWRON_START_INT = 1	NPWRON_START_MASK	NPWRON_IN	Write 1 to NPWRON_START_INT bit
Long low state in NPWRON pin	ORDERLY_SHUTDOWN	All regulators disabled and Output GPIOx set to low in a sequence and interrupt[1]	Valid power-on request	NPWRON_LONG_INT = 1	NPWRON_LONG_MASK	NPWRON_IN	Write 1 to NPWRON_LONG_INT bit
Low state in ENABLE pin	TRIGGER_FORCE_STANDBY/ TRIGGER_FORCE_LP_STANDBY	Transition to STANDBY or LP_STANDBY depending on the LP_STANDBY_SEL bit setting[1]	ENABLE pin rise	N/A	N/A	N/A	N/A
ENABLE pin rise	TRIGGER_SU_x	[1]	Not valid	ENABLE_INT = 1	ENABLE_MASK	ENABLE_STAT	Write 1 to ENABLE_INT bit
Fault causing orderly shutdown	ORDERLY_SHUTDOWN	All regulators disabled and Output GPIOx set to low in a sequence and interrupt[1]	Automatic start-up to STARTUP_DEST[1:0] state	ORD_SHUTDOWN_INT	ORD_SHUTDOWN_MASK	N/A	Write 1 to ORD_SHUTDOWN_INT
Fault causing immediate shutdown	IMMEDIATE_SHUTDOWN	All regulators disabled with pull-down resistors and Output GPIOx set to low immediately and interrupt[1]	Automatic start-up to STARTUP_DEST[1:0] state	IMM_SHUTDOWN_INT	IMM_SHUTDOWN_MASK	N/A	Write 1 to IMM_SHUTDOWN_INT
Power supply error for MCU	MCU_POWER_ERROR	Transition according to FSM trigger and interrupt	Depends on PFSM configuration, see PFSM transition diagram	MCU_PWR_ERR_INT	MCU_PWR_ERR_MASK	N/A	Write 1 to MCU_PWR_ERR_INT
Power supply error for SOC	SOC_POWER_ERROR	Transition according to FSM trigger and interrupt	Depends on PFSM configuration, see PFSM transition diagram	SOC_PWR_ERR_INT	SOC_PWR_ERR_MASK	N/A	Write 1 to SOC_PWR_ERR_INT
VCCA over-voltage ($VCCA_{OVP}$)	IMMEDIATE_SHUTDOWN (SEVERE_ERR_INT)	All regulators disabled with pull-down resistors and Output GPIOx set to low immediately and interrupt[1]	Automatic start-up to STARTUP_DEST[1:0] state after VCCA voltage is below $VCCA_{OVP}$	VCCA_OVP_INT = 1	N/A	VCCA_OVP_STAT	Write 1 to INT_OVP_INT bit Interrupt is not cleared if VCCA voltage is above $VCCA_{OVP}$ level
GPIO interrupt	According to GPIOx_FSM_MASK and GPIOx_FSM_MASK_POL bits	Transition according to FSM trigger and interrupt	Not valid	GPIOx_INT = 1	GPIOx_RISE_MASK GPIOx_FALL_MASK	GPIOx_IN	Write 1 to GPIOx_INT bit
WKUP1 and LP_WKUP1 signals	WKUP1	Transition to ACTIVE state and interrupt[1]	Not valid	N/A	GPIOx_RISE_MASK GPIOx_FALL_MASK	GPIOx_IN	Write 1 to GPIOx_INT bit
WKUP2 and LP_WKUP2 signals	WKUP2	Transition to MCU ONLY state and interrupt[1]	Not valid	N/A	GPIOx_RISE_MASK GPIOx_FALL_MASK	GPIOx_IN	Write 1 to GPIOx_INT bit
NSLEEP1 signal, NSLEEP1B bit	According to NSLEEP1 and NSLEEP2	State transition based on NSLEEP1 and NSLEEP2	Not valid	N/A	NSLEEP1_MASK	GPIOx_IN	N/A
NSLEEP2 signal, NSLEEP2B bit	According to NSLEEP1 and NSLEEP2	State transition based on NSLEEP1 and NSLEEP2	Not valid	N/A	NSLEEP2_MASK	GPIOx_IN	N/A
LDOVINT over- or undervoltage	IMMEDIATE_SHUTDOWN	All regulators disabled with pull-down resistors and Output GPIOx set to low immediately[1]	Valid LDOVINT voltage	N/A	N/A	N/A	N/A
Main clock outside valid frequency	IMMEDIATE_SHUTDOWN	All regulators disabled with pull-down resistors and Output GPIOx set to low immediately[1]	VCCA power cycle	N/A	N/A	N/A	N/A
Recovery counter limit exceeded[3]	ORDERLY_SHUTDOWN	All regulators disabled and Output GPIOx set to low in a sequence[1]	VCCA power cycle	N/A	N/A	N/A	N/A
VCCA supply falling below $VCCA_{UVLO}$	IMMEDIATE_SHUTDOWN	Immediate shutdown[1]	VCCA voltage rising	N/A	N/A	N/A	N/A

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Table 8-6. Summary of Interrupt Signals (continued)

EVENT	TRIGGER FOR FSM	RESULT (1)	RECOVERY	INTERRUPT BIT	MASK FOR INTERRUPT	LIVE STATUS BIT	INTERRUPT CLEAR
First supply detection, VCCA supply rising above $VCCA_{UVLO}$	TRIGGER_SU_x	Start-up to STARTUP_DEST[1:0] state and interrupt(1)	Not valid	FSD_INT = 1	FSD_MASK	N/A	Write 1 to FSD_INT bit

(1) The results shown in this column are selected to meet functional safety assumptions and device specifications. The actual results can be configured differently in NVM memory. TI recommends reviewing of the system and device functional safety goal and documentation before deviating from these recommendations.
(2) Interrupt is generated during clock detector operation and in case clock is not available when clock detector is enabled.
(3) This event does not occur if RECOV_CNT_THR = 0, even though RECOV_CNT continues to accumulate and increase, and eventually saturates when it reaches the maximum count of 15.
(4) Due to a digital logic errata in the device, a write or read SPI command which coincide with the rising edge of the CS signal may not cause the COMM_FRM_ERR_INT interrupt.
(5) I2C1, I2C2, or SPI address error only occur in safety applications if the interface CRC feature is enabled, when both I2C1_SPI_CRC_EN and I2C2_CRC_EN are set to '1'.

8.3.10 RTC

8.3.10.1 General Description

The RTC is driven by the 32-kHz oscillator and it provides the alarm and time-keeping functions.

The main functions of the RTC block are:

- Time information (seconds, minutes, and hours) in binary-coded decimal (BCD) code
- Calendar information (day, month, year, and day of the week) in BCD code up to year 2099
- Configurable interrupts generation; the RTC can generate two types interrupts which can be enabled and masked individually:
  - Timer interrupts periodically (1-second, 1-minute, 1-hour, or 1-day periods)
  - Alarm interrupt at a precise time of the day (alarm function)
- Oscillator frequency calibration and time correction with 1/32768 resolution

Figure 8-16 shows the RTC block diagram.

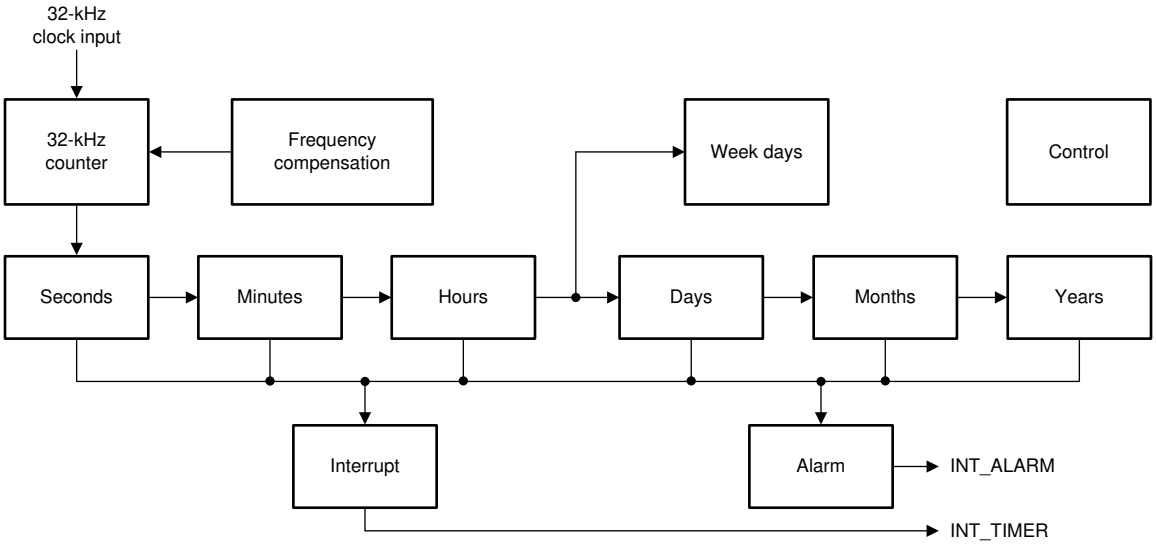

Figure 8-16. RTC Block Diagram

8.3.10.2 Time Calendar Registers

All the time and calendar information is available in the time calendar (TC) dedicated registers: SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, WEEKS_REG, MONTHS_REG, and YEARS_REG. The TC register values are written in BCD code.

- Year data ranges from 00 to 99.
  - Leap Year = Year divisible by four (2000, 2004, 2008, 2012, and so on)

  - Common Year = Other years
- Month data ranges from 01 to 12.
- Day value ranges:
  - 1 to 31 when months are 1, 3, 5, 7, 8, 10, 12
  - 1 to 30 when months are 4, 6, 9, 11
  - 1 to 29 when month is 2 and year is a leap year
  - 1 to 28 when month is 2 and year is a common year
- Weekday value ranges from 0 to 6.
- Hour value ranges from 0 to 23 in 24-hour mode and ranges from 1 to 12 in AM or PM mode.
- Minutes value ranges from 0 to 59.
- Seconds value ranges from 0 to 59.

Example: Time is 10H54M36S PM (PM_AM mode set), 2008 September 5; previous registers values are listed in Table 8-7:

Table 8-7. RTC Time Calendar Registers Example

REGISTER	CONTENT
RTC_SECONDS	0x36
RTC_MINTURES	0x54
RTC_HOURS	0x10
RTC_DAYS	0x05
RTC_MONTHS	0x09
RTC_YEARS	0x08
RTC_WEEKS	0x06

The user can round to the closest minute, by setting the ROUND_30S register bit in the RTC_CTRL_REG register. TC values are set to the closest minute value at the next second. The ROUND_30S bit is automatically cleared when the rounding time is performed.

Example:
- If current time is 10H59M45S, round operation changes time to 11H00M00S
- If current time is 10H59M29S, round operation changes time to 10H59M00S

8.3.10.2.1 TC Registers Read Access

TC register read access can be done in two ways:
- A direct read to the TC registers. In this case, there can be a discrepancy between the final time read and the real time because the RTC keeps running because some of the registers can toggle in between register accesses. Software must manage the register change during the reading.
- Read access to shadowed TC registers. These registers are at the same addresses as the normal TC registers. They are selected by setting the GET_TIME bit in the RTC_CTRL_REG register. When this bit is set, the content of all TC registers is transferred into shadow registers so they represent a coherent timestamp, avoiding any possible discrepancy between them. When processing the read accesses to the TC registers, the value of the shadowed TC registers is returned so it is completely transparent in terms of register access.

8.3.10.2.2 TC Registers Write Access

TC registers write accesses can be done while RTC is stopped. MCU can stop the RTC by the clearing the STOP_RTC bit of the control register and checking the RUN bit of the status to be sure that RTC is frozen. MCU then updates the TC values and restarts the RTC by setting the STOP_RTC bit, which ensures that the final written values are aligned with the targeted values.

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8.3.10.3 RTC Alarm

RTC alarm registers (ALARM_SECONDS_REG, ALARM_MINUTES_REG, ALARM_HOURS_REG, ALARM_DAYS_REG, ALARM_MONTHS_REG, and ALARM_YEARS_REG) are used to set the alarm time or date to the corresponding generated ALARM interrupts. See Section 8.3.10.2 for how these register values are written in BCD code, with the same data range as described for the TC registers.

8.3.10.4 RTC Interrupts

The RTC supports two types of interrupts:

- ALARM interrupt. This interrupt is generated when the configured date or time in the corresponding ALARM registers is reached. This interrupt is enabled and disabled by setting the IT_ALARM bit. It is important to set the IT_ALARM = 0 to disable the alarm interrupt prior to configuring the ALARM registers to prevent the interrupt from mis-firing.
- TIMER interrupt. This interrupt is generated when the periodic time (day, hour, minute, second) set in the EVERY bits of the RTC_INTERRUPTS register is reached. The first of the periodic interrupt occurs when the RTC counter reaches the next day, hour, minute, or second counter value. For example, if a timer interrupt is set for every hour at 2:59 AM, the first interrupt occurs at 3:00 AM instead of 3:59 AM. This interrupt is enabled and disabled by setting the IT_TIMER bit. It is important to set the IT_TIMER = 0 to disable the timer interrupt prior to configuring the periodic time value to prevent the interrupt from mis-firing.

Both types of the RTC interrupts can be used to wake-up the device from the STANDBY state or the LP_STANDBY state when they are not masked.

8.3.10.5 RTC 32-kHz Oscillator Drift Compensation

The RTC_COMP_MSB_REG and RTC_COMP_LSB_REG registers are used to compensate for any inaccuracy of the 32-kHz clock output from the 32-kHz crystal oscillator. To compensate for any inaccuracy, MCU must perform an external calibration of the oscillator frequency by calculating the needed drift compensation compared to one hour time-period, and load the compensation registers with the drift compensation value.

The compensation mechanism is enabled by the AUTO_COMP_EN bit in the RTC_CTRL_REG register. The process happens after the first second of each hour. The time between second 1 to second 2 (T_ADJ) is adjusted based on the settings of the two RTC_COMP_MSB_REG and RTC_COMP_LSB_REG registers. These two registers form a 16-bit, 2 s complement value COMP_REG (from –32767 to 32767) that is subtracted from the 32-kHz counter as per the following formula to adjust the length of T_ADJ: (32768 - COMP_REG) / 32768. It is therefore possible to adjust the compensation with a 1/32768-second time unit accuracy per hour and up to 1 second per hour.

Software must ensure that these registers are updated before each compensation process (there is no hardware protection). For example, software can load the compensation value into these registers after each hour event, during second 0 to second 1, just before the compensation period, happening from second 1 to second 2.

It is also possible to preload the internal 32-kHz counter with the content of the RTC_COMP_MSB_REG and RTC_COMP_LSB_REG registers by setting the SET_32_COUNTER bit in the RTC_CTRL_REG register. This preloading of the internal 32-kHz counter can only be done when the RTC is stopped.

Figure 8-17 shows the RTC compensation scheduling.

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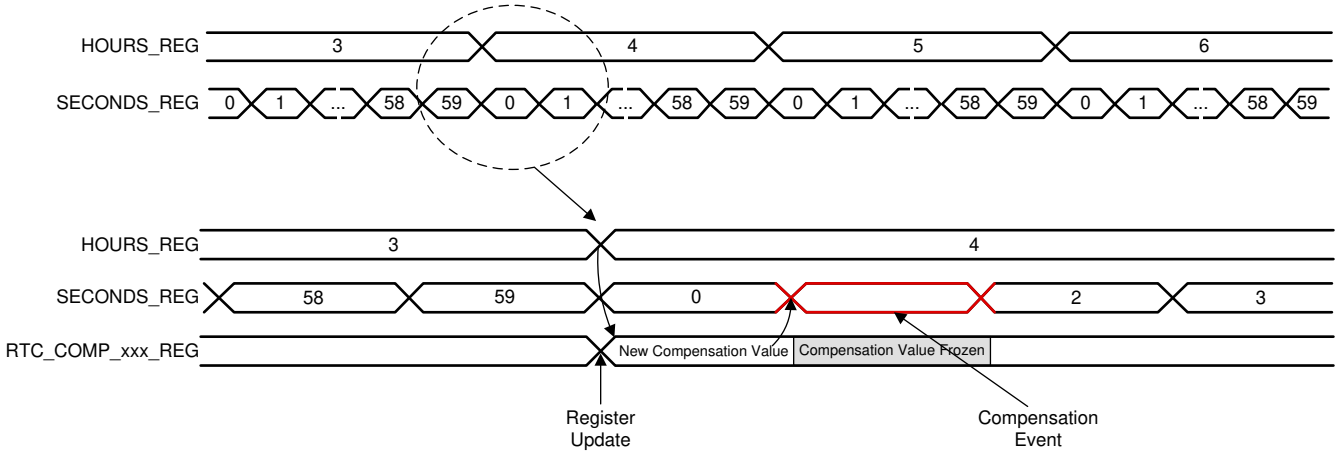

Figure 8-17. RTC Compensation Scheduling

8.3.11 Watchdog (WDOG)

The watchdog monitors the correct operation of the MCU. This watchdog requires specific messages from the MCU in specific time intervals to detect correct operation of the MCU. The MCU can control the logic-level of the EN_DRV pin when the watchdog detects correct operation of the MCU. When the watchdog detects an incorrect operation of the MCU, the TPS6594-Q1 device pulls the EN_DRV pin low . This EN_DRV pin can be used in the application as a control-signal to deactivate the power output stages, for example a motor driver, in case of incorrect operation of the MCU.

The watchdog has two different modes which are defined as follows:

Trigger mode	In trigger mode, the MCU applies a pulse signal with a minimum pulse width of t_{WD_pulse} on the pre-assigned GPIO input pin to send the required watchdog trigger. To select this mode, the MCU must clear bit WD_MODE_SELECT. Watchdog Trigger Mode provides more details.
Q&A (question and answer) mode	In Q&A mode, the MCU sends watchdog answers through the I2C bus or SPI bus. To select this mode, the MCU must set bit WD_MODE_SELECT. Watchdog Q&A Related Definitions provides more details.

8.3.11.1 Watchdog Fail Counter and Status

The watchdog includes a watchdog fail counter WD_FAIL_CNT[3:0] that increments because of *bad events* or decrements because of *good events*. Furthermore, the watchdog includes two configurable thresholds:

1. Fail-threshold (configurable through bits WD_FAIL_TH[2:0])
2. Reset-threshold (configurable through bits WD_RST_TH[2:0])

When the WD_FAIL_CNT[3:0] counter value is greater than the configured Watchdog-Fail threshold (WD_FAIL_CNT[3:0] > WD_FAIL_TH[2:0]), the device sets the error-flag WD_FAIL_INT, and pulls the nINT pin low.

When the WD_FAIL_CNT[3:0] counter value is greater than the configured Watchdog-Fail plus Watchdog-Reset threshold (WD_FAIL_CNT[3:0] > (WD_FAIL_TH[2:0] + WD_RST_TH[2:0])) and the watchdog-reset function is enabled (configuration bit WD_RST_EN=1), the device generates a WD_ERROR trigger in the state machine and sets the error-flag WD_RST_INT, and pulls the nINT pin low.

The device clears the WD_FAIL_CNT[3:0] each time the watchdog enters the Long Window. The status bits WD_FAIL_INT and WD_RST_INT are latched until the MCU writes a ‘1’ to these bits.

Overview of Watchdog Fail Counter Value Ranges and Corresponding Device Status gives an overview of the Watchdog Fail Counter value ranges and the corresponding device status.

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Table 8-8. Overview of Watchdog Fail Counter Value Ranges and Corresponding Device Status

Watchdog Fail Counter value WD_FAIL_CNT[3:0]	Device Status
WD_FAIL_CNT[3:0] ≤ WD_FAIL_TH[2:0]	no other error-flags are set
WD_FAIL_TH[2:0] < WD_FAIL_CNT[3:0] ≤ (WD_FAIL_TH[2:0] + WD_RST_TH[2:0])	The device sets error-flag WD_FAIL_INT and pulls the nINT pin low
WD_FAIL_CNT[3:0] > (WD_FAIL_TH[2:0] + WD_RST_TH[2:0])	If configuration bit WD_RST_EN=1, device generates WD_ERROR trigger in the state machine and reacts as defined in the PFSM, sets the error-flag WD_RST_INT, and pulls the nINT pin low. See Summary of Interrupt Signals for the interrupt handling of WD_RTS.

The WD_FAIL_CNT[3:0] counter responds as follows:

- When the Watchdog is in the Long-Window, the WD_FAIL_CNT[3:0] is cleared to 4'b0000
- A good event decrements the WD_FAIL_CNT[3:0] by one before the start of the next Window-1
- A bad event increments the WD_FAIL_CNT[3:0] by one before the start of the next Window-1

Refer to Watchdog Trigger Mode and Watchdog Q&A Related Definitions respectively for definitions of good events and bad events.

8.3.11.2 Watchdog Start-Up and Configuration

When the device releases the nRSTOUT pin, the watchdog starts with the Long Window. This Long Window has a time interval (t_{LONG_WINDOW}) with a default value set in bits WD_LONGWIN[7:0].

As long as the watchdog is in the Long Window, the MCU can configure the watchdog through the following register bits:

- WD_EN to enable or disable the watchdog
- WD_LONGWIN[7:0] to increase the duration of the Long-Window time-interval
- WD_MODE_SELECT to select the Watchdog mode (Trigger mode or Q&A Mode)
- WD_PWRHOLD to activate the Watchdog Disable function (more detail in Section 8.3.11.4)
- WD_RETURN_LONGWIN to configure whether to return to Long-Window or continue to the next sequence after the completion of the current watchdog sequence (more detail in Section 8.3.11.4)
- WD_WIN1[6:0] to configure the duration of the Window-1 time-interval
- WD_WIN2[6:0] to configure the duration of the Window-2 time-interval
- WD_RST_EN to enable or disable the watchdog-reset function
- WD_FAIL_TH[2:0] to configure the Watchdog-Fail threshold
- WD_RST_TH[2:0] to configure the Watchdog-Reset threshold

The device keeps the above register bit values configured by the MCU as long as the device is powered.

The MCU can configure the time interval of the Long Window (t_{LONG_WINDOW}) with the WD_LONGWIN[7:0] bits. The WD_LONGWIN[7:0] bits are defined as:

- 0x00: 80 ms
- 0x01 - 0x40: 125 ms to 8 sec, in 125-ms steps
- 0x41 - 0xFF: 12 sec to 772 sec, in 4-sec steps

Use Equation 4 and Equation 5 to calculate the minimum and maximum values for the Long Window (t_{LONG_WINDOW}) time interval when WD_LONGWIN[7:0] > 0x00:

$$t_{LONG_WINDOW_MIN} = WD_LONGWIN[7:0] \times 0.95 \quad (4)$$

$$t_{LONG_WINDOW_MAX} = WD_LONGWIN[7:0] \times 1.05 \quad (5)$$

Note

If the MCU software changes the duration of the Long-Window to an interval shorter than the time in which the watchdog has been in the Long-Window, the time-out function of the Long-Window does no longer operate.

When the MCU clears bit WD_EN, the watchdog goes out of the Long Window and disables the watchdog. When the watchdog is disabled in this way, the MCU can set bit WD_EN back to '1' to enable the watchdog again, and the MCU can control the ENABLE_DRV bit when no other error-flags are set. The MCU must clear bit WD_PWRHOLD before setting bit WD_EN back to '1' to start the watchdog in Long Window.

The watchdog locks the following configuration register bits when it goes out of the Long Window and starts the first watchdog sequence:

- WD_WIN1[6:0]
- WD_WIN2[6:0]
- WD_LONGWIN[7:0]
- WD_MODE_SELECT
- WD_RST_EN, WD_EN, WD_FAIL_TH[2:0] and WD_RST_TH[2:0]

8.3.11.3 MCU to Watchdog Synchronization

In order to go out of the Long Window and start the first watchdog sequence, the MCU must do the following:

- Clear bits WD_PWRHOLD (more detail in Section 8.3.11.4)
- Apply a pulse signal with a minimum pulse-width t_{WD_pulse} on the pre-assigned GPIO pin in the case the watchdog is configured for Trigger mode, or
- Write four times to WD_ANSWER[7:0] in the case the watchdog is configured for Q&A mode

When the MCU fails to get the watchdog out of the Long Window before the configured Long Window time interval (t_{LONG_WINDOW}) elapses, the device goes through a warm reset, and sets the WD_LONGWIN_TIMEOUT_INT. This bit latched until the MCU writes a '0' to it '1' to clear it.

8.3.11.4 Watchdog Disable Function

The watchdog in the TPS6594-Q1 device has a Watchdog Disable function to prevent an unwanted MCU reset in case the MCU is un-programmed or needs to be reprogrammed. In order to activate this Watchdog Disable function for an un-programmed MCU, DISABLE_WDOG pin must be asserted to a logic-high level for a time-interval longer than t_{WD_DIS} prior to the moment the device releases the nRSTOUT pin. If the Watchdog Disable function is activated in this way, the device sets bit WD_PWRHOLD to keep the watchdog in the Long Window. The watchdog stays in the Long Window until the MCU clears the WD_PWRHOLD bit.

In case the MCU needs to be reprogrammed while the watchdog monitors the correct operation of the MCU, the MCU can set bit WD_RETURN_LONGWIN to put the watchdog back in the Long Window. When the MCU set this bit, the watchdog returns to the Long Window after the current Watchdog Sequence completes. In order to make the watchdog stay in the Long Window as long as needed the MCU can either re-configure the Long Window (t_{LONG_WINDOW}) time interval, or set the WD_PWRHOLD bit. Once the MCU starts the first watchdog sequence (as described in Section 8.3.11.3), the MCU must clear bit WD_RETURN_LONGWIN before the end of the first watchdog sequence in order to continue the watchdog sequence operation.

8.3.11.5 Watchdog Sequence

Once the watchdog is out of the Long Window, each watchdog sequence starts with a Window-1 followed by a Window-2. The watchdog ends the current sequence and starts a next sequence when one of the events below occurs:

- The configured Window-2 time period elapses
- The watchdog detects a pulse signal with a minimum pulse-width t_{WD_pulse} on the pre-assigned GPIO pin if the watchdog is used in Trigger mode
- The watchdog detects four times a write access to WD_ANSWER[7:0] in case the watchdog is used in Q&A mode

The MCU can configure the time periods of the Window-1 ($t_{WINDOW1}$) and Window-2 ($t_{WINDOW2}$) with the bits WD_WIN1[6:0] and WD_WIN2[6:0] respectively, before starting the sequence.

Use Equation 6 and Equation 7 to calculate the minimum and maximum values for the $t_{WINDOW1}$ time interval.

$$t_{WINDOW1_MIN} = (WD_WIN1[6:0] + 1) \times 0.55 \times 0.95 \text{ ms} \quad (6)$$

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$$t_{WINDOW1_MAX} = (WD_WIN1[6:0] + 1) \times 0.55 \times 1.05 \text{ ms} \quad (7)$$

Use Equation 8 and Equation 9 to calculate the minimum and maximum values for the $t_{WINDOW-2}$ time interval.

$$t_{WINDOW2_MIN} = (WD_WIN2[6:0] + 1) \times 0.55 \times 0.95 \text{ ms} \quad (8)$$

$$t_{WINDOW2_MAX} = (WD_WIN2[6:0] + 1) \times 0.55 \times 1.05 \text{ ms} \quad (9)$$

8.3.11.6 Watchdog Trigger Mode

When the TPS6594-Q1 device is configured to use the Watchdog Trigger Mode, the watchdog receives the watchdog-triggers from the MCU on the pre-assigned GPIO pin. A rising edge on this GPIO pin, followed by a stable logic-high level on that pin for more than the maximum pulse time, $t_{WD_pulse(max)}$, is a watchdog-trigger. The watchdog uses a deglitch filter with a t_{WD_pulse} filter time and an internal system clock to create the internally-generated trigger pulse from the watchdog-trigger on the pre-assigned GPIO pin.

The watchdog detects a *good event* when the watchdog-trigger comes in Window-2. The rising edge of the watchdog-trigger on the pre-assigned GPIO pin must occur for at least the t_{WD_pulse} time before the end of Window-2 to generate such a good event.

The watchdog detects a *bad event* when one of the following events occurs:

- The watchdog-trigger comes in Window-1. The rising edge of the watchdog-trigger on the pre-assigned GPIO pin must occur for at least the t_{WD_pulse} time before the end of Window-1 to generate such a bad event. In case of this bad event, the device sets bits WD_TRIG_EARLY and WD_BAD_EVENT.
- No watchdog-trigger comes in Window-2. In case of this bad event (also referred to as time-out event), the device sets bits WD_TIMEOUT and WD_BAD_EVENT.

Please consider that the minimum WD-pulse duration needs to meet the maximum deglitch time $t_{WD_pulse\ (max)}$.

The status bit WD_BAD_EVENT is read-only. The watchdog clears the WD_BAD_EVENT status bit at the end of the watchdog-sequence.

Flow Chart for WatchDog Monitor in Trigger Mode shows the flow-chart of the watchdog in Trigger mode.

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8.3.11.7 WatchDog Flow Chart and Timing Diagrams in Trigger Mode

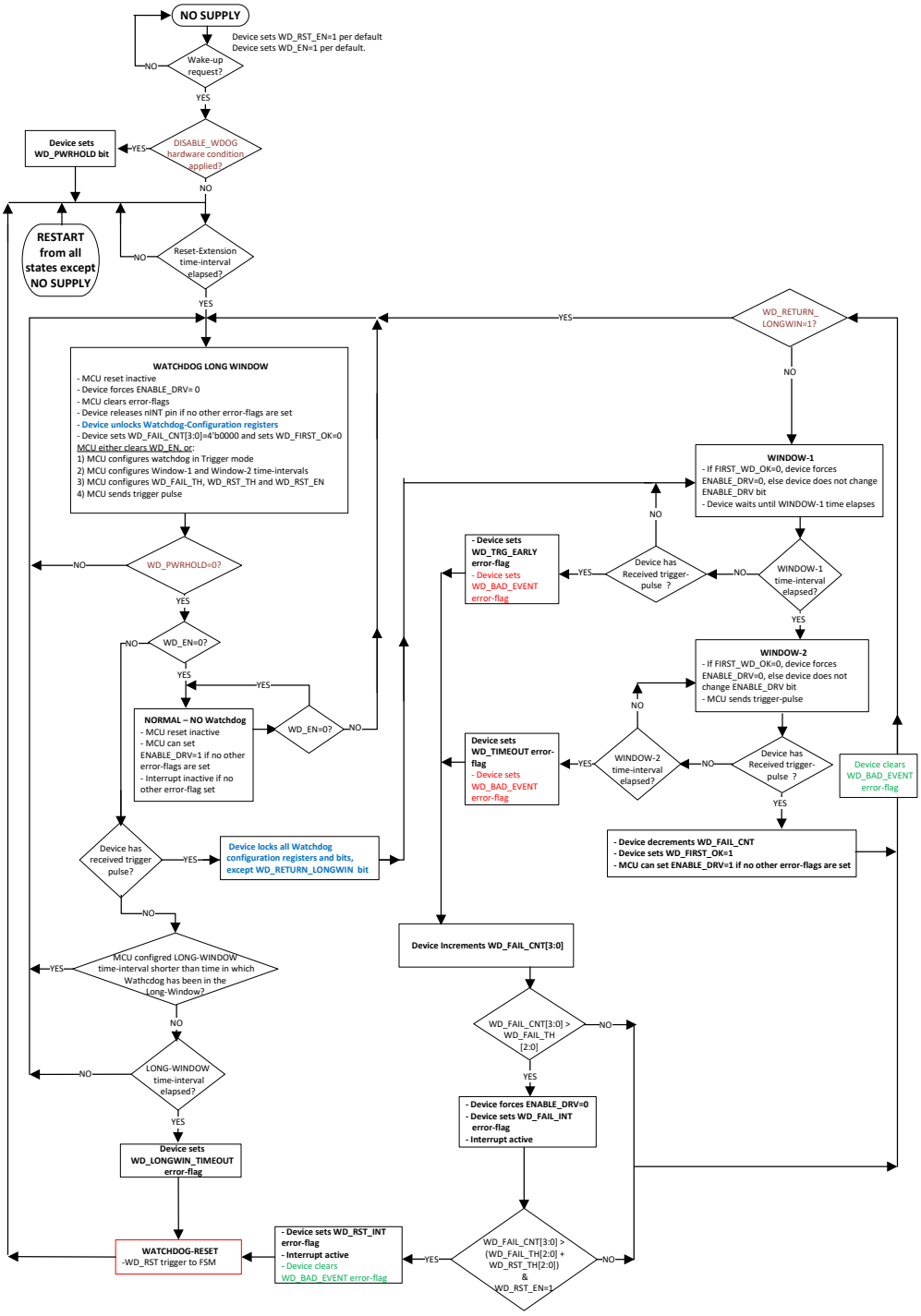

Figure 8-18. Flow Chart for WatchDog Monitor in Trigger Mode

Figure 8-19, Figure 8-20, Figure 8-21, Figure 8-22, and Figure 8-23 give examples of watchdog is trigger mode with good and bad events after device start-up.

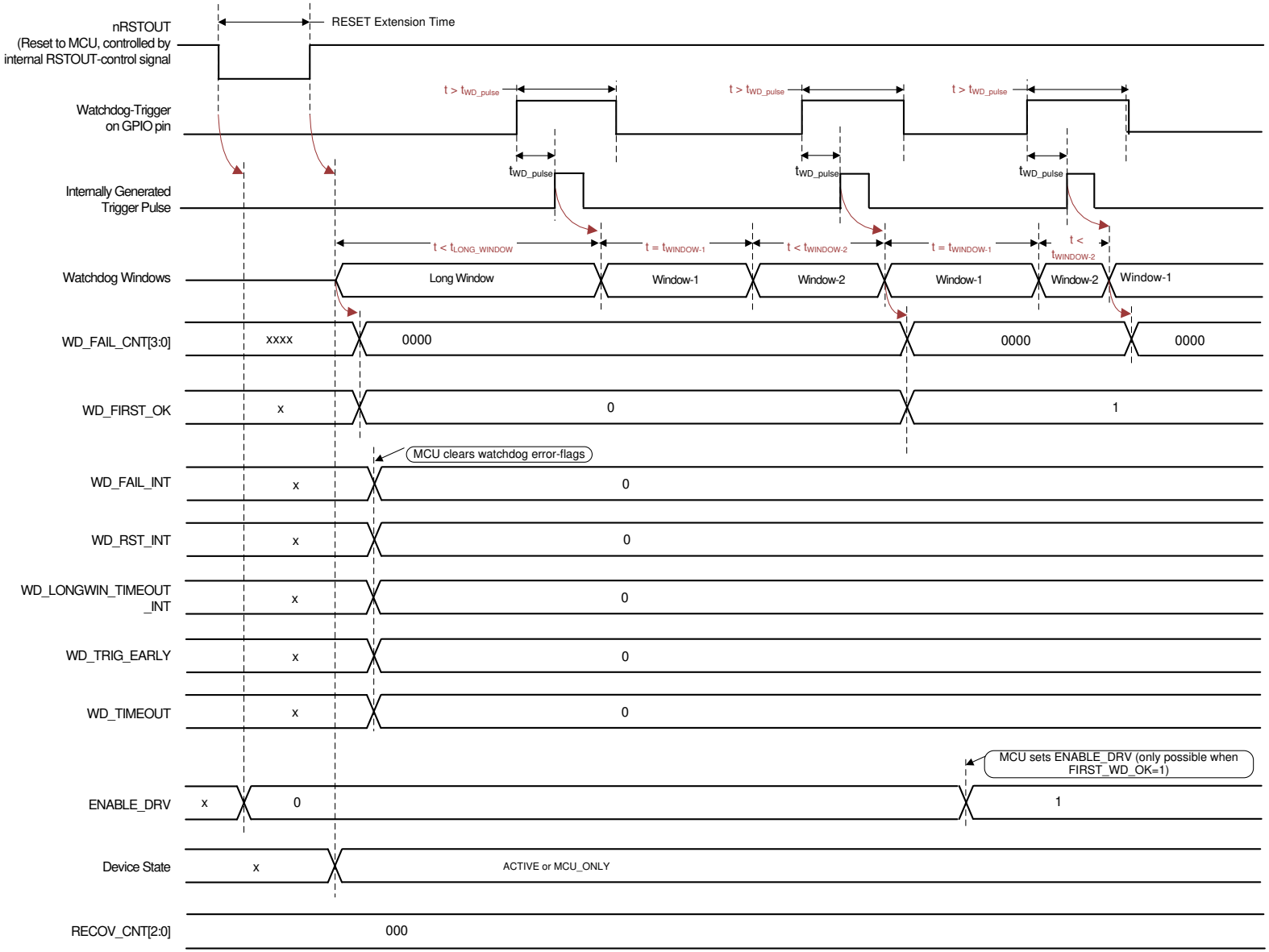

Figure 8-19. Watchdog in Trigger Mode – Normal MCU Start-up with Correct Watchdog-Triggers

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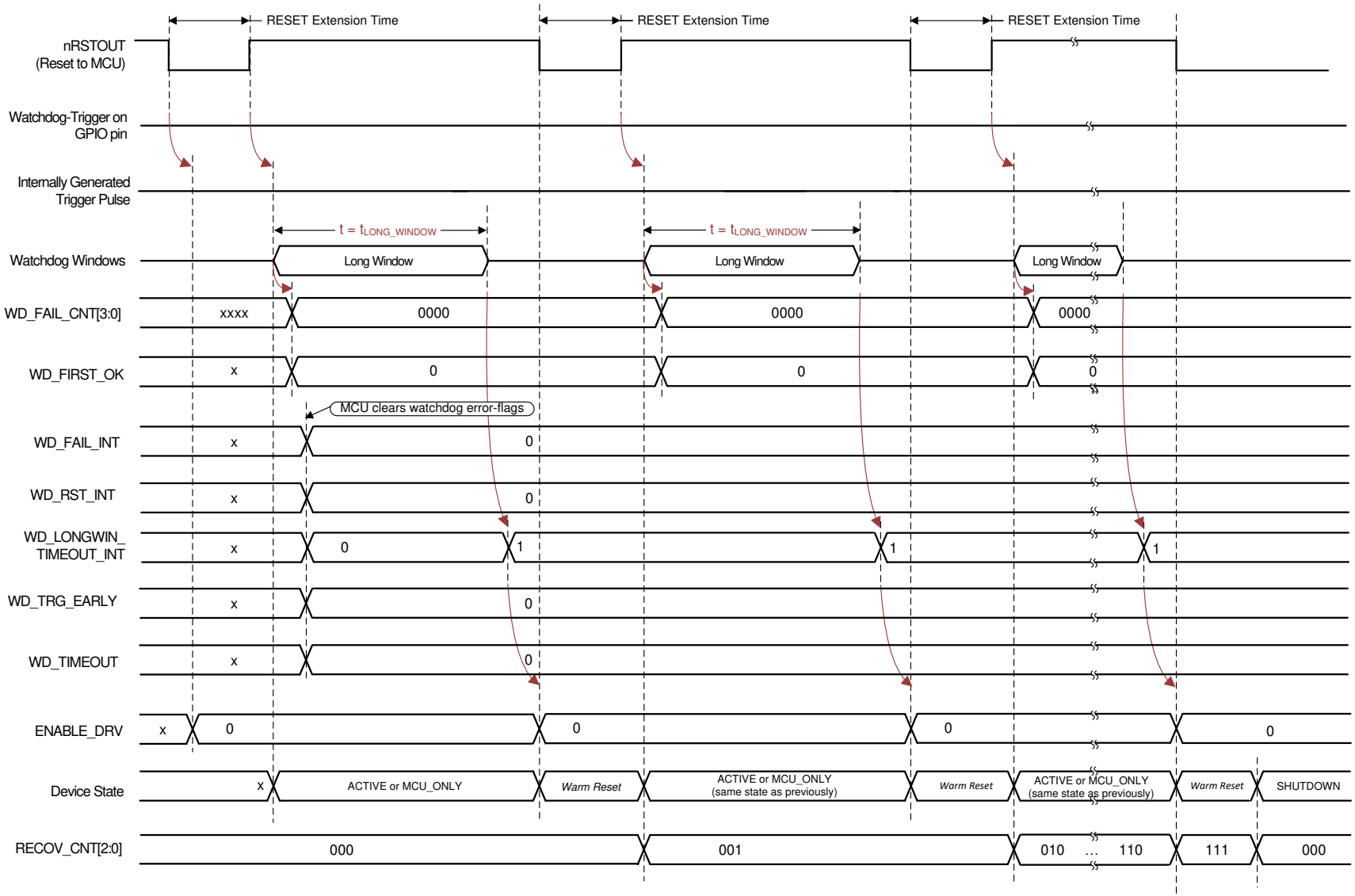

Figure 8-20. Watchdog in Trigger Mode – MCU Does Not Send Watchdog-Triggers After Start-up

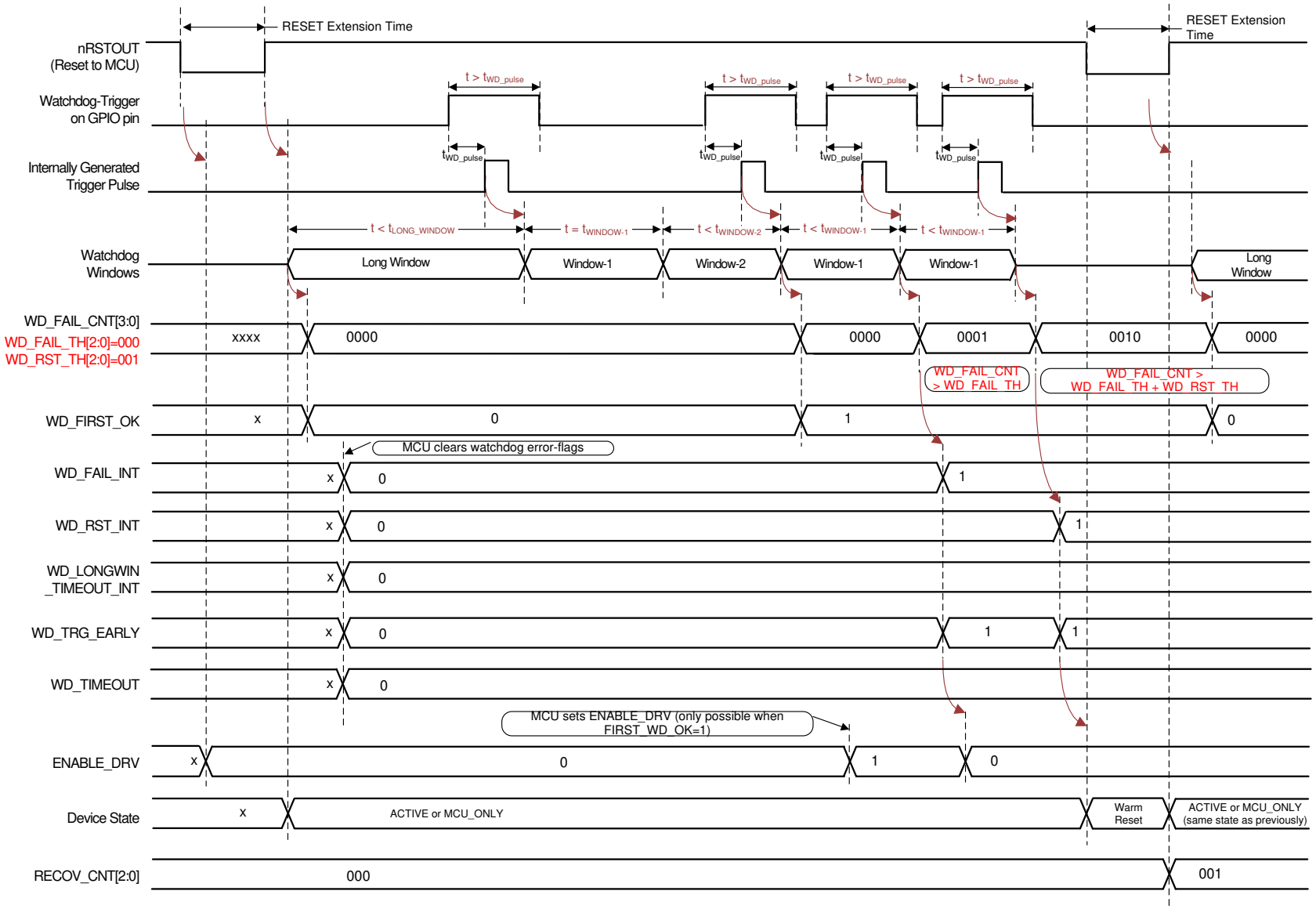

Figure 8-21. Watchdog in Trigger Mode – Bad Event (Watchdog-Triggers in Window-1) After Start-up

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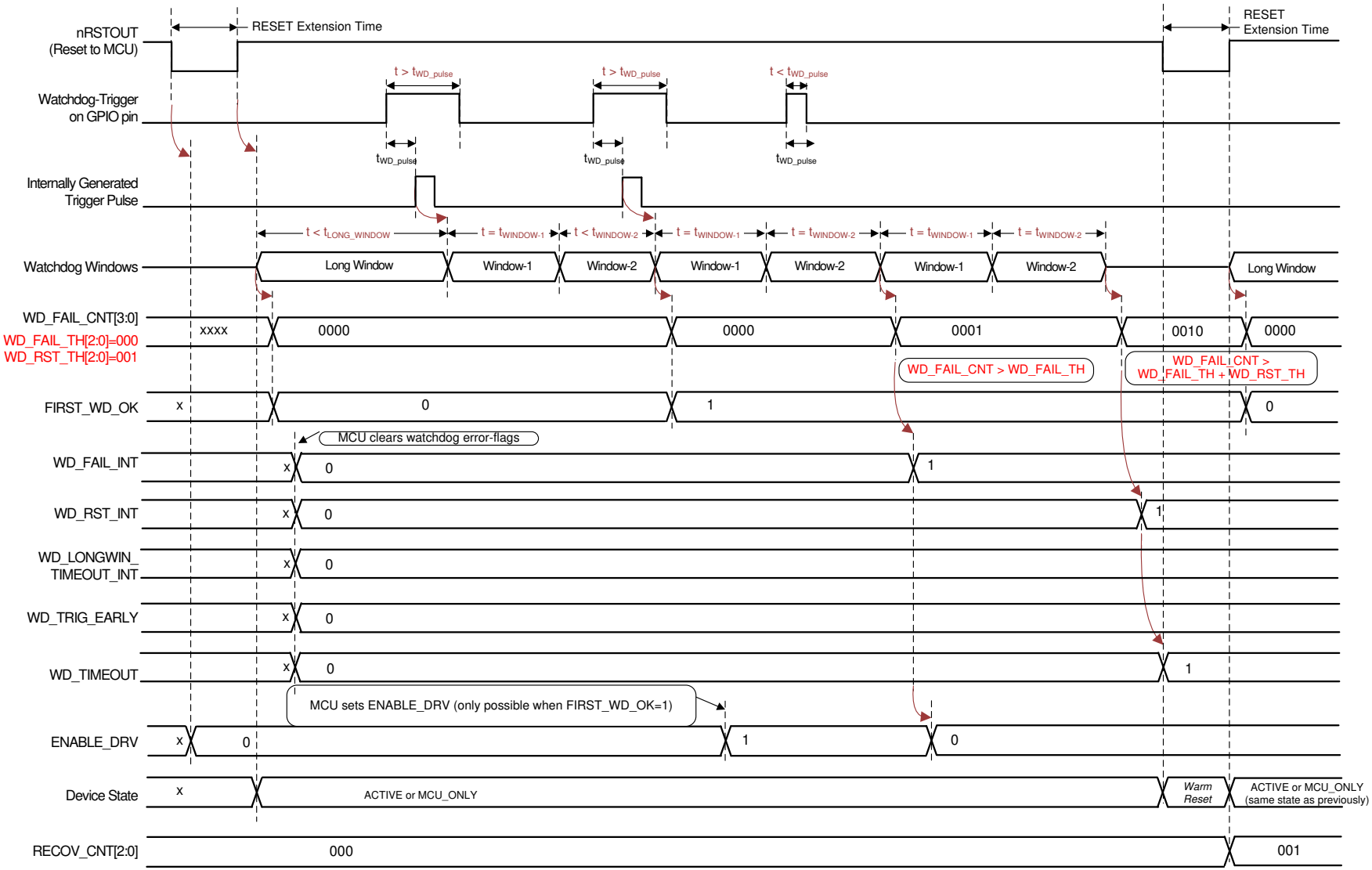

Figure 8-22. Watchdog in Trigger Mode – Bad Events (Too Short or no Trigger in Window-2) After Start-up

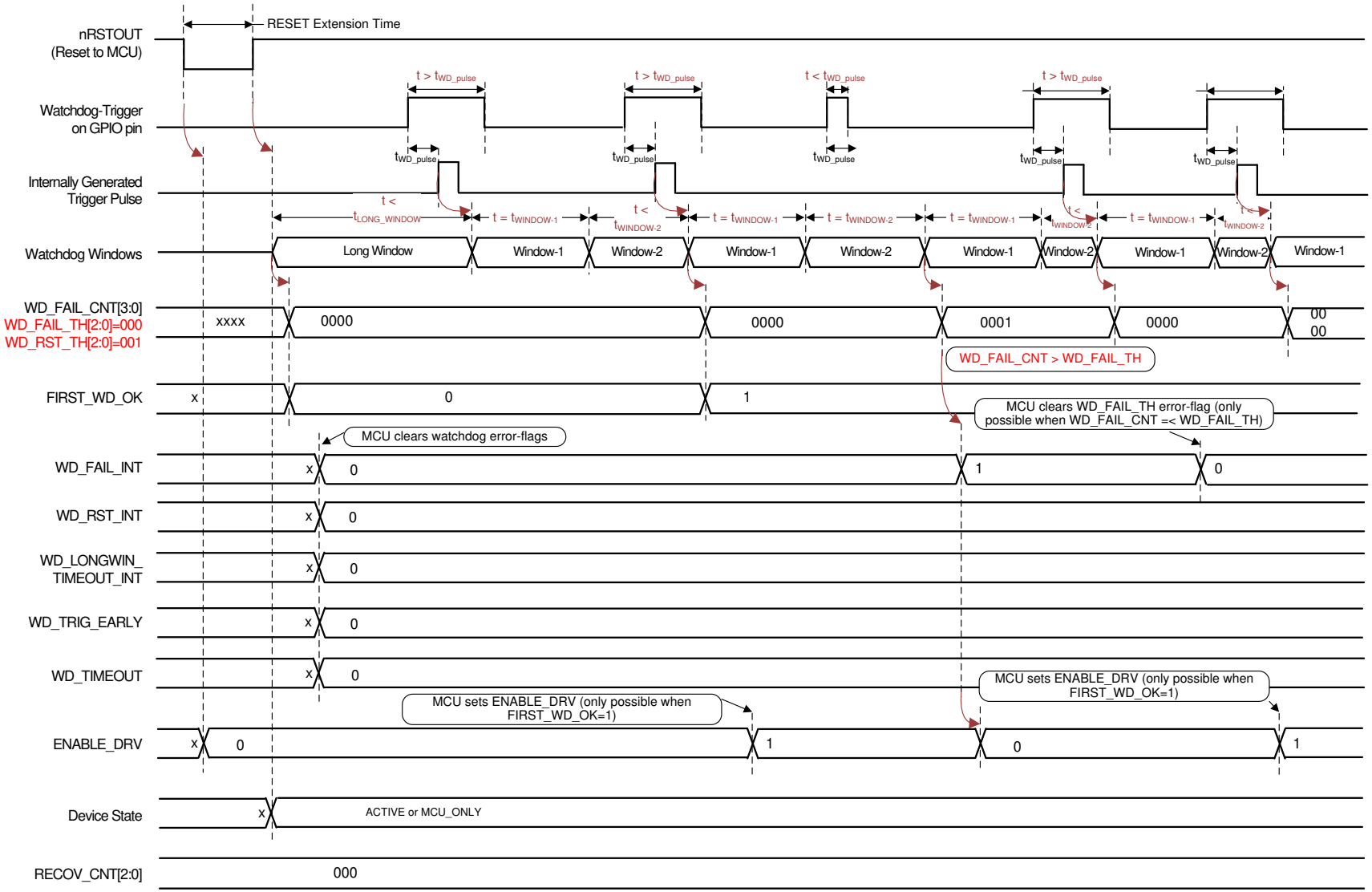

Figure 8-23. Watchdog in Trigger Mode – Good Events (Correct Watchdog-Triggers) After Start-up, Followed by a Bad-Event (No Watchdog-Trigger in Window-2) and After That Followed by a Good Event.

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8.3.11.8 Watchdog Question-Answer Mode

When the TPS6594-Q1 device is configured to use the Watchdog Question Answer mode, the watchdog requires specific messages from the MCU in specific time intervals to detect correct operation of the MCU.

The device provides a question for the MCU in WD_QUESTION[3:0] during operation. The MCU performs a fixed series of arithmetic operations on this question to calculate the required 32-bit answer. This answer is split into four answer bytes: Answer-3, Answer-2, Answer-1, and Answer-0. The MCU writes these answer bytes one byte at a time into WD_ANSWER[7:0] from the SPI or the dedicated I^2C2 interface, mapped to GPIO1 and GPIO2 pins.

A good event occurs when the MCU sends the correct answer-bytes calculated for the current question in the correct watchdog window and in the correct sequence.

A bad event occurs when one of the events that follows occur:

- The MCU sends the correct answer-bytes, but not in the correct watchdog window.
- The MCU sends incorrect answer-bytes.
- The MCU returns correct answer-bytes, but in the incorrect sequence.

If the MCU stops providing answer-bytes for the duration of the watchdog time-period, the watchdog detects a time-out event. This time-out event sets the WD_TIMEOUT status bit, increments the WD_FAIL_CNT[3:0] counter, and starts a new watchdog sequence.

8.3.11.8.1 Watchdog Q&A Related Definitions

A question and answer are defined as follows:

Question A question is a 4-bit word (see Section 8.3.11.8.2).

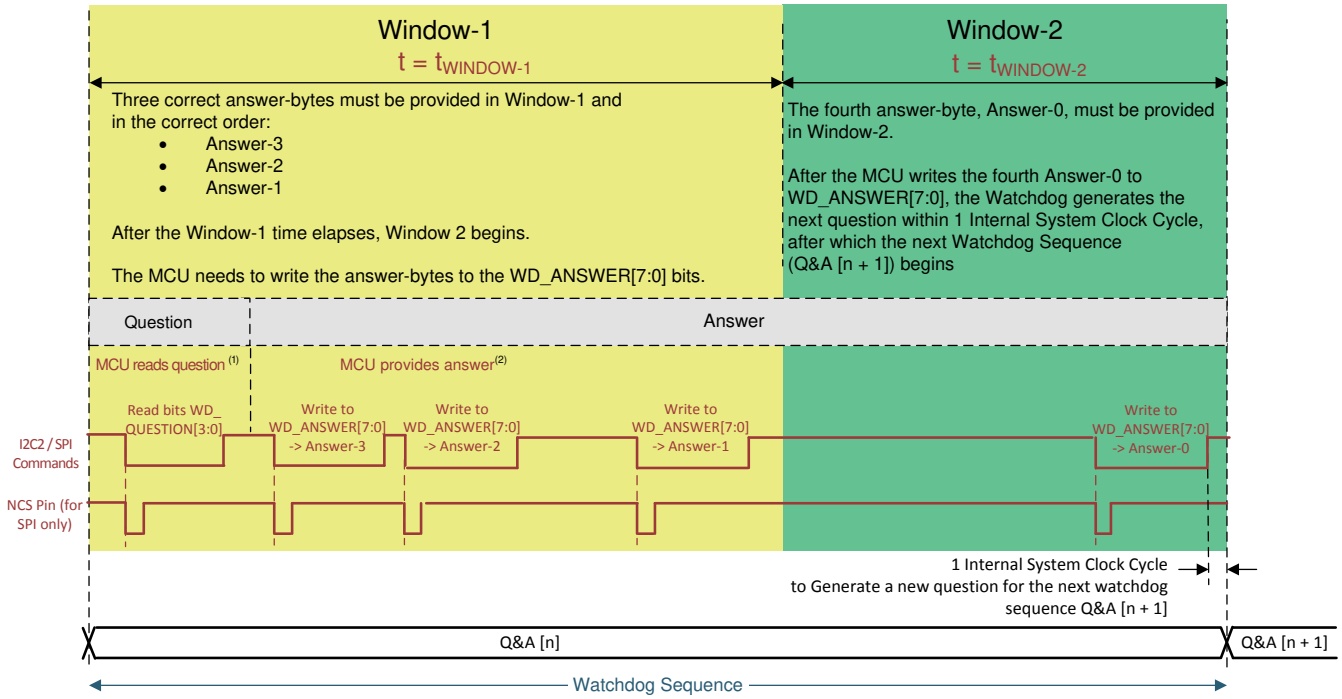
The watchdog provides the question to the MCU when the MCU reads the WD_QUESTION[3:0] bits.

The MCU can request each new question at the start of the watchdog sequence, but this is not required to calculate the answer. The MCU can also have a software implementation, which generates the question according the circuit shown in Figure 8-26. Nevertheless, the answer and therefore the answer-bytes are always based on the question generated inside the watchdog of the device. So, if the MCU generates an incorrect question and gives answer-bytes calculated from this incorrect question, the watchdog detects a bad event

Answer An answer is a 32-bit word that is split into four answer bytes: Answer-3, Answer-2, Answer-1, and Answer-0.

The watchdog receives an answer-byte when the MCU writes to the WD_ANSWER[7:0] bits. For each question, the watchdog requires four correct answer-bytes from the MCU in the correct timing and order (Answer-3, Answer-2, and Answer-1 in Window 1 in the correct sequence, and Answer-0 in Window 2) to detect a good event.

The watchdog sequence in Q&A mode ends after the MCU writes the fourth answer byte (Answer-0), or after a time-out event when the Window-2 time-interval elapses.



(1) The MCU is not required to read the question. The MCU can give correct answer-bytes Answer-3, Answer-2, Answer-1 as soon as Window-1 starts. The next watchdog sequence always starts in 1 system clock cycle after the watchdog receives the final Answer-0.
(2) The MCU can put other I^{2}C or SPI commands in-between the write-commands to WD_ANSWER[7:0] (even re-requesting the question). This has no influence on the detection of a good event, as long as the three correct answer-bytes in Window-1 are in the correct sequence, and the fourth correct answer-byte is provided before the configured Window-2 time-interval elapses.

Figure 8-24. Watchdog Sequence in Q&A Mode

8.3.11.8.2 Question Generation

The watchdog uses a 4-bit *question counter* (QST_CNT[3:0] bits in Figure 8-25), and a 4-bit Markov chain to generate a 4-bit question. The MCU can read this question in the WD_QUESTION[3:0] bits. The watchdog generates a new question when the question counter increments, which only occurs when the watchdog detects a good event. The watchdog does not generate a new question when it detects a bad event or a time-out event.

The question-counter provides a clock pulse to the Markov chain when it transitions from 4'b1111 to 4'b0000. The question counter and the Markov chain are set to the default value of 4'b0000 when the watchdog goes out of the Long Window.

Note

The Question-Generator is only re-initialized (starting with question 0000) at device power-up. In following situations, the MCU software needs to read the current question in order to synchronize with the Question-Generator:

- After MCU re-boot from a warm-reset
- After MCU software sets bit WD_RETURN_LONGWIN=1 to put the Watchdog back into Long Window
- After MCU wrote WD_EN=0, then reenable Watchdog again with WD_EN=1

Figure 8-25 shows the logic combination for the WD_QUESTION[3:0] generation.

Figure 8-26 shows how the logic combination of the question-counter with the WD_ANSW_CNT[1:0] status bits generates the reference answer-bytes.

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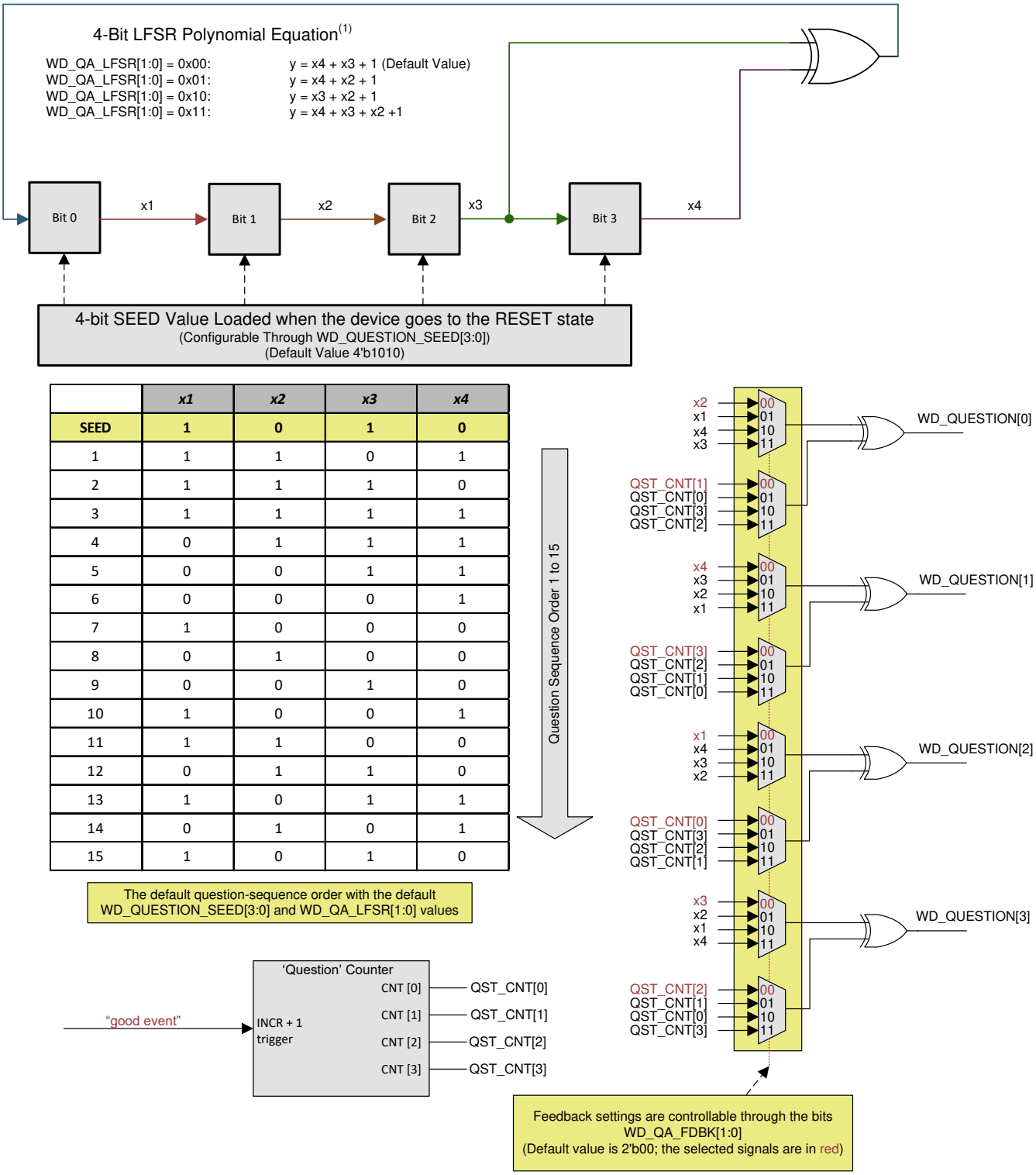

	x1	x2	x3	x4
SEED	**1**	**0**	**1**	**0**
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1
6	0	0	0	1
7	1	0	0	0
8	0	1	0	0
9	0	0	1	0
10	1	0	0	1
11	1	1	0	0
12	0	1	1	0
13	1	0	1	1
14	0	1	0	1
15	1	0	1	0

(1) If the current value for bits (x1, x2, x3, x4) is 4'b0000, the next value for these bits (x1, x2, x3, x4) is 4'b0001, and all further question generation begins from this value.

Figure 8-25. Watchdog Question Generation

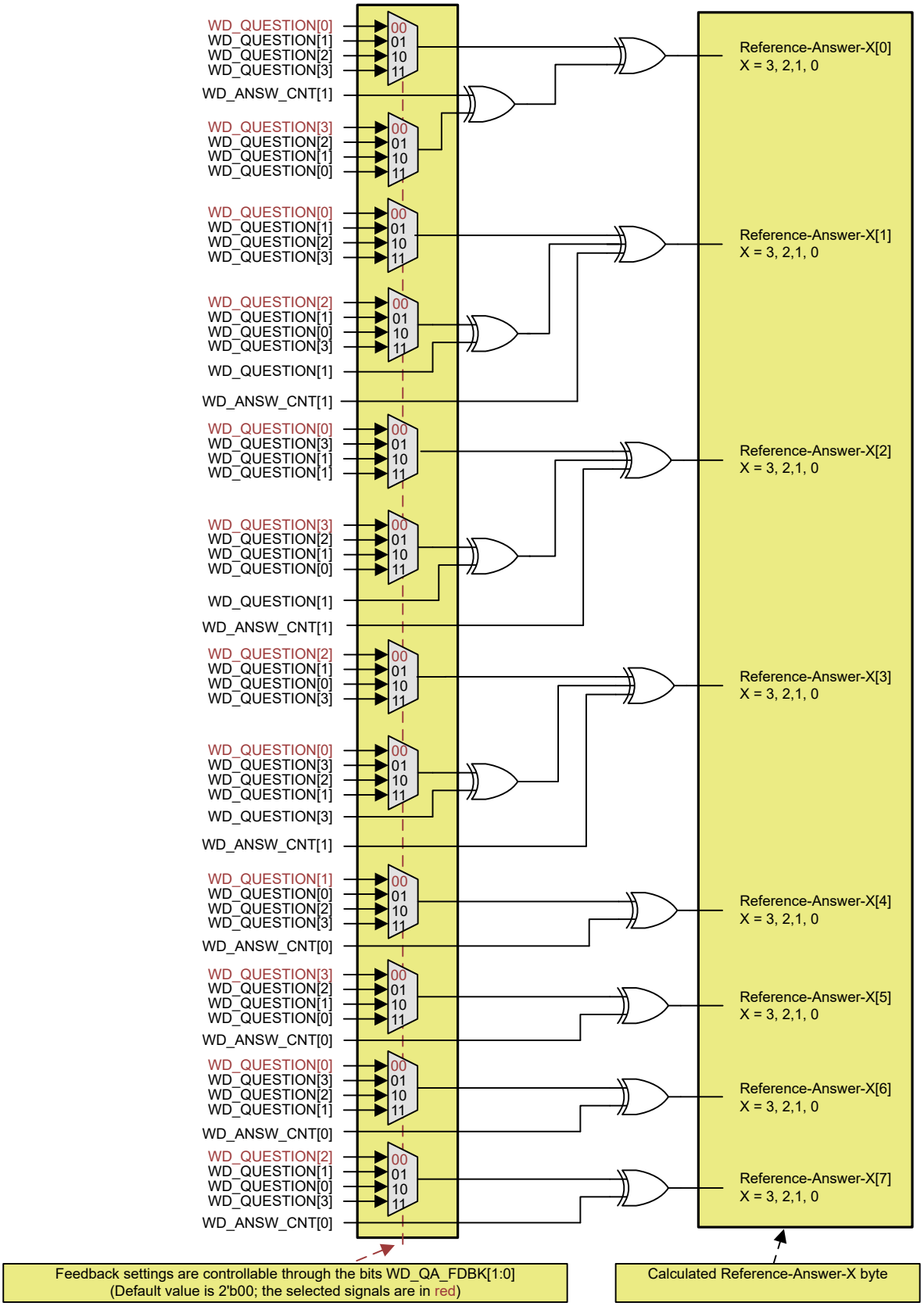

Figure 8-26. Watchdog Reference Answer Calculation

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8.3.11.8.3 Answer Comparison

The 2-bit, watchdog-answer counter, WD_ANSW_CNT[1:0], counts the number of received answer-bytes and controls the generation of the reference answer-byte as shown in Figure 8-26. At the start of each watchdog sequence, the default value of the WD_ANSW_CNT[1:0] counter is 2'b11 to indicate that the watchdog expects the MCU to write the correct Answer-3 in WD_ANSWER[7:0].

The device sets the WD_ANSW_ERR status bit as soon as one answer byte is not correct. The device clears this status bit only if the MCU writes a '1' to this bit.

8.3.11.8.3.1 Sequence of the 2-bit Watchdog Answer Counter

The sequence of the 2-bit, watchdog answer-counter is as follows for each counter value:

- WD_ANSW_CNT[1:0] = 2'b11:
  1. The watchdog calculates the reference Answer-3.
  2. A write access occurs. The MCU writes the Answer-3 byte in WD_ANSWER[7:0].
  3. The watchdog compares the reference Answer-3 with the Answer-3 byte in WD_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 2b'10 and sets the WD_ANSW_ERR status bit to 1 if the Answer-3 byte was incorrect.

- WD_ANSW_CNT[1:0] = 2b‘10:
  1. The watchdog calculates the reference Answer-2.
  2. A write access occurs. The MCU writes the Answer-2 byte in WD_ANSWER[7:0].
  3. The watchdog compares the reference Answer-2 with the Answer-2 byte in WD_ANSWER[7:0]..
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 2b‘01 and sets the WD_ANSW_ERR status bit to 1 if the Answer-2 byte was incorrect.
- WD_ANSW_CNT[1:0] = 2b‘01:
  1. The watchdog calculates the reference Answer-1.
  2. A write access occurs. The MCU writes the Answer-1 byte in WD_ANSWER[7:0].
  3. The watchdog compares the reference Answer-1 with the Answer-1 byte in WD_ANSWER[7:0]..
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 2b‘00 and sets the WD_ANSW_ERR status bit to 1 if the Answer-1 byte was incorrect.
- WD_ANSW_CNT[1:0] = 2b‘00:
  1. The watchdog calculates the reference Answer-0.
  2. A write access occurs. The MCU writes the Answer-0 byte in WD_ANSWER[7:0].
  3. The watchdog compares the reference Answer-0 with the Answer-0 byte in WD_ANSWER[7:0].
  4. The watchdog sets the WD_ANSW_ERR status bit to 1 if the Answer-0 byte was incorrect.
  5. The watchdog starts a new watchdog sequence and sets the WD_ANSW_CNT[1:0] to 2‘b11’.

  The MCU needs to clear the bit by writing a '1' to the WD_ANSW_ERR bit.

Table 8-9. Set of Questions and Corresponding Answer-Bytes Using the Default Setting of WD_QA_CFG Register

WD QUESTION	ANSWER-BYTES (EACH BYTE TO BE WRITTEN INTO WD_ANSWER[7:0])			
	ANSWER-3	ANSWER-2	ANSWER-1	ANSWER-0
WD_QUESTION[3:0]	WD_ANSW_CNT [1:0] = 2’b11	WD_ANSW_CNT [1:0] = 2’b10	WD_ANSW_CNT [1:0] = 2’b01	WD_ANSW_CNT [1:0] = 2’b00
0x0	FF	0F	F0	00
0x1	B0	40	BF	4F
0x2	E9	19	E6	16
0x3	A6	56	A9	59
0x4	75	85	7A	8A
0x5	3A	CA	35	C5
0x6	63	93	6C	9C
0x7	2C	DC	23	D3
0x8	D2	22	DD	2D
0x9	9D	6D	92	62
0xA	C4	34	CB	3B
0xB	8B	7B	84	74
0xC	58	A8	57	A7
0xD	17	E7	18	E8
0xE	4E	BE	41	B1
0xF	01	F1	0E	FE

8.3.11.8.3.2 Watchdog Sequence Events and Status Updates

The watchdog sequence events are as follows for the different scenarios listed:

- A good event occurs when all answer bytes are correct in value and timing. After such a good event, following events occur:
  1. The WD_FAIL_CNT[2:0] counter decrements by one at the end of the watchdog-sequence.
  2. The question-counter increments by one and the watchdog generates a new question.
- A bad event occurs when all answer-bytes are correct in value but not in correct timing. After such a bad event, following events occur:

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1. The WD_SEQ_ERR and WD_BAD_EVENT status bits are set if Window-1 time-interval elapses before watchdog has received Answer-3, Answer-2 and Answer-1.
2. The WD_ANSW_EARLY and WD_BAD_EVENT status bits are set if watchdog receives all four answers in Window-1.
3. The WD_FAIL_CNT[2:0] counter increments by one at the end of the watchdog-sequence.
4. The question-counter does not change, and hence the watchdog does not generate a new question.

- A bad event occurs when one or more of the answer-bytes are not correct in value but in correct timing. After such a bad event, following events occur:
  1. The WD_ANSW_ERR and WD_BAD_EVENT status bits are set as soon as the watchdog detects an incorrect answer-byte.
  2. The WD_FAIL_CNT[2:0] counter increments by one at the end of the watchdog-sequence.
  3. The question-counter does not change, and hence the watchdog does not generate a new question.
- A bad event occurs when one or more of the answer-bytes are not correct in value and not in correct timing. After such a bad event, following events occur:
  1. The WD_ANSW_ERR and WD_BAD_EVENT status bits are set as soon as the watchdog detects an incorrect answer-byte.
  2. The WD_SEQ_ERR and WD_BAD_EVENT status bits are set if Window-1 time-interval elapses before watchdog has received Answer-3, Answer-2 and Answer-1.
  3. The WD_ANSW_EARLY and WD_BAD_EVENT status bits are set if watchdog receives all four answer-bytes in Window-1.
  4. The WD_FAIL_CNT[2:0] counter increments by one at the end of the watchdog-sequence.
  5. The question-counter does not change, and hence the watchdog does not generate a new question.
- A time-out event occurs when the device receives less than 4 answer-bytes before Window-2 time-interval elapses. After a time-out event occurs, following events occur:
  1. WD_SEQ_ERR and WD_BAD_EVENT status bits are set if Window-1 time-interval elapses before watchdog has received Answer-3, Answer-2 and Answer-1.
  2. The WD_TIMEOUT and WD_BAD_EVENT status bits are set at the end of the watchdog-sequence.
  3. The WD_FAIL_CNT[2:0] counter increments by one at the end of the watchdog-sequence.
  4. The question-counter does not change, and hence the watchdog does not generate a new question.

The status bit WD_BAD_EVENT is read-only. The watchdog clears the WD_BAD_EVENT status bit at the end of the watchdog-sequence.

The status bits WD_SEQ_ERR, WD_ANSW_EARLY, and WD_TIMEOUT are latched until the MCU writes a ‘1’ to these bits. If one or more of these status bits are set, the watchdog can still detect a good event in the next watchdog-sequence. These status bits are read-only. The watchdog clears the WD_BAD_EVENT status bit at the end of the watchdog-sequence.

Note

The WD_FIRST_OK bit is set after receiving 4 answers in the correct time frames, regardless of the correctness of the answers. In order to not clear the bit in case of incorrect answers, the following procedure is recommended:

- When WD_FIRST_OK bit is set, the MCU must read the WD_FAIL_CNT (address 0x40).
- If WD_FAIL_CNT is zero, the MCU must clear the WD_FIRST_OK bit.
- If WD_FAIL_CNT is not zero, the MCU must continue sending frames until WD_FAIL_CNT decrements before clearing WD_FIRST_OK.

Figure 8-27 shows the flow-chart of the watchdog in Q&A mode.

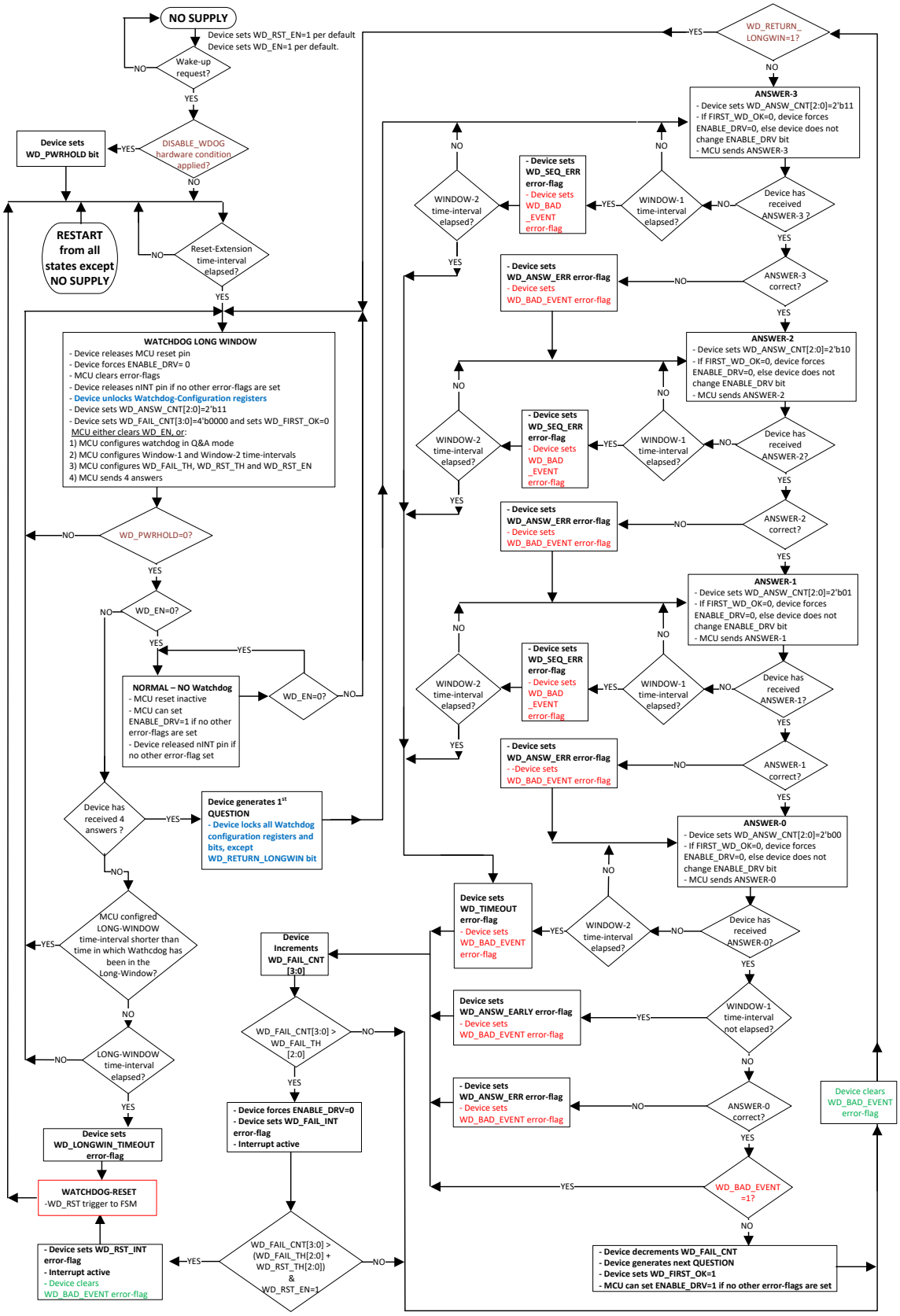

Figure 8-27. Flow Chart for WatchDog in Q&A Mode

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8.3.11.8.3.3 Watchdog Q&A Sequence Scenarios

Table 8-10. Correct and Incorrect WD Q&A Sequence Run Scenarios

NUMBER OF WD ANSWERS		ACTION	WD STATUS BITS IN WDT_STATUS REGISTER				COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2		ANSW_ERR	ANSW_EARLY	SEQ_ERR	TIME_OUT	
0 answers	0 answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	1b	No answers
0 answers	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	0b	WD_ANSW_CNT[1:0] = 3
0 answers	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	0b	WD_ANSW_CNT[1:0] = 3
0 answers	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 CORRECT ANSWER in RESPONSE WINDOW 2 (WD_ANSW_CNT[1:0] < 3)
1 CORRECT answer	1 CORRECT answer						
2 CORRECT answer	1 CORRECT answer						
0 answers	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (WD_ANSW_CNT[1:0] < 3)
1 CORRECT answer	1 INCORRECT answer						
2 CORRECT answers	1 INCORRECT answer						
0 answers	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	0b	Less than 3 CORRECT ANSWER in WIN1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (WD_ANSW_CNT[1:0] = 3)
1 CORRECT answer	3 CORRECT answers						
2 CORRECT answers	2 CORRECT answers						
0 answers	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	0b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (WD_ANSW_CNT[1:0] = 3)
1 CORRECT answer	3 INCORRECT answers						
2 CORRECT answers	2 INCORRECT answers						
0 answers	3 CORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (WD_ANSW_CNT[1:0] < 3)
1 INCORRECT answer	2 CORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	1b	
2 INCORRECT answers	1 CORRECT answer						
0 answers	3 INCORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (WD_ANSW_CNT[1:0] < 3)
1 INCORRECT answer	2 INCORRECT answer						
2 INCORRECT answer	1 INCORRECT answer						
0 answers	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	0b	1b	0b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (WD_ANSW_CNT[1:0] = 3)
1 INCORRECT answer	3 CORRECT answers		1b	0b	1b	0b	
2 INCORRECT answers	2 CORRECT answers						
0 answers	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	1b	0b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (WD_ANSW_CNT[1:0] = 3)
1 INCORRECT answer	3 INCORRECT answers						
2 INCORRECT answers	2 INCORRECT answers						

Table 8-10. Correct and Incorrect WD Q&A Sequence Run Scenarios (continued)

NUMBER OF WD ANSWERS		ACTION	WD STATUS BITS IN WDT_STATUS REGISTER				COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2		ANSW_ERR	ANSW_EARLY	SEQ_ERR	TIME_OUT	
3 CORRECT answers	0 answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD Question	0b	0b	0b	1b	Less than 4 CORRECT ANSW in RESPONSE WINDOW 1 and more than 0 ANSWER in RESPONSE WINDOW 2 (WD_ANSW_CNT[1:0] < 3)
2 CORRECT answers	0 answers		0b	0b	1b	1b	
1 CORRECT answers	0 answers						
3 CORRECT answers	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Decrement WD failure counter -New WD cycle starts with a new WD question	0b	0b	0b	0b	CORRECT SEQUENCE
3 CORRECT answers	1 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	0b	0b	WD_ANSW_CNT[1:0] = 3
3 INCORRECT answers	0 answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	0b	1b	WD_ANSW_CNT[1:0] < 3
3 INCORRECT answers	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	0b	0b	WD_ANSW_CNT[1:0] = 3
3 INCORRECT answers	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	0b	0b	0b	WD_ANSW_CNT[1:0] = 3
4 CORRECT answers	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	0b	0b	4 CORRECT or INCORRECT ANSWER in RESPONSE WINDOW 1
3 CORRECT answers + 1 INCORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	0b	0b	
2 CORRECT answers + 2 INCORRECT answers	Not applicable						
1 CORRECT answer + 3 INCORRECT answers	Not applicable						

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8.3.12 Error Signal Monitor (ESM)

The TPS6594-Q1 device has two error signal monitor (ESMs): one ESM_MCU to monitor the MCU error output signal at the nERR_MCU input pin, and one ESM_SoC to monitor the SoC error output signal at the nERR_SoC input pin.

At device start-up, the ESM_MCU and ESM_SoC can be enabled or disabled through configuration bits ESM_MCU_EN and ESM_SOC_EN. The values for these configuration bits are stored in the NVM memory of the device. To start the enabled ESM, the MCU sets the start bits ESM_MCU_START or ESM_SOC_START for the corresponding ESM through software after the system is powered up and the initial software configuration is completed. If the MCU clears a start bit, the ESM stops monitoring its input pin. The MCU can set the ENABLE_DRV bit only when the MCU has either started or disabled the ESM. When the corresponding ESM is started, the following configuration registers are write protected and can only be read:

Configuration registers write-protected by the ESM_MCU_START register bit:

- ESM_MCU_DELAY1_REG
- ESM_MCU_DELAY2_REG
- ESM_MCU_MODE_CFG
- ESM_MCU_HMAX_REG
- ESM_MCU_HMIN_REG
- ESM_MCU_LMAX_REG
- ESM_MCU_LMIN_REG

Configuration registers write-protected by the ESM_SOC_START register bit:

- ESM_SOC_DELAY1_REG
- ESM_SOC_DELAY2_REG
- ESM_SOC_MODE_CFG
- ESM_SOC_HMAX_REG
- ESM_SOC_HMIN_REG
- ESM_SOC_LMAX_REG
- ESM_SOC_LMIN_REG

The ESM uses a deglitch-filter with deglitch-time t_{degl_ESMx} to monitor its related input pin.

The MCU can configure the ESM in two different modes which are defined as follows:

Level Mode the ESM detects an ESM-error when the input pin remains low for a time equal to or longer than the deglitch-time t_{degl_ESMx}.

To select this mode for the ESM_MCU, the MCU must clear bit ESM_MCU_MODE. To select this mode for the ESM_SoC, the MCU must clear bit ESM_SOC_MODE. See Section 8.3.12.1.1 for further detail

.

PWM Mode the ESM monitors a PWM signal at its input pin. The ESM detects a bad-event when the frequency or duty cycle of the PWM input signal deviates from the expected signal. The ESM detects a good-event when the frequency and duty cycle of the PWM signal match with the expected signal for one signal period.

The ESM has an error-counter (ESM_MCU_ERR_CNT[4:0] or ESM_SOC_ERR_CNT[4:0]), which increments with +2 after each bad-event, and decrements with -1 after each good-event. The ESM detects an ESM-error when the error-counter value is more than its related threshold value.

To select this mode for the ESM_MCU, the MCU must set bit ESM_MCU_MODE. To select this mode for the ESM_SoC, the MCU must set bit ESM_SOC_MODE. See Section 8.3.12.1.2 for further details.

The MCU can configure each ESM as long as its related start bit is cleared to 0 (bit ESM_MCU_START or ESM_SOC_START). As soon as the MCU sets a start bit, the device sets a write-protection on the configuration registers of the related ESM except the related start bits ESM_MCU_START and ESM_SOC_START.

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8.3.12.1 ESM Error-Handling Procedure

Each ESM has two of its own configurable delay-timers, which are reset when the device clears the respective ESM_x_START bit. Below steps describe the procedure through which the ESM goes in case it detects an ESM-error:

1. If the respective mask bit ESM_x_PIN_MASK=0, the device sets interrupt bit ESM_MCU_PIN_INT or ESM_SOC_PIN_INT, and pulls the nINT pin low.
2. The ESM starts the delay-1 timer (configurable through related ESM_MCU_DELAY1[7:0] or ESM_SOC_DELAY1[7:0] bits).
3. If the ESM-error is no longer present and MCU has cleared the related interrupt bit ESM_MCU_PIN_INT or ESM_SOC_PIN_INT before the delay-1 timer elapses, the device releases the nINTpin, the ESM resets the delay-1 and delay-2 timers and continues to monitor its input pin.
4. If the ESM-error is still present, or if MCU has not cleared the related interrupt bit ESM_MCU_PIN_INT or ESM_SOC_PIN_INT, and the delay-1 timer elapses, then the ESM clears the ENABLE_DRV bit if bit ESM_MCU_ENDRV=1 or if bit ESM_SOC_ENDRV=1.
5. If the delay-2 timer (configurable through related ESM_MCU_DELAY2[7:0] or ESM_SOC_DELAY2[7:0] bits) is set to 0, then the ESM skips steps 6 of this list, and performs step 7.
6. If the delay-2 timer is not set to 0, then:
   a. ESM starts the delay-2 timer,
   b. If ESM_MCU_FAIL_MASK = 0, the device sets interrupt bit ESM_MCU_FAIL_INT and pulls the nINT pin low and starts the delay-2 timer.
   c. If ESM_SOC_FAIL_MASK = 0, the device sets interrupt bit ESM_SOC_FAIL_INT, pulls the nINT pin low and starts the delay-2 timer.
7. If the ESM-error is no longer present and the MCU has cleared the related interrupt bits listed below before the delay-2 timer elapses, the device releases the nINTpin, the ESM resets the delay-1 and delay-2 timers and continues to monitor its input pin:
   - ESM_MCU_PIN_INT (and ESM_MCU_FAIL_INT if set in step 6), or
   - ESM_SOC_PIN_INT (and ESM_SOC_FAIL_INT if set in step 6)
8. If the ESM-error is still present, or if MCU has not cleared the related interrupt bits ESM_MCU_PIN_INT and ESM_MCU_FAIL_INT, or ESM_SOC_PIN_INT amd ESM_SOC_FAIL_INT, and the delay-2 timer elapses, then :
   a. For ESM_MCU, the device:
      i. clears the ESM_MCU_START BIT
      ii. sets interrupt bits ESM_MCU_FAIL_INT and ESM_MCU_RST_INT, which the device handles as an ESM_MCU_RST trigger for FSM, described in Table 8-6
      iii. After this trigger handling completes, the device re-initializes the ESM_MCU
   b. For ESM_SoC, the device:
      i. clears the ESM_SOC_START bit
      ii. sets interrupt bits ESM_SOC_FAIL_INT and ESM_SOC_RST_INT, which the device handles as an ESM_SOC_RST trigger for FSM, described in Table 8-6
      iii. After this trigger handling completes, the device re-initializes the ESM_SoC

ESM_MCU_DELAY1[7:0] and ESM_SOC_DELAY1[7:0] set the delay-1 time-interval ($t_{DELAY-1}$) for the related ESM_MCU or ESM_SoC. Use Equation 10 and Equation 11 to calculate the worst-case values for the $t_{DELAY-1}$:

$$\text{Min. } t_{DELAY-1} = (\text{ESM_x_DELAY1[7:0]} \times 2.048 \text{ ms}) \times 0.95 \quad (10)$$

$$\text{Max. } t_{DELAY-1} = (\text{ESM _x_DELAY1[7:0]} \times 2.048 \text{ ms}) \times 1.05 \quad (11)$$

, in which x stands for either MCU or SoC.

ESM_MCU_DELAY2[7:0] or ESM_SOC_DELAY2[7:0] bits set the delay-2 time-interval ($t_{DELAY-2}$) for the related ESM_MCU or ESM_SoC. Use Equation 12 and Equation 13 to calculate the worst-case values for the $t_{DELAY-2}$:

$$\text{Min. } t_{DELAY-2} = (\text{ESM_x_DELAY2[7:0]} \times 2.048 \text{ ms}) \times 0.95 \quad (12)$$

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$$\text{Max. } t_{DELAY\text{-}2} = (\text{ESM_x_DELAY2[7:0]} \times 2.048 \text{ ms}) \times 1.05 \quad (13)$$

, in which x stands for either MCU or SoC.

8.3.12.1.1 Level Mode

In Level Mode, after MCU has set the start bit (bit ESM_MCU_START or bit ESM_SOC_START), the ESM monitors its nERR_MCU or nERR_SoC input pin. Each ESM detects an ESM-error when the voltage level on its input pin remains low for a time equal or longer than the deglitch-time t_{degl_ESMx}. When an ESM_x detects an ESM-error, it starts the ESM Error-Handling procedure as described in Section 8.3.12.1. Section 8.3.12.1 describes how if the voltage level on its input pin remains high for a time equal or longer than the deglitch-time t_{degl_ESMx}, before the elapse of the configured delay-1 or delay-2 time-intervals, and the MCU software clears all ESM related interrupt bits, then the ESM-error is no longer present and the ESM stops the Error-Handling Procedure. If the ESM-error persists such that the configured delay-1 and delay-2 times elapse, the ESM sends a ESM_x_RST trigger to the PFSM and the device clear the ESM_x_START bit. After the PFSM completes the handling of the ESM_x_RST trigger, the device re-initializes the ESM.

For a complete overview on how the ESM works in Level Mode, please refer to the flow-chart in Figure 8-28. In this flow-chart, the _x stands for either _MCU or _SoC. Figure 8-29, Figure 8-30, Figure 8-31, and Figure 8-32 show example wave forms for several error-cases for the ESM in Level Mode. In these examples, only the ESM_MCU is shown.

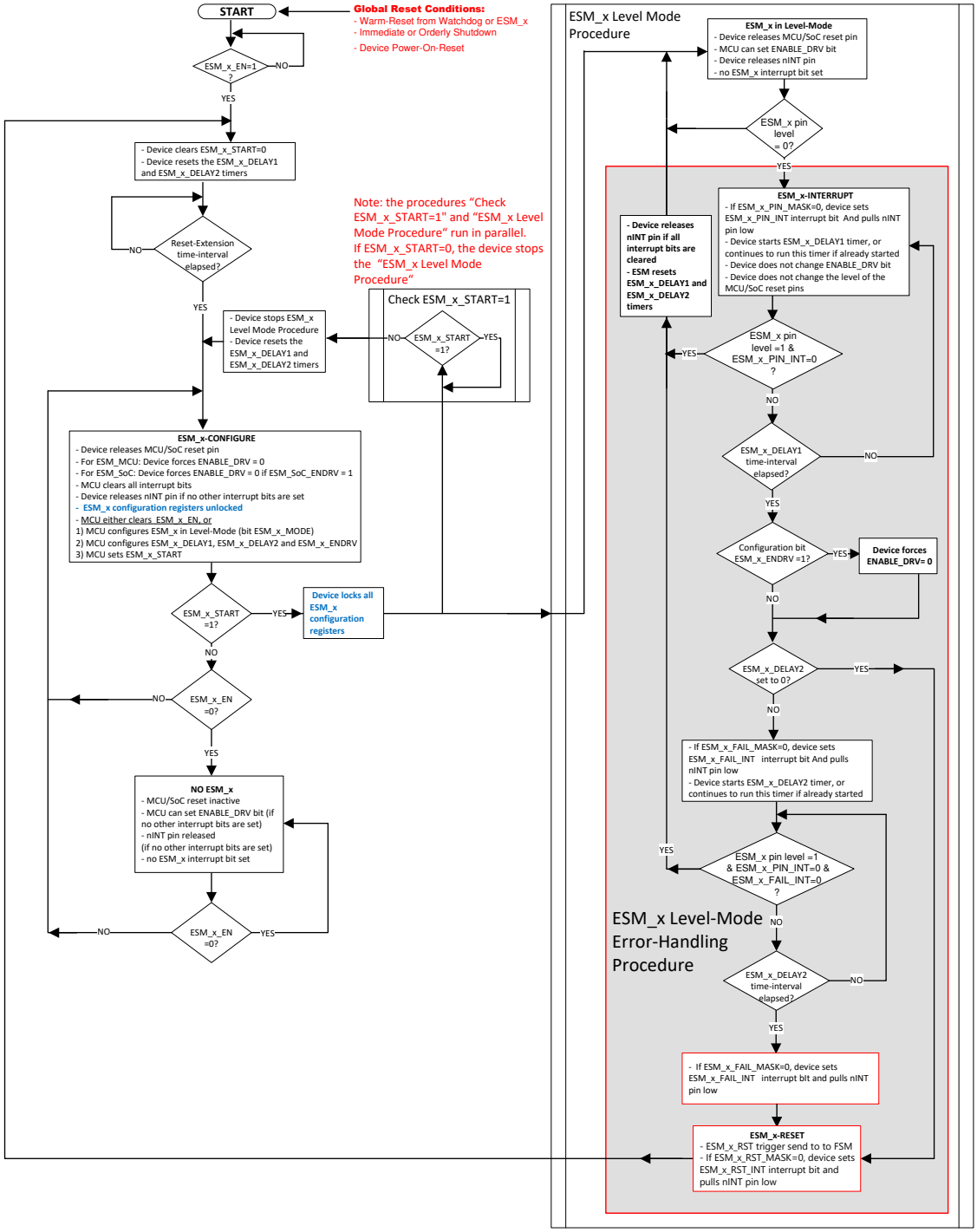

Figure 8-28. Flow Chart for Error Detection in Level Mode

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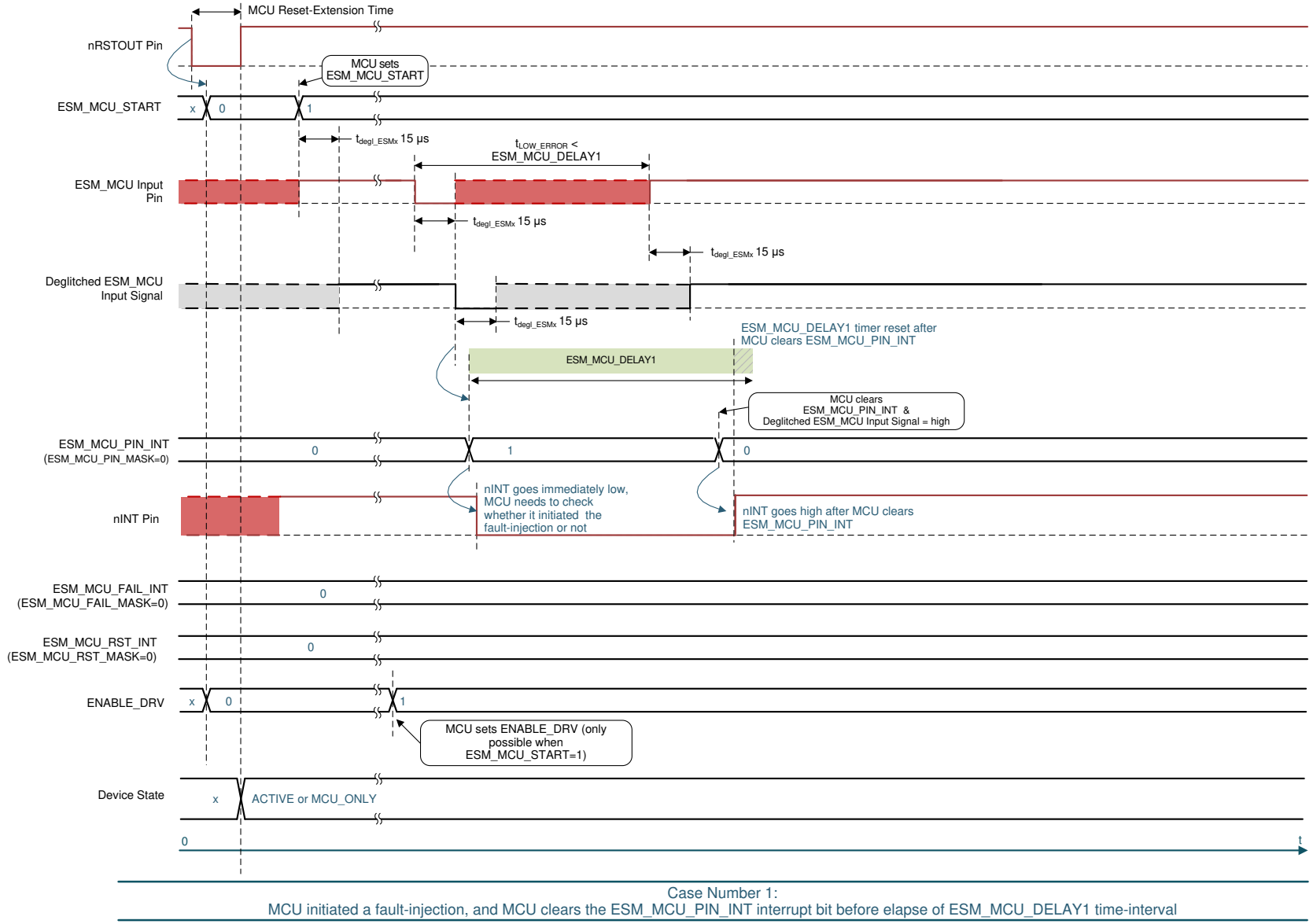
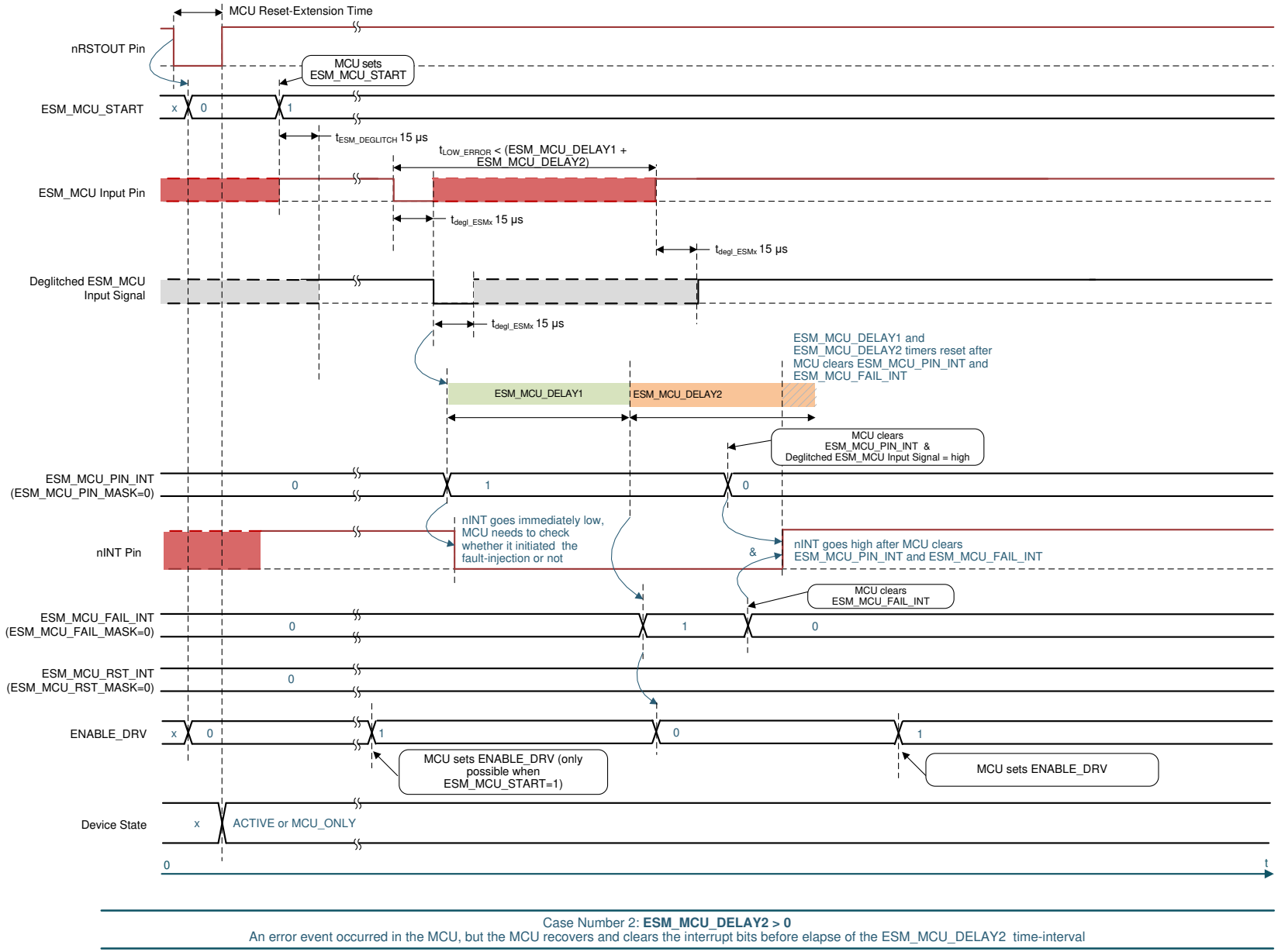


Figure 8-29. Example Waveform for ESM in Level Mode - Case Number 1: ESM_MCU Signal Recovers Before Elapse of Delay-1 time-interval



Case Number 2: **ESM_MCU_DELAY2 > 0**
An error event occurred in the MCU, but the MCU recovers and clears the interrupt bits before elapse of the ESM_MCU_DELAY2 time-interval

Figure 8-30. Example Waveform for ESM in Level Mode – Case Number 2: Delay-2 Not Set To 0 and ESM_MCU_ENDRV=1, ESM_MCU Signal Recovers Elapse of Delay-2 Time-Interval

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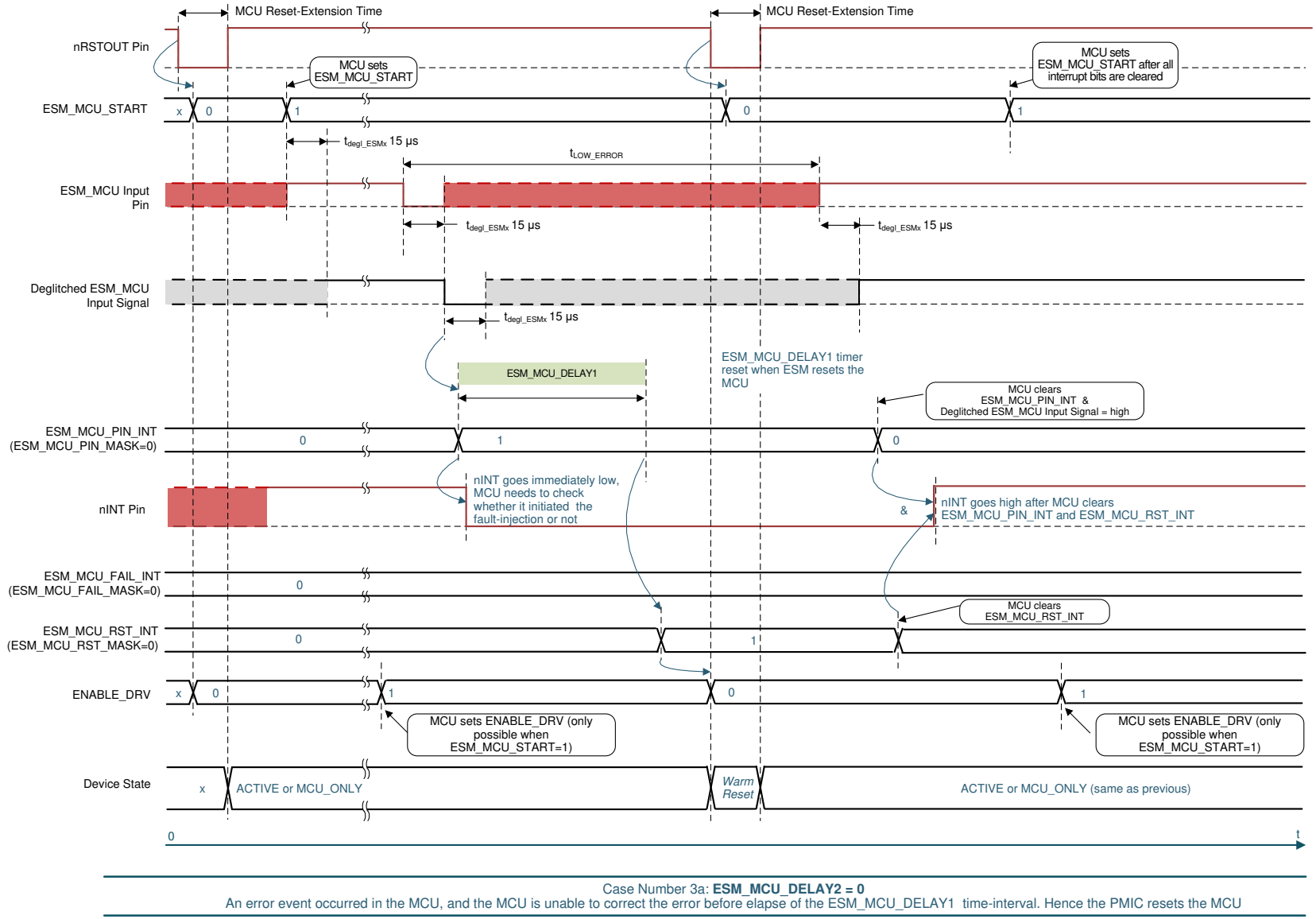

Figure 8-31. Example Waveform for ESM in Level Mode – Case Number 3a: Delay-2 Set To 0 and ESM_MCU_ENDRV=1, ESM_MCU Input Signal Recovers Too Late and MCU-Reset Occurs

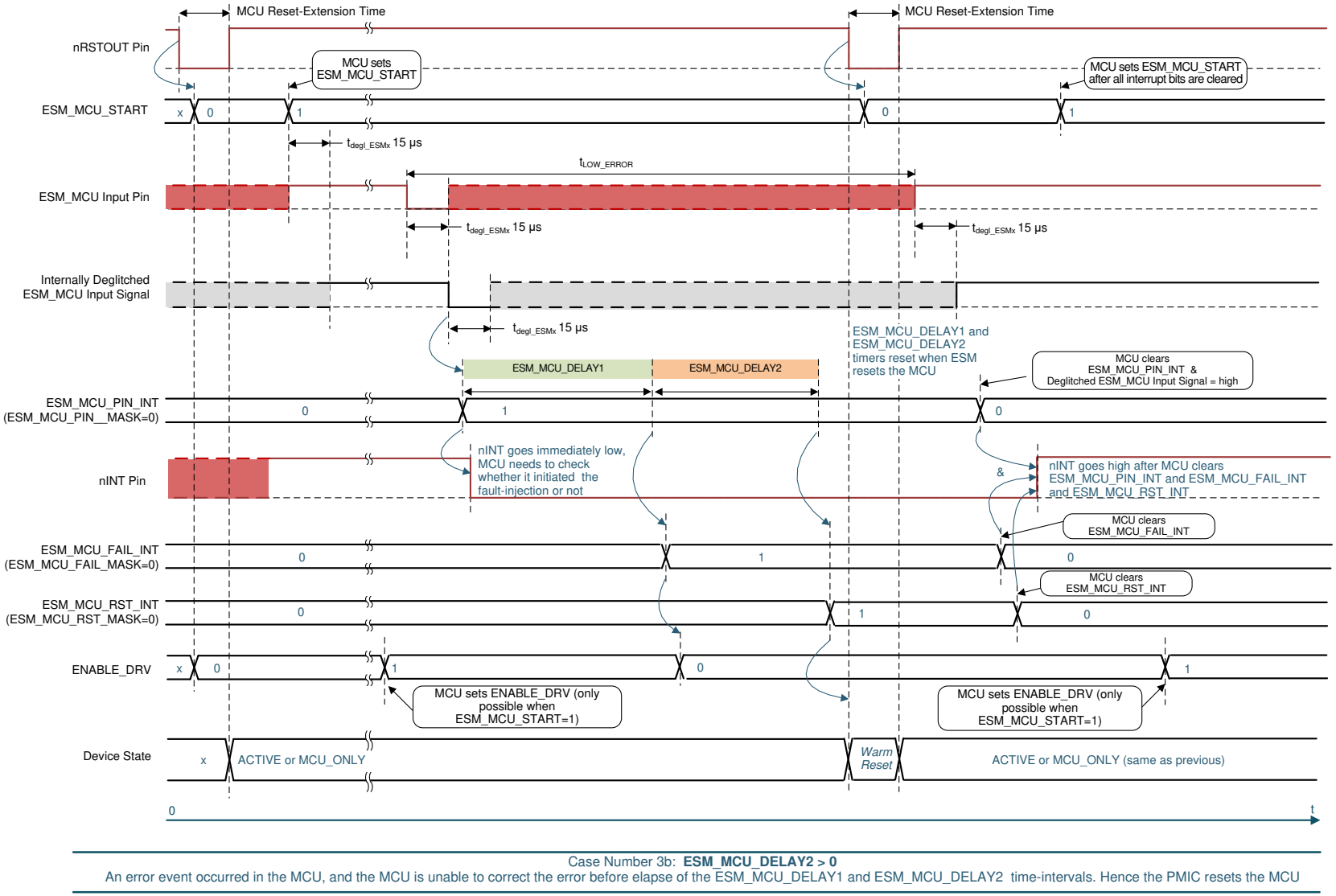

Figure 8-32. Example Waveform for ESM in Level Mode – Case Number 3b: Delay-2 Not Set to 0 and ESM_MCU_ENDRV=1, ESM_MCU Input Signal Recovers Too Late and MCU-Reset Occurs

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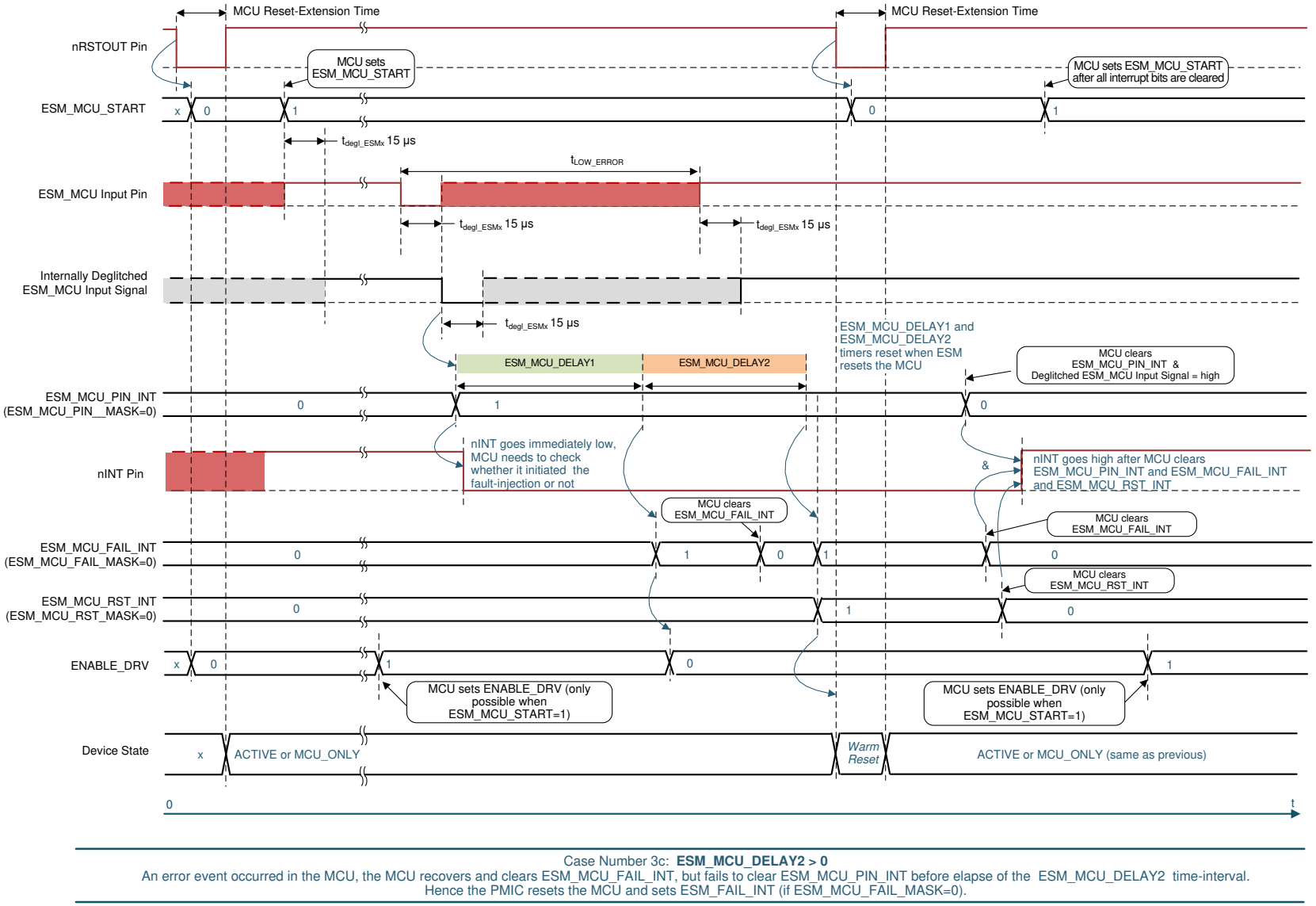

Case Number 3c: **ESM_MCU_DELAY2 > 0**
An error event occurred in the MCU, the MCU recovers and clears ESM_MCU_FAIL_INT, but fails to clear ESM_MCU_PIN_INT before elapse of the ESM_MCU_DELAY2 time-interval.
Hence the PMIC resets the MCU and sets ESM_FAIL_INT (if ESM_MCU_FAIL_MASK=0).

Figure 8-33. Example Waveform for ESM in Level Mode – Case Number 3c: Delay-2 Not Set to 0 and ESM_MCU_ENDRV=1, MCU Fails to Clear ESM_MCU_PIN_INT Before Elapse of the ESM_MCU_DELAY2

8.3.12.1.2 PWM Mode

8.3.12.1.2.1 Good-Events and Bad-Events

In PWM mode, each ESM monitors the high-pulse and low-pulse duration times its PWM inputs signal as follows:

- After a falling edge, the ESM starts monitoring the low-pulse time-duration. If the input signal remains low after exceeding the maximum low-pulse time-threshold ($t_{LOW_MAX_TH}$), the ESM detects a bad event and the low-pulse duration counter reinitializes. Each time the signal further exceeds the maximum threshold, the ESM detects a bad event. On the next rising edge on the input signal, the ESM starts the high-pulse time-duration monitoring
- After a rising edge, the ESM starts monitoring the high-pulse time-duration. If the input signal remains high after exceeding the maximum high-pulse time-threshold ($t_{HIGH_MAX_TH}$), the ESM detects a bad event and the high-pulse duration counter reinitializes. Each time the signal further exceeds the maximum threshold, the ESM detects a bad event. On the next falling edge on the input signal, the ESM starts the low-pulse time-duration monitoring.

In addition, each ESM detects a bad-event in PWM mode if one of the events that follow occurs on the deglitched signal of the related input pin nERR_MCU or nERR_SoC:

- A high-pulse time-duration which is longer than the maximum high-pulse time-threshold ($t_{HIGH_MAX_TH}$) that is configured in corresponding register bits ESM_MCU_HMAX[7:0] or ESM_SOC_HMAX[7:0].
- A high-pulse time-duration which is shorter than the minimum high-pulse time-threshold ($t_{HIGH_MIN_TH}$) that is configured in corresponding register bits ESM_MCU_HMIN[7:0] or ESM_SOC_HMIN[7:0].
- A low-pulse time-duration which is longer than the maximum low-pulse time-threshold ($t_{LOW_MAX_TH}$) that is configured in corresponding register bits ESM_MCU_LMAX[7:0] or ESM_SOC_LMAX[7:0].
- A low-pulse time-duration which is less than the minimum low-pulse time-threshold ($t_{LOW_MIN_TH}$) that is configured in register corresponding register bits ESM_MCU_LMIN[7:0] or ESM_SOC_LMIN[7:0].

Each ESM detects a good-event in PWM mode if one of the events that follow occurs on the deglitched signal of the related input pin nERR_MCU or nERR_SoC:

- A low-pulse time-duration within the minimum and maximum low-pulse time-thresholds is followed by a high-pulse time-duration within the minimum and maximum high-pulse time-thresholds, or
- A high-pulse duration within the minimum and maximum high-pulse time-thresholds is followed by a low-pulse duration within the minimum and maximum low-pulse time-thresholds

Register bits ESM_MCU_HMAX[7:0] and ESM_SOC_HMAX[7:0] set the maximum high-pulse time-threshold ($t_{HIGH_MAX_TH}$) for the related ESM. Use Equation 14 and Equation 15 to calculate the worst-case values for the $t_{HIGH_MAX_TH}$:

$$\text{Min. } t_{HIGH_MAX_TH} = (15\ \mu s + ESM_x_HMAX[7:0] \times 15\ \mu s) \times 0.95 \quad (14)$$

$$\text{Max. } t_{HIGH_MAX_TH} = (15\ \mu s + ESM_x_HMAX[7:0] \times 15\ \mu s) \times 1.05 \quad (15)$$

, in which x stands for either MCU or SoC.

ESM_MCU_HMIN[7:0] and ESM_SOC_HMIN[7:0] set the minimum high-pulse time-threshold ($t_{HIGH_MIN_TH}$) for the related ESM. Use Equation 16 and Equation 17 to calculate the worst-case values for the $t_{HIGH_MIN_TH}$:

$$\text{Min. } t_{HIGH_MIN_TH} = (15\ \mu s + ESM_x_HMIN[7:0] \times 15\ \mu s) \times 0.95 \quad (16)$$

$$\text{Max. } t_{HIGH_MIN_TH} = (15\ \mu s + ESM_x_HMIN[7:0] \times 15\ \mu s) \times 1.05 \quad (17)$$

, in which x stands for either MCU or SoC.

ESM_MCU_LMAX[7:0] and ESM_SOC_LMAX[7:0] set the maximum low-pulse time-threshold ($t_{LOW_MAX_TH}$) for the related ESM. Use Equation 18 and Equation 19 to calculate the worst-case values for the $t_{LOW_MAX_TH}$:

$$\text{Min. } t_{LOW_MAX_TH} = (15\ \mu s + ESM_x_LMAX[7:0] \times 15\ \mu s) \times 0.95 \quad (18)$$

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$$\text{Max. } t_{LOW_MAX_TH} = (15\ \mu s + ESM_x_LMAX[7:0] \times 15\ \mu s) \times 1.05 \quad (19)$$

, in which x stands for either MCUor SoC.

ESM_MCU_LMIN[7:0] and ESM_SOC_LMIN[7:0] set the minimum low-pulse time-threshold ($t_{LOW_MIN_TH}$) for the related ESM. Use Equation 20 and Equation 21 to calculate the worst-case values for the $t_{LOW_MIN_TH}$:

$$\text{Min. } t_{LOW_MIN_TH} = (15\ \mu s + ESM_x_LMIN[7:0] \times 15\ \mu s) \times 0.95 \quad (20)$$

$$\text{Max. } t_{LOW_MIN_TH} = (15\ \mu s + ESM_x_LMIN[7:0] \times 15\ \mu s) \times 1.05 \quad (21)$$

, in which x stands for either MCU or SoC.

Please note that when setting up the minimum and the maximum low/high-pulse time-thresholds need to be configured such that clock tolerances from the TPS6594-Q1 and from the processor are incorporated. Equation 22, Equation 23, Equation 24, and Equation 25 are a guideline on how to incorporate these clock-tolerances:

$$ESM_x_HMIN[7:0] < 0.5 \times (ESM_x_HMAX[7:0] + ESM_x_HMIN[7:0]) \times 0.95 \times (1 - \text{MCU/SoC clock tolerance}) \quad (22)$$

$$ESM_x_HMAX[7:0] > 0.5 \times (ESM_x_HMAX[7:0] + ESM_x_HMIN[7:0]) \times 1.05 \times (1 + \text{MCU/SoC clock tolerance}) \quad (23)$$

$$ESM_x_LMIN[7:0] < 0.5 \times (ESM_x_LMAX[7:0] + ESM_x_LMIN[7:0]) \times 0.95 \times (1 - \text{MCU/SoC clock tolerance}) \quad (24)$$

$$ESM_x_LMAX[7:0] > 0.5 \times (ESM_x_LMAX[7:0] + ESM_x_LMIN[7:0]) \times 1.05 \times (1 + \text{MCU/SoC clock tolerance}) \quad (25)$$

, in which x stands for either MCU or SoC.

8.3.12.1.2.2 ESM Error-Counter

If an ESM detects a bad-event, it increments its related error-counter (bits ESM_MCU_ERR_CNT[4:0] or bits ESM_SOC_ERR_CNT[4:0]) by 2. If an ESM detects a good-event, it decrements its related error-counter (bits ESM_MCU_ERR_CNT[4:0] or bits ESM_SOC_ERR_CNT[4:0]) by 1.

The device clears each ESM error counter when ESM_x_START=0. Furthermore, the device clears the error-counter ESM_SOC_ERR[4:0] when it resets the SoC.

Each ESM error-counter has a related threshold (bits ESM_MCU_ERR_CNT_TH[3:0] or bits ESM_SOC_ERR_CNT_TH[3:0]) which the MCU can configure if the related ESM_x_START bit is 0. If the ESM error-counter value is above its configured threshold, the related ESM has detected a so-called ESM-error and starts the Error-Handling Procedure as described in Section 8.3.12.1. If the ESM error-counter reached a value equal or less its configured threshold before the elapse of the configured delay-1 or delay-2 intervals and the MCU software clears all ESM related interrupt bits, the ESM-error is no longer present and the ESM stops the Error-Handling Procedure as described in Section 8.3.12.1. If the ESM-error persists such that the configured delay-1 and delay-2 times elapse, the ESM sends a ESM_x_RST trigger to the PFSM and the device clears the ESM_x_START bit. After the PFSM completes the handling of the ESM_x_RST trigger, the device re-initializes the related ESM.

8.3.12.1.2.3 ESM Start-Up in PWM Mode

After the MCU has set the start bit of an ESM (bit ESM_MCU_START or bit ESM_SOC_START), there are two possible scenarios:

1. The deglitched signal of the monitored input pin has a low level at the moment the MCU sets the start bit. In this scenario, the related ESM starts the following procedure:
   a. Start a timer with a time-length according the value configured in corresponding ESM_MCU_LMAX[7:0] or ESM_SOC_LMAX[7:0].
   b. Wait for a first rising edge on its deglitched input signal.
   c. If the rising edge comes before the configured time-length elapses, the ESM skips the next step and starts to monitor the high-pulse duration time. Hereafter, the ESM detects good-events or bad-events as described in Section 8.3.12.1.2.1. Figure 8-35 shows an example this scenario as Case Number 1.

   d. If the configured time-length (configured in corresponding ESM_MCU_LMAX[7:0] or ESM_SOC_LMAX[7:0]) elapses, the ESM detects a bad-event and increments the related error-counter with +2. Hereafter, the ESM detects good-events or bad-events as described in Section 8.3.12.1.2.1. Figure 8-37 shows an example this scenario as Case Number 3.
   e. If the ESM error-counter value is above its configured threshold, the related ESM has detected a so-called ESM-error and starts the Error-Handling Procedure as described in Section 8.3.12.1.2.1.
   f. During this Error-Handling Procedure, the ESM continues to monitor its related input pin, and updates the error-counter accordingly when it detects good-events or bad-events, until the Error-Handling Procedure reaches the step in which the ESM sends an ESM_x_RST trigger to the PFSM, which, depending on the PFSM configuration, resets the MCU or SoC. Figure 8-38 shows a scenario in which the device resets the MCU or SoC as Case Number 4.
   g. If the ESM error-counter reaches a value equal or less its configured threshold before the elapse of the configured delay-1 or delay-2 time-intervals and the MCU software clears all ESM related interrupt bits, the ESM-error is no longer present and the ESM stops the Error-Handling Procedure as described in Section 8.3.12.1.2.1.
2. The deglitched signal monitored input pin has a high level at the moment the MCU sets the start bit. In this scenario, the related ESM starts the following procedure:
   a. Start a timer with a time-length according the value configured in corresponding ESM_MCU_HMAX[7:0] or ESM_SOC_HMAX[7:0].
   b. Wait for a first falling edge on its deglitched input signal.
   c. If the falling edge comes before the configured time-length elapses, the ESM skips the next step and starts to monitor the low-pulse duration time. Hereafter, the ESM detects good-events or bad-events as described in Section 8.3.12.1.2.1. Figure 8-36 shows an example this scenario as Case Number 2.
   d. If the configured time-length (configured in corresponding ESM_MCU_HMAX[7:0] or ESM_SOC_HMAX[7:0]) elapses, the ESM detects a bad-event and increments the related error-counter with +2. Hereafter, the ESM detects good-events or bad-events as described in Section 8.3.12.1.2.1.
   e. If the ESM error-counter value is above its configured threshold, the related ESM has detected a so-called ESM-error and starts the Error-Handling Procedure as described in Section 8.3.12.1.2.1.
   f. During this Error-Handling Procedure, the ESM continues to monitor its related input pin, and updates the error-counter accordingly when it detects good-events or bad-events, until the Error-Handling Procedure reaches the step in which the ESM sends an ESM_x_RST trigger to the PFSM, which, depending on the PFSM configuration, resets the MCU or SoC, as Case Number 4.
   g. If the ESM error-counter reaches a value equal or less its configured threshold before the elapse of the configured delay-1 or delay-2 time-intervals and the MCU software clears all ESM related interrupt bits, the ESM-error is no longer present and the ESM stops the Error-Handling Procedure as described in Section 8.3.12.1.2.1.

8.3.12.1.2.4 ESM Flow Chart and Timing Diagrams in PWM Mode

For a complete overview on how the ESM works in PWM Mode, please refer to the flow-chart in Figure 8-34. In this flow-chart, the _x stands for either _MCU or _SoC Figure 8-35, Figure 8-36, Figure 8-37, and Figure 8-38 show example waveforms for several error-cases for the ESM in PWM Mode. In this flow-chart, the _x stands for either _MCU or _SoC

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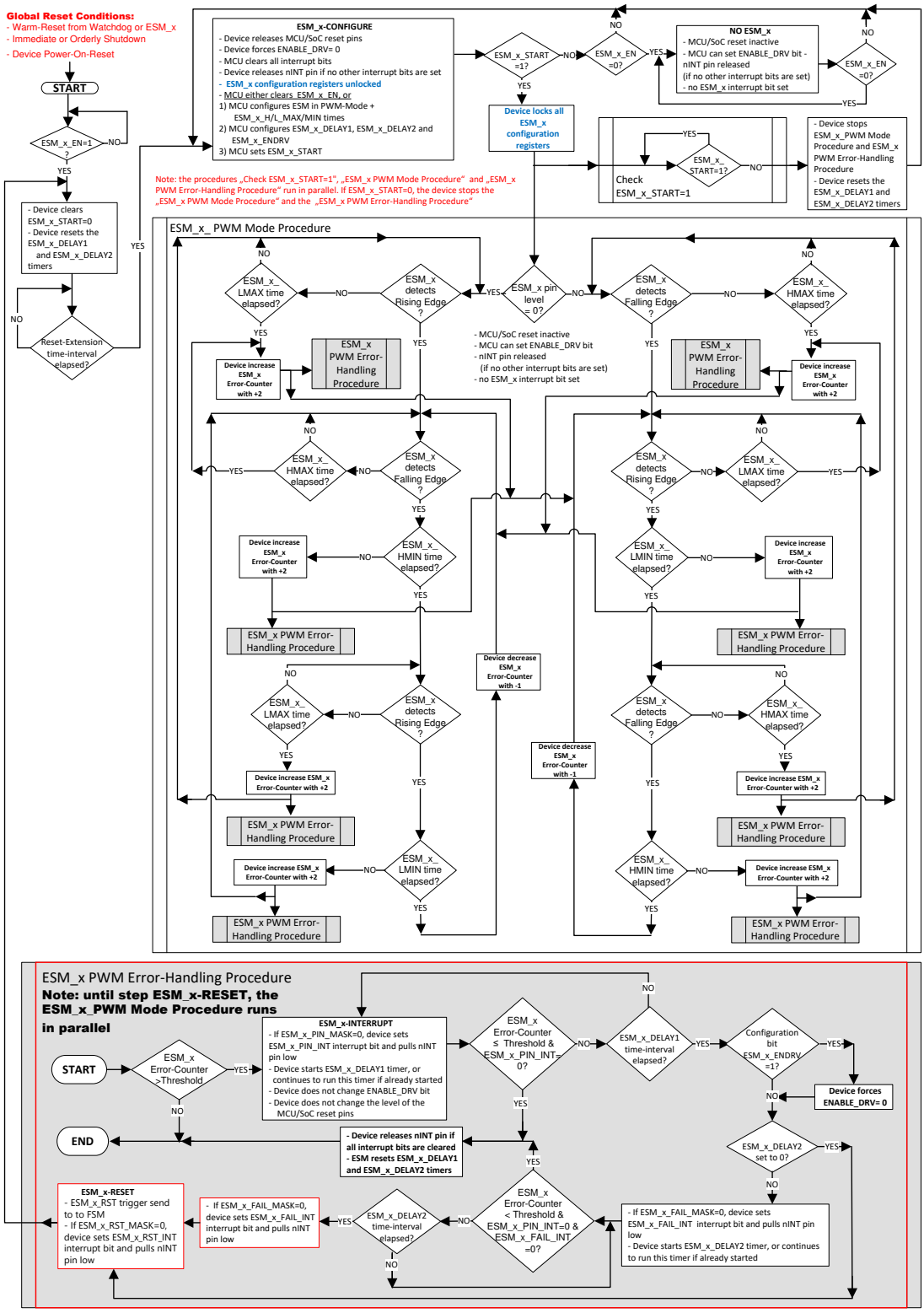

Figure 8-34. Flow-Chart for ESM_MCU and ESM_SoC in PWM Mode

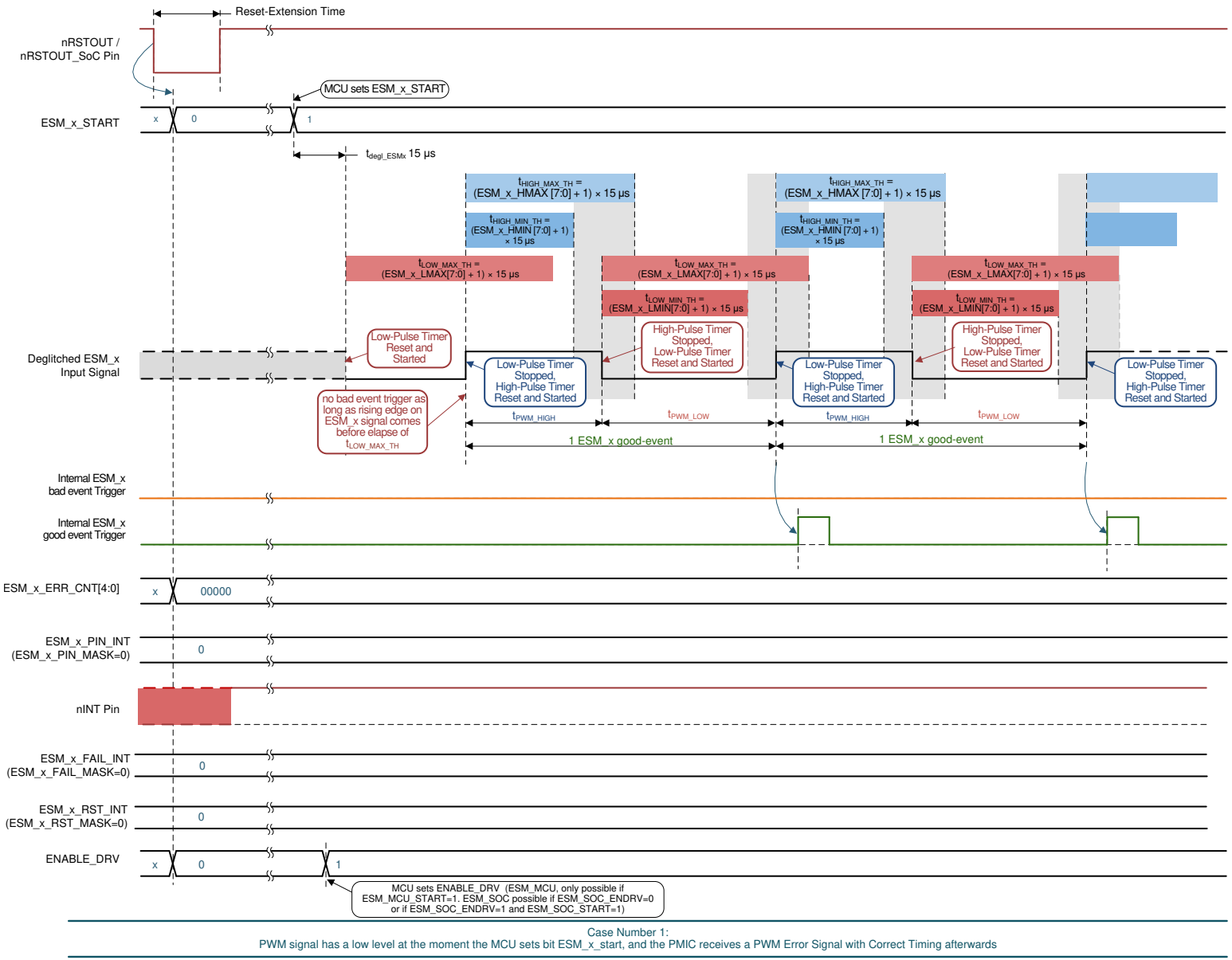

Figure 8-35. Example Waveform for ESM in PWM Mode – Case Number 1: ESM Starts with Low-Level at Deglitched Input signal, and Receives Correct PWM Signal Afterwards. (The _x stand for _MCU or _SoC)

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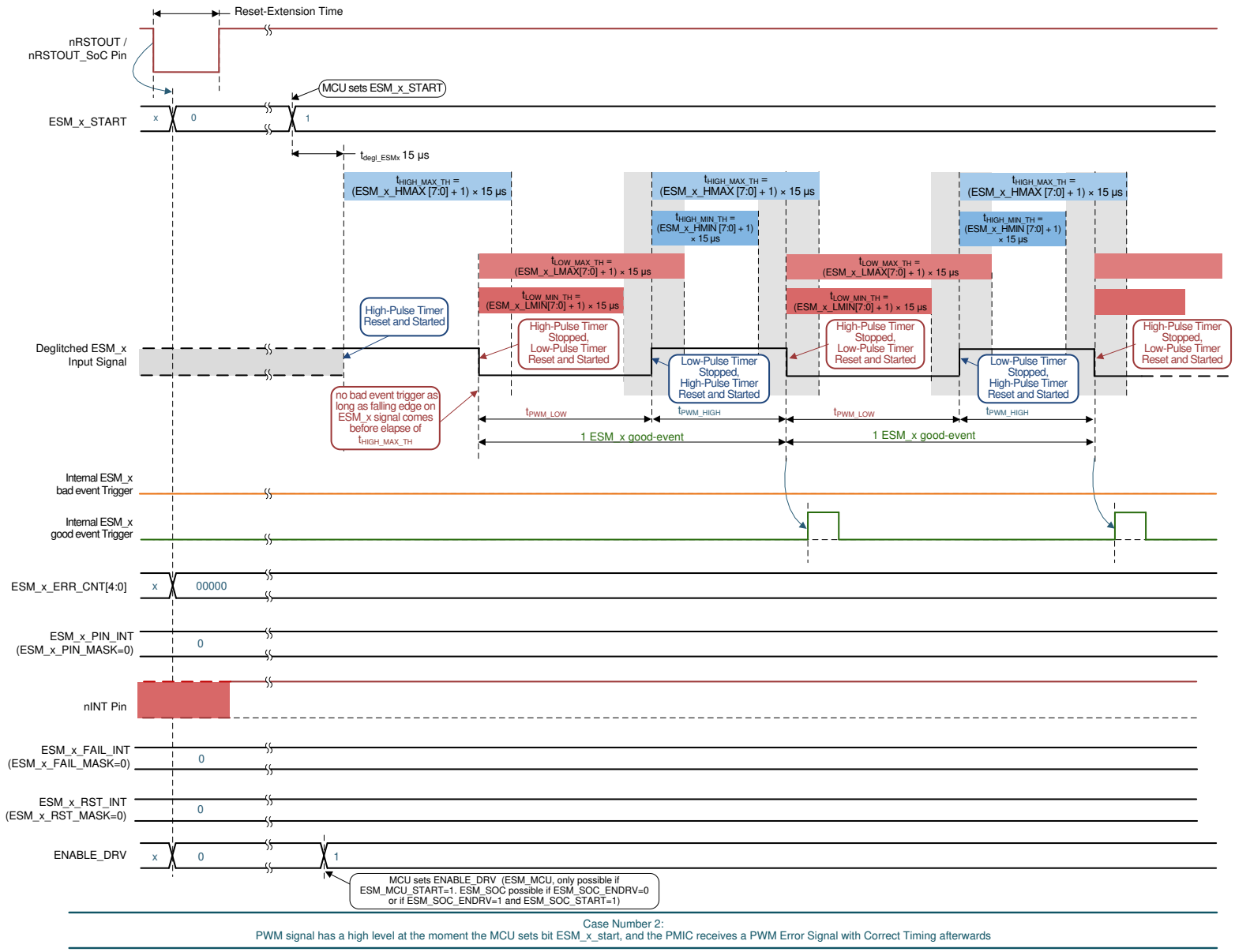

Figure 8-36. Example Waveform for ESM in PWM Mode – Case Number 2: ESM Starts with High-Level at Deglitched Input Signal, and Receives Correct PWM Signal Afterwards (The _x stand for _MCU or _SoC)

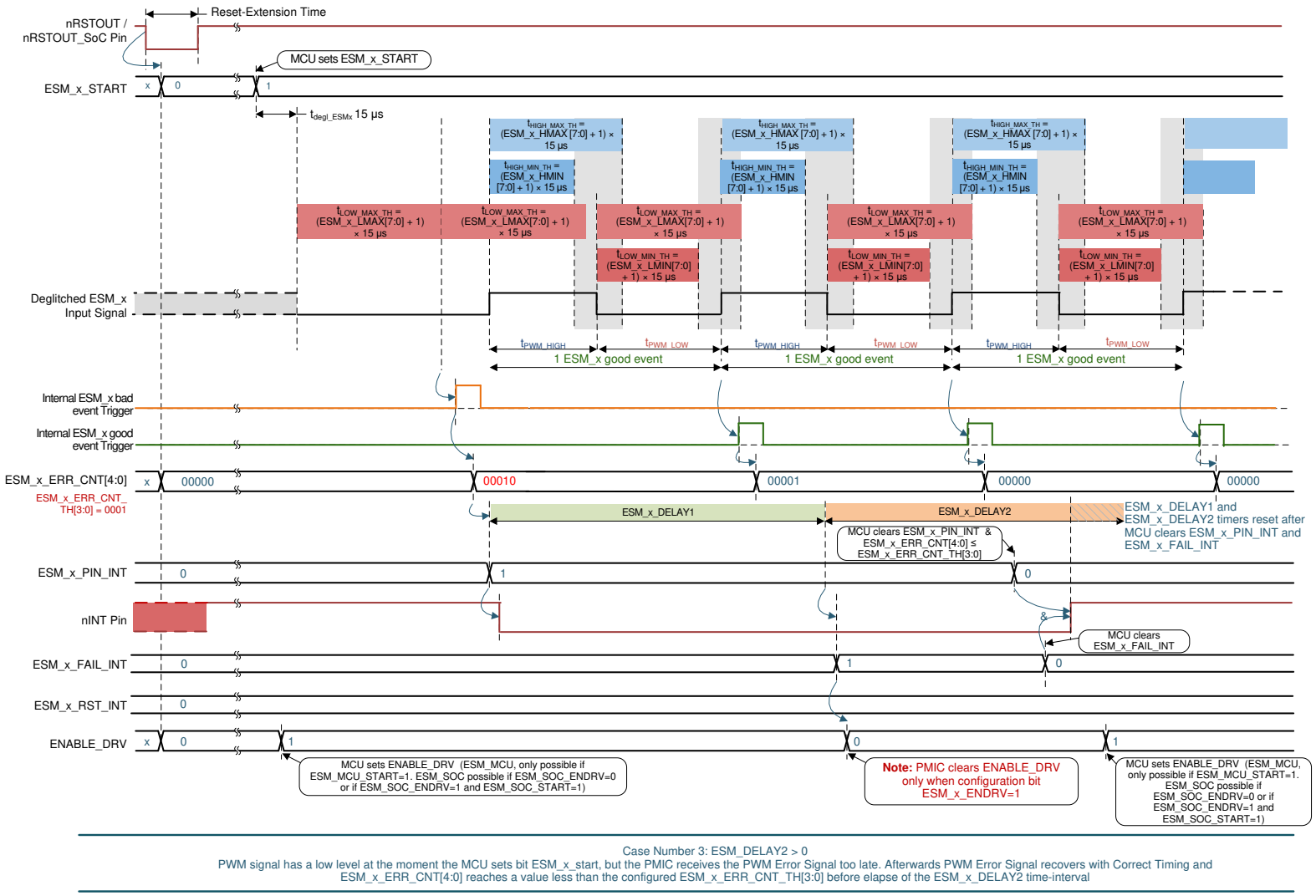

Figure 8-37. Example Waveform for ESM in PWM Mode – Case Number 3: ESM Starts with Low-Level at Deglitched Input Signal, but Receives Too Late a Correct PWM Signal Afterwards (The _x stand for _MCU or _SoC)

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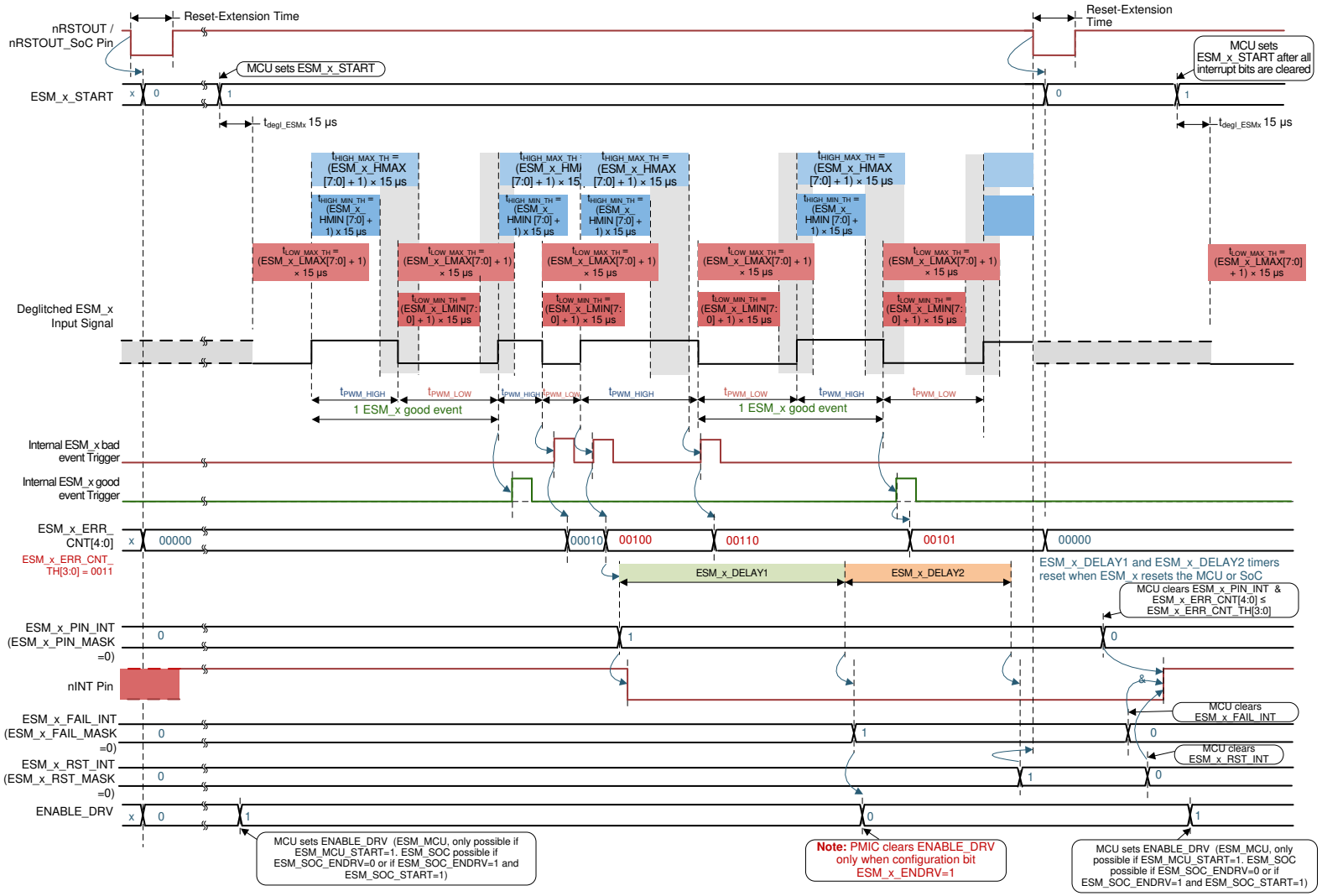

Case Number 4: _DELAY2 > 0
PWM signal has an error after start-up, and the ESM_x_ERR_CNT[4:0] > ESM_x_ERR_CNT_TH[3:0] during the elapse of ESM_x_DELAY1 and ESM_x_DELAY2. Hence the PMIC pulls the nRSTOUT / nRSOUT_SoC pin low, and releases this pin after the reset-extension time. After this, MCU clears all errors and restarts the ESM_x

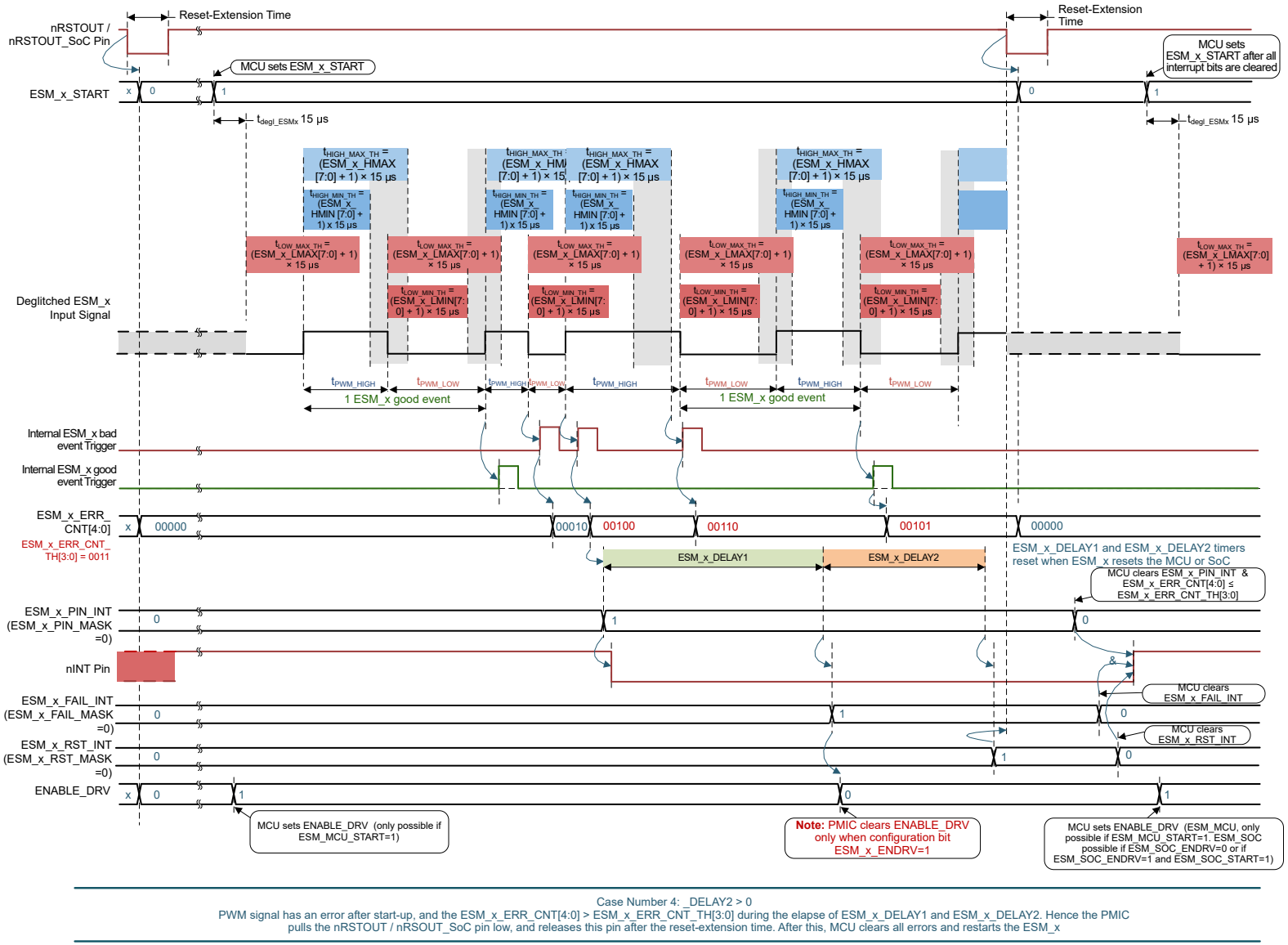

Figure 8-38. Example Waveform for ESM in PWM Mode – Case Number 4: ESM Starts with Low-Level at Deglitched Input Signal and Receives a Correct PWM Signal. Afterwards the ESM Detects Bad Events, and the PWM Signal Recovers Too Late which Leads to an ESM_x Reset Trigger to the PFSM (The _x stand for _MCU or _SoC)

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8.4 Device Functional Modes

8.4.1 Device State Machine

The TPS6594-Q1 device integrates a finite state machine (FSM) engine, which manages the state of the device during operating state transitions. It supports NVM-configurable mission states with configurable input triggers for transitions between states. Any resources, including the 5 BUCK regulators, 4 LDO regulators, and all of the digital IO pins including the 11 GPIO pins on the device can be controlled during power sequencing. When a resource is not controlled or configured through a power sequence, the resource is left in the default state as pre-configured by the NVM.

Each resource can be pre-configured through the NVM configuration, or re-configured through register bits. Therefore, the user can statically control the resource through the control interfaces (I^2C or SPI), or the FSM can automatically control the resource during state sequences.

The FSM is powered by an internal LDO which is automatically enabled when VCCA supply is available to the device. Ensuring that the VCCA supply is the first supply available to the device is important to ensure proper operation of all the power resources as well as the control interface and device IOs.

There are 3 parts of the FSM which control the operational modes of the TPS6594-Q1 device:

- Fixed Device Power Finite State Machine (FFSM)
- Pre-configurable Finite State Machine (PFSM) for Mission States (ACTIVE, MCU_ONLY, S2R, DEEP_SLEEP)
- Error Handling Operations

The PFSM provides configurable rail and voltage monitoring sequencing utilizing instructions in configuration memory. This flexibility enables customers to alter power-up sequences on a platform basis. The FFSM handles the majority of fixed functionality that is internally mandated and common to all platforms.

8.4.1.1 Fixed Device Power FSM

The Fixed Device Power portion of the FSM engine manages the power up of the device before the power rails are fully enabled and ready to power external loadings, and the power down of the device when in the event of insufficient power supply or device or system error conditions. While the device is in one of the Hardware Device Powers states, the ENABLE_DRV bit remains low.

The definitions and transition triggers of the Device Power States are fixed and cannot be reconfigured.

Following are the definitions of the Device Power states:

NO SUPPLY The device is not powered by a valid energy source on the system power rail. The device is completely powered off.

BACKUP (RTC backup battery) The device is not powered by a valid supply on the system power rail (VCCA < VCCA_UVLO); a backup power source, however, is present and is within the operating range of the LDOVRTC. The RTC clock counter remains active in this state if it has been previously activated by appropriate register enable bit. The calendar function of the RTC block is activated, but not accessible in this state. Customer has the option to enable the *shelf mode* by disconnecting the VCCA supply completely, even while the backup battery is connected to the VBACKUP pin. The *shelf mode* forces the device to skip the BACKUP state and enters the NO SUPPLY state under VCCA_UVLO condition to reduce current draining from the backup battery.

LP_STANDBY The device can enter this state from a mission state after receiving a valid OFF request or an I2C trigger, and the LP_STANDBY_SEL= 1. When the device is in this state, the RTC clock counter and the RTC Alarm or Timer Wake-up functions are active if they have been previously activated by appropriate register enable bit. Low Power Wake-up input monitor in the LDOVRTC domain (LP_WKUP secondary function through GPIO3 or GPIO4) and the on request monitors are also enabled in this state. When a logic level transition from high-to-low or low-to-high with a minimum pulse length of t_{LP_WKUP} is detected on the assigned LP_WKUP pin, or if the device detects a valid on-request or a wake-up signal from the RTC block, the

device proceeds to power up the device and reach the default mission state. More details regarding the LP_WAKE function can be found in Section 8.4.1.2.4.5.

INIT The device is powered by a valid supply on the system power rail (VCCA ≥ VCCA_UV). If the device was previously in LP_STANDBY state, it has received an external wake-up signal at the LP_WKUP1/2 pins, the RTC alarm or timer wake-up signal, or an On Request from the nPWRON/ENABLE pin. Device digital and monitor circuits are powered up. The PMIC reads its internal NVM memory in this state and configures default values to registers, IO configuration and FSM accordingly.

BOOT BIST The device is running the built-in self-test routine which includes both the LBIST and the ABIST/CRC. An option is available to shorten the device power up time from the NO_SUPPLY state by setting the NVM bit FAST_BOOT_BIST = '1' to skip the LBIST. Software can also set the FAST_BIST = '1' to skip LBIST after the device wakes up from the LP STANDBY state. When the device arrives at this state from the SAFE_RECOVERY state, LBIST is automatically skipped if it has not previously failed. If LBIST failed, but passed after multiple re-tries before exceeding the recovery counter limit, the device powers up normally. The following NVM bits are additional options which can be set to disable parts of the ABIST/CRC tests if further sequence time reduction is required:

- REG_CRC_EN = '0': disables the register map and SRAM CRC check
- VMON_ABIST_EN = '0': disables the ABIST for the VMON OV/UV function

Note

Note: the BIST tests are executed as parallel processes, and the longest process determines the total BIST duration

RUNTIME BIST A request was received from the MCU to exercise a run-time built-in self-test (RUNTIME_BIST) on the device. No rails are modified and all external signals, including all I^2C or SPI interface communications, are ignored during BIST. If the device passed BIST, it resumes the previous operation. If the device failed BIST, it shuts down all of the regulator outputs and proceed to the SAFE RECOVERY state. In order to avoid a register CRC error, all register writes must be avoided after the request for the BIST operation until the device pulls the nINT pin low to indicate the completion of BIST. The results of the BIST are indicated by the BIST_PASS_INT or the BIST_FAIL_INT bits.

Note

For executing the RUNTIME_BIST, the system software must perform following steps:

Before RUNTIME_BIST request:

1) clear all LDOx_VMON_EN bits to 0

2) Set VCCA_UV_MASK, VCCA_OV_MASK, all BUCKx_UV_MASK, all BUCKx_OV_MASK, all LDOx_UV_MASK and all LDOx_OV_MASK bits to 1

After completion of RUNTIME_BIST:

1) Clear VCCA_UV_MASK, VCCA_OV_MASK, all BUCKx_UV_MASK and all BUCKx_OV_MASK bits to 0

2) Set all LDOx_VMON_EN bits to 1

3) After 1 millisecond (if LDOx_SLOW_RAMP=0) respectively 3.5 milliseconds (if LDOx_SLOW_RAMP=1), clear all LDOx_UV_MASK and LDOx_OV_MASK bits to 0

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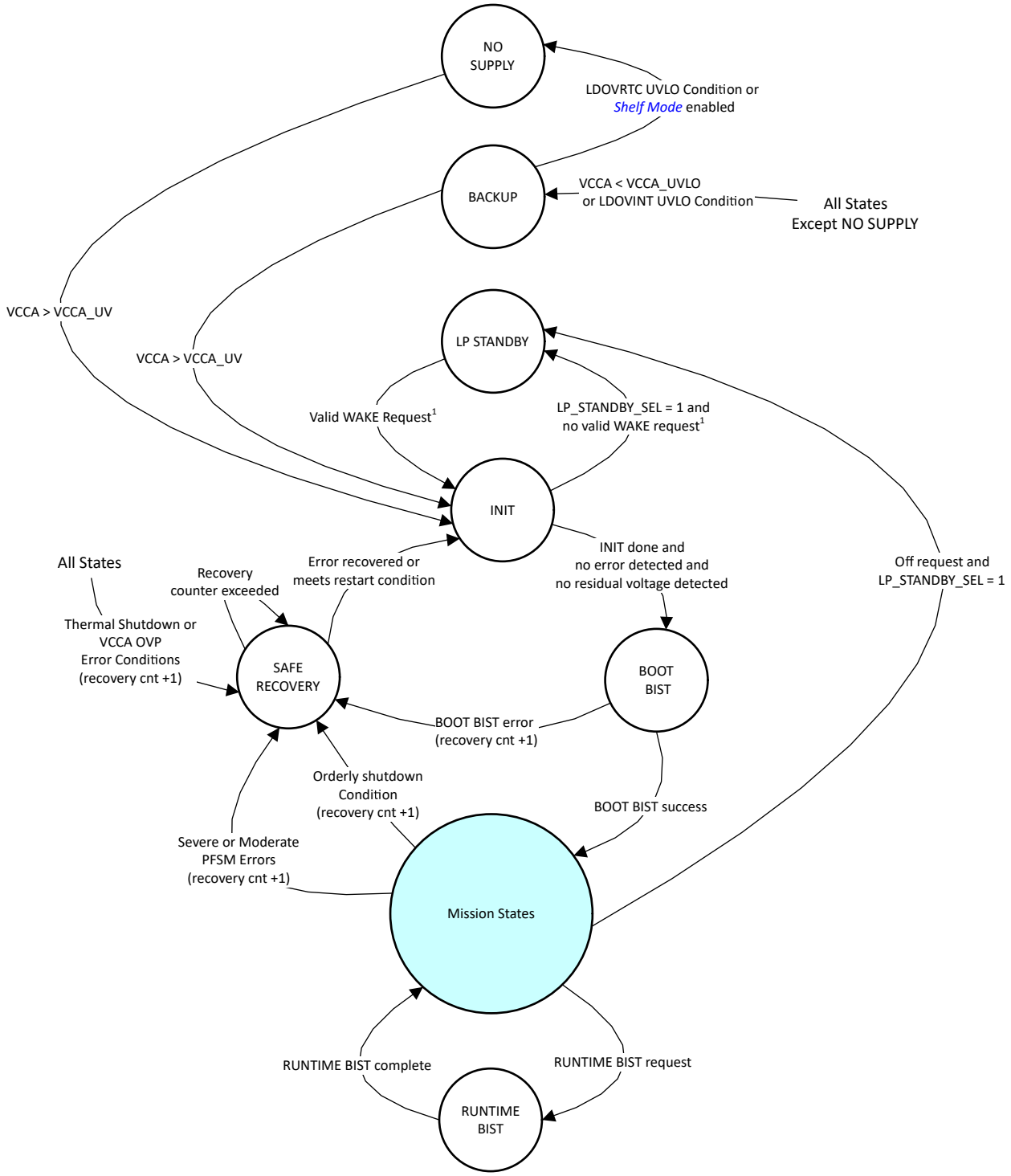
SAFE RECOVERY The device meets the qualified error condition for immediate or ordered shutdown request. If the error is recovered within the recovery time interval or meets the restart condition, the device increments the recovery counter, and returns to INIT state if the recovery counter value does not exceed the threshold value. If the recovery counter exceeds the threshold value or if the error cannot be recovered, such as the die temperature cannot be reduced to < T_{WARN}, or if VCCA stays above OVP threshold, the device stays in SAFE RECOVERY state until a supply power cycle occurs.

When multiple system conditions occur simultaneously which demands power state arbitration, the device goes to the higher priority state according to the following priority order:

1. NO SUPPLY
2. BACKUP
3. SAFE_RECOVERY
4. LP_STANDBY
5. MISSION STATES

Figure 8-39 shows the power transition states of the FSM engine.



[1] A valid WAKE request consist of:

- nPWRON/ENABLE on request detection if the device arrived the LP_STANDBY state through the long key-press of the nPWRON pin or by disabling the ENABLE pin, or
- RTC Alarm, RTC Timer, LP_WKUP1 or LP_WKUP2 detection if the device arrived the LP_STANDBY state through writing to a TRIGGER_I2C_0 bit.

Figure 8-39. State Diagram for Device Power States

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8.4.1.1.1 Register Resets and NVM Read at INIT State

Several registers inside the TPS6594-Q1 have pre-configured default values that are stored in the NVM of the TPS6594-Q1. These registers are referred to as NVM pre-configured registers.

When the device transitions from the LP_STANDBY or the SAFE_RECOVERY to the INIT state, based on FIRST_STARTUP_DONE bit, the registers are reset and the NVM is read. When the FIRST_STARTUP_DONE is '0', registers which are not in the RTC domain are reset, and all of the NVM pre-configured registers including the ones in the RTC domain, are loaded from the NVM. When the FIRST_STARTUP_DONE bit is set to '1', typically after the initial power up from a supply power cycle, the registers in the RTC domain are not reset, and the NVM pre-configured registers in the RTC domain are not re-loaded from the NVM. This prevents the control and status bits stored in the RTC domain registers from being over written.

Table 8-11. Register resets and NVM read at INIT state

FIRST _STARTUP_DONE	NVM pre-configured registers in RTC Domain	Registers without NVM pre-configuration in RTC Domain	Other NVM pre-configured registers	Registers without NVM pre-configuration
0	Defaults read from NVM	No changes	Reset and defaults read from NVM	Reset
1	No changes	No changes	Reset and defaults read from NVM	Reset

Below are the NVM pre-configured register bits in the RTC domain:

- GPIO3_CONF and GPIO4_CONF registers, except the GPIOn_DEGLITCH_EN bits
- GPIO3_RISE_MASK, GPIO3_FALL_MASK, GPIO4_RISE_MASK, and GPIO4_FALL_MASK bits
- NPWRON_CONF register except ENALBE_DEGLITCH_EN and NRSTOUT_OD bits
- FSD_MASK, ENABLE_MASK, NPWRON, START_MASK, and NPWRON_LONG_MASK bits
- STARTUP_DEST, FAST_BIST, LP_STANDBY_SEL, XTAL_SEL, and XTAL_EN bits
- PFSM_DELAYn, and RTC_SPARE_n bits

Below are the register bits without NVM pre-configuration in the RTC domain:

- FIRST_STARTUP_DONE bit
- SCRATCH_PAD_n bits
- All of RTC control and configuration registers

8.4.1.2 Pre-Configurable Mission States

When the device arrives at a mission state, all rail sequencing is controlled by the pre-configurable FSM engine (PFSM) through the configuration memory. The configuration memory allows configurations of the triggers and the operation states which together form the configurable sub state machine within the scope of mission states. This sub state machine can be used to control and sequence the different voltage outputs as well as any GPIO outputs that can be used as enable for external rails. When the device is in a mission state, it has the capacity to supply the processor and other platform modules depending on the power rail configuration. The definitions and transition triggers of the mission states are configurable through the NVM configuration. Unlike the user registers, the PFSM definition stored in the NVM cannot be modified during normal operation. When the PMIC determines that a transition to another operation state is necessary, it reads the configuration memory to determine what sequencing is needed for the state transition.

Table 8-15 shows how the trigger signals for each state transition can come from a variety of interface or GPIO inputs, or potential error sources. Figure 8-40 shows how the device processes all of the possible error sources inside the PFSM engine, a hierarchical mask system is applied to filter out the common errors which can be handled by interrupt only, and categorize the other error sources as Severe Global Error, Moderate Global Error, and so forth. The filtered and categorized triggers are sent into the PFSM engine, which then determines the entry and exit condition for each configured mission state.

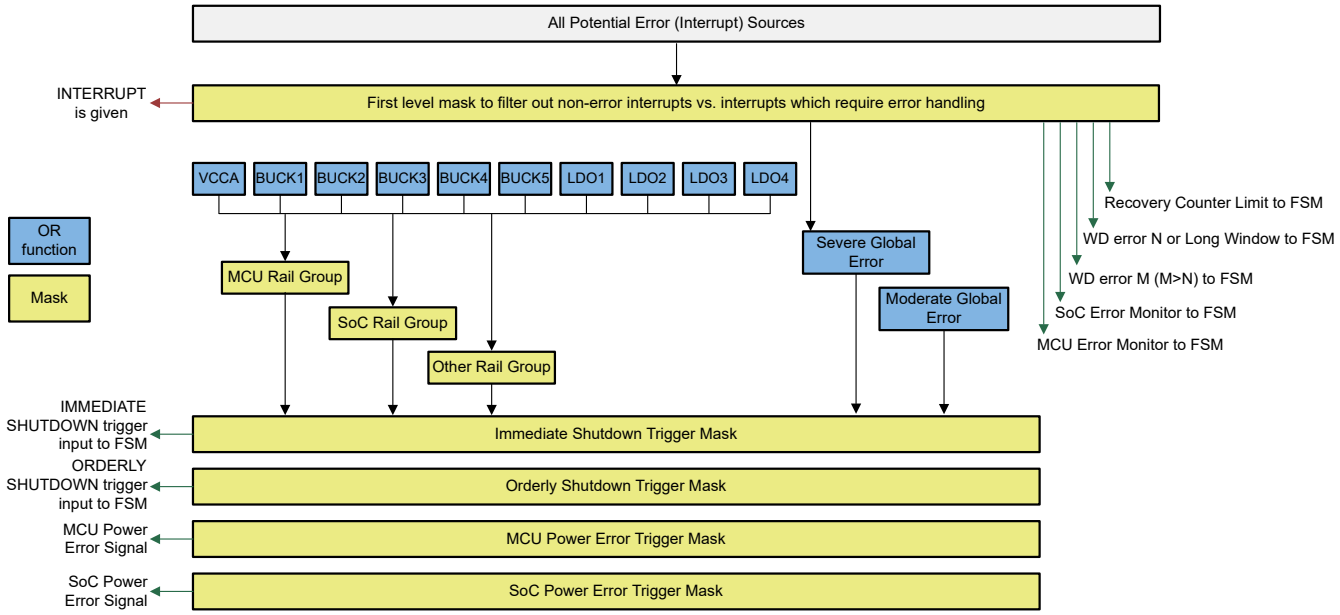

Figure 8-40. Error Source Hierarchical Mask System

Figure 8-42 shows an example of how the PFSM engine utilizes instructions to execute the configured device state and sequence transitions of the mission state-machine. Table 8-12 provides the instruction set and usage description of each instruction in the following sections. Section 8.4.1.2.2 describes how the instructions are stored in the NVM memory.

Table 8-12. Configurable FSM Instruction set

Command Opcode	Command	Command Description
"0000"	REG_WRITE_MASK_PAGE0_IMM	Write the specified data, except the masked bits, to the specified page 0 register address.
"0001"	REG_WRITE_IMM	Write the specified data to the specified register address.
"0010"	REG_WRITE_MASK_IMM	Write the specified data, except the masked bits, to the specified register address.
"0011"	REG_WRITE_VOUT_IMM	Write the target voltage of a specified regulator after a specified delay.
"0100"	REG_WRITE_VCTRL_IMM	Write the operation mode of a specified regulator after a specified delay.
"0101"	REG_WRITE_MASK_SREG	Write the data from a scratch register, except the masked bits, to the specified register address.
"0110"	SREG_READ_REG	Write scratch register (REG0-3) with data from a specified address.
"0111"	WAIT	Execution is paused until the specified type of the condition is met or timed out.
"1000"	DELAY_IMM	Delay the execution by a specified time.
"1001"	DELAY_SREG	Delay the execution by a time value stored in the specified scratch register.
"1010"	TRIG_SET	Set a trigger destination address for a given input signal or condition.
"1011"	TRIG_MASK	Sets a trigger mask that determines which triggers are active.
"1100"	END	Mark the final instruction in a sequential task.
"1101"	REG_WRITE_BIT_PAGE0_IMM	Write the specified data to the BIT_SEL location of the specified page 0 register address.
"1110"	REG_WRITE_WIN_PAGE0_IMM	Write the specified data to the SHIFT location of the specified page 0 register address.

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Table 8-12. Configurable FSM Instruction set (continued)

Command Opcode	Command	Command Description
"1111"	SREG_WRITE_IMM	Write the specified data to the scratch register (REG0-3).

8.4.1.2.1 PFSM Commands

Following section describes each PFSM command in detail and provides example usage codes. More information on example NVM configuration, available device options and documentations can be found at Fully Customizable Integrated Power.

8.4.1.2.1.1 REG_WRITE_IMM Command

Description: Write the specified data to the specified register address

Assembly command: **REG_WRITE_IMM [ADDR=]<Address> [DATA=]<Data>**

Address and Data can be in any literal integer format (decimal, hex, and so forth).

'ADDR=' and 'DATA=' are optional. When included, the parameters can be in any order.

Examples:
- **REG_WRITE_IMM 0x1D 0x55** — Write value 0x55 to address 0x1D
- **REG_WRITE_IMM ADDR=0x10 DATA=0xFF** — Write value 0xFF to address 0x10
- **REG_WRITE_IMM DATA=0xFF ADDR=0x10** — Write value 0xFF to address 0x10

8.4.1.2.1.2 REG_WRITE_MASK_IMM Command

Description: Write the specified data, except the masked bits, to the specified register address

Assembly command: **REG_WRITE_MASK_IMM [ADDR=]<Address> [DATA=]<Data> [MASK=]<Mask>**

Address, Data, and Mask can be in any literal integer format (decimal, hex, and so forth).

'ADDR=', 'DATA=', and 'MASK=' are optional. When included, the parameters can be in any order.

Examples:
- **REG_WRITE_MASK_IMM 0x1D 0x80 0xF0** — Write 0b1000 to the upper 4 bits of the register at address 0x1D
- **REG_WRITE_MASK_IMM ADDR=0x10 DATA=0x0F MASK=0xF0** — Write 0b1111 to the lower 4 bits of the register at address 0x10
- **REG_WRITE_MASK_IMM DATA=0x0F MASK=0xF0 ADDR=0x10** — Write 0b1111 to the lower 4 bits of the register at address 0x10

8.4.1.2.1.3 REG_WRITE_MASK_PAGE0_IMM Command

Description: Write the specified data, except the masked bits, to the specified page 0 register address

Assembly command: **REG_WRITE_MASK_PAGE0_IMM [ADDR=]<Address> [DATA=]<Data> [MASK=]<Mask>**

Address, Data, and Mask can be in any literal integer format (decimal, hex, and so forth).

'ADDR=', 'DATA=', and 'MASK=' are optional. When included, the parameters can be in any order.

Examples:
- **REG_WRITE_MASK_PAGE0_IMM 0x1D 0x80 0xF0** — Write 0b1000 to the upper 4 bits of the register at address 0x1D
- **REG_WRITE_MASK_PAGE0_IMM ADDR=0x10 DATA=0x0F MASK=0xF0** — Write 0b1111 to the lower 4 bits of the register at address 0x10
- **REG_WRITE_MASK_PAGE0_IMM DATA=0x0F MASK=0xF0 ADDR=0x10** — Write 0b1111 to the lower 4 bits of the register at address 0x10

8.4.1.2.1.4 REG_WRITE_BIT_PAGE0_IMM Command

Description: Write the specified data to the BIT_SEL location of the specified page 0 register address

Assembly command: **REG_WRITE_BIT_PAGE0_IMM [ADDR=]<Address> [BIT=]<Bit> [DATA=]<Data>**

Address, Bit, and Data can be in any literal integer format (decimal, hex, and so forth).

'ADDR=', 'BIT=', and 'DATA=' are optional. When included, the parameters can be in any order.

Examples:

- **REG_WRITE_BIT_PAGE0_IMM 0x1D 7 0** — Write '0' to bit 7 of the register at address 0x1D
- **REG_WRITE_BIT_PAGE0_IMM ADDR=0x10 BIT=3 DATA=1** — Write 0b1 to bit 3 of the register at address 0x10

8.4.1.2.1.5 REG_WRITE_WIN_PAGE0_IMM Command

Description: Write the specified data to the SHIFT location of the specified page 0 register address

Assembly command: **REG_WRITE_WIN_PAGE0_IMM [ADDR=]<Address> [DATA=]<Data> [MASK=]<Mask> [SHIFT=]<Shift>**

Address, Data, Mask, and Shift can be in any literal integer format (decimal, hex, and so forth).

'ADDR=', 'DATA=', 'MASK=', and 'SHIFT=' are optional. When included, the parameters can be in any order.

Examples:

- **REG_WRITE_WIN_PAGE0_IMM ADDR=0x1D DATA=0x8 MASK=0x13 SHIFT=2** — Write bits 5:4 to 0b10 to the register at address 0x1D. Data and mask give 5-bit value 0bx10xx. These two bits are then left shifted 2 bit-positions to give full byte value of 0bxx10xxxx, hence sets bits 5:4 to 0b10.

8.4.1.2.1.6 REG_WRITE_VOUT_IMM Command

Description: Write the target voltage of a specified regulator after a specified delay. This command is a spin-off of the REG_WRITE_IMM command with the intention to save instruction bits.

Assembly command: **REG_WRITE_VOUT_IMM [REGULATOR=]<Regulator ID> [SEL=]<VSEL> [VOUT=]<Vout> [DELAY=]<Delay>**

'REGULATOR=', "SEL=', 'VOUT=', and 'DELAY=' are options. When included, the parameters can be in any order.

Regulator ID = BUCK1, BUCK2, BUCK3, BUCK4, BUCK5, LDO1, LDO2, LDO3, or LDO4.

VSEL selects the BUCKn_VSET1 or BUCKn_VSET2 bits which the command writes to if Regulator ID is BUCK1-5. It is defined as: '0': BUCKn_VSET1, '1': BUCKn_VSET2, '2': Currently Active BUCKn_VSET, '3': Currently Inactive BUCKn_VSET. If Regulator ID is LDO1-4, VSEL value is ignored.

VOUT = output voltage in mV or V. Unit must be listed.

DELAY = delay time in ns, µs, ms, or s. If no unit is entered, this field must be an integer value between 0-63, which becomes the threshold count for the counter running a step size specified in the register PFSM_DELAY_STEP. The delay value is rounded to the nearest achievable delay time based on the current step size. Current step size is based on the default NVM setting or a SET_DELAY value from a previous command in the same sequence. Assembler reports an error if the step size is too large or too small to meet the delay.

Examples:

- **REG_WRITE_VOUT_IMM BUCK3 2 1.05 V 100 µs** — Sets BUCK3 to 1.05 V by updating the active BUCK3_VSET register after 100 µs
- **REG_WRITE_VOUT_IMM REGULATOR=LDO1 SEL=0 VOUT=700 mV DELAY=6 ms** — Sets LDO1 to 700 mV after 6 ms.

8.4.1.2.1.7 REG_WRITE_VCTRL_IMM Command

Description: Write the operation mode of a specified regulator after a specified delay. This command is a spin-off of the REG_WRITE_IMM command with the intention to save instruction bits.

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Assembly command: **REG_WRITE_VCTRL_IMM [REGULATOR=]<Regulator ID> [VCTRL=]<VCTRL> [MASK=]<Mask> [DELAY=]<Delay> [DELAY_MODE=]<Delay Mode>**

'REGULATOR=', 'VCTRL=', 'MASK=', and 'DELAY=' are options. When included, the parameters can be in any order.

Regulator ID = BUCK1, BUCK2, BUCK3, BUCK4, BUCK5, LDO1, LDO2, LDO3, or LDO4.

VCTRL = 0-15, in hex, decimal, or binary format. Data to write to the following regulator control fields:

- BUCKs: BUCKn_PLDN, BUCKn_VMON_EN, BUCKn_VSEL, BUCKn_FPWM_MP, BUCKn_FPWM, and BUCKn_EN
- LDOs: LDOn_PLDN, LDOn_VMON_EN, 0, 0, LDOn_EN

DELAY = delay time in ns, µs, ms, or s. If no unit is entered, this field must be an integer value between 0-63, which becomes the threshold count for the counter running a step size specified in the register PFSM_DELAY_STEP. Delay value is be rounded to the nearest achievable delay time based on the current step size. Current step size is based on the default NVM setting or a SET_DELAY value from a previous command in the same sequence. Assembler reports an error if the step size is too large or too small to meet the delay.

Delay Mode must be one of the below options: MATCH_EN = 0 (Delay if VCTRL enable bit mismatches) MATCH_ALL = 1 (Delay if any VCTRL bits mismatch) ALWAYS = 2 (Delay always)

Examples:

- **REG_WRITE_VCTRL_IMM BUCK3 0x00 0xE0 100 µs** — Sets BUCK3 to OFF (VCTRL bits = 0b00000) after 100 µs
- **REG_WRITE_VCTRL_IMM REGULATOR=LDO1 VCTRL=0x09 MASK=0x36 DELAY=10 ms** — Set LDO1_VMON and LDO1_EN to '1' after 10 ms

8.4.1.2.1.8 REG_WRITE_MASK_SREG Command

Description: Write the data from a scratch register, except the masked bits, to the specified register address

Assembly command: **REG_WRITE_MASK_SREG [REG=]<Scratch Register> [ADDR=]<Address> [MASK=]<Mask>**

'REG=', 'ADDR=', and 'MASK=' are options. When included, the parameters can be in any order.

Scratch Register can be R0, R1, R2, or R3.

Address and Mask can be in any literal integer format (decimal, hex, and so forth).

Examples:

- **REG_WRITE_MASK_SREG R2 0x22 0x00** — Write the content of scratch register 2 to address 0x22
- **REG_WRITE_MASK_SREG REG=R0 ADDR=0x054 MASK=0xF0** — Write the lower 4 bits of scratch register 0 to address 0x54

8.4.1.2.1.9 SREG_READ_REG Command

Description: Write scratch register (REG0-3) with data from a specified address

Assembly command: **SREG_READ_REG [REG=]<Scratch Register> [ADDR=]<Address>**

'REG=' and 'ADDR=' are options. When included, the parameters can be in any order.

Scratch Register can be R0, R1, R2, or R3.

Address can be in any literal integer format (decimal, hex, and so forth).

Examples:

- **SREG_READ_REG R2 0x15** — Read the content of address 0x15 and write the data to scratch register 2
- **SREG_READ_REG ADDR=0x077 REG=R3** — Read the content of address 0x77 and write the data to scratch register 3

8.4.1.2.1.10 SREG_WRITE_IMM Command

Description: Write the specified data to the scratch register (REG0-3)

Assembly command: **SREG_WRITE_IMM [REG=]<Register> [DATA=]<Data>**

Data can be in any literal integer format (decimal, hex, and so forth).

Register can be R0, R1, R2, or R3.

'REG=' and 'DATA=' are options. When included, the parameters can be in any order.

Examples:

- **SREG_WRITE_IMM R2 0x15** — Write 0x15 to scratch register 2
- **SREG_WRITE_IMM ADDR=0x077 REG=R3** — Read 0x77 to scratch register 3

8.4.1.2.1.11 WAIT Command

Description: Wait upon a condition of a given type. Execution is paused until the specified type of the condition is met or timed out

Assembly command: **WAIT [COND=]<Condition> [TYPE=]<Type> [TIMEOUT=]<Timeout> [DEST=]<Destination>**

Alternative assembly command: **JUMP [DEST=]<Destination>**

'COND=', 'TYPE=', 'TIMEOUT=', and 'DEST=' are options. When included, the parameters can be in any order.

Condition are listed in Table 8-13. Examples: GPIO1, BUCK1_PG, I2C_1

Type = LOW, HIGH, RISE, or FALL

Timeout = timeout value in ns, µs, ms, or s. If no unit is entered, this field must be an integer value between 0-63. Timeout value is be rounded to the nearest achievable time based on the current step size. Current step size is based on the default NVM setting or a SET_DELAY value from a previous command in the same sequence. Assembler reports an error if the step size is too large or too small to meet the delay.

Destination = Label to jump to if when timeout occurs. Destination must be after the WAIT statement in memory.

Memory space can be either '0' or '1'. '0' indicates the destination address is in the PFSM memory space. '1' indicates the destination address is external and represents a FSM state ID.

When using the jump command, the PFSM performs an unconditional jump. The command is be compiled as "WAIT COND=63 TYPE=LOW TIMEOUT=0 DEST=<Destination>". Condition 63 is a hardcoded 1, so the condition is never satisfied and hence always times out. Therefore this command always jumps to the destination.

Examples:

- **WAIT GPIO4 RISE 1 s <Destination> 0** — Wait to execute the command at the specified SRAM address when a rise edge is detected at GPIO4, or after 1 second
- **WAIT COND=BUCK1_PG TYPE=HIGH TIMEOUT=500 µs DEST=<mcu2act_seq>** — Wait to execute the commands at <mcu2act_seq> address as soon as BUCK1 output is within power-good range, or after 500 µs

Table 8-13. WAIT Command Conditions

COND_SEL	Condition Name	COND_SEL	Condition Name	COND_SEL	Condition Name	COND_SEL	Condition Name
0	GPIO1	16	LDO1_PG	32	I2C_0	48	LP_STANDBY_SEL
1	GPIO2	17	LDO2_PG	33	I2C_1	49	N/A
2	GPIO3	18	LDO3_PG	34	I2C_2	50	N/A
3	GPIO4	19	LDO4_PG	35	I2C_3	51	N/A
4	GPIO5	20	PGOOD	36	I2C_4	52	N/A
5	GPIO6	21	TWARN_EVENT	37	I2C_5	53	N/A
6	GPIO7	22	INTERRUPT_PIN	38	I2C_6	54	N/A
7	GPIO8	23	N/A	39	I2C_7	55	N/A
8	GPIO9	24	N/A	40	SREG0_0	56	N/A
9	GPIO10	25	N/A	41	SREG0_1	57	N/A

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Table 8-13. WAIT Command Conditions (continued)

COND_ SEL	Condition Name	COND_ SEL	Condition Name	COND_ SEL	Condition Name	COND_ SEL	Condition Name
10	GPIO11	26	N/A	42	SREG0_2	58	N/A
11	BUCK1_PG	27	N/A	43	SREG0_3	59	N/A
12	BUCK2_PG	28	N/A	44	SREG0_4	60	N/A
13	BUCK3_PG	29	N/A	45	SREG0_5	61	N/A
14	BUCK4_PG	30	N/A	46	SREG0_6	62	0
15	BUCK5_PG(use for EXT_VMON PowerGood)	31	N/A	47	SREG0_7	63	1

8.4.1.2.1.12 DELAY_IMM Command

Description: Delay the execution by a specified time

Assembly command: **DELAY_IMM <Delay>**

Delay = delay time in ns, µs, ms, or s. If no unit is entered, this field must be an integer value between 0-63. Delay value is be rounded to the nearest achievable time based on the current step size. Current step size is based on the default NVM setting or a SET_DELAY value from a previous command in the same sequence. Assembler reports an error if the step size is too large or too small to meet the delay.

Examples:

- **DELAY_IMM 100 µs** — Delay execution by 100 µs
- **DELAY_IMM 10 ms** — Delay execution by 10 ms
- **DELAY_IMM 8** — Delay execution by 8 ticks of the current PFSM time step

8.4.1.2.1.13 DELAY_SREG Command

Description: Delay the execution by a time value stored in the specified scratch register.

Assembly command: **DELAY_SREG <Register>**

Register can be R0, R1, R2, or R3.

Examples:

- **DELAY_SREG R0** — Delay execution by the time value stored in scratch register0

8.4.1.2.1.14 TRIG_SET Command

Description: Set a trigger destination address for a given input signal or condition. These commands must be defined at the beginning of PFSM configuration memory.

Assembly command: **TRIG_SET [DEST=]<Destination> [ID=]<Trig_ID> [SEL=]<Trig_sel> [TYPE=]<Trig_type> [IMM=]<IMM> [EXT=]<Memory space>**

'DEST=', 'ID=', 'SEL='. 'TYPE=', 'IMM=', and 'EXT=' are options. When included, the parameters can be in any order.

Destination is the label where this trigger starts executing.

Trig_ID is the ID of the hardware trigger module to be configured (value range 0-27). They must be defined in numeric order based on the priority of the trigger.

Trig_Sel is the 'Trigger Name' from the Table 8-15. This 'Trigger Name' is the trigger signal to be associated with the specified TRIG_ID.

Trig_type = LOW, HIGH, RISE, or FALL.

IMM can be either '0' or '1'. = '0' if the trigger is not activated until the END command of a given task; '1' if the trigger is activated immediately and can abort a sequence.

REENTRANT can be either '0' or '1'. '1' permits a trigger to return to the current state, which allows a self-branching trigger to execute the current sequence again.

Memory space can be either '0' or '1'. '0' indicates the destination address is in the PFSM memory space. '1' indicates the destination address is external and represents a FSM state ID.

Examples:

- **TRIG_SET seq1 20 GPIO_1 LOW 0 0** — Set trigger 20 to be GPIO_1=Low, not immediate. When triggered, start executing at ‘seq1’ label.
- **TRIG_SET DEST=seq2 ID=15 SEL=WD_ERROR TYPE=RISE IMM=0 EXT=0** — Set trigger 15 to be rising WD_ERROR trigger, not immediate. When triggered, start executing at ‘seq2’ label.

8.4.1.2.1.15 TRIG_MASK Command

Description: Sets a trigger mask that determines which triggers are active. Setting a ‘0’ enables the trigger, setting a ‘1’ disables (masks) the trigger.

Assembly command: **TRIG_MASK <Mask value>**

Mask Value = 28-bit mask in any literal integer format (decimal, hex, and so forth).

Examples:

- **TRIG_MASK 0x5FF82F0** — Set the trigger mask to 0x5FF82F0

8.4.1.2.1.16 END Command

Table 8-14 shows the format of the END commands.

Table 8-14. END Command Format

Bit[3:0]
CMD
4 bits

Description: Marks the final instruction in a sequential task

Fields:

- CMD: Command opcode (0xC)

Assembly command: **END**

8.4.1.2.2 Configuration Memory Organization and Sequence Execution

The configuration memory is loaded from NVM into an SRAM. Figure 8-41 shows an example configuration memory with only two configured sequences.

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```
pfsm_start:
TRIG_SET DEST=sequence_name1 ID=0 SEL=trigger_name TYPE=high/low/rise/fall IMM=0/1 EXT=0/1
TRIG_SET DEST=sequence_name2 ID=1 SEL=trigger_name TYPE=high/low/rise/fall IMM=0/1 EXT=0/1
TRIG_SET DEST=sequence_name3 ID=2 SEL=trigger_name TYPE=high/low/rise/fall IMM=0/1 EXT=0/1
TRIG_SET DEST=sequence_name4 ID=4 SEL=trigger_name TYPE=high/low/rise/fall IMM=0/1 EXT=0/1
TRIG_SET DEST=sequence_name5 ID=4 SEL=trigger_name TYPE=high/low/rise/fall IMM=0/1 EXT=0/1
……
TRIG_MASK 0xFFFFFF0
END
sequence_name1
REG_WRITE_MASK_IMM ADDR=register_addr DATA=data MASK=mask_setting
REG_WRITE_MASK_IMM ADDR=register_addr DATA=data MASK=mask_setting
REG_WRITE_MASK_IMM ADDR=register_addr DATA=data MASK=mask_setting
REG_WRITE_VCTRL_IMM REGULATOR=regulator VCTRL=ctrl_setting MASK=mask_setting DELAY=delay_time
REG_WRITE_VCTRL_IMM REGULATOR=regulator VCTRL=ctrl_setting MASK=mask_setting DELAY=delay_time
DELAY_IMM delay_time
REG_WRITE_MASK_IMM ADDR=register_addr DATA=data MASK=mask_setting
REG_WRITE_VCTRL_IMM REGULATOR=regulator VCTRL=ctrl_setting MASK=mask_setting DELAY=delay_time
REG_WRITE_MASK_IMM ADDR=register_addr DATA=data MASK=mask_setting
TRIG_MASK 0xFC00EDF
END
……
sequence_name4
REG_WRITE_MASK_IMM ADDR=register_addr DATA=data MASK=mask_setting
DELAY_IMM delay_time
REG_WRITE_MASK_IMM ADDR=register_addr DATA=data MASK=mask_setting
REG_WRITE_VCTRL_IMM REGULATOR=regulator VCTRL=ctrl_setting MASK=mask_setting DELAY=delay_time
REG_WRITE_VCTRL_IMM REGULATOR=regulator VCTRL=ctrl_setting MASK=mask_setting DELAY=delay_time
DELAY_IMM delay_time
REG_WRITE_VCTRL_IMM REGULATOR=regulator VCTRL=ctrl_setting MASK=mask_setting DELAY=delay_time
REG_WRITE_MASK_IMM ADDR=register_addr DATA=data MASK=mask_setting
REG_WRITE_VCTRL_IMM REGULATOR=regulator VCTRL=ctrl_setting MASK=mask_setting DELAY=delay_time
REG_WRITE_MASK_IMM ADDR=register_addr DATA=data MASK=mask_setting
TRIG_MASK 0xFEF6EDC
END
```

These TRIG_SET instructions are used to define the trigger types which initiates each power state sequence. There are a total of 28 TRIG_SET available for each PMIC. TYPE parameter defines the type of trigger as:

High: active high (level sensitive)
Low: active low (level sensitive)
Rise: active high (edge sensitive)
Fall: active low (edge sensitive)

Figure 8-41. Configuration Memory Script Example

As soon as the PMIC state reaches the mission states, it starts reading from the configuration memory until it hits the first END command. Setting up the triggers (1-28) must be the first section of the configuration memory, as well as the first set of trigger configurations. The trigger configurations are read and mapped to an internal lookup table, which contains the starting address associated with each trigger in the configuration memory. If the trigger destination is an FFSM state then the address contains the fixed state value. After the trigger configurations are read and mapped into the SRAM, these triggers control the execution flow of the state transitions. The signal source of each trigger is listed under Table 8-15.

When a trigger or multiple triggers are activated, the PFSM execution engine looks up the starting address associated with the highest priority trigger which is unmasked, and starts executing commands until it hits an END command. The last commands before END statement is generally the TRIG_MASK command, which directs the PFSM to a new set of unmasked trigger configurations, and the trigger with the highest priority in the new set is serviced next. Trigger priority is determined by the Trigger ID associated with each trigger. The priority of the trigger decreases as the associated trigger ID increases. As a result, the critical error triggers are usually located at the lowest trigger IDs.

The TRIG_SET commands specify if a trigger is immediate or non-immediate. Immediate triggers are serviced immediately, which involves branching from the current sequence of commands to reach a new target destination. The non-immediate triggers are accumulated and serviced in the order of priority through the execution of each given sequence until the END command in reached. Therefore, the trigger ID assignment for each trigger can be arranged to produce the desired PFSM behavior.

The TRIG_MASK command determines which triggers are active at the end of each sequence, and is usually placed just before the END instruction. The TRIG_MASK takes a 28 bit input to allow any combination of triggers to be enabled with a single command. Through the definition of the active triggers after each sequence execution the TRIG_MASK command can be conceptualized as establishing a power state.

The above sequence of waiting for triggers and executing the sequence associated with an activated trigger is the normal operating condition of the PFSM execution engine when the PMIC is in the MISSION state. The

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FFSM state machine takes over control from the execution engine each time an event occurs that requires a transition from the MISSION state of the PMIC to a fixed device state.

Table 8-15. PFSM Trigger Selections

Trigger Name	Trigger Source
IMMEDIATE_SHUTDOWN	An error event causes one of the triggers defined in the FSM_TRIG_SEL_1/2 register to activate, and the intended action for the activated trigger is to *immediate shutdown* the device
MCU_POWER_ERROR	Output failure detection from a regulator which is assigned to the MCU rail group (x_GRP_SEL = '01')
ORDERLY_SHUTDOWN	An event which causes MODERATE_ERR_INT = '1'
FORCE_STANDBY	nPWRON long-press event when NPOWRON_SEL = '01', or ENABLE = '0' when NPOWERON_SEL = '00'
SPMI_WD_BIST_DONE	Completion of SPMI WatchDog BIST
ESM_MCU_ERROR	An event which causes ESM_MCU_FAIL_INT
WD_ERROR	An event which causes WD_INT
SOC_POWER_ERROR	Output failure detection from a regulator which is assigned to the SOC rail group (x_GRP_SEL = '10')
ESM_SOC_ERROR	An event which causes ESM_SOC_FAIL_INT
A	NSLEEP2 and NSLEEP1 = '11'. More information regarding the NSLEEP1 and NSLEEP2 functions can be found under Section 8.4.1.2.4.3
WKUP1	A rising or falling edge detection on a GPIO pin which is configured as WKUP1 or LP_WKUP1
SU_ACTIVE	A valid On-Request detection when STARTUP_DEST = '11'
B	NSLEEP2 and NSLEEP1 = '10'. More information regarding the NSLEEP1 and NSLEEP2 functions can be found under Section 8.4.1.2.4.3
WKUP2	A rising or falling edge detection on a GPIO pin which is configured as WKUP2 or LP_WKUP2
SU_MCU_ONLY	A valid On-Request detection when STARTUP_DEST = '10'
C	NSLEEP2 and NSLEEP1 = '01', More information regarding the NSLEEP1 and NSLEEP2 functions can be found under Section 8.4.1.2.4.3
D	NSLEEP2 and NSLEEP1 = '00'. More information regarding the NSLEEP1 and NSLEEP2 functions can be found under Section 8.4.1.2.4.3
SU_STANDBY	A valid On-Request detection when STARTUP_DEST = '00'
SU_X	A valid On-Request detection when STARTUP_DEST = '01'
WAIT_TIMEOUT	PFSM WAIT command condition timed out. More information regarding the WAIT command can be found under Section 8.4.1.2.1.11
GPIO1	Input detection at GPIO1 pin
GPIO2	Input detection at GPIO2 pin
GPIO3	Input detection at GPIO3 pin
GPIO4	Input detection at GPIO4 pin
GPIO5	Input detection at GPIO5 pin
GPIO6	Input detection at GPIO6 pin
GPIO7	Input detection at GPIO7 pin
GPIO8	Input detection at GPIO8 pin
GPIO9	Input detection at GPIO9 pin
GPIO10	Input detection at GPIO10 pin
GPIO11	Input detection at GPIO11 pin
I2C_0	Input detection of TRIGGER_I2C_0 bit
I2C_1	Input detection of TRIGGER_I2C_1 bit
I2C_2	Input detection of TRIGGER_I2C_2 bit
I2C_3	Input detection of TRIGGER_I2C_3 bit
I2C_4	Input detection of TRIGGER_I2C_4 bit
I2C_5	Input detection of TRIGGER_I2C_5 bit
I2C_6	Input detection of TRIGGER_I2C_6 bit

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Table 8-15. PFSM Trigger Selections (continued)

Trigger Name	Trigger Source
I2C_7	Input detection of TRIGGER_I2C_7 bit
SREG0_0	Input detection of SCRATCH_PAD_REG_0 bit 0
SREG0_1	Input detection of SCRATCH_PAD_REG_0 bit 1
SREG0_2	Input detection of SCRATCH_PAD_REG_0 bit 2
SREG0_3	Input detection of SCRATCH_PAD_REG_0 bit 3
SREG0_4	Input detection of SCRATCH_PAD_REG_0 bit 4
SREG0_5	Input detection of SCRATCH_PAD_REG_0 bit 5
SREG0_6	Input detection of SCRATCH_PAD_REG_0 bit 6
SREG0_7	Input detection of SCRATCH_PAD_REG_0 bit 7
0	Always '0'
1	Always '1'

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8.4.1.2.3 Mission State Configuration

The Mission States portion of the FSM engine manages the sequencing of power rails and external outputs in the user defined states. For the rest of Section 8.4.1 the Figure 8-42 is used as an example state machine which is defined through the configuration memory using the configuration FSM instructions.

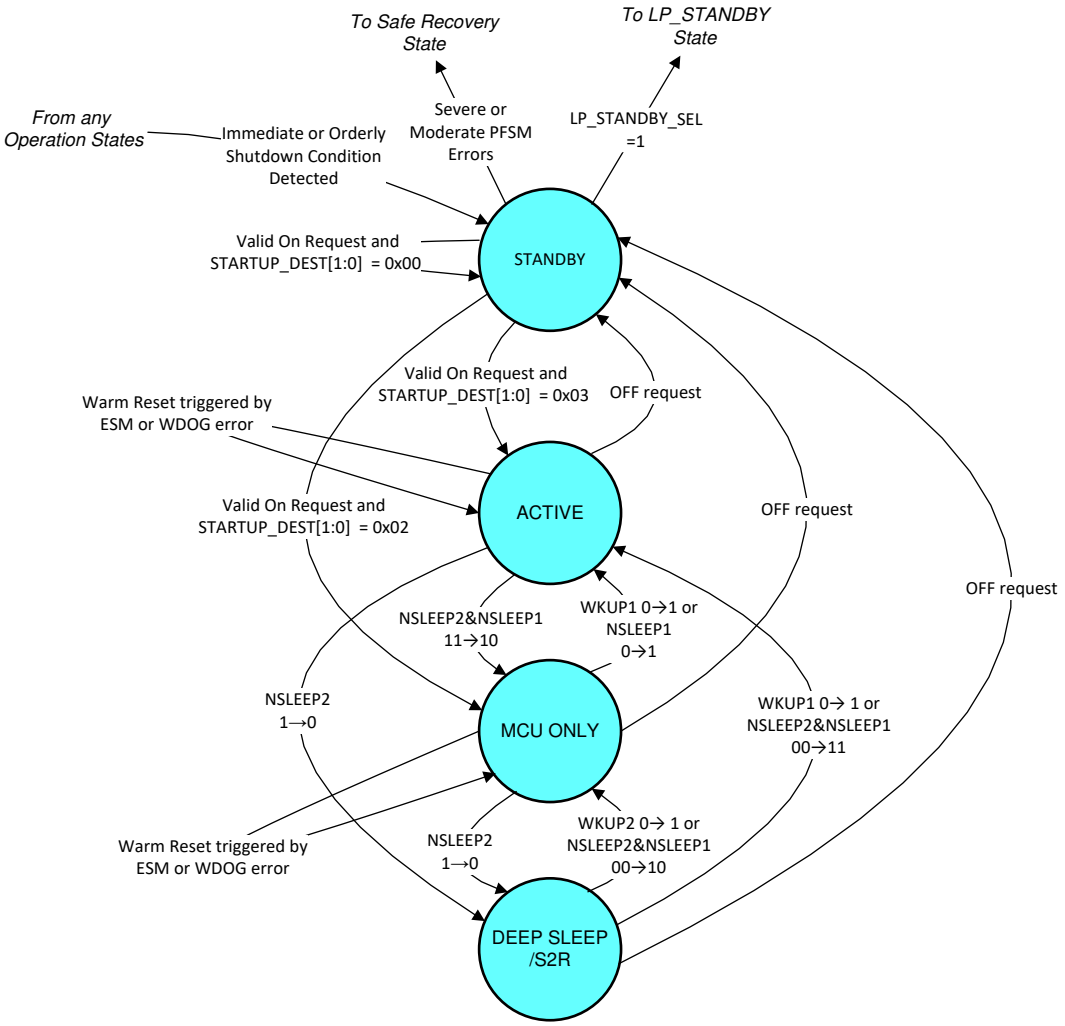

Figure 8-42. Example of a Mission State-Machine

Each power state (light blue bubbles in Figure 8-42) defines the ON or OFF state and the sequencing timing of the external regulators and GPIO outputs. This example defines 4 power states: STANDBY, ACTIVE, MCU ONLY, and DEEP_SLEEP/S2R states. The priority order of these states is as follows:

1. ACTIVE
2. MCU ONLY
3. DEEP SLEEP/S2R
4. STANDBY

The transitions between each power state is determined by the trigger signals source pre-selected from Table 8-15. These triggers are then placed in the order of priority through the trigger ID assignment of each trigger source. The critical error triggers are placed first, some specified as immediate triggers that can interrupt an on-going sequence. The non-error triggers, which are used to enable state transitions during normal device operation, are then placed according to the priority order of the state the device is transitioning to. Table 8-16 list the trigger signal sources, in the order of priority, used to define the power states and transitions of the example mission state machine shown in Figure 8-42. This table also helps to determine which triggers must be masked by the TRIG_MASK command upon arriving a pre-defined power state to produce the desired PFSM behavior.

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Table 8-16. List of Trigger Used in Example Mission State Machine

Trigger ID	Trigger Signal	State Transitions	Trigger Masked In Each User Defined Power State			
			STANDBY	ACTIVE	MCU ONLY	DEEP SLEEP / S2R
0	IMMEDIATE_SHUTDOWN (1)	From any state to SAFE RECOVERY				
1	MCU_POWER_ERROR (1)	From any state to SAFE RECOVERY				
2	ORDERLY_SHUTDOWN (1)	From any state to SAFE RECOVERY				
3	TRIGGER_FORCE_STANDBY	From any state to STANDBY or LP_STANDBY	Masked			
4	WD_ERROR	Perform warm reset of all power rails and return to ACTIVE	Masked		Masked	Masked
5	ESM_MCU_ERROR	Perform warm reset of all power rails and return to ACTIVE	Masked		Masked	Masked
6	ESM_SOC_ERROR	Perform warm reset of power rails in SOC domain and return to ACTIVE	Masked		Masked	Masked
7	WD_ERROR	Perform warm reset of all power rails and return to MCU ONLY	Masked	Masked		Masked
8	ESM_MCU_ERROR	Perform warm reset of all power rails and return to MCU ONLY	Masked	Masked		Masked
9	SOC_POWER_ERROR	ACTIVE to MCU ONLY	Masked		Masked	Masked
10	TRIGGER _I2C_1 (self-cleared)	Start RUNTIME_BIST	Masked			Masked
11	TRIGGER_I2C_2 (self-cleared)	Enable I2C CRC Function	Masked			Masked
12	TRIGGER_SU_ACTIVE	STANDBY to ACTIVE			Masked	Masked
13	TRIGGER_WKUP1	Any State to ACTIVE				
14	TRIGGER_A (NSLEEP2&NSLEEP1 = '11')	MCU ONLY or DEEP SLEEP/S2R to ACTIVE	Masked			
15	TRIGGER_SU_MCU_ONLY	STANDBY to MCU ONLY		Masked		Masked
16	TRIGGER_WKUP2	STANDBY or DEEP SLEEP/S2R to MCU ONLY		Masked		
17	TRIGGER_B (NSLEEP2&NSLEEP1 = '10')	ACTIVE or DEEP SLEEP/S2R to MCU ONLY	Masked			
18	TRIGGER_D or TRIGGER_C (NSLEEP2 = '0')	ACTIVE or MCU ONLY to DEEP SLEEP/S2R	Masked			Masked
19	TRIGGER_I2C_0 (self-cleared)	Any state to STANDBY	Masked			Masked
20	Always '1' (2)	STANDBY to SAFE RECOVERY	Mask	Masked	Masked	Masked
21	Not Used		Mask	Masked	Masked	Masked
22	Not Used		Mask	Masked	Masked	Masked
23	Not Used		Mask	Masked	Masked	Masked
24	Not Used		Mask	Masked	Masked	Masked
25	Not Used		Mask	Masked	Masked	Masked
26	Not Used		Mask	Masked	Masked	Masked

Table 8-16. List of Trigger Used in Example Mission State Machine (continued)

Trigger ID	Trigger Signal	State Transitions	Trigger Masked In Each User Defined Power State			
			STANDBY	ACTIVE	MCU ONLY	DEEP SLEEP / S2R
27	Not Used		Mask	Masked	Masked	Masked
28-bit TRIG_MASK Value in Hex format:			0xFFE4FF8	0xFF18180	0xFF01270	0xFFC9FF0

(1) This is an immediate trigger.
(2) When an error occurs, which requires the device to enter directly to the SAFE RECOVERY state, the mask for this trigger must be removed while all other non-immediate triggers are masked. The device exits the mission states and the FFSM state machine takes over control of the device power states once this trigger is executed.

8.4.1.2.4 Pre-Configured Hardware Transitions

There are some pre-defined trigger sources, such as on-requests and off-requests, which are constructed with the combination of hardware input signals and register bits settings. This section provides more detail to these pre-defined trigger sources and shows how they can be utilized in the PFSM configuration to initiate state to state transitions.

8.4.1.2.4.1 ON Requests

ON requests are used to switch on the device, which transitions the device from the STANDBY or the LP_STANDBY to the state specified by STARTUP_DEST[1:0].

After the device arrives at the corresponding STARTUP_DEST[1:0] operation state, the MCU must setup the NSLEEP1 and NSLEEP2 signals accordingly before clearing the STARTUP_INT interrupt. Once the interrupt is cleared, the device stays or moves to the next state corresponding to the NSLEEP signals state assignment as specified in Table 8-20.

Table 8-17 lists the available ON requests.

Table 8-17. ON Requests

EVENT	MASKABLE	COMMENT	DEBOUNCE
nPWRON (pin)	Yes	Edge sensitive	50 ms
ENABLE (pin)	Yes	Level sensitive	8 µs
First Supply Detection (FSD)	Yes	VCCA > VCCA_UV and FSD unmasked	N/A
RTC ALARM Interrupt	Yes		N/A
RTC TIMER Interrupt	Yes		N/A
WKUP1 or WKUP2 Detection	Yes	Edge sensitive	8 µs
LP_WKUP1 or LP_WKUP2 Detection	Yes	Edge sensitive	N/A
Recovery from Immediate and Orderly Shutdown	Yes	Recover from system errors which caused immediate or orderly shutdown of the device	N/A

If one of the events listed in Table 8-17 occurs, then the event powers on the device unless one of the gating conditions listed in Table 8-18 is present.

Table 8-18. ON Requests Gating Conditions

EVENT	MASKABLE	COMMENT
VCCA_OVP (event)	No	VCCA > VCCA_OVP, VSYS_DEAD_LOCK_EN = 1
VCCA_UVLO (event)	No	VCCA < VCCA_UVLO
VINT_OVP (event)	No	LDOVINT > 1.98 V
VINT_UVLO (event)	No	LDOVINT < 1.62 V
TSD (event)	No	Device stays in SAFE RECOVERY until temperature decreases below TWARN level

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The NPWRON_SEL NVM register bit determines whether the nPWRON/ENABLE pin is treated as a power on press button or a level sensitive enable switch. When this pin is configured as the nPWRON button, a short button press detection is latched internally as a device enable signal until the NPWRON_START_INT is cleared, or a long press key event is detected. The short button press detection occurs when an falling edge is detected at the nPWRON pin. When the NPWRON_START_MASK bit is set to '1', the device does no longer react to the changing state of the pin as the nPWRON press button.

The nPWRON/ENABLE pin is a level sensitive pin when it is configured as an ENABLE pin, and an assertion enables the device until the pin is released. When the ENABLE_MASK bit is set to '1', the device does no longer react to the changing state of the pin as the ENABLE switch.

8.4.1.2.4.2 OFF Requests

An OFF request is used to orderly switch off the device. OFF requests initiate transition from any other mission state to the STANDBY state or the LP_STANDBY state depending on the setting of the LP_STANDBY_SEL bit. Table 8-19 lists the conditions to generate the OFF requests and the corresponding destination state.

Table 8-19. OFF Requests

EVENT	DEBOUNCE	LP_STANDBY_SEL BIT SETTING	DESTINATION STATE
nPWRON (pin) (long press key event)	8 s	LP_STANDBY_SEL = 0	STANDBY
		LP_STANDBY_SEL = 1	LP_STANDBY
ENABLE (pin)	8 µs	LP_STANDBY_SEL = 0	STANDBY
		LP_STANDBY_SEL = 1	LP_STANDBY
I2C_TRIGGER_0	NA	LP_STANDBY_SEL = 0	STANDBY
		LP_STANDBY_SEL = 1	LP_STANDBY

The long press key event occurs when the nPWRON pin stays low for longer than t_{LPK_TIME} while the device is in a mission state.

When the nPWRON or ENABLE pin is used as the OFF request, the device wakes up from the STANDBY or the LP_STANDBY state through the ON request initiated by the same pin. The NPWRON_START_MASK or the ENABLE_MASK must remain low in this case to allow the detection of the ON request initiated by the pin. If the device needs to enter the LP_STANDBY state through the OFF request, it is important that the state of the nPWRON or ENABLE pin must remain the same until the state transition is completed. Failure to do so may result in unsuccessful wake-up from the LP_STANDBY state when the pin re-initiates On request.

Using the I2C_TRIGGER_0 bit as the OFF request enables the device to wake up from the STANDBY or the LP_STANDBY states through the detection of LP_WKUPn/WKUPn pins, as well as RTC alarm or timer interrupts. To enable this feature, the device must set the I2C_TRIGGER_0 bit to '1' while the NSLEEPn signals are masked, and the ON request (initialized by the nPWRON or ENABLE pins) must remain active.

8.4.1.2.4.3 NSLEEP1 and NSLEEP2 Functions

The SLEEP requests are activated through the assertion of nSLEEP1 or nSLEEP2 pins, which are the secondary functions of the 11 GPIO pins and can be selected through GPIO configuration using the GPIOx_SEL register bits. If the nSLEEP1 or nSLEEP2 pins are not available, the NSLEEP1B and NSLEEP2B register bits can be configured in place for their functions. The input of nSLEEP1 pin and the state of the NSLEEP1B register bit are combined to create the NSLEEP1 signal through an *OR* function. Similarly for the input of the nSLEEP2 pin and the NSLEEP2B register bit as they are combined to create the NSLEEP2 signal.

A 1 → 0 logic level transition of the NSLEEP signal generates a sleep request, while a 0 → 1 logic level transition reverses the sleep request in the example PFSM from Figure 8-42. When a NSLEEPn signal transitions from 1 → 0, it generates a sleep request to go from a higher power state to a lower power state. When the signal transitions from 0 → 1, it reverses the sleep request and returns the device to the higher power state.

The NSLEEP1 signal is designed to control the SoC supply rails. The NSLEEP2 signal is designed to control the MCU supply rails. When NSLEEP1 signal changes from 1 → 0, depending on the state of NSLEEP2, the

TPS6594-Q1 device exits ACTIVE state and enters either the MCU ONLY or the S2R states. When NSLEEP2 signal changes from 1 → 0, the device enters the S2R state regardless the state of NSLEEP1.

When the NSLEEP2 input signal changes from 0 →1, the MCU supply rails are enabled and the device exits S2R state. Depending on the state of NSLEEP1 signal, the device enters either the MCU ONLY or the ACTIVE state. In order for the system to function correctly, the MCU rails must be enabled when the NSLEEP1 input signal changes from 0 →1, which enables the SOC supply rails. NSLEEP1 0 →1 transition is ignored if NSLEEP2 is 0.

The NSLEEPn_MASK bit can be used to mask the sleep request associated with the corresponding NSLEEPn signal. When the NSLEEPn_MASK = 1, the corresponding NSLEEPn signal is ignored. Table 8-20 shows how the combination of the NSLEEPn signals and NSLEEPn_MASK bits creates triggers A/B/C/D to the FSM to control the power state of the device.

The states of the resources during ACTIVE, SLEEP, and DEEP SLEEP/S2R states are defined in the LDOn_CTRL and BUCKn_CTRL registers. For each resource, a transition to the MCU ONLY or the DEEP SLEEP/S2R states is controlled by the FSM when the resource is associated to the SLEEP or DEEP SLEEP/S2R states.

Table 8-20 shows the corresponding state assignment based on the state of the NSLEEPn and their corresponding mask signals using the example PFSM from Figure 8-42.

Table 8-20. NSLEEPn Transitions and Mission State Assignments

Current State	NSLEEP1	NSLEEP2	NSLEEP1 MASK	NSLEEP2 MASK	Trigger to FSM	Next State
DEEP SLEEP/S2R	0	0 → 1	0	0	TRIGGER B	MCU ONLY
DEEP SLEEP/S2R	0 → 1	0 → 1	0	0	TRIGGER A	ACTIVE
DEEP SLEEP/S2R	Don't care	0 → 1	1	0	TRIGGER A	ACTIVE
DEEP SLEEP/S2R or MCU ONLY	0 → 1	Don't care	0	1	TRIGGER A	ACTIVE
MCU ONLY	0 → 1	1	0	0	TRIGGER A	ACTIVE
MCU ONLY	0	1 → 0	0	0	TRIGGER D	DEEP SLEEP or S2R
MCU ONLY	Don't care	1 → 0	1	0	TRIGGER D	DEEP SLEEP or S2R
ACTIVE	1 → 0	1	0	0	TRIGGER B	MCU ONLY
ACTIVE	1 → 0	1 → 0	0	0	TRIGGER D	DEEP SLEEP or S2R
ACTIVE	Don't care	1 → 0	1	0	TRIGGER D	DEEP SLEEP or S2R
ACTIVE	1 → 0	Don't care	0	1	TRIGGER B	MCU ONLY

8.4.1.2.4.4 WKUP1 and WKUP2 Functions

The WKUP1 and WKUP2 functions are activated through the edge detection on all GPIO pins. Any one of these GPIO pins when configured as an input pin can be configured to wake up the device by setting GPIOn_SEL bit to select the WKUP1 or WKUP2 functions. In the example PFSM depicted in Figure 8-42, when a GPIO pin is configured as a WKUP1 pin, a rising or falling edge detected at the input of this pin (configurable by the GPIOn_FALL_MASK and the GPIOn_RISE_MASK bits) wakes up the device to the ACTIVE state. Likewise if a GPIO pin is configured as a WKUP2 pin, a detected edge wakes up the device to the MCU ONLY state. If multiple edge detections of WKUP signals occur simultaneous, the device goes to the state in the following priority order:

1. ACTIVE
2. MCU ONLY

When a valid edge is detected at a WKUP pin, the nINT pin generates an interrupt to signal the MCU of the wake-up event, and the GPIOx_INT interrupt bit is set. The wake request remains active until the GPIOx_INT bit is cleared by the MCU. While the wake request is executing, the device does not react to sleep requests to enter a lower power state until the corresponding GPIOx_INT interrupt bit is cleared to cancel the wake request. After

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the wake request is canceled, the device returns to the state indicated by the NSLEEP1 and NSLEEP2 signals as shown in Table 8-20.

8.4.1.2.4.5 LP_WKUP Pins for Waking Up from LP STANDBY

The LP_WKUP functions are activated through the edge detection of LP_WKUP pins, configurable as secondary functions of GPIO3 and GPIO4. They are specially designed to wake the device up from the LP STANDBY state when a high speed wake-up signal is detected. Similar to the WKUP1 and WKUP2 pins, when GPIO3 or GPIO4 pin is configured as an LP_WKUP1 pin, a rising or falling edge detected at the input of this pin (configurable by the GPIOn_FALL_MASK and the GPIOn_RISE_MASK bits) wakes up the device to the ACTIVE state. Likewise, if the pin is configured as an LP_WKUP2 pin, a detected edge wakes up the device to the MCU ONLY state. If multiple edge detections of LP_WKUP signals occur simultaneously, the device goes to the state in the following priority order:

1. ACTIVE
2. MCU ONLY

Note

Due to a digital control erratum in the device, the ENABLE_MASK/NPWRON_START_MASK bit must be set to '1' before the device enters LP_STANDBY state in order for the LP_WKUP2 pin to correctly wake up the device to the MCU_ONLY state.

The TPS6594-Q1 device supports limited CAN wake-up capability through the LP_WKUP1/2 pins. When an input signal (without deglitch) with logic level transition from high-to-low or low-to-high with a minimum pulse width of $t_{WK_PW_MIN}$ is detected on the assigned LP_WKUP1/2 pins, the device wakes up asynchronously and executes the power up sequence. CAN-transceiver RXD- or INH-outputs can be connected to the LP_WKUP pin. If RXD-output is used, it is assumed that the transceiver RXD-pin IO is powered by the transceiver itself from an external supply when TPS6594-Q1 is in the LP_STANDBY state. If INH-signal is used it has to be scaled down to the recommenced GPIO input voltage level specified in the electrical characteristics table.

In this PFSM example, the device can wake up from the LP_STANDBY state through the detection of LP_WKUP pins only if it enters the LP_STANDBY state through the TRIGGER_I2C_0 OFF request while the NSLEEPn signals are masked, and the on request initialized by the nPWRON/ENABLE pin remains active. Once a valid wake-up signal is detected at the LP_WKUP pin, it is handled as a WAKE request. The nINT pin generates an interrupt to signal the MCU of the wake-up event, and the corresponding GPIOx_INT interrupt bit is set. The wake request remains active until the interrupt bit is cleared by the MCU. Table 8-20 shows how the device returns to the state indicated by the NSLEEP1 and NSLEEP2 signals after the wake request is canceled.

Figure 8-43 illustrates the valid wake-up signal at the LP_WKUP1/2 pins, and the generation and clearing of the internal wake-up signal.

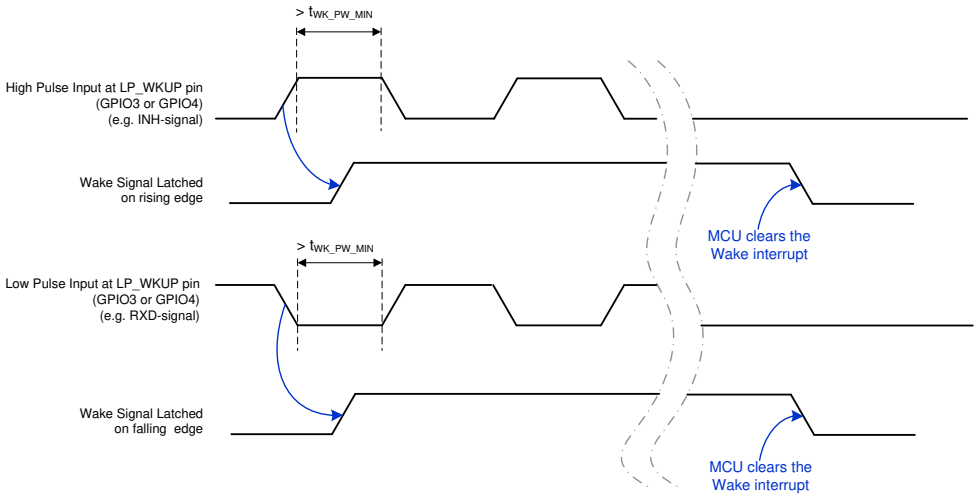

Figure 8-43. CAN Wake-Up Timing Diagram

8.4.1.3 Error Handling Operations

The FSM engine of the TPS6594-Q1 device is designed to handle the following types of errors throughout the operation:

- Power Rail Output Error
- Boot BIST Error
- Runtime BIST Error
- Catastrophic Error
- Watchdog Error
- Error Signal Monitor (ESM) Error
- Warnings

8.4.1.3.1 Power Rail Output Error

A power rail output error occurs when an error condition is detected from the output rails of the device, which are used to power the attached MCU or SoC. These errors include the following:

- Rails not reaching or maintaining within the power good voltage level threshold.
- A short condition that is detected at a regulator output.
- The load current that exceeds the forward current limit.

The BUCKn_GRP_SEL, LDOn_GRP_SEL, and VCCA_GRP_SEL registers are used to configure the rail group for all of the Bucks, LDOs, and the voltage monitors, which are available for external rails. The selectable rail groups are MCU rail group, SoC rail group, or other rail group. The TPS6594-Q1 device is designed to react differently when an error is detected from a power resource assigned to the different rail groups.

Figure 8-40 shows how the SOC_RAIL_TRIG[1:0], MCU_RAIL_TRIG[1:0], and OTHER_RAIL_TRIG[1:0] registers are used as the *Immediate Shutdown Trigger Mask*, *Orderly Shutdown Trigger Mask*, *MCU Power Error Trigger Mask*, or the *SoC Power Error Trigger Mask*. The settings of these register bits determine the error handling sequence which the assigned groups of rails perform in case of an output error. The PFSM engine can be configured to execute the appropriate error handling sequence for the following error handling sequence options: *immediate shutdown*, *orderly shutdown*, *MCU power error*, or *SOC power error*. For example, if an *immediate shutdown* sequence is assigned to the MCU rail group through the MCU_RAIL_TRIG[1:0], any failure detected in this group of rails causes the IMMEDIATE_SHUTDOWN trigger to be executed. This trigger is expected to start the immediate shutdown sequence and cause the device to enter the SAFE RECOVERY state. The device immediately resets the attached MCU and SoC by driving the nRSTOUT and nRSTOUT_SoC (GPO1 or GPIO11) pins low. All of the power resources assigned to the MCU and SOC shut down immediately without a sequencing order. The nINT pin signals that an MCU_PWR_ERR_INT interrupt event has occurred and the EN_DRV pin is forced low. If the error is recoverable within the recovery time interval, the device increments the recovery count, returns to INIT state, and reattempts the power up sequence (if the recovery count has not exceeded the counter threshold). If the recovery count has already exceeded the threshold, the device stays in the SAFE RECOVERY state until VCCA voltage is below the VCCA_UVLO threshold and the device is power cycled.

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The power resources assigned to the SoC rail group are typically assigned to the SOC power error handling sequence. In this PFSM example depicted in Figure 8-42, when a power resource in this group is detected, the PFSM typically causes the device to execute the shutdown of all the resources assigned to the SoC rail group, and the device enters the MCU ONLY state. The device immediately resets the attached SoC by toggling the nRSTOUT_SoC (GPO1 or GPIO11) pin. The reset output to the MCU and the resources assigned to the MCU rail group remain unchanged. The EN_DRV pin also remains unchanged, and the nINT pin signals that an SOC_PWR_ERR_INT interrupt event has occurred. To recover from the MCU_ONLY state after a SOC power error, the MCU software must set NSLEEP1 signal to '0' while NSLEEP2 signal remains '1'. This action signals TPS6594-Q1 that MCU has acknowledged the SOC power error, and is ready to return to normal operation. MCU can then set the NSLEEP1 signal back to '1' for the device to return to ACTIVE state and reattempt the SoC power up. Refer to Section 8.4.1.2.4.3 for information regarding the setting of the NSLEEP1 and NSLEEP2 signals.

8.4.1.3.2 Boot BIST Error

Boot BIST error occurs when the device is not able to pass the BOOT BIST during device power up. Every failure of the BOOT BIST attempt causes the recovery count to increment as the device enters the SAFE RECOVERY state. If the count value is smaller than the counter threshold, the device attempts to enter the INIT state again and reattempts the BOOT BIST until the recovery count reaches the maximum threshold. When this occurs, the device stays in the SAFE RECOVERY state until VCCA voltage is below the VCCA_UVLO threshold and the device is power cycled.

8.4.1.3.3 Runtime BIST Error

Runtime BIST error occurs when the device is not able to pass the Runtime BIST while the device is in an operation state. This error creates an immediate shutdown condition, which causes the device to execute the immediate shutdown sequence and enter the SAFE RECOVERY state. The device immediately resets the attached MCU and SoC by driving the nRSTOUT and nRSTOUT_SoC (GPO1 or GPIO11)) pins low. All of the power resources assigned to the MCU and SOC are immediately shut down. The EN_DRV pin is forced low, and the nINT pin is driven low to signal an interrupt event has occurred.

8.4.1.3.4 Catastrophic Error

Catastrophic errors are errors that affect multiple power resources such as errors detected in supply voltage, LDOVINT supply for control logic, clocks monitors, and device temperature passing the thermal shutdown threshold, or error detected in the SPMI communication network. These errors are grouped as the severe errors. If bits SEVERE_ERR_TRIG[1:0] are set, an immediate or orderly shutdown condition is created. The PFSM executes the corresponding sequence for the IMMEDIATE_SHUTDOWN trigger or the ORDERLY_SHUTDOWN trigger and enters the SAFE RECOVERY state. The device resets the attached MCU and SoC by driving the nRSTOUT and nRSTOUT_SoC (GPO1 or GPIO11) pins low. All of the power resources assigned to the MCU and SOC are shut down. The nINT pin is driven low to signal an interrupt event has occurred, and the EN_DRV pin is forced low.

8.4.1.3.5 Watchdog (WDOG) Error

Section 8.3.11 describes details about the Watchdog (WDOG) errors detection mechanisms.

8.4.1.3.6 Error Signal Monitor (ESM) Error

There are two Error Signal Monitors (ESM) available for the TPS6594-Q1 device, one designed to detect and handle the error signals received from the attached SoC, while the other one for the attached MCU. Section 8.3.12 describes the error detection mechanisms for both monitors in detail.

8.4.1.3.7 Warnings

Warning are non-catastrophic errors. When such an error occurs while the device is in the operating states, the device detects the error and handles the error through the interrupt handler. These are errors such as thermal warnings, I2C, or SPI communication errors, or power resource over current limit detection while the output voltage still maintains within the power good threshold. When these errors occur, the nINT pin is driven low to signal an interrupt event has occurred. The device remains in the operation state and the state of the EN_DRV pin, the power resources, and the reset outputs remain unchanged.

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8.4.1.4 Device Start-up Timing

Figure 8-44 shows the timing diagram of the TPS6594-Q1 after the first supply detection.

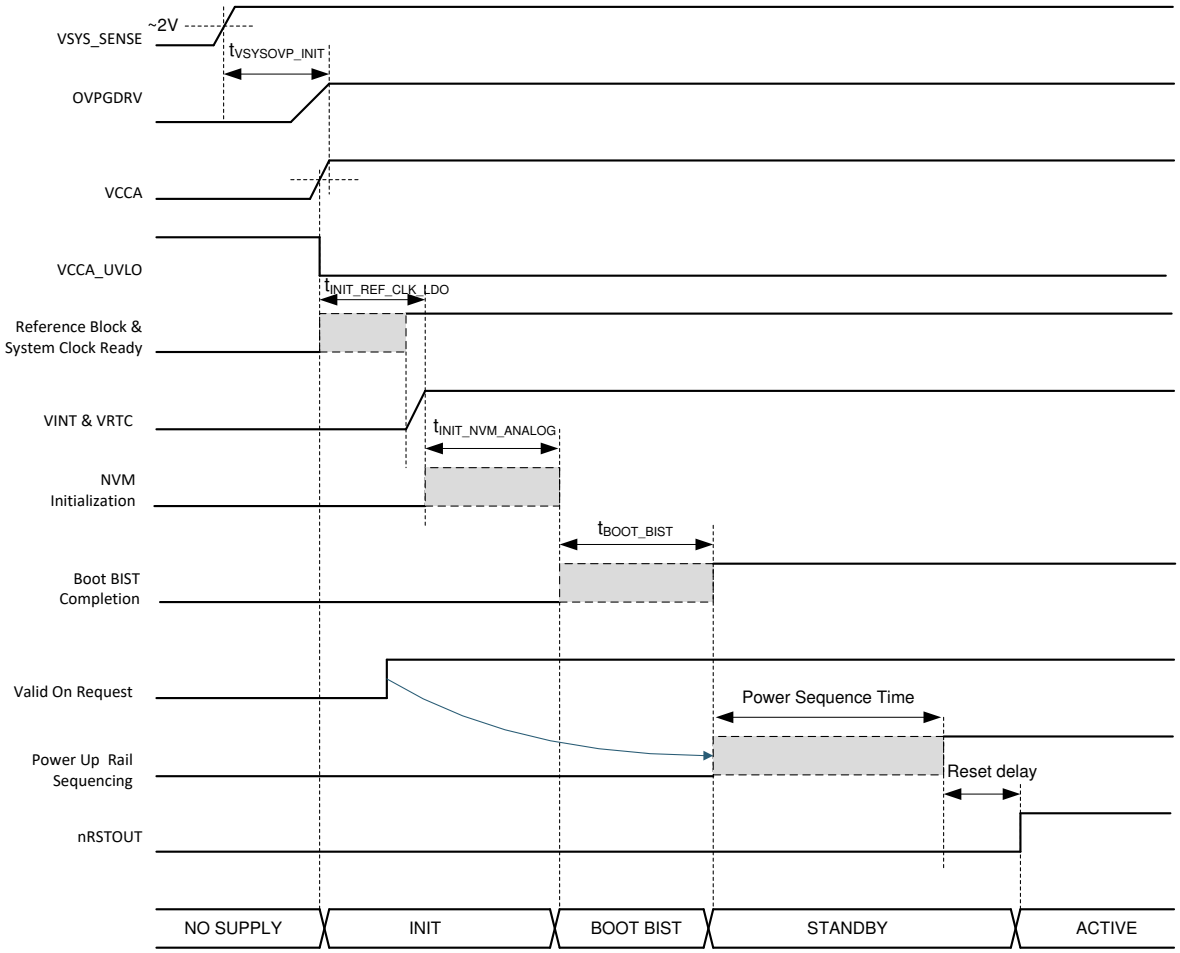

Figure 8-44. Device Start-up Timing Diagram

$t_{VSYSOVP_INIT}$ is the time between VSYS detection and when the VSYS Over Voltage Protection Module is in operation and the external protection FET connects the VSYS_SENSE to VCCA and the PVINx pins.

$t_{INIT_REFCLK_LDO}$ is the start-up time for the reference block. $t_{INIT_NVM_ANALOG}$ is the time for the device to load the default values of the NVM configurable registers from the NVM memory, and the start-up time for the analog circuits in the device. $t_{INIT_REFCLK_LDO}$ and $t_{INIT_NVM_ANALOG}$ are defined in the electrical characteristics table.

t_{BOOT_BIST} is the sum of $t_{ABISTrun}$ and $t_{LBISTrun}$, which are defined in the electrical characterization tables.

The Power Sequence time is the total time for the device to complete the power up sequence. Please refer to Section 8.4.1.5 for more details.

The reset delay time is a configurable wait time for the nRSTOUT and the nRSTOUT_SoC release after the power up sequence is completed.

8.4.1.5 Power Sequences

A power sequence is an automatic preconfigured sequence the TPS6594-Q1 device applies to its resources, which include the states of the BUCKs, LDOs, 32-kHz clock and the GPIO output signals. For a detailed description of the GPIOs signals, please refer to Section 8.3.7.

Figure 8-45 shows an example of a power up transition followed by a power down transition. The power up sequence is triggered through a valid on request, and the power down sequence is trigger by a valid off request.

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The resources controlled (for this example) are: BUCK3, LDO1, BUCK2, LDO2, GPIO1, LDO4, and LDO3. The time between each resource enable and disable (TinstX) is also part of the preconfigured sequence definition.

When a resource is not assigned to any power sequence, it remains in off mode. The MCU can enable and configure this resource independently when the power sequence completes.

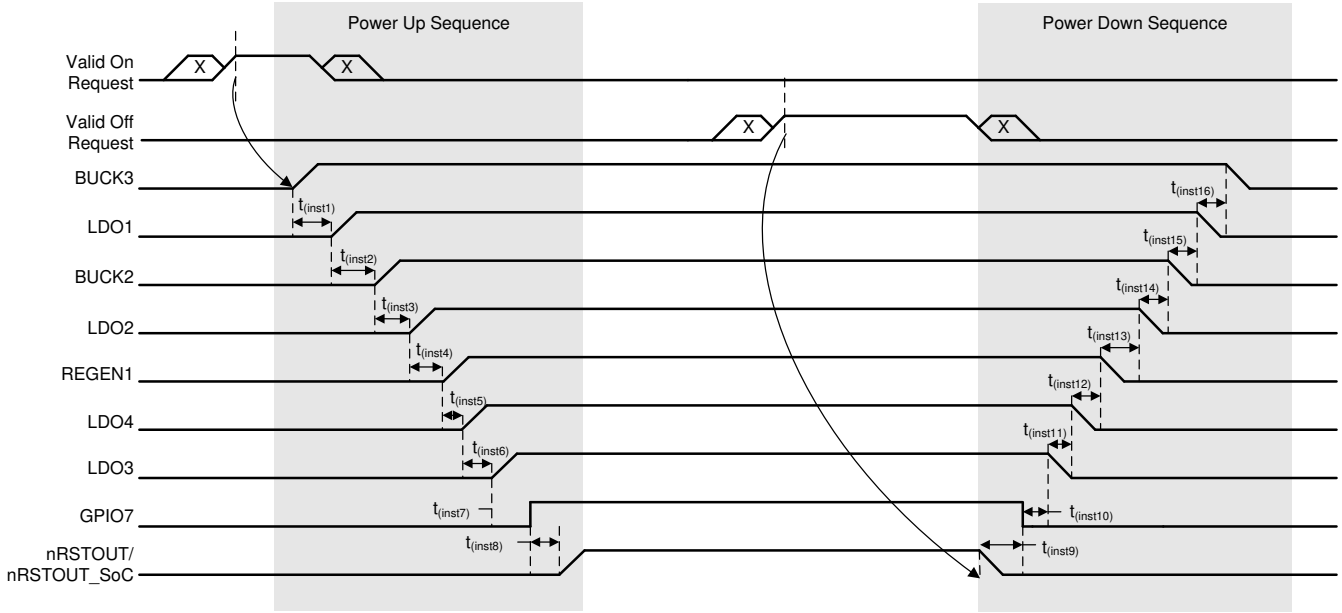

Figure 8-45. Power Sequence Example

As the power sequences of the TPS6594-Q1 device are defined according to the processor requirements, the total time for the completion of the power sequence varies across various system definitions.

8.4.1.6 First Supply Detection

The TPS6594-Q1 device can be configured to automatically start up from a first supply-detection (FSD) event detection. This feature is enabled by setting the FSD_MASK register bit to '0', and setting the NPWRON_SEL[1:0] registers bits to '10' or '11' to mask the functionality of the nPWRON/ENABLE pin. When the device is powered up from the NO SUPPLY state, the FSD detection is validated after the NVM default for this feature is loaded into the device memory.

When the FSD feature is enabled, the PMIC immediately powers up from the NO SUPPLY state to an operation state, configured by the STARTUP_DEST[1:0] bits when VCCA > VCCA_UV, while VCCA_UV gating is performed, and only when VCCA voltage monitoring is enabled (VCCA_VMON_EN = 1). After the device arrives the corresponding STARTUP_DEST[1:0] operation state, the MCU must setup the NSLEEP1 and NSLEEP2 signals accordingly before clearing the FSD_INT interrupt. Once the interrupt is cleared, the device either stays in the current state or moves to the destination state according to the state of the NSLEEP1/2 signals as specified in Table 8-20.

8.4.1.7 Register Power Domains and Reset Levels

The TPS6594-Q1 registers are defined by the following categories:

- LDOVINT registers
- LDOVRTC registers (registers in RTC domain)

LDOVINT registers The LDOVINT registers are powered by the internal LDOVINT, and retain their values until the device enters the LP_STANDBY state or the BACKUP state after the device was fully powered up and in operation. When this occurs, LDOVINT is powered off, all LDOVINT registers (including the VSET registers which store the output voltage levels for all of the external power rails) are reset. As the device re-enters the INIT state from a wake up signal or an On-request, the registers powered by the LDOVINT are re-written with the default values from NVM (Non-Volatile

Memory). All registers in the device, except the LDOVRTC registers (registers in RTC domain), are powered by LDOVINT.

LDOVRTC registers (registers in RTC domain)

The LDOVRTC registers (registers in RTC domain) retain their values until a Power-On-Reset (POR) occurs. POR occurs when the device loses supply power and enters the NO SUPPLY state. When this occurs, LDOVRTC is powered off, and all LDOVRTC registers are reset.

Following are the LDOVRTC registers:

- All RTC registers
- RTC and Crystal Oscillator bits
- Status registers for the following events: TSD and RTC reset
- Control registers for PWRON/ENABLE, GPIO3, and GPIO4 pins (for wake signal monitor during LP_STANDBY state)
- Following interrupt registers:
  - FSD_INT
  - RECOV_CNT_INT
  - TSD_ORD_INT
  - TSD_IMM_INT
  - PFSM_ERR_INT
  - VCCA_OVP_INT
  - ESM_MCU_RST_INT
  - ESM_SOC_RST_INT
  - WD_RST_INT
  - WD_LONGWIN_TIMEOUT_INT
  - NPWRON_LONG_INT

8.4.2 Multi-PMIC Synchronization

A multi-PMIC synchronization scheme is implemented in the TPS6594-Q1 device to synchronize the power state changes with other PMIC devices. This feature consolidates and simplifies the IO control signals required between the application processor or the microcontroller and multiple PMICs in the system. The control interface consists of an SPMI protocol which communicates the next power state information from the primary PMIC to up to 5 secondary PMICs, and receives feedback signal from the secondary PMICs to indicate any error condition. Figure 8-46 is the block diagram of the power state synchronization scheme. The primary PMIC in this block diagram is responsible for broadcasting the synchronous system power state data, and processing the error feedback signals from the secondary PMICs. The primary PMIC is the *controller* device on the SPMI bus, and the secondary PMICs are the *target* devices on the SPMI bus.

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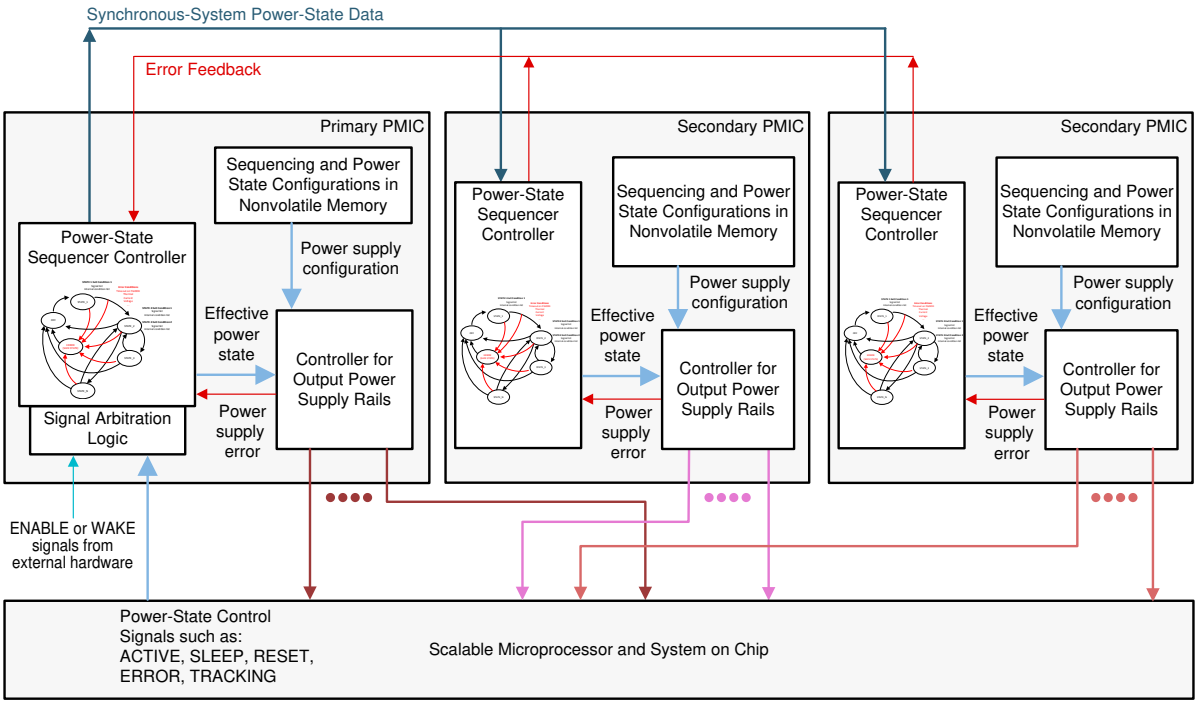

Figure 8-46. Multi-PMIC Power State Synchronization Block Diagram

In this scheme, each primary and secondary PMIC runs on its own system clock, and maintains its own register map. Each PMIC monitors its own activities and pulls down the open-drain output of nINT or PGOOD pin when errors are detected. The microprocessor must read the status bits from each PMIC device through the I2C or SPI interface to find out the source of the error that is reported.

To synchronize the timing when entering and exiting from the LP_STANDBY state, the VOUT_LDOVINT of the TPS6594-Q1 device must be connected to the ENABLE input of the secondary PMICs, which are the target devices in the SPMI interface bus. Figure 8-47 illustrates the pin connections between the primary, the secondary, and the application processor or the System-on-Chip.

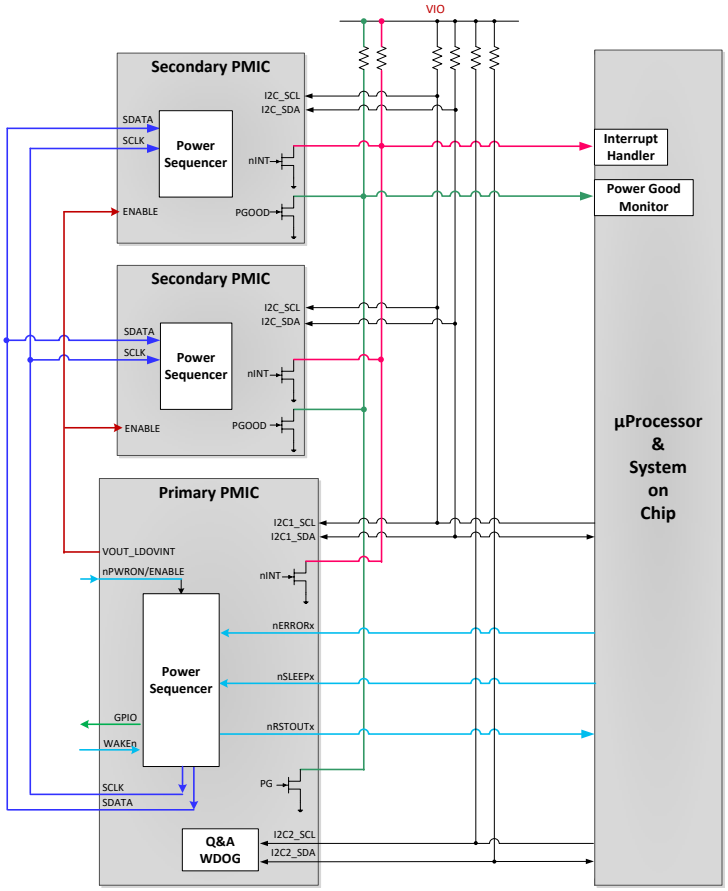

Figure 8-47. multi-PMIC Pin Connections

The power sequencer of the multiple PMICs are synchronized at the beginning of each power up and power down sequence; a variation in the sequence timing, however, is still possible due to the ±5% clock accuracy of the independent system clocks on the primary and secondary PMICs. The worst-case sequence timing variation from different PMIC rails is up to ±10% of the target delay time. Figure 8-48 illustrates the creation of this timing variation between PMICs.

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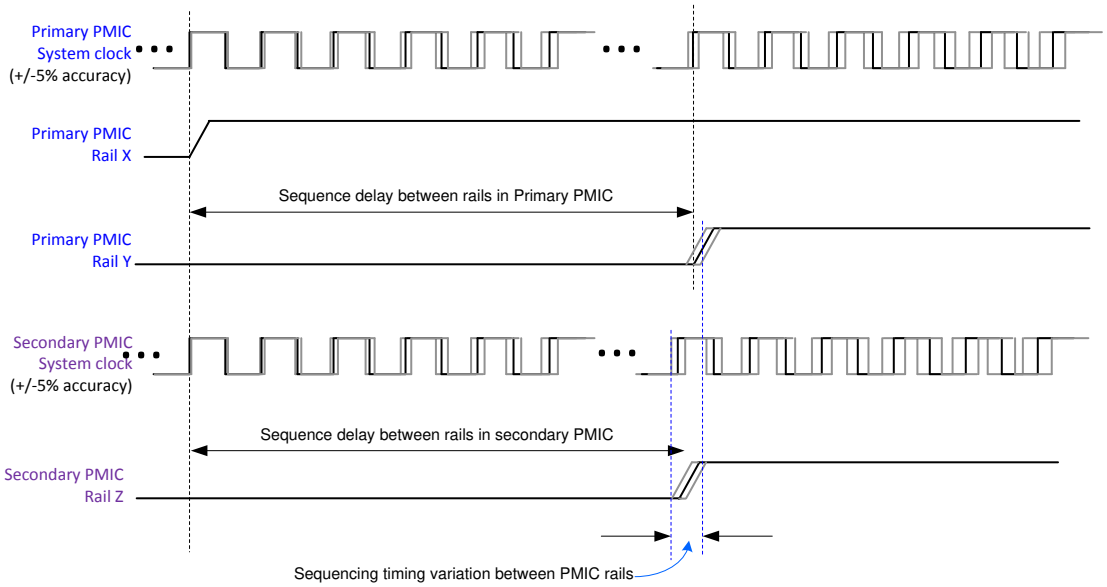

Figure 8-48. Multi-PMIC Rail Sequencing Timing Variation

8.4.2.1 SPMI Interface System Setup

An SPMI interface in the TPS6594-Q1 device is utilized to communicate the power state transition across multiple PMICs in the system. The SPMI interface contains a *controller* block and a *target* block. There is only one PMIC, which is the primary PMIC, that acts as SPMI controller in any given system. As the SPMI controller it initiates SPMI interface BIST and executes periodic checking of the SPMI bus health.

The primary PMIC has a controller-ID (CID)= 1. The target block of SPMI interfac in the primary PMIC device is activated as well, in order to receive SPMI communication messages from the secondary PMICs. The primary PMIC has a target-ID (TID) = 0101.

Each secondary PMIC on the SPMI network only has the target block of its SPMI interface enabled. There cannot be more than five secondary PMICs in the system. The target-IDs (TIDs) for the five secondary PMICs are:

- 1st target device: 0011
- 2nd target device: 1100
- 3rd target device: 1001
- 4th target device: 0110
- 5th target device: 1010

All devices in the SPMI network listen to the group target-ID (GTID): 1111. This address is used to communicate all power state transition information in broadcast mode to all connected devices on the SPMI bus.

8.4.2.2 Transmission Protocol and CRC

The communication between the devices on the network utilizes Extended Register Write command to GTID address *1111* with byte length of 2. Sequence format complies with MIPI SPMI 2.0 specification. First data frame carries the data payload of 5 bits and 3 filler bits.

Communication over the SPMI interface may contain information regarding the power state transition or the unique TID of one or more target devices. In the case of power state information, the data payload contains 5 bits of Trigger ID information and 3 trigger state bits. In the case of TID information, all 8 bits contain the TID of the target device.

Second data frame carries 8 bits of CRC information. CRC polynomial used is $X^8 + X^2 + X + 1$. CRC is calculated over the SPMI command frame, the address frame, and the first data frame (which contains the payload and excludes the parity bits in these three frames).

Figure 8-49 shows the data format of the SPMI Extended Register Write Command.

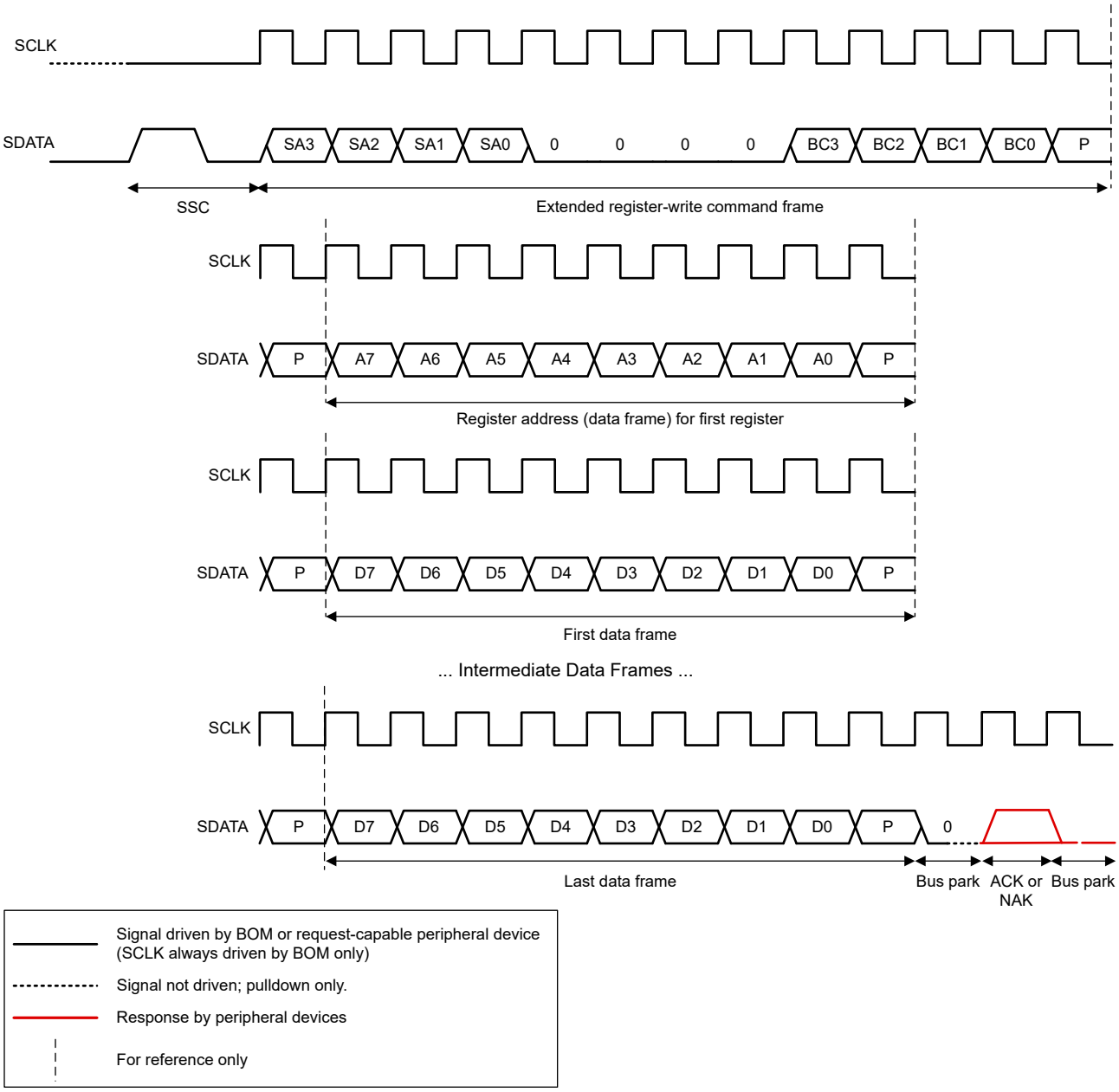

Figure 8-49. SPMI Extended Register Write Command

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8.4.2.2.1 Operation with Transmission Errors

If the receiving device detects a parity or CRC error in the incoming sequence it responds with negative ACK/NACK per SPMI standard.

If the transmitting device sees NACK response, it tries to resend the message as many times as indicated by SPMI_RETRY_LIMIT register bits. After that it considers the SPMI bus inoperable, sets SPMI_ERR_INT interrupt and goes to the safe recovery state and executes an orderly shutdown. Bus arbitration requests do not count as failed attempts if a target device loses bus arbitration. SPMI_RETRY_LIMIT counter is reset after each successful transmission by the device.

If a target device has determined that SPMI does not work reliably it does not respond to any SPMI commands anymore until power-on-reset event has occurred. This "no-response" behavior is to prevent continued operation in a situation where SPMI is unreliable. If a target device does no longer respond to any SPMI command, the controller device on the SPMI bus detects a missing target device on the network during the periodic testing of SPMI bus. The target device then internally handles the SPMI error condition per error handling rules set for the device (in general executing an orderly shutdown). SPMI block signals to the device that SPMI bus error has occurred after the retry limit has been exceeded.

8.4.2.2.2 Transmitted Information

The SPMI bus is used to carry two types of information:

- PFSM Trigger ID between the SPMI controller and target devices
- TID from SPMI target devices to SPMI controller device

The SPMI controller device reads the TID of the target devices periodically to check the health of the interface. Exchanging Trigger IDs for the power state transition is sufficient to keep the PFSMs of all the devices on the SPMI network in synchronization. Device interrupts provides insights to the reason which cause power state transitions.

8.4.2.3 SPMI Target Device Communication to SPMI Controller Device

An SPMI target device communicates to the SPMI controller device and any other SPMI target devices, only if there is an internal error, which is not SPMI related. The target device initiates the error communication using Arbitration Request with A-bit as defined in the SPMI 2.0 specification. SPMI 2.0 protocol manages the situation with multiple target devices requesting error communication at the same time, by using the target arbitration process as described in SPMI 2.0 specification. Once the SPMI target device wins the arbitration using the A-bit protocol, it performs an Extended Register Write command to Group Target ID (GTID) address *1111* by using the protocol described in Section 8.4.2.2 for communicating PFSM trigger ID.

8.4.2.3.1 Incomplete Communication from SPMI Target Device to SPMI Controller Device

In case the SPMI controller device detects an arbitration request on the SPMI interface, but the received sequence has an error or is incomplete, the SPMI controller device immediately performs the SPMI Built-In Self-Test (SPMI-BIST). If this SPMI-BIST fails, the SPMI controller device executes the error handling for the SPMI error. If the SPMI-BIST passes successfully, the SPMI controller device resumes normal operation.

8.4.2.4 SPMI-BIST Overview

The SPMI-BIST is performed during BIST state and regularly during runtime operation. Figure 8-50 below illustrates how the SPMI-BIST operates during device power-up.

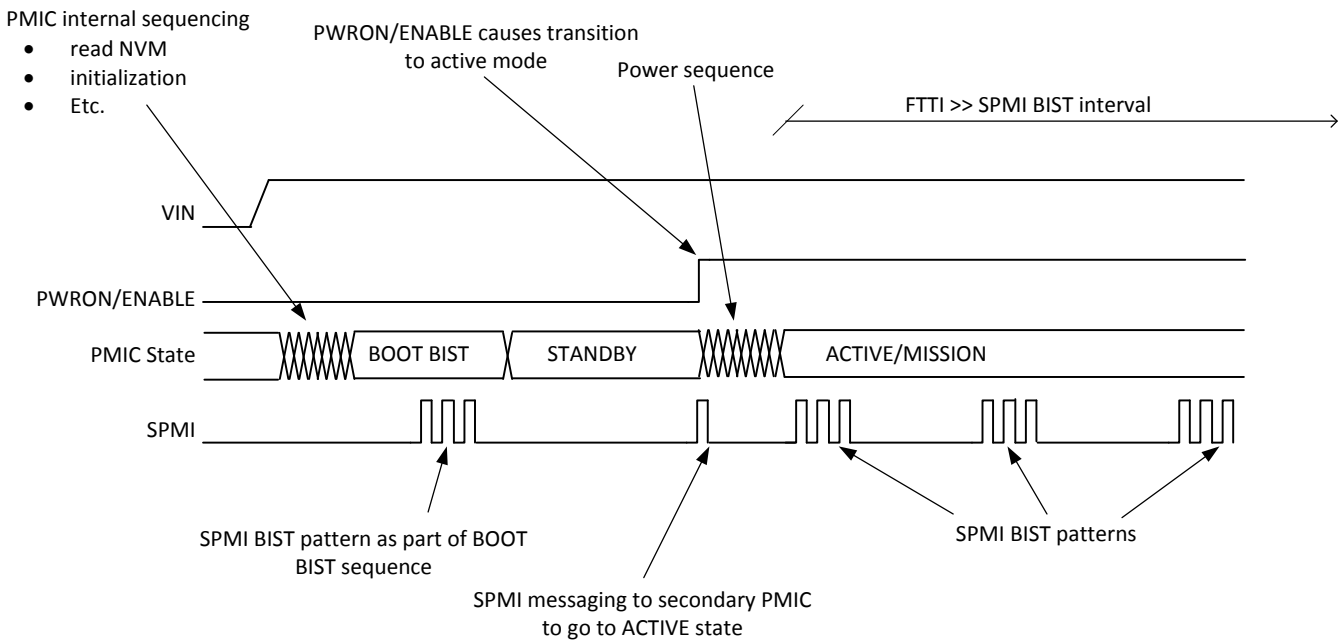

Figure 8-50. SPMI-BIST Operation

After the input power is detected and verified to be at the correct level, the TPS6594-Q1 initializes itself by reading the NVM and performs all actions that are needed to prepare for operation . After this initialization, the TPS6594-Q1 enters the BOOT BIST state, in which the internal logic performs a series of tests to verify that the TPS6594-Q1 device is OK. As part of this test, the SPMI- BIST is performed. After it is completed successfully, the TPS6594-Q1 device goes to the standby state and waits for further signals from the system to initiate the power-up sequence of the processor.

A valid on request initiates the processor power-up sequence. The controller device communicates this event through the SPMI bus to all of the target devices. After that, the power-up sequence is executed and TPS6594-Q1 enters the configured mission state.

8.4.2.4.1 SPMI Bus during Boot BIST and RUNTIME BIST

During Boot BIST and RUNTIME BIST, both the Logic BIST (LBIST) on the SPMI logic and the SPMI-BIST are performed to check correct operation of the SPMI bus. The LBIST is performed first before the SPMI-BIST during BOOT BIST and RUNTIME BIST. The SPMI-BIST is implemented by reading TID from each target device on the SPMI bus into the controller device, and ensuring they are unique and match the expected amount of target devices. This process of checking the TID of each target device ensures that:

- All SPMI target devices are present in the system as expected
- The SPMI logic blocks are working on the SPMI controller device and all of the SPMI target devices
- The pins and wires on the ICs and PCB are in working order

The SPMI-BIST is initiated by the SPMI controller block in the primary PMIC by writing a request to all SPMI target device(s) (using GTID) to send their TIDs to the SPMI controller block of the primary PMIC. Upon receiving this command from the SPMI controller device, the SPMI target devices request SPMI bus arbitration using the SR-bit protocol. Upon winning the bus arbitration the SPMI target devices transmit their TID into the SPMI target block of the primary PMIC.

The SPMI controller block of the primary PMIC contains a list of all SPMI target device(s) on the SPMI bus and their TIDs in the register set. The SPMI controller block of the primary PMIC reads the TID from each SPMI target device and compares the result with the stored TID for the corresponding SPMI target device. The SPMI controller device has to ensure that every non-zero TID on its list is returned, in order to support use cases in which there are two or more identical SPMI target devices, with same TID, in the system. In these cases, it is mandatory that the expected number of the same TIDs is returned. If no identical PMICs are to be used, then a return of the same TID multiple times is an error due to incorrect assembly of identical PMICs onto the PCB. An

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all-zero TID stored in the list of the primary PMIC indicates that there are no SPMI target device(s) present on the SPMI Bus.

8.4.2.4.2 Periodic Checking of the SPMI

The SPMI controller block in the primary PMIC executes the SPMI-BIST periodically while device is operating. The time-period after which the SPMI-BIST is repeated according factory-configured settings during the device boot time, and after the device reaches mission states. The factory-configured settings of this SPMI-BIST time period must be the same for all PMICs on the same SPMI network. The SPMI target devices on the SPMI bus expect a request for sending its TID from the SPMI controller device within 1.5x the factory-configured period . This factor 1.5x provides enough margin for clock uncertainty between the SPMI controller device and the SPMI target device.

During mission state operation, the SPMI controller device expects the SPMI target devices to respond to the TID request within the factory-configured polling time-out period . In other words, from the polling start command each SPMI target device must respond within this factory-configured time interval.

During boot time or when the device enters Safe Recovery state, to prevent the SPMI controller device from polling the SPMI target devices too often while one or more of these recovering from a system error such as a thermal shutdown event, the device sets a longer timeout period which allows the SPMI target devices to respond to the SPMI controller device before he SPMI controller device reports an error.

If one or more devices on the SPMI bus cause a violating of the polling time-out period either during start-up or during normal operation, the SPMI controller block in the affected PMIC(s) sets a SPMI error trigger signal to the PFSM of the affected PMIC(s), causing a complete shutdown of the affected PMIC(s). As a result, the affected PMIC(s) no longer respond on the SPMI bus, which in turn is detected by the SPMI controller block off the non-affected PMICs on the SPMI bus. The SPMI controller block in these PMICs sets an SPMI error to the PFSM in these PMICs, causing a complete shutdown of these PMICs. Therefore, all PMICs are finally shutdown if one or more devices on the SPMI bus cause a violating of the polling time-out period .

8.4.2.4.3 SPMI Message Priorities

The SPMI Bus uses the protocol priority levels listed in Table 8-21 for each type of communication message.

Table 8-21. SPMI Message Types and Priorities

SPMI protocol priority level	Name of priority level in SPMI standard	Message types
Highest	A-bit arbitration	State transition messages from target device(s) to controller device
	priority arbitration	State transition messages from controller device to target device(s)
	SR-bit arbitration	target device TID to controller device
Lowest	secondary arbitration	Controller device request of TIDs from target device(s)

8.5 Control Interfaces

The device has two, exclusive selectable (from factory settings) interfaces. Please refer to the User's Guide of the orderable part number which option has been selected. The first selection is up to two high-speed I^2C interfaces. The second selection is one SPI interface. The SPI and I2C1 interfaces are used to fully control and configure the device, and have access to all of the configuration registers and Watchdog registers. During normal operating mode, when the I^2C configuration is selected, and GPIO1 and GPIO2 pins can be configured as the SCL_I2C2 and SDA_I2C2 pins, the I2C2 interface becomes the dedicated interface for the Q&A Watchdog communication channel, while I2C1 interface no longer has access to the Watchdog registers. The I2C2 interface is automatically disabled and has access to all of the registers, including the Watchdog registers, when the device enters the NVM programing mode.

8.5.1 CRC Calculation for I^2C and SPI Interface Protocols

For safety applications, the TPS6594-Q1 supports read and write protocols with embedded CRC data fields. The TPS6594-Q1 uses a standard CRC-8 polynomial to calculate the checksum value: $X^8 + X^2 + X + 1$. The CRC algorithm details are as follows:

- Initial value for the remainder is all 1s
- Big-endian bit stream order
- Result inversion is enabled

For I^2C Interface, the TPS6594-Q1 uses the above mentioned CRC-8 polynomial to calculate the checksum value on every bit except the ACK and NACK bits it receives from the MCU during a write protocol. The TPS6594-Q1 compares this calculated checksum with the R_CRC checksum value which it receives from the MCU. The TPS6594-Q1 also uses the above mentioned CRC-8 polynomial to calculate the R_CRC checksum value based on every bit except the ACK and NACK bits, which the TPS6594-Q1 transmits to the MCU during a read protocol. The MCU must use this same CRC-8 polynomial to calculate the checksum value based on the bits, which the MCU receives from the TPS6594-Q1. The MCU must compare this calculated checksum with the T_CRC checksum value which it receives from the TPS6594-Q1.

For the SPI interface, the TPS6594-Q1 uses the above mentioned CRC-8 polynomial to calculate the checksum value on every bit it receives from the MCU during a write protocol. The TPS6594-Q1 compares this calculated checksum with the R_CRC checksum value, which it receives from the MCU. During a read protocol, the device also uses the above mentioned CRC-8 polynomial to calculate the T_CRC checksum value based on the first 16 bits sent by the MCU, and the next 8 bits the TPS6594-Q1 transmits to the MCU. The MCU must use this same CRC-8 polynomial to calculate the checksum value based on the bits which the MCU sends to and receives from the TPS6594-Q1, and compare it with the T_CRC checksum value which it receives from the TPS6594-Q1.

Figure 8-51 and Figure 8-52 are examples for the 8-bit R_CRC and the T_CRC calculation from 16-bit databus.

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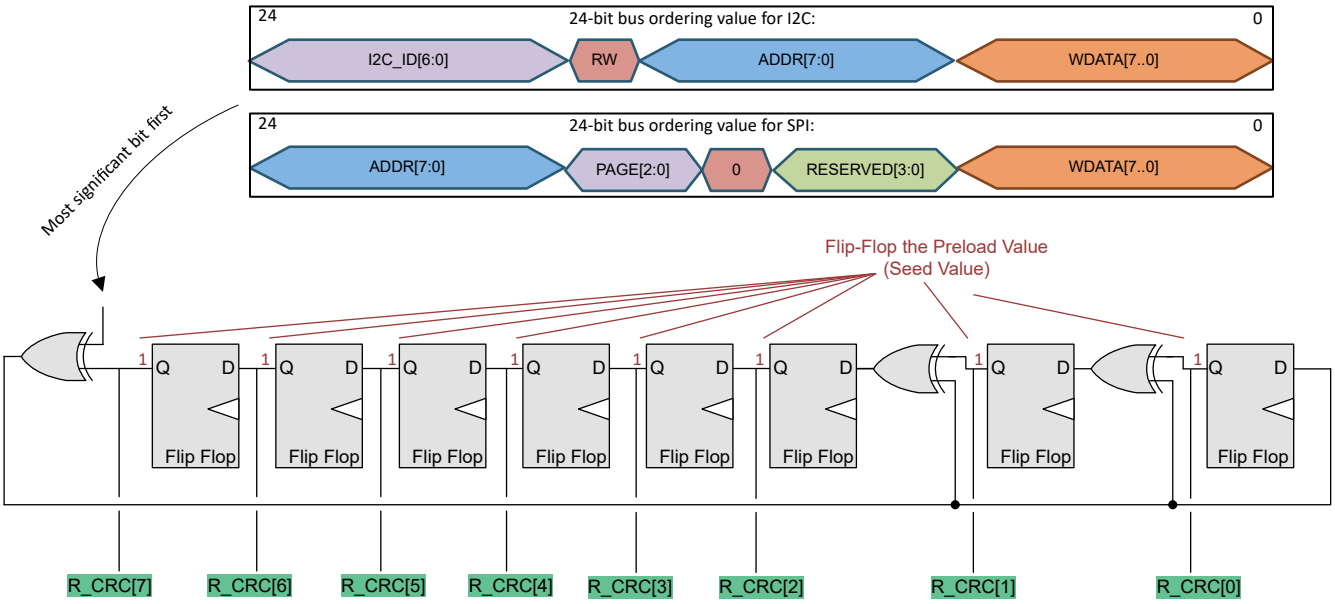

Figure 8-51. Calculation of 8-Bit CRC on Received Data (R_CRC)

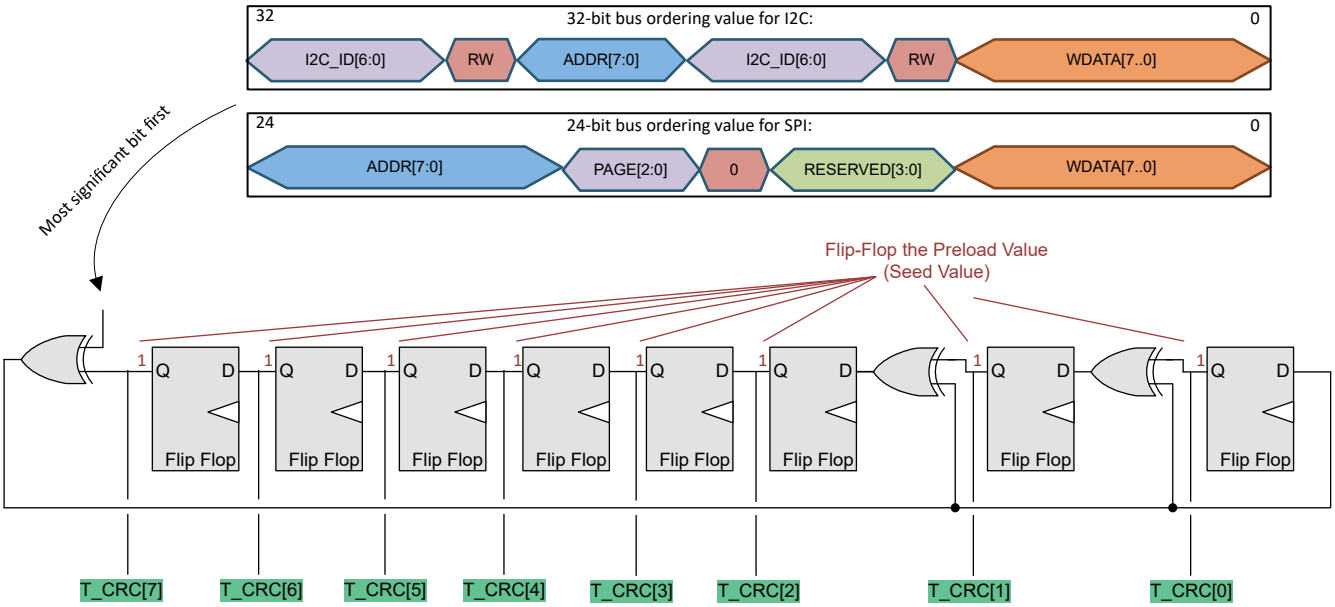

Figure 8-52. Calculation of 8-Bit CRC on Transmitted Data (T_CRC)

8.5.2 I²C-Compatible Interface

The default I²C1 7-bit device address of the TPS6594-Q1 device is set to a binary value which is described in the User's Guide of the orderable part number of the TPS6594-Q1 PMIC, while the two least-significant bits can be changed for alternative page selection listed under Section 8.6.1. The default 7-bit device address for the I²C2 interface, for accessing the watchdog configuration registers and for operating the watchdog in Q&A mode, is described in the User's Guide of the orderable part number of the TPS6594-Q1 PMIC.

The I²C-compatible synchronous serial interface provides access to the configurable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a controller or a target depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle. The device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode plus (1 MHz) when VIO is 3.3 V or 1.8 V, and high-speed mode (3.4 MHz) only when VIO is 1.8 V.

8.5.2.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when clock signal is LOW.

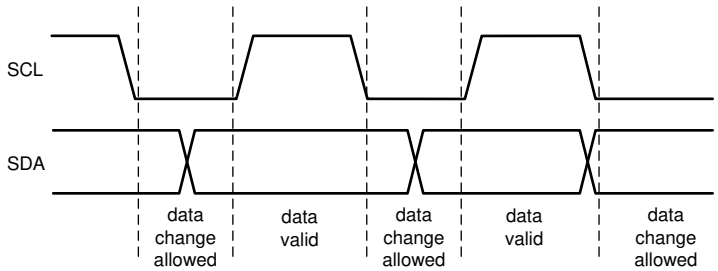

Figure 8-53. Data Validity Diagram

8.5.2.2 Start and Stop Conditions

The device is controlled through an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as the SDA signal going from HIGH to LOW while the SCL signal is HIGH. A STOP condition is defined as the SDA signal going from LOW to HIGH while the SCL signal is HIGH. The I²C controller device always generates the START and STOP conditions.

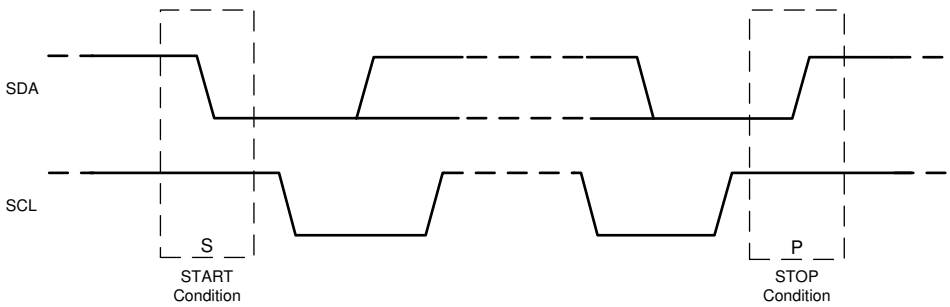

Figure 8-54. Start and Stop Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. The I²C controller can generate repeated START conditions during data transmission. A START and a repeated START condition are equivalent function-wise. Figure 8-55 shows the SDA and SCL signal timing for the I²C-compatible bus. For timing values, see the *Specification* section.

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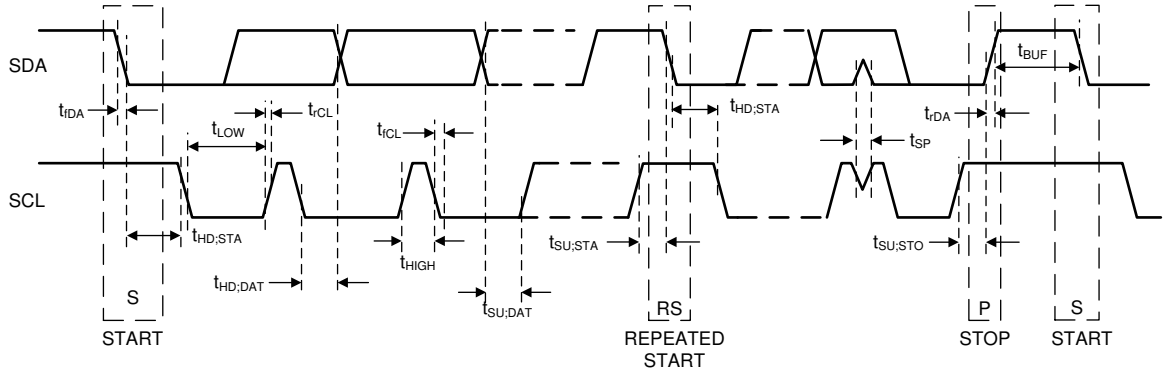


Figure 8-55. I²C-Compatible Timing

8.5.2.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the I²C controller. The controller releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the *acknowledge after every byte* rule. When the controller is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*) the last byte clocked out of the target. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the controller), but the SDA line is not pulled down.

After the START condition, the bus controller sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE and a 1 indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register. Figure 8-56 shows an example bit format of device address 110000-Bin = 60Hex.

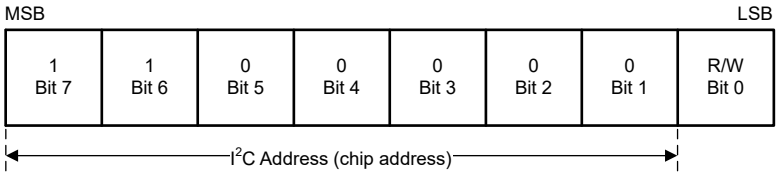


Figure 8-56. Example Device Address

For safety applications, the device supports read and write protocols with embedded CRC data fields. In a write cycle, the I²C controller device (i.e. the MCU) must provide the 8-bit CRC value after sending the write data bits and receiving the ACK from the target. The CRC value must be calculated from every bit included in the write protocol except the ACK bits from the target. See CRC Calculation for I2C and SPI Interface Protocols. In a read cycle, the I²C target must provide the 8-bit CRC value after sending the read data bits and the ACK bit, and expect to receive the NACK from the controller at the end of the protocol. The CRC value must be calculated from every bit included in the read protocol except the ACK and NACK bits. See CRC Calculation for I2C and SPI Interface Protocols.

Note

If I2C CRC is enabled in the device and an I2C write without R_CRC bits is done, the device does not process the write request. The device does not set any interrupt bit and does not pull the nINT pin low.

The embedded CRC field can be enabled or disabled from the protocol by setting the I2C1_SPI_CRC_EN (for I2C1) or I2C2_CRC_EN (for I2C2) register bit to '1' - enabled, '0' - disabled. The default of this bit is configurable through the NVM.

In case the calculated CRC-value does not match the received CRC-check-sum, an I²C-CRC-error is detected, the COMM_CRC_ERR_INT (for I2C1) or I2C2_CRC_ERR_INT (for I2C2) bit is set, unless it is masked by the COMM_CRC_ERR_MASK or I2C2_CRC_ERR_MASK bit. The MCU must clear this bit by writing a '1' to the COMM_CRC_ERR_INT (for I2C1) or I2C2_CRC_ERR_INT (for I2C2) bit.

When the CRC field is enabled, in the case when MCU attempts to write to a read-only register or a register-address that does not exist, the device sets the COMM_ADR_ERR_INT (for I2C1) or I2C2_ADR_ERR_INT (for I2C2) bit, unless the COMM_ADR_ERR_MASK or I2C2_ADR_ERR_MASK bit is set. The MCU must clear this bit by writing a '1' to the COMM_ADR_ERR_INT (for I2C1) or I2C2_ADR_ERR_INT (for I2C2) bit.

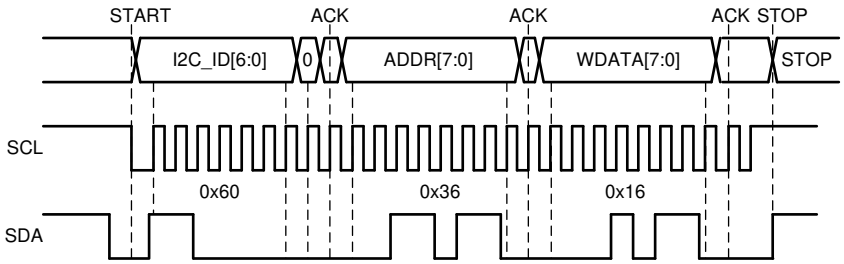
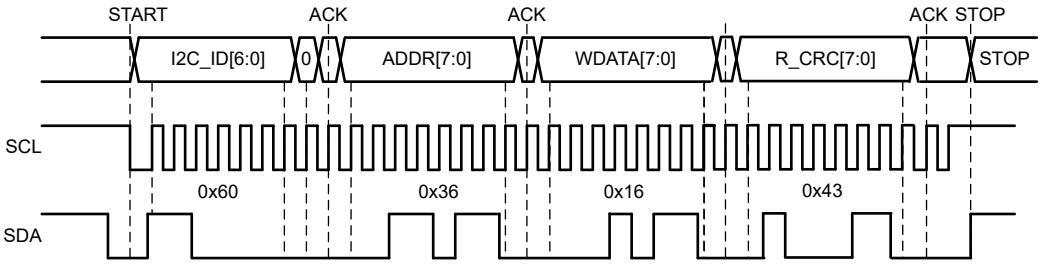
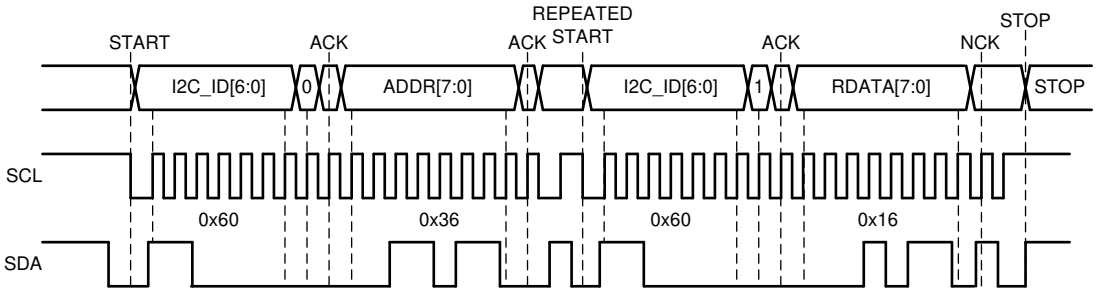


Figure 8-57. I²C Write Cycle without CRC



The I²C controller device (i.e. the MCU) provides R_CRC[7:0], which is calculated from the I2C_ID, R/W, ADDR, and the WDATA bits (24 bits). See CRC Calculation for I2C and SPI Interface Protocols.

Figure 8-58. I²C Write Cycle with CRC



When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

Figure 8-59. I²C Read Cycle without CRC

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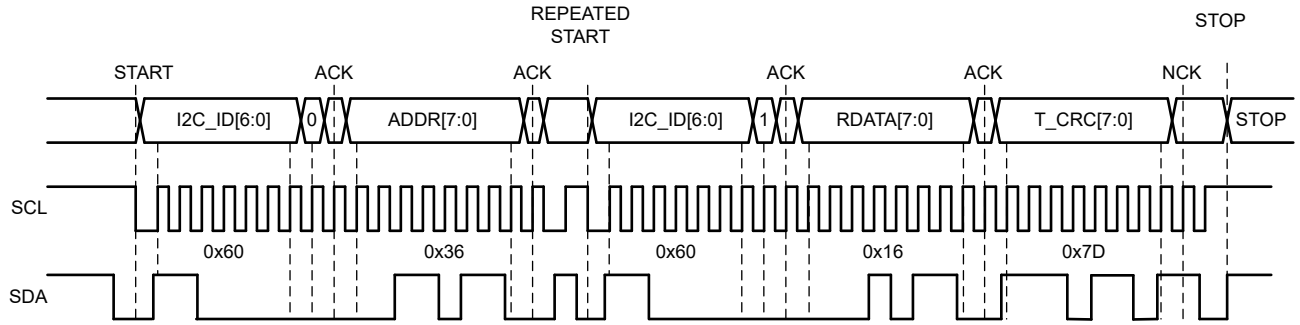

The I²C target device (i.e. the TPS6594-Q1) provides T_CRC[7:0], which is calculated from the I2C_ID, R/W, ADDR, I2C_ID, R/W, and the RDATA bits (32 bits). See CRC Calculation for I2C and SPI Interface Protocols.

Figure 8-60. I²C READ Cycle with CRC

8.5.2.4 Auto-Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the device, the internal address index counter is incremented by one and the next register is written. Table 8-22 lists the writing sequence to two consecutive registers. Note that auto increment feature does not support CRC protocol.

Table 8-22. Auto-Increment Example

ACTION	START	DEVICE ADDRESS = 0x60	WRITE		REGISTER ADDRESS		DATA		DATA		STOP
PMIC device				ACK		ACK		ACK		ACK	

8.5.3 Serial Peripheral Interface (SPI)

The device supports SPI serial-bus interface and it operates as a peripheral device. The MCU in the system acts as the controller device. A single read and write transmission consists of 24-bit write and read cycles (32-bit if CRC is enabled) in the following order:

- Bits 1-8: ADDR[7:0], Register address
- Bits 9-11: PAGE[2:0], Page address for register
- Bit 12: Read/Write definition, 0 = WRITE, 1 = READ.
- Bits 13-16: RESERVED[4:0], Reserved, use all zeros.
- For Write: Bits 17-24: WDATA[7:0], write data
- For Write with CRC enabled: Bits 25-32: R_CRC[7:0], CRC error code calculated from bits 1-24 sent by the controller device (i.e. the MCU). See Section 8.5.1.
- For Read: Bits 17-24: RDATA[7:0], read data
- For Read with CRC enabled: Bits 25-32: T_CRC[7:0], CRC error code calculated from bits 1-16 sent by the controller device (i.e. the MCU), and bits 17-24, sent by the peripheral device (i.e. the TPS6594-Q1). See Section 8.5.1.

The embedded CRC filed can be enabled or disabled from the protocol by setting the I2C1_SPI_CRC_EN register bit to '1' - enabled, '0' - disabled. The default of this bit is configurable through the NVM.

The SDO output is in a high-impedance state when the CS pin is high. When the CS pin is low, the SDO output is always driven low except when the RDATA or SCRC bits are sent. When the RDATA or SCRC bits are sent, the SDO output is driven accordingly.

The address, page, data, and CRC are transmitted MSB first. The chip-select signal (CS) must be low during the cycle transmission. The CS signal resets the interface when it is high, and must be taken high between successive cycles. Data is clocked in on the rising edge of the SCLK clock signal and it is clocked out on the falling edge of SCLK clock signal.

The *SPI Timing* diagram shows the timing information for these signals.

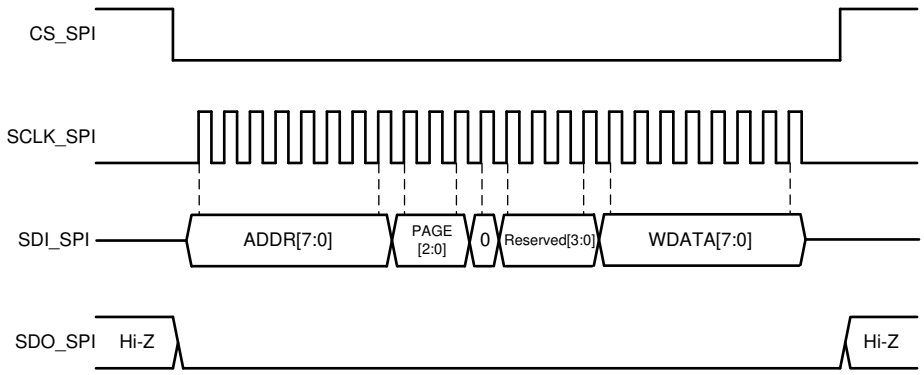

Figure 8-61. SPI Write Cycle

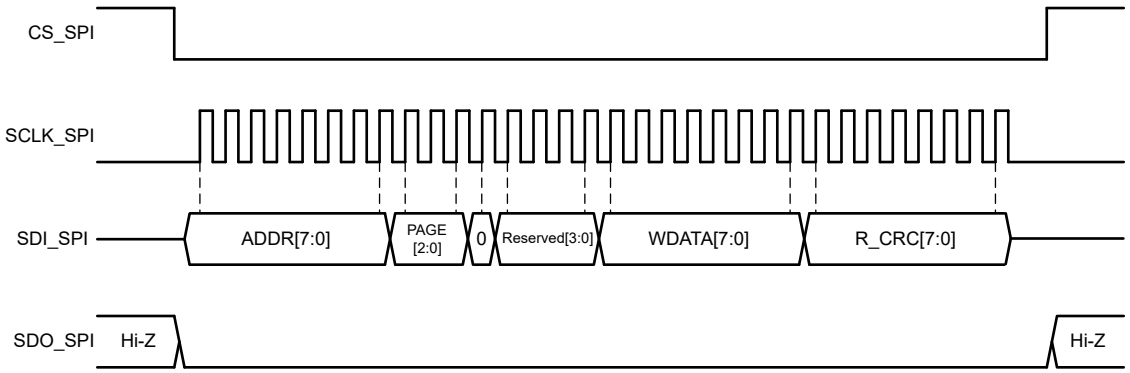

Figure 8-62. SPI Write Cycle with CRC

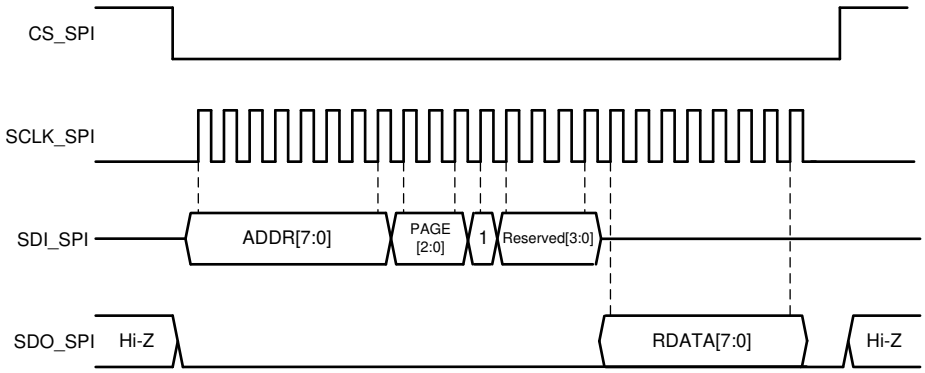

Figure 8-63. SPI Read Cycle

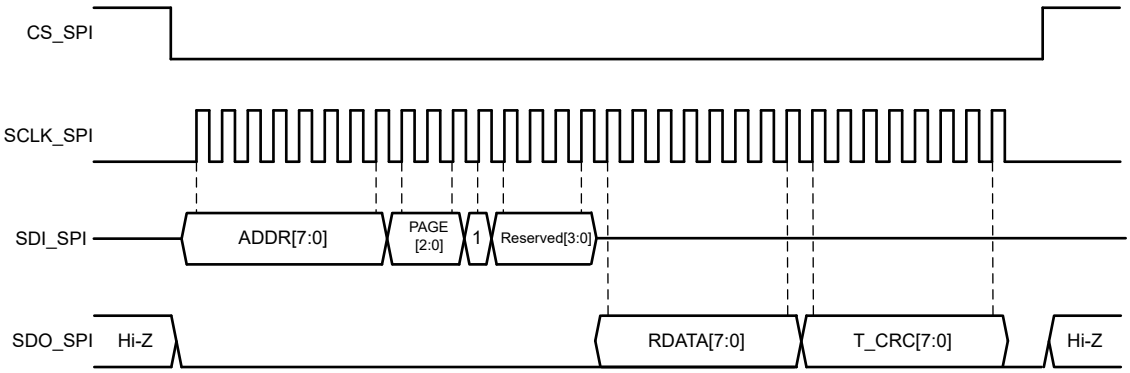

Figure 8-64. SPI Read Cycle with CRC

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Note

Due to a digital control erratum in the device, the TPS6594-Q1 pulls the nINT pin low and sets interrupt bit COMM_FRM_ERR_INT if the pin CS_SPI is low during device power-up and goes high afterwards. After system startup, the MCU must clear this COMM_FRM_ERR_INT bit such that the TPS6594-Q1 can release the nINT pin.

8.6 Configurable Registers

8.6.1 Register Page Partitioning

The registers in the TPS6594-Q1 device are organized into five internal pages. Each page represents a different type of register. The below list shows the pages with their register types:

- Page 0: User Registers
- Page 1: NVM Control, Configuration, and Test Registers
- Page 2: Trim Registers
- Page 3: SRAM for PFSM Registers
- Page 4: Watchdog Registers

Note

When I^2C Interfaces are used, each of the above listed register pages has its own 7-bit I^2C device address. The I^2C device address for Page 0 is according register bits I2C1_ID, for Page 1 the I^2C device address is I2C1_ID + 1, for Page 2 the I^2C device address is I2C1_ID + 2, and for Page 3 the I^2C device address is I2C1_ID + 3. For Page 4 the I^2C device address is according register bits I2C2_ID. Therefore, in case both I^2C1 and I^2C2 Interfaces are used, each TPS6594-Q1 device occupies four I^2C device addresses (for Page 0, Page 1, Page 2 and Page 3) on the I^2C1 bus and one I^2C device address (for Page 4) on the I^2C2 bus. And in case only I^2C1 Interfaces is used, each TPS6594-Q1 device occupies five I^2C device addresses (for Page 0, Page 1, Page 2, Page 3 and Page 4) on the I^2C1 bus. In case multiple devices are used on a common I^2C bus, care must be taken to avoid overlapping I^2C device addresses.

Note

When SPI Interface is used, the above listed register pages are addresses with the PAGE[2:0] bits: 0x0 addresses Page 0, 0x1 addresses Page 1, 0x2 addresses Page 2, 0x3 addresses Page 3

8.6.2 CRC Protection for Configuration, Control, and Test Registers

The TPS6594-Q1 device includes a static CRC-16 engine to protect all the static registers of the device. Static registers are registers in Page 1, 2, and 3, with values that do not change once loaded from NVM. The CRC-16 engine continuously checks the control registers on the device. The expected CRC-16 value is stored in the NVM. When the CRC-16 engine detects a mismatch between the calculated and expected CRC-16 values, the interrupt bit REG_CRC_ERR_INT is set and the device forces an orderly shutdown sequence to return to the SAFE RECOVERY state. The device NVM control, configuration, and test registers in page 1 are protected against read or write access when the device is in normal functional mode. .

The CRC-16 engine uses a standard CRC-16 polynomial to calculate the internal known-good checksum-value, which is $X^{16} + X^{14} + X^{13} + X^{12} + X^{10} + X^{8} + X^{6} + X^{4} + X^{3} + X + 1$.

The initial value for the remainder of the polynomial is all 1s and is in big-endian bit-stream order. The inversion of the calculated result is enabled.

Note

The CRC-16 engine assumes a default value of '0' for all undefined or reserved bits in all control registers. Therefore, the software MUST NOT write the value of '1' to any of these undefined or reserved bits. If the value of '1 is written to any undefined or reserved bit of a writable register, the CRC-16 engine detects a mismatch between the calculated and expected CRC-16 values, and hence the interrupt bit REG_CRC_ERR_INT is set and the device forces an orderly shutdown sequence to return to the SAFE RECOVERY state.

8.6.3 CRC Protection for User Registers

A dynamic CRC-8 engine exists to protect registers that have values which can change during operation. These are registers in Page 1 and 4. When writes occur to these pages, the dynamic CRC-8 is checked, computed, and updated. Continuously during operation the CRC-8 are evaluated and verified in a round-robin fashion.

The CRC-8 engine utilizes the Polynomial(0xA6) = $X^8 + X^6 + X^3 + X^2 + 1$, which provides a H4 hamming distance.

Note

If a RESERVED bit in a R/W configuration register gets set to 1h through a I2C/SPI write, the TPS6594-Q1 detects a CRC error in the register map. Therefore, it is important that system software involved in the I2C/SPI write-access to the TPS6594-Q1 keeps all RESERVED bits (i.e. all bits with the word RESERVED in the Register Field Description tables in the Register Map section Section 8.7.1 at 0h.

8.6.4 Register Write Protection

For safety application, in order to prevent unintentional writes to the control registers, the TPS6594-Q1 device implements locking and unlocking mechanisms to many of its configuration/control registers described in the following subsections.

8.6.4.1 ESM and WDOG Configuration Registers

The configuration registers for the watchdog and the ESM are locked when their monitoring functions are in operation. The locking mechanism and the list of the locked watchdog register is described under Section 8.3.11.2. The locking mechanism and the list of the locked ESM registers is described under Section 8.3.12

8.6.4.2 User Registers

User registers in page 0, except the ESM and the WDOG configuration registers described in Section 8.6.4.1, and the interrupt registers (x_INT) at address 0x5a through 0x6c in page 0, can be write protected by a dedicated lock. User must write '0x9B' to the REGISTER_LOCK register to unlock the register. Writing any value other than '0x9B' activates the lock again. To check the register lock status, user must read the REGISTER_LOCK_STATUS bit. When this bit is '0', it indicates the user registers are unlocked. When this bit is '1', the user registers are locked. During start-up sequence such as powering up for the first time, waking up from LP_STANDBY, or recovering from SAFE_RECOVERY, the user registers are unlocked automatically.

As an extra measure of protection to prevent the accidental change of the buck frequency while the buck is in operation, the BUCKn_FREQ_SEL register bits are locked by the REGISTER_LOCK register as well as the FREQ_SEL_UNLOCK bit. Users must set the FREQ_SEL_UNLOCK bit to '1' in addition to writing '0x9B' to the REGISTER_LOCK register in order to change the BUCKn_FREQ_SEL bit setting. The default setting of the FREQ_SEL_UNLOCK bit comes from the NVM register setting. User is advised against changing the buck frequency while the buck is in operation.

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8.7 Register Maps

8.7.1 TPS6594-Q1 Registers

Table 8-23 lists the memory-mapped registers for the TPS6594-Q1 registers. All register offset addresses not listed in Table 8-23 should be considered as reserved locations and the register contents should not be modified.

Table 8-23. TPS6594-Q1 Registers

Offset	Acronym	Register Name	Section
1h	DEV_REV		Section 8.7.1.1
2h	NVM_CODE_1		Section 8.7.1.2
3h	NVM_CODE_2		Section 8.7.1.3
4h	BUCK1_CTRL		Section 8.7.1.4
5h	BUCK1_CONF		Section 8.7.1.5
6h	BUCK2_CTRL		Section 8.7.1.6
7h	BUCK2_CONF		Section 8.7.1.7
8h	BUCK3_CTRL		Section 8.7.1.8
9h	BUCK3_CONF		Section 8.7.1.9
Ah	BUCK4_CTRL		Section 8.7.1.10
Bh	BUCK4_CONF		Section 8.7.1.11
Ch	BUCK5_CTRL		Section 8.7.1.12
Dh	BUCK5_CONF		Section 8.7.1.13
Eh	BUCK1_VOUT_1		Section 8.7.1.14
Fh	BUCK1_VOUT_2		Section 8.7.1.15
10h	BUCK2_VOUT_1		Section 8.7.1.16
11h	BUCK2_VOUT_2		Section 8.7.1.17
12h	BUCK3_VOUT_1		Section 8.7.1.18
13h	BUCK3_VOUT_2		Section 8.7.1.19
14h	BUCK4_VOUT_1		Section 8.7.1.20
15h	BUCK4_VOUT_2		Section 8.7.1.21
16h	BUCK5_VOUT_1		Section 8.7.1.22
17h	BUCK5_VOUT_2		Section 8.7.1.23
18h	BUCK1_PG_WINDOW		Section 8.7.1.24
19h	BUCK2_PG_WINDOW		Section 8.7.1.25
1Ah	BUCK3_PG_WINDOW		Section 8.7.1.26
1Bh	BUCK4_PG_WINDOW		Section 8.7.1.27
1Ch	BUCK5_PG_WINDOW		Section 8.7.1.28
1Dh	LDO1_CTRL		Section 8.7.1.29
1Eh	LDO2_CTRL		Section 8.7.1.30
1Fh	LDO3_CTRL		Section 8.7.1.31
20h	LDO4_CTRL		Section 8.7.1.32
22h	LDORTC_CTRL		Section 8.7.1.33
23h	LDO1_VOUT		Section 8.7.1.34
24h	LDO2_VOUT		Section 8.7.1.35
25h	LDO3_VOUT		Section 8.7.1.36
26h	LDO4_VOUT		Section 8.7.1.37
27h	LDO1_PG_WINDOW		Section 8.7.1.38
28h	LDO2_PG_WINDOW		Section 8.7.1.39
29h	LDO3_PG_WINDOW		Section 8.7.1.40
2Ah	LDO4_PG_WINDOW		Section 8.7.1.41
2Bh	VCCA_VMON_CTRL		Section 8.7.1.42

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Table 8-23. TPS6594-Q1 Registers (continued)

Offset	Acronym	Register Name	Section
2Ch	VCCA_PG_WINDOW		Section 8.7.1.43
31h	GPIO1_CONF		Section 8.7.1.44
32h	GPIO2_CONF		Section 8.7.1.45
33h	GPIO3_CONF		Section 8.7.1.46
34h	GPIO4_CONF		Section 8.7.1.47
35h	GPIO5_CONF		Section 8.7.1.48
36h	GPIO6_CONF		Section 8.7.1.49
37h	GPIO7_CONF		Section 8.7.1.50
38h	GPIO8_CONF		Section 8.7.1.51
39h	GPIO9_CONF		Section 8.7.1.52
3Ah	GPIO10_CONF		Section 8.7.1.53
3Bh	GPIO11_CONF		Section 8.7.1.54
3Ch	NPWRON_CONF		Section 8.7.1.55
3Dh	GPIO_OUT_1		Section 8.7.1.56
3Eh	GPIO_OUT_2		Section 8.7.1.57
3Fh	GPIO_IN_1		Section 8.7.1.58
40h	GPIO_IN_2		Section 8.7.1.59
41h	RAIL_SEL_1		Section 8.7.1.60
42h	RAIL_SEL_2		Section 8.7.1.61
43h	RAIL_SEL_3		Section 8.7.1.62
44h	FSM_TRIG_SEL_1		Section 8.7.1.63
45h	FSM_TRIG_SEL_2		Section 8.7.1.64
46h	FSM_TRIG_MASK_1		Section 8.7.1.65
47h	FSM_TRIG_MASK_2		Section 8.7.1.66
48h	FSM_TRIG_MASK_3		Section 8.7.1.67
49h	MASK_BUCK1_2		Section 8.7.1.68
4Ah	MASK_BUCK3_4		Section 8.7.1.69
4Bh	MASK_BUCK5		Section 8.7.1.70
4Ch	MASK_LDO1_2		Section 8.7.1.71
4Dh	MASK_LDO3_4		Section 8.7.1.72
4Eh	MASK_VMON		Section 8.7.1.73
4Fh	MASK_GPIO1_8_FALL		Section 8.7.1.74
50h	MASK_GPIO1_8_RISE		Section 8.7.1.75
51h	MASK_GPIO9_11		Section 8.7.1.76
52h	MASK_STARTUP		Section 8.7.1.77
53h	MASK_MISC		Section 8.7.1.78
54h	MASK_MODERATE_ERR		Section 8.7.1.79
56h	MASK_FSM_ERR		Section 8.7.1.80
57h	MASK_COMM_ERR		Section 8.7.1.81
58h	MASK_READBACK_ERR		Section 8.7.1.82
59h	MASK_ESM		Section 8.7.1.83
5Ah	INT_TOP		Section 8.7.1.84
5Bh	INT_BUCK		Section 8.7.1.85
5Ch	INT_BUCK1_2		Section 8.7.1.86
5Dh	INT_BUCK3_4		Section 8.7.1.87

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Table 8-23. TPS6594-Q1 Registers (continued)

Offset	Acronym	Register Name	Section
5Eh	INT_BUCK5		Section 8.7.1.88
5Fh	INT_LDO_VMON		Section 8.7.1.89
60h	INT_LDO1_2		Section 8.7.1.90
61h	INT_LDO3_4		Section 8.7.1.91
62h	INT_VMON		Section 8.7.1.92
63h	INT_GPIO		Section 8.7.1.93
64h	INT_GPIO1_8		Section 8.7.1.94
65h	INT_STARTUP		Section 8.7.1.95
66h	INT_MISC		Section 8.7.1.96
67h	INT_MODERATE_ERR		Section 8.7.1.97
68h	INT_SEVERE_ERR		Section 8.7.1.98
69h	INT_FSM_ERR		Section 8.7.1.99
6Ah	INT_COMM_ERR		Section 8.7.1.100
6Bh	INT_READBACK_ERR		Section 8.7.1.101
6Ch	INT_ESM		Section 8.7.1.102
6Dh	STAT_BUCK1_2		Section 8.7.1.103
6Eh	STAT_BUCK3_4		Section 8.7.1.104
6Fh	STAT_BUCK5		Section 8.7.1.105
70h	STAT_LDO1_2		Section 8.7.1.106
71h	STAT_LDO3_4		Section 8.7.1.107
72h	STAT_VMON		Section 8.7.1.108
73h	STAT_STARTUP		Section 8.7.1.109
74h	STAT_MISC		Section 8.7.1.110
75h	STAT_MODERATE_ERR		Section 8.7.1.111
76h	STAT_SEVERE_ERR		Section 8.7.1.112
77h	STAT_READBACK_ERR		Section 8.7.1.113
78h	PGOOD_SEL_1		Section 8.7.1.114
79h	PGOOD_SEL_2		Section 8.7.1.115
7Ah	PGOOD_SEL_3		Section 8.7.1.116
7Bh	PGOOD_SEL_4		Section 8.7.1.117
7Ch	PLL_CTRL		Section 8.7.1.118
7Dh	CONFIG_1		Section 8.7.1.119
7Eh	CONFIG_2		Section 8.7.1.120
80h	ENABLE_DRV_REG		Section 8.7.1.121
81h	MISC_CTRL		Section 8.7.1.122
82h	ENABLE_DRV_STAT		Section 8.7.1.123
83h	RECOV_CNT_REG_1		Section 8.7.1.124
84h	RECOV_CNT_REG_2		Section 8.7.1.125
85h	FSM_I2C_TRIGGERS		Section 8.7.1.126
86h	FSM_NSLEEP_TRIGGERS		Section 8.7.1.127
87h	BUCK_RESET_REG		Section 8.7.1.128
88h	SPREAD_SPECTRUM_1		Section 8.7.1.129
8Ah	FREQ_SEL		Section 8.7.1.130
8Bh	FSM_STEP_SIZE		Section 8.7.1.131
8Ch	LDO_RV_TIMEOUT_REG_1		Section 8.7.1.132

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Table 8-23. TPS6594-Q1 Registers (continued)

Offset	Acronym	Register Name	Section
8Dh	LDO_RV_TIMEOUT_REG_2		Section 8.7.1.133
8Eh	USER_SPARE_REGS		Section 8.7.1.134
8Fh	ESM_MCU_START_REG		Section 8.7.1.135
90h	ESM_MCU_DELAY1_REG		Section 8.7.1.136
91h	ESM_MCU_DELAY2_REG		Section 8.7.1.137
92h	ESM_MCU_MODE_CFG		Section 8.7.1.138
93h	ESM_MCU_HMAX_REG		Section 8.7.1.139
94h	ESM_MCU_HMIN_REG		Section 8.7.1.140
95h	ESM_MCU_LMAX_REG		Section 8.7.1.141
96h	ESM_MCU_LMIN_REG		Section 8.7.1.142
97h	ESM_MCU_ERR_CNT_REG		Section 8.7.1.143
98h	ESM_SOC_START_REG		Section 8.7.1.144
99h	ESM_SOC_DELAY1_REG		Section 8.7.1.145
9Ah	ESM_SOC_DELAY2_REG		Section 8.7.1.146
9Bh	ESM_SOC_MODE_CFG		Section 8.7.1.147
9Ch	ESM_SOC_HMAX_REG		Section 8.7.1.148
9Dh	ESM_SOC_HMIN_REG		Section 8.7.1.149
9Eh	ESM_SOC_LMAX_REG		Section 8.7.1.150
9Fh	ESM_SOC_LMIN_REG		Section 8.7.1.151
A0h	ESM_SOC_ERR_CNT_REG		Section 8.7.1.152
A1h	REGISTER_LOCK		Section 8.7.1.153
A6h	MANUFACTURING_VER		Section 8.7.1.154
A7h	CUSTOMER_NVM_ID_REG		Section 8.7.1.155
ABh	SOFT_REBOOT_REG		Section 8.7.1.156
B5h	RTC_SECONDS		Section 8.7.1.157
B6h	RTC_MINUTES		Section 8.7.1.158
B7h	RTC_HOURS		Section 8.7.1.159
B8h	RTC_DAYS		Section 8.7.1.160
B9h	RTC_MONTHS		Section 8.7.1.161
BAh	RTC_YEARS		Section 8.7.1.162
BBh	RTC_WEEKS		Section 8.7.1.163
BCh	ALARM_SECONDS		Section 8.7.1.164
BDh	ALARM_MINUTES		Section 8.7.1.165
BEh	ALARM_HOURS		Section 8.7.1.166
BFh	ALARM_DAYS		Section 8.7.1.167
C0h	ALARM_MONTHS		Section 8.7.1.168
C1h	ALARM_YEARS		Section 8.7.1.169
C2h	RTC_CTRL_1		Section 8.7.1.170
C3h	RTC_CTRL_2		Section 8.7.1.171
C4h	RTC_STATUS		Section 8.7.1.172
C5h	RTC_INTERRUPTS		Section 8.7.1.173
C6h	RTC_COMP_LSB		Section 8.7.1.174
C7h	RTC_COMP_MSB		Section 8.7.1.175
C8h	RTC_RESET_STATUS		Section 8.7.1.176
C9h	SCRATCH_PAD_REG_1		Section 8.7.1.177

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Table 8-23. TPS6594-Q1 Registers (continued)

Offset	Acronym	Register Name	Section
CAh	SCRATCH_PAD_REG_2		Section 8.7.1.178
CBh	SCRATCH_PAD_REG_3		Section 8.7.1.179
CCh	SCRATCH_PAD_REG_4		Section 8.7.1.180
CDh	PFSM_DELAY_REG_1		Section 8.7.1.181
CEh	PFSM_DELAY_REG_2		Section 8.7.1.182
CFh	PFSM_DELAY_REG_3		Section 8.7.1.183
D0h	PFSM_DELAY_REG_4		Section 8.7.1.184
401h	WD_ANSWER_REG		Section 8.7.1.185
402h	WD_QUESTION_ANSW_CNT		Section 8.7.1.186
403h	WD_WIN1_CFG		Section 8.7.1.187
404h	WD_WIN2_CFG		Section 8.7.1.188
405h	WD_LONGWIN_CFG		Section 8.7.1.189
406h	WD_MODE_REG		Section 8.7.1.190
407h	WD_QA_CFG		Section 8.7.1.191
408h	WD_ERR_STATUS		Section 8.7.1.192
409h	WD_THR_CFG		Section 8.7.1.193
40Ah	WD_FAIL_CNT_REG		Section 8.7.1.194

Complex bit access types are encoded to fit into small table cells. Table 8-24 shows the codes that are used for access types in this section.

Table 8-24. TPS6594-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WSelfClrF	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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8.7.1.1 DEV_REV Register (Offset = 1h) [Reset = 00h]

DEV_REV is shown in Figure 8-60 and described in Table 8-25.

Return to the Table 8-23.

Figure 8-60. DEV_REV Register

7	6	5	4	3	2	1	0
TI_DEVICE_ID							
R/W-0h							

Table 8-25. DEV_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TI_DEVICE_ID	R/W	0h	Refer to Technical Reference Manual / User's Guide for specific numbering. Note: This register can be programmed only by the manufacturer. (Default from NVM memory)

8.7.1.2 NVM_CODE_1 Register (Offset = 2h) [Reset = 00h]

NVM_CODE_1 is shown in Figure 8-61 and described in Table 8-26.

Return to the Table 8-23.

Figure 8-61. NVM_CODE_1 Register

7	6	5	4	3	2	1	0
TI_NVM_ID							
R/W-0h							

Table 8-26. NVM_CODE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TI_NVM_ID	R/W	0h	0x00 - 0xF0 are reserved for TI manufactured NVM variants 0xF1 - 0xFF are reserved for special use 0xF1 = Engineering sample, blank NVM [trim and basic defaults only], customer programmable for engineering use only 0xF2 = Production unit, blank NVM [trim and basic defaults only], customer programmable in volume production 0xF3-FF = Reserved, do not use Note: This register can be programmed only by the manufacturer. (Default from NVM memory)

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8.7.1.3 NVM_CODE_2 Register (Offset = 3h) [Reset = 00h]

NVM_CODE_2 is shown in Figure 8-62 and described in Table 8-27.

Return to the Table 8-23.

Figure 8-62. NVM_CODE_2 Register

7	6	5	4	3	2	1	0
TI_NVM_REV							
R/W-0h							

Table 8-27. NVM_CODE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TI_NVM_REV	R/W	0h	NVM revision of the IC Note: This register can be programmed only by the manufacturer. (Default from NVM memory)

8.7.1.4 BUCK1_CTRL Register (Offset = 4h) [Reset = 22h]

BUCK1_CTRL is shown in Figure 8-63 and described in Table 8-28.

Return to the Table 8-23.

Figure 8-63. BUCK1_CTRL Register

7	6	5	4	3	2	1	0
BUCK1_RV_SEL	RESERVED	BUCK1_PLDN	BUCK1_VMON_EN	BUCK1_VSEL	BUCK1_FPWM_MP	BUCK1_FPWM	BUCK1_EN
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

Table 8-28. BUCK1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK1_RV_SEL	R/W	0h	Select residual voltage checking for BUCK1 feedback pin. (Default from NVM memory) 0h = Disabled 1h = Enabled
6	RESERVED	R/W	0h	
5	BUCK1_PLDN	R/W	1h	Enable output pull-down resistor when BUCK1 is disabled: (Default from NVM memory) 0h = Pull-down resistor disabled 1h = Pull-down resistor enabled
4	BUCK1_VMON_EN	R/W	0h	Enable BUCK1 OV, UV, SC and ILIM comparators: (Default from NVM memory) 0h = OV, UV, SC and ILIM comparators are disabled 1h = OV, UV, SC and ILIM comparators are enabled
3	BUCK1_VSEL	R/W	0h	Select output voltage register for BUCK1: (Default from NVM memory) 0h = BUCK1_VOUT_1 1h = BUCK1_VOUT_2
2	BUCK1_FPWM_MP	R/W	0h	Forces the BUCK1 regulator to operate always in multi-phase and forced PWM operation mode: (Default from NVM memory) 0h = Automatic phase adding and shedding. 1h = Forced to multi-phase operation, all phases in the multi-phase configuration.
1	BUCK1_FPWM	R/W	1h	Forces the BUCK1 regulator to operate in PWM mode: (Default from NVM memory) 0h = Automatic transitions between PFM and PWM modes (AUTO mode). 1h = Forced to PWM operation.
0	BUCK1_EN	R/W	0h	Enable BUCK1 regulator: (Default from NVM memory) 0h = BUCK regulator is disabled 1h = BUCK regulator is enabled

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8.7.1.5 BUCK1_CONF Register (Offset = 5h) [Reset = 22h]

BUCK1_CONF is shown in Figure 8-64 and described in Table 8-29.

Return to the Table 8-23.

Figure 8-64. BUCK1_CONF Register

7	6	5	4	3	2	1	0
RESERVED		BUCK1_ILIM			BUCK1_SLEW_RATE		
R/W-0h		R/W-4h			R/W-2h		

Table 8-29. BUCK1_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK1_ILIM	R/W	4h	Sets the switch peak current limit of BUCK1. Can be programmed at any time during operation: (Default from NVM memory) 0h = Reserved 1h = Reserved 2h = 2.5 A 3h = 3.5 A 4h = 4.5 A 5h = 5.5 A 6h = Reserved 7h = Reserved
2-0	BUCK1_SLEW_RATE	R/W	2h	Sets the output voltage slew rate for BUCK1 regulator (rising and falling edges): (Default from NVM memory) 0h = 33 mV/µs 1h = 20 mV/µs 2h = 10 mV/µs 3h = 5.0 mV/µs 4h = 2.5 mV/µs 5h = 1.3 mV/µs 6h = 0.63 mV/µs 7h = 0.31 mV/µs

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8.7.1.6 BUCK2_CTRL Register (Offset = 6h) [Reset = 22h]

BUCK2_CTRL is shown in Figure 8-65 and described in Table 8-30.

Return to the Table 8-23.

Figure 8-65. BUCK2_CTRL Register

7	6	5	4	3	2	1	0
BUCK2_RV_SEL	RESERVED	BUCK2_PLDN	BUCK2_VMON_EN	BUCK2_VSEL	RESERVED	BUCK2_FPWM	BUCK2_EN
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

Table 8-30. BUCK2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK2_RV_SEL	R/W	0h	Select residual voltage checking for BUCK2 feedback pin. (Default from NVM memory) 0h = Disabled 1h = Enabled
6	RESERVED	R/W	0h	
5	BUCK2_PLDN	R/W	1h	Enable output pull-down resistor when BUCK2 is disabled: (Default from NVM memory) 0h = Pull-down resistor disabled 1h = Pull-down resistor enabled
4	BUCK2_VMON_EN	R/W	0h	Enable BUCK2 OV, UV, SC and ILIM comparators: (Default from NVM memory) 0h = OV, UV, SC and ILIM comparators are disabled 1h = OV, UV, SC and ILIM comparators are enabled
3	BUCK2_VSEL	R/W	0h	Select output voltage register for BUCK2: (Default from NVM memory) 0h = BUCK2_VOUT_1 1h = BUCK2_VOUT_2
2	RESERVED	R/W	0h	
1	BUCK2_FPWM	R/W	1h	Forces the BUCK2 regulator to operate in PWM mode: (Default from NVM memory) 0h = Automatic transitions between PFM and PWM modes (AUTO mode). 1h = Forced to PWM operation.
0	BUCK2_EN	R/W	0h	Enable BUCK2 regulator: (Default from NVM memory) 0h = BUCK regulator is disabled 1h = BUCK regulator is enabled

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8.7.1.7 BUCK2_CONF Register (Offset = 7h) [Reset = 22h]

BUCK2_CONF is shown in Figure 8-66 and described in Table 8-31.

Return to the Table 8-23.

Figure 8-66. BUCK2_CONF Register

7	6	5	4	3	2	1	0
RESERVED		BUCK2_ILIM			BUCK2_SLEW_RATE		
R/W-0h		R/W-4h			R/W-2h		

Table 8-31. BUCK2_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK2_ILIM	R/W	4h	Sets the switch peak current limit of BUCK2. Can be programmed at any time during operation: (Default from NVM memory) 0h = Reserved 1h = Reserved 2h = 2.5 A 3h = 3.5 A 4h = 4.5 A 5h = 5.5 A 6h = Reserved 7h = Reserved
2-0	BUCK2_SLEW_RATE	R/W	2h	Sets the output voltage slew rate for BUCK2 regulator (rising and falling edges): (Default from NVM memory) 0h = 33 mV/µs 1h = 20 mV/µs 2h = 10 mV/µs 3h = 5.0 mV/µs 4h = 2.5 mV/µs 5h = 1.3 mV/µs 6h = 0.63 mV/µs 7h = 0.31 mV/µs

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8.7.1.8 BUCK3_CTRL Register (Offset = 8h) [Reset = 22h]

BUCK3_CTRL is shown in Figure 8-67 and described in Table 8-32.

Return to the Table 8-23.

Figure 8-67. BUCK3_CTRL Register

7	6	5	4	3	2	1	0
BUCK3_RV_SEL	RESERVED	BUCK3_PLDN	BUCK3_VMON_EN	BUCK3_VSEL	BUCK3_FPWM_MP	BUCK3_FPWM	BUCK3_EN
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

Table 8-32. BUCK3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK3_RV_SEL	R/W	0h	Select residual voltage checking for BUCK3 feedback pin. (Default from NVM memory) 0h = Disabled 1h = Enabled
6	RESERVED	R/W	0h	
5	BUCK3_PLDN	R/W	1h	Enable output pull-down resistor when BUCK3 is disabled: (Default from NVM memory) 0h = Pull-down resistor disabled 1h = Pull-down resistor enabled
4	BUCK3_VMON_EN	R/W	0h	Enable BUCK3 OV, UV, SC and ILIM comparators: (Default from NVM memory) 0h = OV, UV, SC and ILIM comparators are disabled 1h = OV, UV, SC and ILIM comparators are enabled
3	BUCK3_VSEL	R/W	0h	Select output voltage register for BUCK3: (Default from NVM memory) 0h = BUCK3_VOUT_1 1h = BUCK3_VOUT_2
2	BUCK3_FPWM_MP	R/W	0h	Forces the BUCK3 regulator to operate always in multi-phase and forced PWM operation mode: (Default from NVM memory) 0h = Automatic phase adding and shedding. 1h = Forced to multi-phase operation, all phases in the multi-phase configuration.
1	BUCK3_FPWM	R/W	1h	Forces the BUCK3 regulator to operate in PWM mode: (Default from NVM memory) 0h = Automatic transitions between PFM and PWM modes (AUTO mode). 1h = Forced to PWM operation.
0	BUCK3_EN	R/W	0h	Enable BUCK3 regulator: (Default from NVM memory) 0h = BUCK regulator is disabled 1h = BUCK regulator is enabled

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8.7.1.9 BUCK3_CONF Register (Offset = 9h) [Reset = 22h]

BUCK3_CONF is shown in Figure 8-68 and described in Table 8-33.

Return to the Table 8-23.

Figure 8-68. BUCK3_CONF Register

7	6	5	4	3	2	1	0
RESERVED		BUCK3_ILIM			BUCK3_SLEW_RATE		
R/W-0h		R/W-4h			R/W-2h		

Table 8-33. BUCK3_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK3_ILIM	R/W	4h	Sets the switch peak current limit of BUCK3. Can be programmed at any time during operation: (Default from NVM memory) 0h = Reserved 1h = Reserved 2h = 2.5 A 3h = 3.5 A 4h = 4.5 A 5h = 5.5 A 6h = Reserved 7h = Reserved
2-0	BUCK3_SLEW_RATE	R/W	2h	Sets the output voltage slew rate for BUCK3 regulator (rising and falling edges): (Default from NVM memory) 0h = 33 mV/µs 1h = 20 mV/µs 2h = 10 mV/µs 3h = 5.0 mV/µs 4h = 2.5 mV/µs 5h = 1.3 mV/µs 6h = 0.63 mV/µs 7h = 0.31 mV/µs

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8.7.1.10 BUCK4_CTRL Register (Offset = Ah) [Reset = 22h]

BUCK4_CTRL is shown in Figure 8-69 and described in Table 8-34.

Return to the Table 8-23.

Figure 8-69. BUCK4_CTRL Register

7	6	5	4	3	2	1	0
BUCK4_RV_SEL	RESERVED	BUCK4_PLDN	BUCK4_VMON_EN	BUCK4_VSEL	RESERVED	BUCK4_FPWM	BUCK4_EN
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

Table 8-34. BUCK4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK4_RV_SEL	R/W	0h	Select residual voltage checking for BUCK4 feedback pin. (Default from NVM memory) 0h = Disabled 1h = Enabled
6	RESERVED	R/W	0h	
5	BUCK4_PLDN	R/W	1h	Enable output pull-down resistor when BUCK4 is disabled: (Default from NVM memory) 0h = Pull-down resistor disabled 1h = Pull-down resistor enabled
4	BUCK4_VMON_EN	R/W	0h	Enable BUCK4 OV, UV, SC and ILIM comparators: (Default from NVM memory) 0h = OV, UV, SC and ILIM comparators are disabled 1h = OV, UV, SC and ILIM comparators are enabled
3	BUCK4_VSEL	R/W	0h	Select output voltage register for BUCK4: (Default from NVM memory) 0h = BUCK4_VOUT_1 1h = BUCK4_VOUT_2
2	RESERVED	R/W	0h	
1	BUCK4_FPWM	R/W	1h	Forces the BUCK4 regulator to operate in PWM mode: (Default from NVM memory) 0h = Automatic transitions between PFM and PWM modes (AUTO mode). 1h = Forced to PWM operation.
0	BUCK4_EN	R/W	0h	Enable BUCK4 regulator: (Default from NVM memory) 0h = BUCK regulator is disabled 1h = BUCK regulator is enabled

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8.7.1.11 BUCK4_CONF Register (Offset = Bh) [Reset = 22h]

BUCK4_CONF is shown in Figure 8-70 and described in Table 8-35.

Return to the Table 8-23.

Figure 8-70. BUCK4_CONF Register

7	6	5	4	3	2	1	0
RESERVED		BUCK4_ILIM			BUCK4_SLEW_RATE		
R/W-0h		R/W-4h			R/W-2h		

Table 8-35. BUCK4_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK4_ILIM	R/W	4h	Sets the switch peak current limit of BUCK4. Can be programmed at any time during operation: (Default from NVM memory) 0h = Reserved 1h = Reserved 2h = 2.5 A 3h = 3.5 A 4h = 4.5 A 5h = 5.5 A 6h = Reserved 7h = Reserved
2-0	BUCK4_SLEW_RATE	R/W	2h	Sets the output voltage slew rate for BUCK4 regulator (rising and falling edges): (Default from NVM memory) 0h = 33 mV/µs 1h = 20 mV/µs 2h = 10 mV/µs 3h = 5.0 mV/µs 4h = 2.5 mV/µs 5h = 1.3 mV/µs 6h = 0.63 mV/µs 7h = 0.31 mV/µs

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8.7.1.12 BUCK5_CTRL Register (Offset = Ch) [Reset = 22h]

BUCK5_CTRL is shown in Figure 8-71 and described in Table 8-36.

Return to the Table 8-23.

Figure 8-71. BUCK5_CTRL Register

7	6	5	4	3	2	1	0
BUCK5_RV_SEL	RESERVED	BUCK5_PLDN	BUCK5_VMON_EN	BUCK5_VSEL	RESERVED	BUCK5_FPWM	BUCK5_EN
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

Table 8-36. BUCK5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK5_RV_SEL	R/W	0h	Select residual voltage checking for BUCK5 feedback pin. (Default from NVM memory) 0h = Disabled 1h = Enabled
6	RESERVED	R/W	0h	
5	BUCK5_PLDN	R/W	1h	Enable output pull-down resistor when BUCK5 is disabled: (Default from NVM memory) 0h = Pull-down resistor disabled 1h = Pull-down resistor enabled
4	BUCK5_VMON_EN	R/W	0h	Enable BUCK5 OV, UV, SC and ILIM comparators: (Default from NVM memory) 0h = OV, UV, SC and ILIM comparators are disabled 1h = OV, UV, SC and ILIM comparators are enabled
3	BUCK5_VSEL	R/W	0h	Select output voltage register for BUCK5: (Default from NVM memory) 0h = BUCK5_VOUT_1 1h = BUCK5_VOUT_2
2	RESERVED	R/W	0h	
1	BUCK5_FPWM	R/W	1h	Forces the BUCK5 regulator to operate in PWM mode: (Default from NVM memory) 0h = Automatic transitions between PFM and PWM modes (AUTO mode). 1h = Forced to PWM operation.
0	BUCK5_EN	R/W	0h	Enable BUCK5 regulator: (Default from NVM memory) 0h = BUCK regulator is disabled 1h = BUCK regulator is enabled

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8.7.1.13 BUCK5_CONF Register (Offset = Dh) [Reset = 22h]

BUCK5_CONF is shown in Figure 8-72 and described in Table 8-37.

Return to the Table 8-23.

Figure 8-72. BUCK5_CONF Register

7	6	5	4	3	2	1	0
RESERVED		BUCK5_ILIM			BUCK5_SLEW_RATE		
R/W-0h		R/W-4h			R/W-2h		

Table 8-37. BUCK5_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK5_ILIM	R/W	4h	Sets the switch peak current limit of BUCK5. Can be programmed at any time during operation: (Default from NVM memory) 0h = Reserved 1h = Reserved 2h = 2.5 A 3h = 3.5 A 4h = Reserved 5h = Reserved 6h = Reserved 7h = Reserved
2-0	BUCK5_SLEW_RATE	R/W	2h	Sets the output voltage slew rate for BUCK5 regulator (rising and falling edges): (Default from NVM memory) 0h = 33 mV/µs 1h = 20 mV/µs 2h = 10 mV/µs 3h = 5.0 mV/µs 4h = 2.5 mV/µs 5h = 1.3 mV/µs 6h = 0.63 mV/µs 7h = 0.31 mV/µs

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8.7.1.14 BUCK1_VOUT_1 Register (Offset = Eh) [Reset = 00h]

BUCK1_VOUT_1 is shown in Figure 8-73 and described in Table 8-38.

Return to the Table 8-23.

Figure 8-73. BUCK1_VOUT_1 Register

7	6	5	4	3	2	1	0
BUCK1_VSET1							
R/W-0h							

Table 8-38. BUCK1_VOUT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK1_VSET1	R/W	0h	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

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8.7.1.15 BUCK1_VOUT_2 Register (Offset = Fh) [Reset = 00h]

BUCK1_VOUT_2 is shown in Figure 8-74 and described in Table 8-39.

Return to the Table 8-23.

Figure 8-74. BUCK1_VOUT_2 Register

7	6	5	4	3	2	1	0
BUCK1_VSET2							
R/W-0h							

Table 8-39. BUCK1_VOUT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK1_VSET2	R/W	0h	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

8.7.1.16 BUCK2_VOUT_1 Register (Offset = 10h) [Reset = 00h]

BUCK2_VOUT_1 is shown in Figure 8-75 and described in Table 8-40.

Return to the Table 8-23.

Figure 8-75. BUCK2_VOUT_1 Register

7	6	5	4	3	2	1	0
BUCK2_VSET1							
R/W-0h							

Table 8-40. BUCK2_VOUT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK2_VSET1	R/W	0h	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

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8.7.1.17 BUCK2_VOUT_2 Register (Offset = 11h) [Reset = 00h]

BUCK2_VOUT_2 is shown in Figure 8-76 and described in Table 8-41.

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Figure 8-76. BUCK2_VOUT_2 Register

7	6	5	4	3	2	1	0
BUCK2_VSET2							
R/W-0h							

Table 8-41. BUCK2_VOUT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK2_VSET2	R/W	0h	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

8.7.1.18 BUCK3_VOUT_1 Register (Offset = 12h) [Reset = 00h]

BUCK3_VOUT_1 is shown in Figure 8-77 and described in Table 8-42.

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Figure 8-77. BUCK3_VOUT_1 Register

7	6	5	4	3	2	1	0
BUCK3_VSET1							
R/W-0h							

Table 8-42. BUCK3_VOUT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK3_VSET1	R/W	0h	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

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8.7.1.19 BUCK3_VOUT_2 Register (Offset = 13h) [Reset = 00h]

BUCK3_VOUT_2 is shown in Figure 8-78 and described in Table 8-43.

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Figure 8-78. BUCK3_VOUT_2 Register

7	6	5	4	3	2	1	0
BUCK3_VSET2							
R/W-0h							

Table 8-43. BUCK3_VOUT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK3_VSET2	R/W	0h	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

8.7.1.20 BUCK4_VOUT_1 Register (Offset = 14h) [Reset = 00h]

BUCK4_VOUT_1 is shown in Figure 8-79 and described in Table 8-44.

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Figure 8-79. BUCK4_VOUT_1 Register

7	6	5	4	3	2	1	0
BUCK4_VSET1							
R/W-0h							

Table 8-44. BUCK4_VOUT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK4_VSET1	R/W	0h	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

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8.7.1.21 BUCK4_VOUT_2 Register (Offset = 15h) [Reset = 00h]

BUCK4_VOUT_2 is shown in Figure 8-80 and described in Table 8-45.

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Figure 8-80. BUCK4_VOUT_2 Register

7	6	5	4	3	2	1	0
BUCK4_VSET2							
R/W-0h							

Table 8-45. BUCK4_VOUT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK4_VSET2	R/W	0h	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

8.7.1.22 BUCK5_VOUT_1 Register (Offset = 16h) [Reset = 00h]

BUCK5_VOUT_1 is shown in Figure 8-81 and described in Table 8-46.

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Figure 8-81. BUCK5_VOUT_1 Register

7	6	5	4	3	2	1	0
BUCK5_VSET1							
R/W-0h							

Table 8-46. BUCK5_VOUT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK5_VSET1	R/W	0h	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

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8.7.1.23 BUCK5_VOUT_2 Register (Offset = 17h) [Reset = 00h]

BUCK5_VOUT_2 is shown in Figure 8-82 and described in Table 8-47.

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Figure 8-82. BUCK5_VOUT_2 Register

7	6	5	4	3	2	1	0
BUCK5_VSET2							
R/W-0h							

Table 8-47. BUCK5_VOUT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK5_VSET2	R/W	0h	Voltage selection for buck regulator. See Buck regulators chapter for voltage levels. (Default from NVM memory)

8.7.1.24 BUCK1_PG_WINDOW Register (Offset = 18h) [Reset = 00h]

BUCK1_PG_WINDOW is shown in Figure 8-83 and described in Table 8-48.

Return to the Table 8-23.

Figure 8-83. BUCK1_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		BUCK1_UV_THR			BUCK1_OV_THR		
R/W-0h		R/W-0h			R/W-0h		

Table 8-48. BUCK1_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK1_UV_THR	R/W	0h	Powergood low threshold level for BUCK1: (Default from NVM memory) 0h = -3% / -30mV 1h = -3.5% / -35 mV 2h = -4% / -40 mV 3h = -5% / -50 mV 4h = -6% / -60 mV 5h = -7% / -70 mV 6h = -8% / -80 mV 7h = -10% / -100mV
2-0	BUCK1_OV_THR	R/W	0h	Powergood high threshold level for BUCK1: (Default from NVM memory) 0h = +3% / +30mV 1h = +3.5% / +35 mV 2h = +4% / +40 mV 3h = +5% / +50 mV 4h = +6% / +60 mV 5h = +7% / +70 mV 6h = +8% / +80 mV 7h = +10% / +100mV

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8.7.1.25 BUCK2_PG_WINDOW Register (Offset = 19h) [Reset = 00h]

BUCK2_PG_WINDOW is shown in Figure 8-84 and described in Table 8-49.

Return to the Table 8-23.

Figure 8-84. BUCK2_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		BUCK2_UV_THR			BUCK2_OV_THR		
R/W-0h		R/W-0h			R/W-0h		

Table 8-49. BUCK2_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK2_UV_THR	R/W	0h	Powergood low threshold level for BUCK2: (Default from NVM memory) 0h = -3% / -30mV 1h = -3.5% / -35 mV 2h = -4% / -40 mV 3h = -5% / -50 mV 4h = -6% / -60 mV 5h = -7% / -70 mV 6h = -8% / -80 mV 7h = -10% / -100mV
2-0	BUCK2_OV_THR	R/W	0h	Powergood high threshold level for BUCK2: (Default from NVM memory) 0h = +3% / +30mV 1h = +3.5% / +35 mV 2h = +4% / +40 mV 3h = +5% / +50 mV 4h = +6% / +60 mV 5h = +7% / +70 mV 6h = +8% / +80 mV 7h = +10% / +100mV

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8.7.1.26 BUCK3_PG_WINDOW Register (Offset = 1Ah) [Reset = 00h]

BUCK3_PG_WINDOW is shown in Figure 8-85 and described in Table 8-50.

Return to the Table 8-23.

Figure 8-85. BUCK3_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		BUCK3_UV_THR			BUCK3_OV_THR		
R/W-0h		R/W-0h			R/W-0h		

Table 8-50. BUCK3_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK3_UV_THR	R/W	0h	Powergood low threshold level for BUCK3: (Default from NVM memory) 0h = -3% / -30mV 1h = -3.5% / -35 mV 2h = -4% / -40 mV 3h = -5% / -50 mV 4h = -6% / -60 mV 5h = -7% / -70 mV 6h = -8% / -80 mV 7h = -10% / -100mV
2-0	BUCK3_OV_THR	R/W	0h	Powergood high threshold level for BUCK3: (Default from NVM memory) 0h = +3% / +30mV 1h = +3.5% / +35 mV 2h = +4% / +40 mV 3h = +5% / +50 mV 4h = +6% / +60 mV 5h = +7% / +70 mV 6h = +8% / +80 mV 7h = +10% / +100mV

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8.7.1.27 BUCK4_PG_WINDOW Register (Offset = 1Bh) [Reset = 00h]

BUCK4_PG_WINDOW is shown in Figure 8-86 and described in Table 8-51.

Return to the Table 8-23.

Figure 8-86. BUCK4_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		BUCK4_UV_THR			BUCK4_OV_THR		
R/W-0h		R/W-0h			R/W-0h		

Table 8-51. BUCK4_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK4_UV_THR	R/W	0h	Powergood low threshold level for BUCK4: (Default from NVM memory) 0h = -3% / -30mV 1h = -3.5% / -35 mV 2h = -4% / -40 mV 3h = -5% / -50 mV 4h = -6% / -60 mV 5h = -7% / -70 mV 6h = -8% / -80 mV 7h = -10% / -100mV
2-0	BUCK4_OV_THR	R/W	0h	Powergood high threshold level for BUCK4: (Default from NVM memory) 0h = +3% / +30mV 1h = +3.5% / +35 mV 2h = +4% / +40 mV 3h = +5% / +50 mV 4h = +6% / +60 mV 5h = +7% / +70 mV 6h = +8% / +80 mV 7h = +10% / +100mV

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8.7.1.28 BUCK5_PG_WINDOW Register (Offset = 1Ch) [Reset = 00h]

BUCK5_PG_WINDOW is shown in Figure 8-87 and described in Table 8-52.

Return to the Table 8-23.

Figure 8-87. BUCK5_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		BUCK5_UV_THR			BUCK5_OV_THR		
R/W-0h		R/W-0h			R/W-0h		

Table 8-52. BUCK5_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK5_UV_THR	R/W	0h	Powergood low threshold level for BUCK5: (Default from NVM memory) 0h = -3% / -30mV 1h = -3.5% / -35 mV 2h = -4% / -40 mV 3h = -5% / -50 mV 4h = -6% / -60 mV 5h = -7% / -70 mV 6h = -8% / -80 mV 7h = -10% / -100mV
2-0	BUCK5_OV_THR	R/W	0h	Powergood high threshold level for BUCK5: (Default from NVM memory) 0h = +3% / +30mV 1h = +3.5% / +35 mV 2h = +4% / +40 mV 3h = +5% / +50 mV 4h = +6% / +60 mV 5h = +7% / +70 mV 6h = +8% / +80 mV 7h = +10% / +100mV

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8.7.1.29 LDO1_CTRL Register (Offset = 1Dh) [Reset = 60h]

LDO1_CTRL is shown in Figure 8-88 and described in Table 8-53.

Return to the Table 8-23.

Figure 8-88. LDO1_CTRL Register

7	6	5	4	3	2	1	0
LDO1_RV_SEL	LDO1_PLDN		LDO1_VMON_EN	RESERVED		LDO1_SLOW_RAMP	LDO1_EN
R/W-0h	R/W-3h		R/W-0h	R/W-0h		R/W-0h	R/W-0h

Table 8-53. LDO1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO1_RV_SEL	R/W	0h	Select residual voltage checking for LDO1 output pin. (Default from NVM memory) 0h = Disabled 1h = Enabled
6-5	LDO1_PLDN	R/W	3h	Enable output pull-down resistor when LDO1 is disabled: (Default from NVM memory) 0h = 50 kOhm 1h = 125 Ohm 2h = 250 Ohm 3h = 500 Ohm
4	LDO1_VMON_EN	R/W	0h	Enable LDO1 OV and UV comparators: (Default from NVM memory) 0h = OV and UV comparators are disabled 1h = OV and UV comparators are enabled.
3-2	RESERVED	R/W	0h	
1	LDO1_SLOW_RAMP	R/W	0h	LDO1 start-up slew rate selection 0h = 25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET 1h = 3mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET
0	LDO1_EN	R/W	0h	Enable LDO1 regulator: (Default from NVM memory) 0h = LDO1 regulator is disabled 1h = LDO1 regulator is enabled.

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8.7.1.30 LDO2_CTRL Register (Offset = 1Eh) [Reset = 60h]

LDO2_CTRL is shown in Figure 8-89 and described in Table 8-54.

Return to the Table 8-23.

Figure 8-89. LDO2_CTRL Register

7	6	5	4	3	2	1	0
LDO2_RV_SEL	LDO2_PLDN		LDO2_VMON_EN	RESERVED		LDO2_SLOW_RAMP	LDO2_EN
R/W-0h	R/W-3h		R/W-0h	R/W-0h		R/W-0h	R/W-0h

Table 8-54. LDO2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO2_RV_SEL	R/W	0h	Select residual voltage checking for LDO2 output pin. (Default from NVM memory) 0h = Disabled 1h = Enabled
6-5	LDO2_PLDN	R/W	3h	Enable output pull-down resistor when LDO2 is disabled: (Default from NVM memory) 0h = 50 kOhm 1h = 125 Ohm 2h = 250 Ohm 3h = 500 Ohm
4	LDO2_VMON_EN	R/W	0h	Enable LDO2 OV and UV comparators: (Default from NVM memory) 0h = OV and UV comparators are disabled 1h = OV and UV comparators are enabled.
3-2	RESERVED	R/W	0h	
1	LDO2_SLOW_RAMP	R/W	0h	LDO2 start-up slew rate selection 0h = 25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET 1h = 3mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET
0	LDO2_EN	R/W	0h	Enable LDO2 regulator: (Default from NVM memory) 0h = LDO1 regulator is disabled 1h = LDO1 regulator is enabled.

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8.7.1.31 LDO3_CTRL Register (Offset = 1Fh) [Reset = 60h]

LDO3_CTRL is shown in Figure 8-90 and described in Table 8-55.

Return to the Table 8-23.

Figure 8-90. LDO3_CTRL Register

7	6	5	4	3	2	1	0
LDO3_RV_SEL	LDO3_PLDN		LDO3_VMON_EN	RESERVED		LDO3_SLOW_RAMP	LDO3_EN
R/W-0h	R/W-3h		R/W-0h	R/W-0h		R/W-0h	R/W-0h

Table 8-55. LDO3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO3_RV_SEL	R/W	0h	Select residual voltage checking for LDO3 output pin. (Default from NVM memory) 0h = Disabled 1h = Enabled
6-5	LDO3_PLDN	R/W	3h	Enable output pull-down resistor when LDO3 is disabled: (Default from NVM memory) 0h = 50 kOhm 1h = 125 Ohm 2h = 250 Ohm 3h = 500 Ohm
4	LDO3_VMON_EN	R/W	0h	Enable LDO3 OV and UV comparators: (Default from NVM memory) 0h = OV and UV comparators are disabled 1h = OV and UV comparators are enabled.
3-2	RESERVED	R/W	0h	
1	LDO3_SLOW_RAMP	R/W	0h	LDO3 start-up slew rate selection 0h = 25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET 1h = 3mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET
0	LDO3_EN	R/W	0h	Enable LDO3 regulator: (Default from NVM memory) 0h = LDO1 regulator is disabled 1h = LDO1 regulator is enabled.

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8.7.1.32 LDO4_CTRL Register (Offset = 20h) [Reset = 60h]

LDO4_CTRL is shown in Figure 8-91 and described in Table 8-56.

Return to the Table 8-23.

Figure 8-91. LDO4_CTRL Register

7	6	5	4	3	2	1	0
LDO4_RV_SEL	LDO4_PLDN		LDO4_VMON_EN	RESERVED		LDO4_SLOW_RAMP	LDO4_EN
R/W-0h	R/W-3h		R/W-0h	R/W-0h		R/W-0h	R/W-0h

Table 8-56. LDO4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4_RV_SEL	R/W	0h	Select residual voltage checking for LDO4 output pin. (Default from NVM memory) 0h = Disabled 1h = Enabled
6-5	LDO4_PLDN	R/W	3h	Enable output pull-down resistor when LDO4 is disabled: (Default from NVM memory) 0h = 50 kOhm 1h = 125 Ohm 2h = 250 Ohm 3h = 500 Ohm
4	LDO4_VMON_EN	R/W	0h	Enable LDO4 OV and UV comparators: (Default from NVM memory) 0h = OV and UV comparators are disabled 1h = OV and UV comparators are enabled.
3-2	RESERVED	R/W	0h	
1	LDO4_SLOW_RAMP	R/W	0h	LDO4 start-up slew rate selection 0h = 25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET 1h = 3mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET
0	LDO4_EN	R/W	0h	Enable LDO4 regulator: (Default from NVM memory) 0h = LDO1 regulator is disabled 1h = LDO1 regulator is enabled.

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8.7.1.33 LDORTC_CTRL Register (Offset = 22h) [Reset = 00h]

LDORTC_CTRL is shown in Figure 8-92 and described in Table 8-57.

Return to the Table 8-23.

Figure 8-92. LDORTC_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							LDORTC_DIS
R/W-0h							R/W-0h

Table 8-57. LDORTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	LDORTC_DIS	R/W	0h	Disable LDORTC regulator: 0h = LDORTC regulator is enabled 1h = LDORTC regulator is disabled

8.7.1.34 LDO1_VOUT Register (Offset = 23h) [Reset = 00h]

LDO1_VOUT is shown in Figure 8-93 and described in Table 8-58.

Return to the Table 8-23.

Figure 8-93. LDO1_VOUT Register

7	6	5	4	3	2	1	0
LDO1_BYPASS	LDO1_VSET						RESERVED
R/W-0h	R/W-0h						R/W-0h

Table 8-58. LDO1_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO1_BYPASS	R/W	0h	Set LDO1 to bypass mode: (Default from NVM memory) 0h = LDO is set to linear regulator mode. 1h = LDO is set to bypass mode.
6-1	LDO1_VSET	R/W	0h	Voltage selection for LDO regulator. See LDO regulators chapter for voltage levels. (Default from NVM memory)
0	RESERVED	R/W	0h	

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8.7.1.35 LDO2_VOUT Register (Offset = 24h) [Reset = 00h]

LDO2_VOUT is shown in Figure 8-94 and described in Table 8-59.

Return to the Table 8-23.

Figure 8-94. LDO2_VOUT Register

7	6	5	4	3	2	1	0
LDO2_BYPASS	LDO2_VSET						RESERVED
R/W-0h	R/W-0h						R/W-0h

Table 8-59. LDO2_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO2_BYPASS	R/W	0h	Set LDO2 to bypass mode: (Default from NVM memory) 0h = LDO is set to linear regulator mode. 1h = LDO is set to bypass mode.
6-1	LDO2_VSET	R/W	0h	Voltage selection for LDO regulator. See LDO regulators chapter for voltage levels. (Default from NVM memory)
0	RESERVED	R/W	0h	

8.7.1.36 LDO3_VOUT Register (Offset = 25h) [Reset = 00h]

LDO3_VOUT is shown in Figure 8-95 and described in Table 8-60.

Return to the Table 8-23.

Figure 8-95. LDO3_VOUT Register

7	6	5	4	3	2	1	0
LDO3_BYPASS	LDO3_VSET						RESERVED
R/W-0h	R/W-0h						R/W-0h

Table 8-60. LDO3_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO3_BYPASS	R/W	0h	Set LDO3 to bypass mode: (Default from NVM memory) 0h = LDO is set to linear regulator mode. 1h = LDO is set to bypass mode.
6-1	LDO3_VSET	R/W	0h	Voltage selection for LDO regulator. See LDO regulators chapter for voltage levels. (Default from NVM memory)
0	RESERVED	R/W	0h	

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8.7.1.37 LDO4_VOUT Register (Offset = 26h) [Reset = 00h]

LDO4_VOUT is shown in Figure 8-96 and described in Table 8-61.

Return to the Table 8-23.

Figure 8-96. LDO4_VOUT Register

7	6	5	4	3	2	1	0
RESERVED	LDO4_VSET						
R/W-0h	R/W-0h						

Table 8-61. LDO4_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-0	LDO4_VSET	R/W	0h	Voltage selection for LDO regulator. See LDO regulators chapter for voltage levels. (Default from NVM memory)

8.7.1.38 LDO1_PG_WINDOW Register (Offset = 27h) [Reset = 00h]

LDO1_PG_WINDOW is shown in Figure 8-97 and described in Table 8-62.

Return to the Table 8-23.

Figure 8-97. LDO1_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		LDO1_UV_THR			LDO1_OV_THR		
R/W-0h		R/W-0h			R/W-0h		

Table 8-62. LDO1_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	LDO1_UV_THR	R/W	0h	Powergood low threshold level for LDO1: (Default from NVM memory) 0h = -3% / -30mV 1h = -3.5% / -35 mV 2h = -4% / -40 mV 3h = -5% / -50 mV 4h = -6% / -60 mV 5h = -7% / -70 mV 6h = -8% / -80 mV 7h = -10% / -100mV
2-0	LDO1_OV_THR	R/W	0h	Powergood high threshold level for LDO1: (Default from NVM memory) 0h = +3% / +30mV 1h = +3.5% / +35 mV 2h = +4% / +40 mV 3h = +5% / +50 mV 4h = +6% / +60 mV 5h = +7% / +70 mV 6h = +8% / +80 mV 7h = +10% / +100mV

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8.7.1.39 LDO2_PG_WINDOW Register (Offset = 28h) [Reset = 00h]

LDO2_PG_WINDOW is shown in Figure 8-98 and described in Table 8-63.

Return to the Table 8-23.

Figure 8-98. LDO2_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		LDO2_UV_THR			LDO2_OV_THR		
R/W-0h		R/W-0h			R/W-0h		

Table 8-63. LDO2_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	LDO2_UV_THR	R/W	0h	Powergood low threshold level for LDO2: (Default from NVM memory) 0h = -3% / -30mV 1h = -3.5% / -35 mV 2h = -4% / -40 mV 3h = -5% / -50 mV 4h = -6% / -60 mV 5h = -7% / -70 mV 6h = -8% / -80 mV 7h = -10% / -100mV
2-0	LDO2_OV_THR	R/W	0h	Powergood high threshold level for LDO2: (Default from NVM memory) 0h = +3% / +30mV 1h = +3.5% / +35 mV 2h = +4% / +40 mV 3h = +5% / +50 mV 4h = +6% / +60 mV 5h = +7% / +70 mV 6h = +8% / +80 mV 7h = +10% / +100mV

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8.7.1.40 LDO3_PG_WINDOW Register (Offset = 29h) [Reset = 00h]

LDO3_PG_WINDOW is shown in Figure 8-99 and described in Table 8-64.

Return to the Table 8-23.

Figure 8-99. LDO3_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		LDO3_UV_THR			LDO3_OV_THR		
R/W-0h		R/W-0h			R/W-0h		

Table 8-64. LDO3_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	LDO3_UV_THR	R/W	0h	Powergood low threshold level for LDO3: (Default from NVM memory) 0h = -3% / -30mV 1h = -3.5% / -35 mV 2h = -4% / -40 mV 3h = -5% / -50 mV 4h = -6% / -60 mV 5h = -7% / -70 mV 6h = -8% / -80 mV 7h = -10% / -100mV
2-0	LDO3_OV_THR	R/W	0h	Powergood high threshold level for LDO3: Default from NVM memory) 0h = +3% / +30mV 1h = +3.5% / +35 mV 2h = +4% / +40 mV 3h = +5% / +50 mV 4h = +6% / +60 mV 5h = +7% / +70 mV 6h = +8% / +80 mV 7h = +10% / +100mV

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8.7.1.41 LDO4_PG_WINDOW Register (Offset = 2Ah) [Reset = 00h]

LDO4_PG_WINDOW is shown in Figure 8-100 and described in Table 8-65.

Return to the Table 8-23.

Figure 8-100. LDO4_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED		LDO4_UV_THR			LDO4_OV_THR		
R/W-0h		R/W-0h			R/W-0h		

Table 8-65. LDO4_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	LDO4_UV_THR	R/W	0h	Powergood low threshold level for LDO4: (Default from NVM memory) 0h = -3% / -30mV 1h = -3.5% / -35 mV 2h = -4% / -40 mV 3h = -5% / -50 mV 4h = -6% / -60 mV 5h = -7% / -70 mV 6h = -8% / -80 mV 7h = -10% / -100mV
2-0	LDO4_OV_THR	R/W	0h	Powergood high threshold level for LDO4: (Default from NVM memory) 0h = +3% / +30mV 1h = +3.5% / +35 mV 2h = +4% / +40 mV 3h = +5% / +50 mV 4h = +6% / +60 mV 5h = +7% / +70 mV 6h = +8% / +80 mV 7h = +10% / +100mV

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8.7.1.42 VCCA_VMON_CTRL Register (Offset = 2Bh) [Reset = 00h]

VCCA_VMON_CTRL is shown in Figure 8-101 and described in Table 8-66.

Return to the Table 8-23.

Figure 8-101. VCCA_VMON_CTRL Register

7	6	5	4	3	2	1	0
RESERVED		VMON_DEGLITCH_SEL	RESERVED				VCCA_VMON_EN
R/W-0h		R/W-0h	R/W-0h				R/W-0h

Table 8-66. VCCA_VMON_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	VMON_DEGLITCH_SEL	R/W	0h	Deglitch time select for BUCKx_VMON, LDOx_VMON and VCCA_VMON (Default from NVM memory) 0h = 4 us 1h = 20 us
4-1	RESERVED	R/W	0h	
0	VCCA_VMON_EN	R/W	0h	Enable VCCA OV and UV comparators: (Default from NVM memory) 0h = OV and UV comparators are disabled 1h = OV and UV comparators are enabled.

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8.7.1.43 VCCA_PG_WINDOW Register (Offset = 2Ch) [Reset = 40h]

VCCA_PG_WINDOW is shown in Figure 8-102 and described in Table 8-67.

Return to the Table 8-23.

Figure 8-102. VCCA_PG_WINDOW Register

7	6	5	4	3	2	1	0
RESERVED	VCCA_PG_SET	VCCA_UV_THR			VCCA_OV_THR		
R/W-0h	R/W-1h	R/W-0h			R/W-0h		

Table 8-67. VCCA_PG_WINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	VCCA_PG_SET	R/W	1h	Powergood level for VCCA pin: (Default from NVM memory) 0h = 3.3 V 1h = 5.0 V
5-3	VCCA_UV_THR	R/W	0h	Powergood low threshold level for VCCA pin: (Default from NVM memory) 0h = -3% 1h = -3.5% 2h = -4% 3h = -5% 4h = -6% 5h = -7% 6h = -8% 7h = -10%
2-0	VCCA_OV_THR	R/W	0h	Powergood high threshold level for VCCA pin: (Default from NVM memory) 0h = +3% 1h = +3.5% 2h = +4% 3h = +5% 4h = +6% 5h = +7% 6h = +8% 7h = +10%

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8.7.1.44 GPIO1_CONF Register (Offset = 31h) [Reset = 0Ah]

GPIO1_CONF is shown in Figure 8-103 and described in Table 8-68.

Return to the Table 8-23.

Figure 8-103. GPIO1_CONF Register

7	6	5	4	3	2	1	0
GPIO1_SEL			GPIO1_DEGLITCH_EN	GPIO1_PU_PD_EN	GPIO1_PU_SEL	GPIO1_OD	GPIO1_DIR
R/W-0h			R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

Table 8-68. GPIO1_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	GPIO1_SEL	R/W	0h	GPIO1 signal function: (Default from NVM memory) 0h = GPIO1 1h = SCL_I2C2/CS_SPI 2h = NRSTOUT_SOC 3h = NRSTOUT_SOC 4h = NSLEEP1 5h = NSLEEP2 6h = WKUP1 7h = WKUP2
4	GPIO1_DEGLITCH_EN	R/W	0h	GPIO1 signal deglitch time when signal direction is input: (Default from NVM memory) 0h = No deglitch, only synchronization. 1h = 8 us deglitch time.
3	GPIO1_PU_PD_EN	R/W	1h	Control for GPIO1 pin pull-up/pull-down resistor: (Default from NVM memory) 0h = Pull-up/pull-down resistor disabled 1h = Pull-up/pull-down resistor enabled
2	GPIO1_PU_SEL	R/W	0h	Control for GPIO1 pin pull-up/pull-down resistor: GPIO1_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0h = Pull-down resistor selected 1h = Pull-up resistor selected
1	GPIO1_OD	R/W	1h	GPIO1 signal type when configured to output: (Default from NVM memory) 0h = Push-pull output 1h = Open-drain output
0	GPIO1_DIR	R/W	0h	GPIO1 signal direction: (Default from NVM memory) 0h = Input 1h = Output

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8.7.1.45 GPIO2_CONF Register (Offset = 32h) [Reset = 0Ah]

GPIO2_CONF is shown in Figure 8-104 and described in Table 8-69.

Return to the Table 8-23.

Figure 8-104. GPIO2_CONF Register

7	6	5	4	3	2	1	0
GPIO2_SEL			GPIO2_DEGLITCH_EN	GPIO2_PU_PD_EN	GPIO2_PU_SEL	GPIO2_OD	GPIO2_DIR
R/W-0h			R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

Table 8-69. GPIO2_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	GPIO2_SEL	R/W	0h	GPIO2 signal function: (Default from NVM memory) 0h = GPIO2 1h = TRIG_WDOG 2h = SDA_I2C2/SDO_SPI 3h = SDA_I2C2/SDO_SPI 4h = NSLEEP1 5h = NSLEEP2 6h = WKUP1 7h = WKUP2
4	GPIO2_DEGLITCH_EN	R/W	0h	GPIO2 signal deglitch time when signal direction is input: (Default from NVM memory) 0h = No deglitch, only synchronization. 1h = 8 us deglitch time.
3	GPIO2_PU_PD_EN	R/W	1h	Control for GPIO2 pin pull-up/pull-down resistor: (Default from NVM memory) 0h = Pull-up/pull-down resistor disabled 1h = Pull-up/pull-down resistor enabled
2	GPIO2_PU_SEL	R/W	0h	Control for GPIO2 pin pull-up/pull-down resistor: GPIO2_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0h = Pull-down resistor selected 1h = Pull-up resistor selected
1	GPIO2_OD	R/W	1h	GPIO2 signal type when configured to output: (Default from NVM memory) 0h = Push-pull output 1h = Open-drain output
0	GPIO2_DIR	R/W	0h	GPIO2 signal direction: (Default from NVM memory) 0h = Input 1h = Output

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8.7.1.46 GPIO3_CONF Register (Offset = 33h) [Reset = 0Ah]

GPIO3_CONF is shown in Figure 8-105 and described in Table 8-70.

Return to the Table 8-23.

Figure 8-105. GPIO3_CONF Register

7	6	5	4	3	2	1	0
GPIO3_SEL			GPIO3_DEGLITCH_EN	GPIO3_PU_PD_EN	GPIO3_PU_SEL	GPIO3_OD	GPIO3_DIR
R/W-0h			R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

Table 8-70. GPIO3_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	GPIO3_SEL	R/W	0h	GPIO3 signal function: (Default from NVM memory) 0h = GPIO3 1h = CLK32KOUT 2h = NERR_SOC 3h = NERR_SOC 4h = NSLEEP1 5h = NSLEEP2 6h = LP_WKUP1 7h = LP_WKUP2
4	GPIO3_DEGLITCH_EN	R/W	0h	GPIO3 signal deglitch time when signal direction is input: (Default from NVM memory) 0h = No deglitch, only synchronization. 1h = 8 us deglitch time.
3	GPIO3_PU_PD_EN	R/W	1h	Control for GPIO3 pin pull-up/pull-down resistor: (Default from NVM memory) 0h = Pull-up/pull-down resistor disabled 1h = Pull-up/pull-down resistor enabled
2	GPIO3_PU_SEL	R/W	0h	Control for GPIO3 pin pull-up/pull-down resistor: GPIO3_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0h = Pull-down resistor selected 1h = Pull-up resistor selected
1	GPIO3_OD	R/W	1h	GPIO3 signal type when configured to output: (Default from NVM memory) 0h = Push-pull output 1h = Open-drain output
0	GPIO3_DIR	R/W	0h	GPIO3 signal direction: (Default from NVM memory) 0h = Input 1h = Output

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8.7.1.47 GPIO4_CONF Register (Offset = 34h) [Reset = 0Ah]

GPIO4_CONF is shown in Figure 8-106 and described in Table 8-71.

Return to the Table 8-23.

Figure 8-106. GPIO4_CONF Register

7	6	5	4	3	2	1	0
GPIO4_SEL			GPIO4_DEGLITCH_EN	GPIO4_PU_PD_EN	GPIO4_PU_SEL	GPIO4_OD	GPIO4_DIR
R/W-0h			R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

Table 8-71. GPIO4_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	GPIO4_SEL	R/W	0h	GPIO4 signal function: (Default from NVM memory) 0h = GPIO4 1h = CLK32KOUT 2h = CLK32KOUT 3h = CLK32KOUT 4h = NSLEEP1 5h = NSLEEP2 6h = LP_WKUP1 7h = LP_WKUP2
4	GPIO4_DEGLITCH_EN	R/W	0h	GPIO4 signal deglitch time when signal direction is input: (Default from NVM memory) 0h = No deglitch, only synchronization. 1h = 8 us deglitch time.
3	GPIO4_PU_PD_EN	R/W	1h	Control for GPIO4 pin pull-up/pull-down resistor: (Default from NVM memory) 0h = Pull-up/pull-down resistor disabled 1h = Pull-up/pull-down resistor enabled
2	GPIO4_PU_SEL	R/W	0h	Control for GPIO4 pin pull-up/pull-down resistor: GPIO4_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0h = Pull-down resistor selected 1h = Pull-up resistor selected
1	GPIO4_OD	R/W	1h	GPIO4 signal type when configured to output: (Default from NVM memory) 0h = Push-pull output 1h = Open-drain output
0	GPIO4_DIR	R/W	0h	GPIO4 signal direction: (Default from NVM memory) 0h = Input 1h = Output

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8.7.1.48 GPIO5_CONF Register (Offset = 35h) [Reset = 0Ah]

GPIO5_CONF is shown in Figure 8-107 and described in Table 8-72.

Return to the Table 8-23.

Figure 8-107. GPIO5_CONF Register

7	6	5	4	3	2	1	0
GPIO5_SEL			GPIO5_DEGLITCH_EN	GPIO5_PU_PD_EN	GPIO5_PU_SEL	GPIO5_OD	GPIO5_DIR
R/W-0h			R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

Table 8-72. GPIO5_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	GPIO5_SEL	R/W	0h	GPIO5 signal function: (Default from NVM memory) 0h = GPIO5 1h = SCLK_SPMI 2h = SCLK_SPMI 3h = SCLK_SPMI 4h = NSLEEP1 5h = NSLEEP2 6h = WKUP1 7h = WKUP2
4	GPIO5_DEGLITCH_EN	R/W	0h	GPIO5 signal deglitch time when signal direction is input: (Default from NVM memory) 0h = No deglitch, only synchronization. 1h = 8 us deglitch time.
3	GPIO5_PU_PD_EN	R/W	1h	Control for GPIO5 pin pull-up/pull-down resistor: (Default from NVM memory) 0h = Pull-up/pull-down resistor disabled 1h = Pull-up/pull-down resistor enabled
2	GPIO5_PU_SEL	R/W	0h	Control for GPIO5 pin pull-up/pull-down resistor: GPIO5_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0h = Pull-down resistor selected 1h = Pull-up resistor selected
1	GPIO5_OD	R/W	1h	GPIO5 signal type when configured to output: (Default from NVM memory) 0h = Push-pull output 1h = Open-drain output
0	GPIO5_DIR	R/W	0h	GPIO5 signal direction: (Default from NVM memory) 0h = Input 1h = Output

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8.7.1.49 GPIO6_CONF Register (Offset = 36h) [Reset = 0Ah]

GPIO6_CONF is shown in Figure 8-108 and described in Table 8-73.

Return to the Table 8-23.

Figure 8-108. GPIO6_CONF Register

7	6	5	4	3	2	1	0
GPIO6_SEL			GPIO6_DEGLITCH_EN	GPIO6_PU_PD_EN	GPIO6_PU_SEL	GPIO6_OD	GPIO6_DIR
R/W-0h			R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

Table 8-73. GPIO6_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	GPIO6_SEL	R/W	0h	GPIO6 signal function: (Default from NVM memory) 0h = GPIO6 1h = SDATA_SPMI 2h = SDATA_SPMI 3h = SDATA_SPMI 4h = NSLEEP1 5h = NSLEEP2 6h = WKUP1 7h = WKUP2
4	GPIO6_DEGLITCH_EN	R/W	0h	GPIO6 signal deglitch time when signal direction is input: (Default from NVM memory) 0h = No deglitch, only synchronization. 1h = 8 us deglitch time.
3	GPIO6_PU_PD_EN	R/W	1h	Control for GPIO6 pin pull-up/pull-down resistor: (Default from NVM memory) 0h = Pull-up/pull-down resistor disabled 1h = Pull-up/pull-down resistor enabled
2	GPIO6_PU_SEL	R/W	0h	Control for GPIO6 pin pull-up/pull-down resistor: GPIO6_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0h = Pull-down resistor selected 1h = Pull-up resistor selected
1	GPIO6_OD	R/W	1h	GPIO6 signal type when configured to output: (Default from NVM memory) 0h = Push-pull output 1h = Open-drain output
0	GPIO6_DIR	R/W	0h	GPIO6 signal direction: (Default from NVM memory) 0h = Input 1h = Output

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8.7.1.50 GPIO7_CONF Register (Offset = 37h) [Reset = 0Ah]

GPIO7_CONF is shown in Figure 8-109 and described in Table 8-74.

Return to the Table 8-23.

Figure 8-109. GPIO7_CONF Register

7	6	5	4	3	2	1	0
GPIO7_SEL			GPIO7_DEGLITCH_EN	GPIO7_PU_PD_EN	GPIO7_PU_SEL	GPIO7_OD	GPIO7_DIR
R/W-0h			R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

Table 8-74. GPIO7_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	GPIO7_SEL	R/W	0h	GPIO7 signal function: (Default from NVM memory) 0h = GPIO7 1h = NERR_MCU 2h = NERR_MCU 3h = NERR_MCU 4h = NSLEEP1 5h = NSLEEP2 6h = WKUP1 7h = WKUP2
4	GPIO7_DEGLITCH_EN	R/W	0h	GPIO7 signal deglitch time when signal direction is input: (Default from NVM memory) 0h = No deglitch, only synchronization. 1h = 8 us deglitch time.
3	GPIO7_PU_PD_EN	R/W	1h	Control for GPIO7 pin pull-up/pull-down resistor: (Default from NVM memory) 0h = Pull-up/pull-down resistor disabled 1h = Pull-up/pull-down resistor enabled
2	GPIO7_PU_SEL	R/W	0h	Control for GPIO7 pin pull-up/pull-down resistor: GPIO7_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0h = Pull-down resistor selected 1h = Pull-up resistor selected
1	GPIO7_OD	R/W	1h	GPIO7 signal type when configured to output: (Default from NVM memory) 0h = Push-pull output 1h = Open-drain output
0	GPIO7_DIR	R/W	0h	GPIO7 signal direction: (Default from NVM memory) 0h = Input 1h = Output

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8.7.1.51 GPIO8_CONF Register (Offset = 38h) [Reset = 0Ah]

GPIO8_CONF is shown in Figure 8-110 and described in Table 8-75.

Return to the Table 8-23.

Figure 8-110. GPIO8_CONF Register

7	6	5	4	3	2	1	0
GPIO8_SEL			GPIO8_DEGLITCH_EN	GPIO8_PU_PD_EN	GPIO8_PU_SEL	GPIO8_OD	GPIO8_DIR
R/W-0h			R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

Table 8-75. GPIO8_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	GPIO8_SEL	R/W	0h	GPIO8 signal function: (Default from NVM memory) 0h = GPIO8 1h = CLK32KOUT 2h = SYNCCLKOUT 3h = DISABLE_WDOG 4h = NSLEEP1 5h = NSLEEP2 6h = WKUP1 7h = WKUP2
4	GPIO8_DEGLITCH_EN	R/W	0h	GPIO8 signal deglitch time when signal direction is input: (Default from NVM memory) 0h = No deglitch, only synchronization. 1h = 8 us deglitch time.
3	GPIO8_PU_PD_EN	R/W	1h	Control for GPIO8 pin pull-up/pull-down resistor: (Default from NVM memory) 0h = Pull-up/pull-down resistor disabled 1h = Pull-up/pull-down resistor enabled
2	GPIO8_PU_SEL	R/W	0h	Control for GPIO8 pin pull-up/pull-down resistor: GPIO8_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0h = Pull-down resistor selected 1h = Pull-up resistor selected
1	GPIO8_OD	R/W	1h	GPIO8 signal type when configured to output: (Default from NVM memory) 0h = Push-pull output 1h = Open-drain output
0	GPIO8_DIR	R/W	0h	GPIO8 signal direction: (Default from NVM memory) 0h = Input 1h = Output

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8.7.1.52 GPIO9_CONF Register (Offset = 39h) [Reset = 0Ah]

GPIO9_CONF is shown in Figure 8-111 and described in Table 8-76.

Return to the Table 8-23.

Figure 8-111. GPIO9_CONF Register

7	6	5	4	3	2	1	0
GPIO9_SEL			GPIO9_DEGLITCH_EN	GPIO9_PU_PD_EN	GPIO9_PU_SEL	GPIO9_OD	GPIO9_DIR
R/W-0h			R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

Table 8-76. GPIO9_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	GPIO9_SEL	R/W	0h	GPIO9 signal function: (Default from NVM memory) 0h = GPIO9 1h = PGOOD 2h = DISABLE_WDOG 3h = SYNCCLKOUT 4h = NSLEEP1 5h = NSLEEP2 6h = WKUP1 7h = WKUP2
4	GPIO9_DEGLITCH_EN	R/W	0h	GPIO9 signal deglitch time when signal direction is input: (Default from NVM memory) 0h = No deglitch, only synchronization. 1h = 8 us deglitch time.
3	GPIO9_PU_PD_EN	R/W	1h	Control for GPIO9 pin pull-up/pull-down resistor: (Default from NVM memory) 0h = Pull-up/pull-down resistor disabled 1h = Pull-up/pull-down resistor enabled
2	GPIO9_PU_SEL	R/W	0h	Control for GPIO9 pin pull-up/pull-down resistor: GPIO9_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0h = Pull-down resistor selected 1h = Pull-up resistor selected
1	GPIO9_OD	R/W	1h	GPIO9 signal type when configured to output: (Default from NVM memory) 0h = Push-pull output 1h = Open-drain output
0	GPIO9_DIR	R/W	0h	GPIO9 signal direction: (Default from NVM memory) 0h = Input 1h = Output

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8.7.1.53 GPIO10_CONF Register (Offset = 3Ah) [Reset = 0Ah]

GPIO10_CONF is shown in Figure 8-112 and described in Table 8-77.

Return to the Table 8-23.

Figure 8-112. GPIO10_CONF Register

7	6	5	4	3	2	1	0
GPIO10_SEL			GPIO10_DEGLITCH_EN	GPIO10_PU_PD_EN	GPIO10_PU_SEL	GPIO10_OD	GPIO10_DIR
R/W-0h			R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

Table 8-77. GPIO10_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	GPIO10_SEL	R/W	0h	GPIO10 signal function: (Default from NVM memory) 0h = GPIO10 1h = SYNCCLKIN 2h = SYNCCLKOUT 3h = CLK32KOUT 4h = NSLEEP1 5h = NSLEEP2 6h = WKUP1 7h = WKUP2
4	GPIO10_DEGLITCH_EN	R/W	0h	GPIO10 signal deglitch time when signal direction is input: (Default from NVM memory) 0h = No deglitch, only synchronization. 1h = 8 us deglitch time.
3	GPIO10_PU_PD_EN	R/W	1h	Control for GPIO10 pin pull-up/pull-down resistor: (Default from NVM memory) 0h = Pull-up/pull-down resistor disabled 1h = Pull-up/pull-down resistor enabled
2	GPIO10_PU_SEL	R/W	0h	Control for GPIO10 pin pull-up/pull-down resistor: GPIO10_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0h = Pull-down resistor selected 1h = Pull-up resistor selected
1	GPIO10_OD	R/W	1h	GPIO10 signal type when configured to output: (Default from NVM memory) 0h = Push-pull output 1h = Open-drain output
0	GPIO10_DIR	R/W	0h	GPIO10 signal direction: (Default from NVM memory) 0h = Input 1h = Output

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8.7.1.54 GPIO11_CONF Register (Offset = 3Bh) [Reset = 0Ah]

GPIO11_CONF is shown in Figure 8-113 and described in Table 8-78.

Return to the Table 8-23.

Figure 8-113. GPIO11_CONF Register

7	6	5	4	3	2	1	0
GPIO11_SEL			GPIO11_DEGLITCH_EN	GPIO11_PU_PD_EN	GPIO11_PU_SEL	GPIO11_OD	GPIO11_DIR
R/W-0h			R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

Table 8-78. GPIO11_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	GPIO11_SEL	R/W	0h	GPIO11 signal function: (Default from NVM memory) 0h = GPIO11 1h = TRIG_WDOG 2h = NRSTOUT_SOC 3h = NRSTOUT_SOC 4h = NSLEEP1 5h = NSLEEP2 6h = WKUP1 7h = WKUP2
4	GPIO11_DEGLITCH_EN	R/W	0h	GPIO11 signal deglitch time when signal direction is input: (Default from NVM memory) 0h = No deglitch, only synchronization. 1h = 8 us deglitch time.
3	GPIO11_PU_PD_EN	R/W	1h	Control for GPIO11 pin pull-up/pull-down resistor: (Default from NVM memory) 0h = Pull-up/pull-down resistor disabled 1h = Pull-up/pull-down resistor enabled
2	GPIO11_PU_SEL	R/W	0h	Control for GPIO11 pin pull-up/pull-down resistor: GPIO11_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0h = Pull-down resistor selected 1h = Pull-up resistor selected
1	GPIO11_OD	R/W	1h	GPIO11 signal type when configured to output: (Default from NVM memory) 0h = Push-pull output 1h = Open-drain output
0	GPIO11_DIR	R/W	0h	GPIO11 signal direction: (Default from NVM memory) 0h = Input 1h = Output

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8.7.1.55 NPWRON_CONF Register (Offset = 3Ch) [Reset = 88h]

NPWRON_CONF is shown in Figure 8-114 and described in Table 8-79.

Return to the Table 8-23.

Figure 8-114. NPWRON_CONF Register

7	6	5	4	3	2	1	0
NPWRON_SEL		ENABLE_POL	ENABLE_DEGLITCH_EN	ENABLE_PU_PD_EN	ENABLE_PU_SEL	RESERVED	NRSTOUT_OD
R/W-2h		R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

Table 8-79. NPWRON_CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	NPWRON_SEL	R/W	2h	NPWRON/ENABLE signal function: (Default from NVM memory) 0h = ENABLE 1h = NPWRON 2h = None 3h = None
5	ENABLE_POL	R/W	0h	Control for ENABLE pin polarity: (Default from NVM memory) 0h = Active high 1h = Active low
4	ENABLE_DEGLITCH_EN	R/W	0h	NPWRON/ENABLE signal deglitch time: (Default from NVM memory) 0h = No deglitch, only synchronization. 1h = 8 us deglitch time when ENABLE, 50 ms deglitch time when NPWRON.
3	ENABLE_PU_PD_EN	R/W	1h	Control for NPWRON/ENABLE pin pull-up resistor: (Default from NVM memory) 0h = Pull-up/pull-down resistor disabled 1h = Pull-up/pull-down resistor enabled
2	ENABLE_PU_SEL	R/W	0h	Control for NPWRON/ENABLE pin pull-down resistor: ENABLE_PU_PD_EN must be 1 to select the resistor. (Default from NVM memory) 0h = Pull-down resistor selected 1h = Pull-up resistor selected
1	RESERVED	R/W	0h	
0	NRSTOUT_OD	R/W	0h	NRSTOUT signal type: (Default from NVM memory) 0h = Push-pull output 1h = Open-drain output

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8.7.1.56 GPIO_OUT_1 Register (Offset = 3Dh) [Reset = 00h]

GPIO_OUT_1 is shown in Figure 8-115 and described in Table 8-80.

Return to the Table 8-23.

Figure 8-115. GPIO_OUT_1 Register

7	6	5	4	3	2	1	0
GPIO8_OUT	GPIO7_OUT	GPIO6_OUT	GPIO5_OUT	GPIO4_OUT	GPIO3_OUT	GPIO2_OUT	GPIO1_OUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-80. GPIO_OUT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_OUT	R/W	0h	Control for GPIO8 signal when configured to GPIO Output: (Default from NVM memory) 0h = Low 1h = High
6	GPIO7_OUT	R/W	0h	Control for GPIO7 signal when configured to GPIO Output: (Default from NVM memory) 0h = Low 1h = High
5	GPIO6_OUT	R/W	0h	Control for GPIO6 signal when configured to GPIO Output: (Default from NVM memory) 0h = Low 1h = High
4	GPIO5_OUT	R/W	0h	Control for GPIO5 signal when configured to GPIO Output: (Default from NVM memory) 0h = Low 1h = High
3	GPIO4_OUT	R/W	0h	Control for GPIO4 signal when configured to GPIO Output: (Default from NVM memory) 0h = Low 1h = High
2	GPIO3_OUT	R/W	0h	Control for GPIO3 signal when configured to GPIO Output: (Default from NVM memory) 0h = Low 1h = High
1	GPIO2_OUT	R/W	0h	Control for GPIO2 signal when configured to GPIO Output: (Default from NVM memory) 0h = Low 1h = High
0	GPIO1_OUT	R/W	0h	Control for GPIO1 signal when configured to GPIO Output: (Default from NVM memory) 0h = Low 1h = High

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8.7.1.57 GPIO_OUT_2 Register (Offset = 3Eh) [Reset = 00h]

GPIO_OUT_2 is shown in Figure 8-116 and described in Table 8-81.

Return to the Table 8-23.

Figure 8-116. GPIO_OUT_2 Register

7	6	5	4	3	2	1	0
RESERVED					GPIO11_OUT	GPIO10_OUT	GPIO9_OUT
R/W-0h					R/W-0h	R/W-0h	R/W-0h

Table 8-81. GPIO_OUT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	GPIO11_OUT	R/W	0h	Control for GPIO11 signal when configured to GPIO Output: (Default from NVM memory) 0h = Low 1h = High
1	GPIO10_OUT	R/W	0h	Control for GPIO10 signal when configured to GPIO Output: (Default from NVM memory) 0h = Low 1h = High
0	GPIO9_OUT	R/W	0h	Control for GPIO9 signal when configured to GPIO Output: (Default from NVM memory) 0h = Low 1h = High

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8.7.1.58 GPIO_IN_1 Register (Offset = 3Fh) [Reset = 00h]

GPIO_IN_1 is shown in Figure 8-117 and described in Table 8-82.

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Figure 8-117. GPIO_IN_1 Register

7	6	5	4	3	2	1	0
GPIO8_IN	GPIO7_IN	GPIO6_IN	GPIO5_IN	GPIO4_IN	GPIO3_IN	GPIO2_IN	GPIO1_IN
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-82. GPIO_IN_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_IN	R	0h	Level of GPIO8 signal: 0h = Low 1h = High
6	GPIO7_IN	R	0h	Level of GPIO7 signal: 0h = Low 1h = High
5	GPIO6_IN	R	0h	Level of GPIO6 signal: 0h = Low 1h = High
4	GPIO5_IN	R	0h	Level of GPIO5 signal: 0h = Low 1h = High
3	GPIO4_IN	R	0h	Level of GPIO4 signal: 0h = Low 1h = High
2	GPIO3_IN	R	0h	Level of GPIO3 signal: 0h = Low 1h = High
1	GPIO2_IN	R	0h	Level of GPIO2 signal: 0h = Low 1h = High
0	GPIO1_IN	R	0h	Level of GPIO1 signal: 0h = Low 1h = High

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8.7.1.59 GPIO_IN_2 Register (Offset = 40h) [Reset = 00h]

GPIO_IN_2 is shown in Figure 8-118 and described in Table 8-83.

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Figure 8-118. GPIO_IN_2 Register

7	6	5	4	3	2	1	0
RESERVED				NPWRON_IN	GPIO11_IN	GPIO10_IN	GPIO9_IN
R-0h				R-0h	R-0h	R-0h	R-0h

Table 8-83. GPIO_IN_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	NPWRON_IN	R	0h	Level of NPWRON/ENABLE signal: 0h = Low 1h = High
2	GPIO11_IN	R	0h	Level of GPIO11 signal: 0h = Low 1h = High
1	GPIO10_IN	R	0h	Level of GPIO10 signal: 0h = Low 1h = High
0	GPIO9_IN	R	0h	Level of GPIO9 signal: 0h = Low 1h = High

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8.7.1.60 RAIL_SEL_1 Register (Offset = 41h) [Reset = 00h]

RAIL_SEL_1 is shown in Figure 8-119 and described in Table 8-84.

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Figure 8-119. RAIL_SEL_1 Register

7	6	5	4	3	2	1	0
BUCK4_GRP_SEL		BUCK3_GRP_SEL		BUCK2_GRP_SEL		BUCK1_GRP_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 8-84. RAIL_SEL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BUCK4_GRP_SEL	R/W	0h	Rail group selection for BUCK4: (Default from NVM memory) 0h = No group assigned 1h = MCU rail group 2h = SOC rail group 3h = OTHER rail group
5-4	BUCK3_GRP_SEL	R/W	0h	Rail group selection for BUCK3: (Default from NVM memory) 0h = No group assigned 1h = MCU rail group 2h = SOC rail group 3h = OTHER rail group
3-2	BUCK2_GRP_SEL	R/W	0h	Rail group selection for BUCK2: (Default from NVM memory) 0h = No group assigned 1h = MCU rail group 2h = SOC rail group 3h = OTHER rail group
1-0	BUCK1_GRP_SEL	R/W	0h	Rail group selection for BUCK1: (Default from NVM memory) 0h = No group assigned 1h = MCU rail group 2h = SOC rail group 3h = OTHER rail group

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8.7.1.61 RAIL_SEL_2 Register (Offset = 42h) [Reset = 00h]

RAIL_SEL_2 is shown in Figure 8-120 and described in Table 8-85.

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Figure 8-120. RAIL_SEL_2 Register

7	6	5	4	3	2	1	0
LDO3_GRP_SEL		LDO2_GRP_SEL		LDO1_GRP_SEL		BUCK5_GRP_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 8-85. RAIL_SEL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LDO3_GRP_SEL	R/W	0h	Rail group selection for LDO3: (Default from NVM memory) 0h = No group assigned 1h = MCU rail group 2h = SOC rail group 3h = OTHER rail group
5-4	LDO2_GRP_SEL	R/W	0h	Rail group selection for LDO2: (Default from NVM memory) 0h = No group assigned 1h = MCU rail group 2h = SOC rail group 3h = OTHER rail group
3-2	LDO1_GRP_SEL	R/W	0h	Rail group selection for LDO1: (Default from NVM memory) 0h = No group assigned 1h = MCU rail group 2h = SOC rail group 3h = OTHER rail group
1-0	BUCK5_GRP_SEL	R/W	0h	Rail group selection for BUCK5: (Default from NVM memory) 0h = No group assigned 1h = MCU rail group 2h = SOC rail group 3h = OTHER rail group

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8.7.1.62 RAIL_SEL_3 Register (Offset = 43h) [Reset = 00h]

RAIL_SEL_3 is shown in Figure 8-121 and described in Table 8-86.

Return to the Table 8-23.

Figure 8-121. RAIL_SEL_3 Register

7	6	5	4	3	2	1	0
RESERVED				VCCA_GRP_SEL		LDO4_GRP_SEL	
R/W-0h				R/W-0h		R/W-0h	

Table 8-86. RAIL_SEL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3-2	VCCA_GRP_SEL	R/W	0h	Rail group selection for VCCA monitoring: (Default from NVM memory) 0h = No group assigned 1h = MCU rail group 2h = SOC rail group 3h = OTHER rail group
1-0	LDO4_GRP_SEL	R/W	0h	Rail group selection for LDO4: (Default from NVM memory) 0h = No group assigned 1h = MCU rail group 2h = SOC rail group 3h = OTHER rail group

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8.7.1.63 FSM_TRIG_SEL_1 Register (Offset = 44h) [Reset = 00h]

FSM_TRIG_SEL_1 is shown in Figure 8-122 and described in Table 8-87.

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Figure 8-122. FSM_TRIG_SEL_1 Register

7	6	5	4	3	2	1	0
SEVERE_ERR_TRIG		OTHER_RAIL_TRIG		SOC_RAIL_TRIG		MCU_RAIL_TRIG	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 8-87. FSM_TRIG_SEL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SEVERE_ERR_TRIG	R/W	0h	Trigger selection for Severe Error: (Default from NVM memory) 0h = Immediate shutdown 1h = Orderly shutdown 2h = MCU power error 3h = SOC power error
5-4	OTHER_RAIL_TRIG	R/W	0h	Trigger selection for OTHER rail group: (Default from NVM memory) 0h = Immediate shutdown 1h = Orderly shutdown 2h = MCU power error 3h = SOC power error
3-2	SOC_RAIL_TRIG	R/W	0h	Trigger selection for SOC rail group: (Default from NVM memory) 0h = Immediate shutdown 1h = Orderly shutdown 2h = MCU power error 3h = SOC power error
1-0	MCU_RAIL_TRIG	R/W	0h	Trigger selection for MCU rail group: (Default from NVM memory) 0h = Immediate shutdown 1h = Orderly shutdown 2h = MCU power error 3h = SOC power error

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8.7.1.64 FSM_TRIG_SEL_2 Register (Offset = 45h) [Reset = 00h]

FSM_TRIG_SEL_2 is shown in Figure 8-123 and described in Table 8-88.

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Figure 8-123. FSM_TRIG_SEL_2 Register

7	6	5	4	3	2	1	0
RESERVED						MODERATE_ERR_TRIG	
R/W-0h						R/W-0h	

Table 8-88. FSM_TRIG_SEL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1-0	MODERATE_ERR_TRIG	R/W	0h	Trigger selection for Moderate Error: (Default from NVM memory) 0h = Immediate shutdown 1h = Orderly shutdown 2h = MCU power error 3h = SOC power error

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8.7.1.65 FSM_TRIG_MASK_1 Register (Offset = 46h) [Reset = 00h]

FSM_TRIG_MASK_1 is shown in Figure 8-124 and described in Table 8-89.

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Figure 8-124. FSM_TRIG_MASK_1 Register

7	6	5	4	3	2	1	0
GPIO4_FSM_MASK_POL	GPIO4_FSM_MASK	GPIO3_FSM_MASK_POL	GPIO3_FSM_MASK	GPIO2_FSM_MASK_POL	GPIO2_FSM_MASK	GPIO1_FSM_MASK_POL	GPIO1_FSM_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-89. FSM_TRIG_MASK_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO4_FSM_MASK_POL	R/W	0h	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0h = Masking sets signal value to '0' 1h = Masking sets signal value to '1'
6	GPIO4_FSM_MASK	R/W	0h	FSM trigger mask for GPIOx: (Default from NVM memory) 0h = Not masked 1h = Masked
5	GPIO3_FSM_MASK_POL	R/W	0h	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0h = Masking sets signal value to '0' 1h = Masking sets signal value to '1'
4	GPIO3_FSM_MASK	R/W	0h	FSM trigger mask for GPIOx: (Default from NVM memory) 0h = Not masked 1h = Masked
3	GPIO2_FSM_MASK_POL	R/W	0h	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0h = Masking sets signal value to '0' 1h = Masking sets signal value to '1'
2	GPIO2_FSM_MASK	R/W	0h	FSM trigger mask for GPIOx: (Default from NVM memory) 0h = Not masked 1h = Masked
1	GPIO1_FSM_MASK_POL	R/W	0h	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0h = Masking sets signal value to '0' 1h = Masking sets signal value to '1'
0	GPIO1_FSM_MASK	R/W	0h	FSM trigger mask for GPIOx: (Default from NVM memory) 0h = Not masked 1h = Masked

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8.7.1.66 FSM_TRIG_MASK_2 Register (Offset = 47h) [Reset = 00h]

FSM_TRIG_MASK_2 is shown in Figure 8-125 and described in Table 8-90.

Return to the Table 8-23.

Figure 8-125. FSM_TRIG_MASK_2 Register

7	6	5	4	3	2	1	0
GPIO8_FSM_MASK_POL	GPIO8_FSM_MASK	GPIO7_FSM_MASK_POL	GPIO7_FSM_MASK	GPIO6_FSM_MASK_POL	GPIO6_FSM_MASK	GPIO5_FSM_MASK_POL	GPIO5_FSM_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-90. FSM_TRIG_MASK_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_FSM_MASK_POL	R/W	0h	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0h = Masking sets signal value to '0' 1h = Masking sets signal value to '1'
6	GPIO8_FSM_MASK	R/W	0h	FSM trigger mask for GPIOx: (Default from NVM memory) 0h = Not masked 1h = Masked
5	GPIO7_FSM_MASK_POL	R/W	0h	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0h = Masking sets signal value to '0' 1h = Masking sets signal value to '1'
4	GPIO7_FSM_MASK	R/W	0h	FSM trigger mask for GPIOx: (Default from NVM memory) 0h = Not masked 1h = Masked
3	GPIO6_FSM_MASK_POL	R/W	0h	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0h = Masking sets signal value to '0' 1h = Masking sets signal value to '1'
2	GPIO6_FSM_MASK	R/W	0h	FSM trigger mask for GPIOx: (Default from NVM memory) 0h = Not masked 1h = Masked
1	GPIO5_FSM_MASK_POL	R/W	0h	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0h = Masking sets signal value to '0' 1h = Masking sets signal value to '1'
0	GPIO5_FSM_MASK	R/W	0h	FSM trigger mask for GPIOx: (Default from NVM memory) 0h = Not masked 1h = Masked

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8.7.1.67 FSM_TRIG_MASK_3 Register (Offset = 48h) [Reset = 00h]

FSM_TRIG_MASK_3 is shown in Figure 8-126 and described in Table 8-91.

Return to the Table 8-23.

Figure 8-126. FSM_TRIG_MASK_3 Register

7	6	5	4	3	2	1	0
RESERVED		GPIO11_FSM_MASK_POL	GPIO11_FSM_MASK	GPIO10_FSM_MASK_POL	GPIO10_FSM_MASK	GPIO9_FSM_MASK_POL	GPIO9_FSM_MASK
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-91. FSM_TRIG_MASK_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	GPIO11_FSM_MASK_POL	R/W	0h	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0h = Masking sets signal value to '0' 1h = Masking sets signal value to '1'
4	GPIO11_FSM_MASK	R/W	0h	FSM trigger mask for GPIOx: (Default from NVM memory) 0h = Not masked 1h = Masked
3	GPIO10_FSM_MASK_POL	R/W	0h	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0h = Masking sets signal value to '0' 1h = Masking sets signal value to '1'
2	GPIO10_FSM_MASK	R/W	0h	FSM trigger mask for GPIOx: (Default from NVM memory) 0h = Not masked 1h = Masked
1	GPIO9_FSM_MASK_POL	R/W	0h	FSM trigger masking polarity select for GPIOx: (Default from NVM memory) 0h = Masking sets signal value to '0' 1h = Masking sets signal value to '1'
0	GPIO9_FSM_MASK	R/W	0h	FSM trigger mask for GPIOx: (Default from NVM memory) 0h = Not masked 1h = Masked

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8.7.1.68 MASK_BUCK1_2 Register (Offset = 49h) [Reset = 00h]

MASK_BUCK1_2 is shown in Figure 8-127 and described in Table 8-92.

Return to the Table 8-23.

Figure 8-127. MASK_BUCK1_2 Register

7	6	5	4	3	2	1	0
BUCK2_ILIM_MASK	RESERVED	BUCK2_UV_MASK	BUCK2_OV_MASK	BUCK1_ILIM_MASK	RESERVED	BUCK1_UV_MASK	BUCK1_OV_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-92. MASK_BUCK1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK2_ILIM_MASK	R/W	0h	Masking for BUCK2 current monitoring interrupt BUCK2_ILIM_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
6	RESERVED	R/W	0h	
5	BUCK2_UV_MASK	R/W	0h	Masking of BUCK2 under-voltage detection interrupt BUCK2_UV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
4	BUCK2_OV_MASK	R/W	0h	Masking of BUCK2 over-voltage detection interrupt BUCK2_OV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
3	BUCK1_ILIM_MASK	R/W	0h	Masking for BUCK1 current monitoring interrupt BUCK1_ILIM_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
2	RESERVED	R/W	0h	
1	BUCK1_UV_MASK	R/W	0h	Masking of BUCK1 under-voltage detection interrupt BUCK1_UV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	BUCK1_OV_MASK	R/W	0h	Masking of BUCK1 over-voltage detection interrupt BUCK1_OV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.69 MASK_BUCK3_4 Register (Offset = 4Ah) [Reset = 00h]

MASK_BUCK3_4 is shown in Figure 8-128 and described in Table 8-93.

Return to the Table 8-23.

Figure 8-128. MASK_BUCK3_4 Register

7	6	5	4	3	2	1	0
BUCK4_ILIM_MASK	RESERVED	BUCK4_UV_MASK	BUCK4_OV_MASK	BUCK3_ILIM_MASK	RESERVED	BUCK3_UV_MASK	BUCK3_OV_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-93. MASK_BUCK3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK4_ILIM_MASK	R/W	0h	Masking for BUCK4 current monitoring interrupt BUCK4_ILIM_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
6	RESERVED	R/W	0h	
5	BUCK4_UV_MASK	R/W	0h	Masking of BUCK4 under-voltage detection interrupt BUCK4_UV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
4	BUCK4_OV_MASK	R/W	0h	Masking of BUCK4 over-voltage detection interrupt BUCK4_OV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
3	BUCK3_ILIM_MASK	R/W	0h	Masking for BUCK3 current monitoring interrupt BUCK3_ILIM_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
2	RESERVED	R/W	0h	
1	BUCK3_UV_MASK	R/W	0h	Masking of BUCK3 under-voltage detection interrupt BUCK3_UV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	BUCK3_OV_MASK	R/W	0h	Masking of BUCK3 over-voltage detection interrupt BUCK3_OV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.70 MASK_BUCK5 Register (Offset = 4Bh) [Reset = 00h]

MASK_BUCK5 is shown in Figure 8-129 and described in Table 8-94.

Return to the Table 8-23.

Figure 8-129. MASK_BUCK5 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK5_ILIM_MASK	RESERVED	BUCK5_UV_MASK	BUCK5_OV_MASK
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-94. MASK_BUCK5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	BUCK5_ILIM_MASK	R/W	0h	Masking for BUCK5 current monitoring interrupt BUCK5_ILIM_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
2	RESERVED	R/W	0h	
1	BUCK5_UV_MASK	R/W	0h	Masking of BUCK5 under-voltage detection interrupt BUCK5_UV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	BUCK5_OV_MASK	R/W	0h	Masking of BUCK5 over-voltage detection interrupt BUCK5_OV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.71 MASK_LDO1_2 Register (Offset = 4Ch) [Reset = 00h]

MASK_LDO1_2 is shown in Figure 8-130 and described in Table 8-95.

Return to the Table 8-23.

Figure 8-130. MASK_LDO1_2 Register

7	6	5	4	3	2	1	0
LDO2_ILIM_MASK	RESERVED	LDO2_UV_MASK	LDO2_OV_MASK	LDO1_ILIM_MASK	RESERVED	LDO1_UV_MASK	LDO1_OV_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-95. MASK_LDO1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO2_ILIM_MASK	R/W	0h	Masking for LDO2 current monitoring interrupt LDO2_ILIM_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
6	RESERVED	R/W	0h	
5	LDO2_UV_MASK	R/W	0h	Masking of LDO2 under-voltage detection interrupt LDO2_UV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
4	LDO2_OV_MASK	R/W	0h	Masking of LDO2 over-voltage detection interrupt LDO2_OV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
3	LDO1_ILIM_MASK	R/W	0h	Masking for LDO1 current monitoring interrupt LDO1_ILIM_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
2	RESERVED	R/W	0h	
1	LDO1_UV_MASK	R/W	0h	Masking of LDO1 under-voltage detection interrupt LDO1_UV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	LDO1_OV_MASK	R/W	0h	Masking of LDO1 over-voltage detection interrupt LDO1_OV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.72 MASK_LDO3_4 Register (Offset = 4Dh) [Reset = 00h]

MASK_LDO3_4 is shown in Figure 8-131 and described in Table 8-96.

Return to the Table 8-23.

Figure 8-131. MASK_LDO3_4 Register

7	6	5	4	3	2	1	0
LDO4_ILIM_MASK	RESERVED	LDO4_UV_MASK	LDO4_OV_MASK	LDO3_ILIM_MASK	RESERVED	LDO3_UV_MASK	LDO3_OV_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-96. MASK_LDO3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4_ILIM_MASK	R/W	0h	Masking for LDO4 current monitoring interrupt LDO4_ILIM_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
6	RESERVED	R/W	0h	
5	LDO4_UV_MASK	R/W	0h	Masking of LDO4 under-voltage detection interrupt LDO4_UV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
4	LDO4_OV_MASK	R/W	0h	Masking of LDO4 over-voltage detection interrupt LDO4_OV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
3	LDO3_ILIM_MASK	R/W	0h	Masking for LDO3 current monitoring interrupt LDO3_ILIM_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
2	RESERVED	R/W	0h	
1	LDO3_UV_MASK	R/W	0h	Masking of LDO3 under-voltage detection interrupt LDO3_UV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	LDO3_OV_MASK	R/W	0h	Masking of LDO3 over-voltage detection interrupt LDO3_OV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.73 MASK_VMON Register (Offset = 4Eh) [Reset = 00h]

MASK_VMON is shown in Figure 8-132 and described in Table 8-97.

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Figure 8-132. MASK_VMON Register

7	6	5	4	3	2	1	0
RESERVED						VCCA_UV_MASK	VCCA_OV_MASK
R/W-0h						R/W-0h	R/W-0h

Table 8-97. MASK_VMON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	VCCA_UV_MASK	R/W	0h	Masking of VCCA under-voltage detection interrupt VCCA_UV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	VCCA_OV_MASK	R/W	0h	Masking of VCCA over-voltage detection interrupt VCCA_OV_INT: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.74 MASK_GPIO1_8_FALL Register (Offset = 4Fh) [Reset = 00h]

MASK_GPIO1_8_FALL is shown in Figure 8-133 and described in Table 8-98.

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Figure 8-133. MASK_GPIO1_8_FALL Register

7	6	5	4	3	2	1	0
GPIO8_FALL_MASK	GPIO7_FALL_MASK	GPIO6_FALL_MASK	GPIO5_FALL_MASK	GPIO4_FALL_MASK	GPIO3_FALL_MASK	GPIO2_FALL_MASK	GPIO1_FALL_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-98. MASK_GPIO1_8_FALL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_FALL_MASK	R/W	0h	Masking of interrupt for GPIO8 low state transition: This bit does not affect GPIO8_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
6	GPIO7_FALL_MASK	R/W	0h	Masking of interrupt for GPIO7 low state transition: This bit does not affect GPIO7_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
5	GPIO6_FALL_MASK	R/W	0h	Masking of interrupt for GPIO6 low state transition: This bit does not affect GPIO6_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
4	GPIO5_FALL_MASK	R/W	0h	Masking of interrupt for GPIO5 low state transition: This bit does not affect GPIO5_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
3	GPIO4_FALL_MASK	R/W	0h	Masking of interrupt for GPIO4 low state transition: This bit does not affect GPIO4_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
2	GPIO3_FALL_MASK	R/W	0h	Masking of interrupt for GPIO3 low state transition: This bit does not affect GPIO3_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
1	GPIO2_FALL_MASK	R/W	0h	Masking of interrupt for GPIO2 low state transition: This bit does not affect GPIO2_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	GPIO1_FALL_MASK	R/W	0h	Masking of interrupt for GPIO1 low state transition: This bit does not affect GPIO1_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.75 MASK_GPIO1_8_RISE Register (Offset = 50h) [Reset = 00h]

MASK_GPIO1_8_RISE is shown in Figure 8-134 and described in Table 8-99.

Return to the Table 8-23.

Figure 8-134. MASK_GPIO1_8_RISE Register

7	6	5	4	3	2	1	0
GPIO8_RISE_MASK	GPIO7_RISE_MASK	GPIO6_RISE_MASK	GPIO5_RISE_MASK	GPIO4_RISE_MASK	GPIO3_RISE_MASK	GPIO2_RISE_MASK	GPIO1_RISE_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-99. MASK_GPIO1_8_RISE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_RISE_MASK	R/W	0h	Masking of interrupt for GPIO8 high state transition: This bit does not affect GPIO8_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
6	GPIO7_RISE_MASK	R/W	0h	Masking of interrupt for GPIO7 high state transition: This bit does not affect GPIO7_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
5	GPIO6_RISE_MASK	R/W	0h	Masking of interrupt for GPIO6 high state transition: This bit does not affect GPIO6_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
4	GPIO5_RISE_MASK	R/W	0h	Masking of interrupt for GPIO5 high state transition: This bit does not affect GPIO5_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
3	GPIO4_RISE_MASK	R/W	0h	Masking of interrupt for GPIO4 high state transition: This bit does not affect GPIO4_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
2	GPIO3_RISE_MASK	R/W	0h	Masking of interrupt for GPIO3 high state transition: This bit does not affect GPIO3_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
1	GPIO2_RISE_MASK	R/W	0h	Masking of interrupt for GPIO2 high state transition: This bit does not affect GPIO2_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	GPIO1_RISE_MASK	R/W	0h	Masking of interrupt for GPIO1 high state transition: This bit does not affect GPIO1_IN status bit in GPIO_IN_1 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.76 MASK_GPIO9_11 Register (Offset = 51h) [Reset = 00h]

MASK_GPIO9_11 is shown in Figure 8-135 and described in Table 8-100.

Return to the Table 8-23.

Figure 8-135. MASK_GPIO9_11 Register

7	6	5	4	3	2	1	0
RESERVED		GPIO11_RISE_MASK	GPIO10_RISE_MASK	GPIO9_RISE_MASK	GPIO11_FALL_MASK	GPIO10_FALL_MASK	GPIO9_FALL_MASK
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-100. MASK_GPIO9_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	GPIO11_RISE_MASK	R/W	0h	Masking of interrupt for GPIO11 high state transition: This bit does not affect GPIO11_IN status bit in GPIO_IN_2 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
4	GPIO10_RISE_MASK	R/W	0h	Masking of interrupt for GPIO10 high state transition: This bit does not affect GPIO10_IN status bit in GPIO_IN_2 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
3	GPIO9_RISE_MASK	R/W	0h	Masking of interrupt for GPIO9 high state transition: This bit does not affect GPIO9_IN status bit in GPIO_IN_2 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
2	GPIO11_FALL_MASK	R/W	0h	Masking of interrupt for GPIO11 low state transition: This bit does not affect GPIO11_IN status bit in GPIO_IN_2 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
1	GPIO10_FALL_MASK	R/W	0h	Masking of interrupt for GPIO10 low state transition: This bit does not affect GPIO10_IN status bit in GPIO_IN_2 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	GPIO9_FALL_MASK	R/W	0h	Masking of interrupt for GPIO9 low state transition: This bit does not affect GPIO9_IN status bit in GPIO_IN_2 register. (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.77 MASK_STARTUP Register (Offset = 52h) [Reset = 00h]

MASK_STARTUP is shown in Figure 8-136 and described in Table 8-101.

Return to the Table 8-23.

Figure 8-136. MASK_STARTUP Register

7	6	5	4	3	2	1	0
RESERVED		SOFT_REBOOT_MASK	FSD_MASK	RESERVED		ENABLE_MASK	NPWRON_START_MASK
R/W-0h		R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h

Table 8-101. MASK_STARTUP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	SOFT_REBOOT_MASK	R/W	0h	Masking of SOFT_REBOOT_MASK interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
4	FSD_MASK	R/W	0h	Masking of FSD_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
3-2	RESERVED	R/W	0h	
1	ENABLE_MASK	R/W	0h	Masking of ENABLE_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	NPWRON_START_MASK	R/W	0h	Masking of NPWRON_START_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.78 MASK_MISC Register (Offset = 53h) [Reset = 00h]

MASK_MISC is shown in Figure 8-137 and described in Table 8-102.

Return to the Table 8-23.

Figure 8-137. MASK_MISC Register

7	6	5	4	3	2	1	0
RESERVED				TWARN_MASK	RESERVED	EXT_CLK_MASK	BIST_PASS_MASK
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-102. MASK_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	TWARN_MASK	R/W	0h	Masking of TWARN_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
2	RESERVED	R/W	0h	
1	EXT_CLK_MASK	R/W	0h	Masking of EXT_CLK_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	BIST_PASS_MASK	R/W	0h	Masking of BIST_PASS_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.79 MASK_MODERATE_ERR Register (Offset = 54h) [Reset = 00h]

MASK_MODERATE_ERR is shown in Figure 8-138 and described in Table 8-103.

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Figure 8-138. MASK_MODERATE_ERR Register

7	6	5	4	3	2	1	0
NRSTOUT_READBACK_MASK	NINT_READBACK_MASK	NPWRON_LONG_MASK	SPMI_ERR_MASK	RESERVED	REG_CRC_ERR_MASK	BIST_FAIL_MASK	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-103. MASK_MODERATE_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NRSTOUT_READBACK_MASK	R/W	0h	Masking of NRSTOUT_READBACK_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
6	NINT_READBACK_MASK	R/W	0h	Masking of NINT_READBACK_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
5	NPWRON_LONG_MASK	R/W	0h	Masking of NPWRON_LONG_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
4	SPMI_ERR_MASK	R/W	0h	Masking of SPMI_ERR_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
3	RESERVED	R/W	0h	
2	REG_CRC_ERR_MASK	R/W	0h	Masking of REG_CRC_ERR_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
1	BIST_FAIL_MASK	R/W	0h	Masking of BIST_FAIL_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	RESERVED	R/W	0h	

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8.7.1.80 MASK_FSM_ERR Register (Offset = 56h) [Reset = 00h]

MASK_FSM_ERR is shown in Figure 8-139 and described in Table 8-104.

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Figure 8-139. MASK_FSM_ERR Register

7	6	5	4	3	2	1	0
RESERVED				SOC_PWR_ERR_MASK	MCU_PWR_ERR_MASK	ORD_SHUTDOWN_MASK	IMM_SHUTDOWN_MASK
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-104. MASK_FSM_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	SOC_PWR_ERR_MASK	R/W	0h	Masking of SOC_PWR_ERR_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
2	MCU_PWR_ERR_MASK	R/W	0h	Masking of MCU_PWR_ERR_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
1	ORD_SHUTDOWN_MASK	R/W	0h	Masking of ORD_SHUTDOWN_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	IMM_SHUTDOWN_MASK	R/W	0h	Masking of IMM_SHUTDOWN_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.81 MASK_COMM_ERR Register (Offset = 57h) [Reset = 00h]

MASK_COMM_ERR is shown in Figure 8-140 and described in Table 8-105.

Return to the Table 8-23.

Figure 8-140. MASK_COMM_ERR Register

7	6	5	4	3	2	1	0
I2C2_ADR_ERR_MASK	RESERVED	I2C2_CRC_ERR_MASK	RESERVED	COMM_ADR_ERR_MASK	RESERVED	COMM_CRC_ERR_MASK	COMM_FRM_ERR_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-105. MASK_COMM_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C2_ADR_ERR_MASK	R/W	0h	Masking of I2C2_ADR_ERR_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
6	RESERVED	R/W	0h	
5	I2C2_CRC_ERR_MASK	R/W	0h	Masking of I2C2_CRC_ERR_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
4	RESERVED	R/W	0h	
3	COMM_ADR_ERR_MASK	R/W	0h	Masking of COMM_ADR_ERR_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
2	RESERVED	R/W	0h	
1	COMM_CRC_ERR_MASK	R/W	0h	Masking of COMM_CRC_ERR_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	COMM_FRM_ERR_MASK	R/W	0h	Masking of COMM_FRM_ERR_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.82 MASK_READBACK_ERR Register (Offset = 58h) [Reset = 00h]

MASK_READBACK_ERR is shown in Figure 8-141 and described in Table 8-106.

Return to the Table 8-23.

Figure 8-141. MASK_READBACK_ERR Register

7	6	5	4	3	2	1	0
RESERVED				NRSTOUT_SOC_READBACK_MASK	RESERVED		EN_DRV_READBACK_MASK
R/W-0h				R/W-0h	R/W-0h		R/W-0h

Table 8-106. MASK_READBACK_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	NRSTOUT_SOC_READBACK_MASK	R/W	0h	Masking of NRSTOUT_SOC_READBACK_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
2-1	RESERVED	R/W	0h	
0	EN_DRV_READBACK_MASK	R/W	0h	Masking of EN_DRV_READBACK_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.83 MASK_ESM Register (Offset = 59h) [Reset = 00h]

MASK_ESM is shown in Figure 8-142 and described in Table 8-107.

Return to the Table 8-23.

Figure 8-142. MASK_ESM Register

7	6	5	4	3	2	1	0
RESERVED		ESM_MCU_RST_MASK	ESM_MCU_FAIL_MASK	ESM_MCU_PIN_MASK	ESM_SOC_RST_MASK	ESM_SOC_FAIL_MASK	ESM_SOC_PIN_MASK
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-107. MASK_ESM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	ESM_MCU_RST_MASK	R/W	0h	Masking of ESM_MCU_RST_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
4	ESM_MCU_FAIL_MASK	R/W	0h	Masking of ESM_MCU_FAIL_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
3	ESM_MCU_PIN_MASK	R/W	0h	Masking of ESM_MCU_PIN_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
2	ESM_SOC_RST_MASK	R/W	0h	Masking of ESM_SOC_RST_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
1	ESM_SOC_FAIL_MASK	R/W	0h	Masking of ESM_SOC_FAIL_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.
0	ESM_SOC_PIN_MASK	R/W	0h	Masking of ESM_SOC_PIN_INT interrupt: (Default from NVM memory) 0h = Interrupt generated 1h = Interrupt not generated.

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8.7.1.84 INT_TOP Register (Offset = 5Ah) [Reset = 00h]

INT_TOP is shown in Figure 8-143 and described in Table 8-108.

Return to the Table 8-23.

Figure 8-143. INT_TOP Register

7	6	5	4	3	2	1	0
FSM_ERR_INT	SEVERE_ERR_INT	MODERATE_ERR_INT	MISC_INT	STARTUP_INT	GPIO_INT	LDO_VMON_INT	BUCK_INT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-108. INT_TOP Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FSM_ERR_INT	R	0h	Interrupt indicating that INT_FSM_ERR register has pending interrupt. The reason for the interrupt is indicated in INT_FSM_ERR register. This bit is cleared automatically when INT_FSM_ERR register is cleared to 0x00.
6	SEVERE_ERR_INT	R	0h	Interrupt indicating that INT_SEVERE_ERR register has pending interrupt. The reason for the interrupt is indicated in INT_SEVERE_ERR register. This bit is cleared automatically when INT_SEVERE_ERR register is cleared to 0x00.
5	MODERATE_ERR_INT	R	0h	Interrupt indicating that INT_MODERATE_ERR register has pending interrupt. The reason for the interrupt is indicated in INT_MODERATE_ERR register. This bit is cleared automatically when INT_MODERATE_ERR register is cleared to 0x00.
4	MISC_INT	R	0h	Interrupt indicating that INT_MISC register has pending interrupt. The reason for the interrupt is indicated in INT_MISC register. This bit is cleared automatically when INT_MISC register is cleared to 0x00.
3	STARTUP_INT	R	0h	Interrupt indicating that INT_STARTUP register has pending interrupt. The reason for the interrupt is indicated in INT_STARTUP register. This bit is cleared automatically when INT_STARTUP register is cleared to 0x00.
2	GPIO_INT	R	0h	Interrupt indicating that INT_GPIO register has pending interrupt. The reason for the interrupt is indicated in INT_GPIO register. This bit is cleared automatically when INT_GPIO register is cleared to 0x00.
1	LDO_VMON_INT	R	0h	Interrupt indicating that INT_LDO_VMON register has pending interrupt. The reason for the interrupt is indicated in INT_LDO_VMON register. This bit is cleared automatically when INT_LDO_VMON register is cleared to 0x00.
0	BUCK_INT	R	0h	Interrupt indicating that INT_BUCK register has pending interrupt. The reason for the interrupt is indicated in INT_BUCK register. This bit is cleared automatically when INT_BUCK register is cleared to 0x00.

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8.7.1.85 INT_BUCK Register (Offset = 5Bh) [Reset = 00h]

INT_BUCK is shown in Figure 8-144 and described in Table 8-109.

Return to the Table 8-23.

Figure 8-144. INT_BUCK Register

7	6	5	4	3	2	1	0
RESERVED					BUCK5_INT	BUCK3_4_INT	BUCK1_2_INT
R-0h					R-0h	R-0h	R-0h

Table 8-109. INT_BUCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2	BUCK5_INT	R	0h	Interrupt indicating that INT_BUCK5 register has pending interrupt. The reason for the interrupt is indicated in INT_BUCK5 register. This bit is cleared automatically when INT_BUCK5 register is cleared to 0x00.
1	BUCK3_4_INT	R	0h	Interrupt indicating that INT_BUCK3_4 register has pending interrupt. This bit is cleared automatically when INT_BUCK3_4 register is cleared to 0x00.
0	BUCK1_2_INT	R	0h	Interrupt indicating that INT_BUCK1_2 register has pending interrupt. This bit is cleared automatically when INT_BUCK1_2 register is cleared to 0x00.

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8.7.1.86 INT_BUCK1_2 Register (Offset = 5Ch) [Reset = 00h]

INT_BUCK1_2 is shown in Figure 8-145 and described in Table 8-110.

Return to the Table 8-23.

Figure 8-145. INT_BUCK1_2 Register

7	6	5	4	3	2	1	0
BUCK2_ILIM_INT	BUCK2_SC_INT	BUCK2_UV_INT	BUCK2_OV_INT	BUCK1_ILIM_INT	BUCK1_SC_INT	BUCK1_UV_INT	BUCK1_OV_INT
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-110. INT_BUCK1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK2_ILIM_INT	R/W1C	0h	Latched status bit indicating that BUCK2 output current limit has been triggered. Write 1 to clear.
6	BUCK2_SC_INT	R/W1C	0h	Latched status bit indicating that the BUCK2 output voltage has fallen below 150 mV level during operation or BUCK2 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
5	BUCK2_UV_INT	R/W1C	0h	Latched status bit indicating that BUCK2 output under-voltage has been detected. Write 1 to clear.
4	BUCK2_OV_INT	R/W1C	0h	Latched status bit indicating that BUCK2 output over-voltage has been detected. Write 1 to clear.
3	BUCK1_ILIM_INT	R/W1C	0h	Latched status bit indicating that BUCK1 output current limit has been triggered. Write 1 to clear.
2	BUCK1_SC_INT	R/W1C	0h	Latched status bit indicating that the BUCK1 output voltage has fallen below 150 mV level during operation or BUCK1 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
1	BUCK1_UV_INT	R/W1C	0h	Latched status bit indicating that BUCK1 output under-voltage has been detected. Write 1 to clear.
0	BUCK1_OV_INT	R/W1C	0h	Latched status bit indicating that BUCK1 output over-voltage has been detected. Write 1 to clear.

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8.7.1.87 INT_BUCK3_4 Register (Offset = 5Dh) [Reset = 00h]

INT_BUCK3_4 is shown in Figure 8-146 and described in Table 8-111.

Return to the Table 8-23.

Figure 8-146. INT_BUCK3_4 Register

7	6	5	4	3	2	1	0
BUCK4_ILIM_INT	BUCK4_SC_INT	BUCK4_UV_INT	BUCK4_OV_INT	BUCK3_ILIM_INT	BUCK3_SC_INT	BUCK3_UV_INT	BUCK3_OV_INT
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-111. INT_BUCK3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK4_ILIM_INT	R/W1C	0h	Latched status bit indicating that BUCK4 output current limit has been triggered. Write 1 to clear.
6	BUCK4_SC_INT	R/W1C	0h	Latched status bit indicating that the BUCK4 output voltage has fallen below 150 mV level during operation or BUCK4 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
5	BUCK4_UV_INT	R/W1C	0h	Latched status bit indicating that BUCK4 output under-voltage has been detected. Write 1 to clear.
4	BUCK4_OV_INT	R/W1C	0h	Latched status bit indicating that BUCK4 output over-voltage has been detected. Write 1 to clear.
3	BUCK3_ILIM_INT	R/W1C	0h	Latched status bit indicating that BUCK3 output current limit has been triggered. Write 1 to clear.
2	BUCK3_SC_INT	R/W1C	0h	Latched status bit indicating that the BUCK3 output voltage has fallen below 150 mV level during operation or BUCK3 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
1	BUCK3_UV_INT	R/W1C	0h	Latched status bit indicating that BUCK3 output under-voltage has been detected. Write 1 to clear.
0	BUCK3_OV_INT	R/W1C	0h	Latched status bit indicating that BUCK3 output over-voltage has been detected. Write 1 to clear.

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8.7.1.88 INT_BUCK5 Register (Offset = 5Eh) [Reset = 00h]

INT_BUCK5 is shown in Figure 8-147 and described in Table 8-112.

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Figure 8-147. INT_BUCK5 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK5_ILIM_INT	BUCK5_SC_INT	BUCK5_UV_INT	BUCK5_OV_INT
R/W-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-112. INT_BUCK5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	BUCK5_ILIM_INT	R/W1C	0h	Latched status bit indicating that BUCK5 output current limit has been triggered. Write 1 to clear.
2	BUCK5_SC_INT	R/W1C	0h	Latched status bit indicating that the BUCK5 output voltage has fallen below 150 mV level during operation or BUCK5 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
1	BUCK5_UV_INT	R/W1C	0h	Latched status bit indicating that BUCK5 output under-voltage has been detected. Write 1 to clear.
0	BUCK5_OV_INT	R/W1C	0h	Latched status bit indicating that BUCK5 output over-voltage has been detected. Write 1 to clear.

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8.7.1.89 INT_LDO_VMON Register (Offset = 5Fh) [Reset = 00h]

INT_LDO_VMON is shown in Figure 8-148 and described in Table 8-113.

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Figure 8-148. INT_LDO_VMON Register

7	6	5	4	3	2	1	0
RESERVED			VCCA_INT	RESERVED		LDO3_4_INT	LDO1_2_INT
R-0h			R-0h	R-0h		R-0h	R-0h

Table 8-113. INT_LDO_VMON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	VCCA_INT	R	0h	Interrupt indicating that INT_VMON register has pending interrupt. The reason for the interrupt is indicated in INT_VMON register. This bit is cleared automatically when INT_VMON register is cleared to 0x00.
3-2	RESERVED	R	0h	
1	LDO3_4_INT	R	0h	Interrupt indicating that INT_LDO3_4 register has pending interrupt. This bit is cleared automatically when INT_LDO3_4 register is cleared to 0x00.
0	LDO1_2_INT	R	0h	Interrupt indicating that INT_LDO1_2 register has pending interrupt. This bit is cleared automatically when INT_LDO1_2 register is cleared to 0x00.

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8.7.1.90 INT_LDO1_2 Register (Offset = 60h) [Reset = 00h]

INT_LDO1_2 is shown in Figure 8-149 and described in Table 8-114.

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Figure 8-149. INT_LDO1_2 Register

7	6	5	4	3	2	1	0
LDO2_ILIM_INT	LDO2_SC_INT	LDO2_UV_INT	LDO2_OV_INT	LDO1_ILIM_INT	LDO1_SC_INT	LDO1_UV_INT	LDO1_OV_INT
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-114. INT_LDO1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO2_ILIM_INT	R/W1C	0h	Latched status bit indicating that LDO2 output current limit has been triggered. Write 1 to clear.
6	LDO2_SC_INT	R/W1C	0h	Latched status bit indicating that LDO2 output voltage has fallen below 150 mV level during operation or LDO2 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
5	LDO2_UV_INT	R/W1C	0h	Latched status bit indicating that LDO2 output under-voltage has been detected. Write 1 to clear.
4	LDO2_OV_INT	R/W1C	0h	Latched status bit indicating that LDO2 output over-voltage has been detected. Write 1 to clear.
3	LDO1_ILIM_INT	R/W1C	0h	Latched status bit indicating that LDO1 output current limit has been triggered. Write 1 to clear.
2	LDO1_SC_INT	R/W1C	0h	Latched status bit indicating that LDO1 output voltage has fallen below 150 mV level during operation or LDO1 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
1	LDO1_UV_INT	R/W1C	0h	Latched status bit indicating that LDO1 output under-voltage has been detected. Write 1 to clear.
0	LDO1_OV_INT	R/W1C	0h	Latched status bit indicating that LDO1 output over-voltage has been detected. Write 1 to clear.

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8.7.1.91 INT_LDO3_4 Register (Offset = 61h) [Reset = 00h]

INT_LDO3_4 is shown in Figure 8-150 and described in Table 8-115.

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Figure 8-150. INT_LDO3_4 Register

7	6	5	4	3	2	1	0
LDO4_ILIM_INT	LDO4_SC_INT	LDO4_UV_INT	LDO4_OV_INT	LDO3_ILIM_INT	LDO3_SC_INT	LDO3_UV_INT	LDO3_OV_INT
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-115. INT_LDO3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4_ILIM_INT	R/W1C	0h	Latched status bit indicating that LDO4 output current limit has been triggered. Write 1 to clear.
6	LDO4_SC_INT	R/W1C	0h	Latched status bit indicating that LDO4 output voltage has fallen below 150 mV level during operation or LDO4 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
5	LDO4_UV_INT	R/W1C	0h	Latched status bit indicating that LDO4 output under-voltage has been detected. Write 1 to clear.
4	LDO4_OV_INT	R/W1C	0h	Latched status bit indicating that LDO4 output over-voltage has been detected. Write 1 to clear.
3	LDO3_ILIM_INT	R/W1C	0h	Latched status bit indicating that LDO3 output current limit has been triggered. Write 1 to clear.
2	LDO3_SC_INT	R/W1C	0h	Latched status bit indicating that LDO3 output voltage has fallen below 150 mV level during operation or LDO3 output didn't reach 150 mV level in TBD us from enable. Write 1 to clear.
1	LDO3_UV_INT	R/W1C	0h	Latched status bit indicating that LDO3 output under-voltage has been detected. Write 1 to clear.
0	LDO3_OV_INT	R/W1C	0h	Latched status bit indicating that LDO3 output over-voltage has been detected. Write 1 to clear.

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8.7.1.92 INT_VMON Register (Offset = 62h) [Reset = 00h]

INT_VMON is shown in Figure 8-151 and described in Table 8-116.

Return to the Table 8-23.

Figure 8-151. INT_VMON Register

7	6	5	4	3	2	1	0
RESERVED						VCCA_UV_INT	VCCA_OV_INT
R/W-0h						R/W1C-0h	R/W1C-0h

Table 8-116. INT_VMON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	VCCA_UV_INT	R/W1C	0h	Latched status bit indicating that the VCCA input voltage has decreased below the under-voltage monitoring level. The actual status of the VCCA under-voltage monitoring is indicated by VCCA_UV_STAT bit. Write 1 to clear interrupt.
0	VCCA_OV_INT	R/W1C	0h	Latched status bit indicating that the VCCA input voltage has exceeded the over-voltage detection level. The actual status of the over-voltage is indicated by VCCA_OV_STAT bit. Write 1 to clear interrupt.

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8.7.1.93 INT_GPIO Register (Offset = 63h) [Reset = 00h]

INT_GPIO is shown in Figure 8-152 and described in Table 8-117.

Return to the Table 8-23.

Figure 8-152. INT_GPIO Register

7	6	5	4	3	2	1	0
RESERVED				GPIO1_8_INT	GPIO11_INT	GPIO10_INT	GPIO9_INT
R/W-0h				R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-117. INT_GPIO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	GPIO1_8_INT	R	0h	Interrupt indicating that INT_GPIO1_8 has pending interrupt. The reason for the interrupt is indicated in INT_GPIO1_8 register. This bit is cleared automatically when INT_GPIO1_8 register is cleared to 0x00.
2	GPIO11_INT	R/W1C	0h	Latched status bit indicating that GPIO11 has pending interrupt. GPIO11_IN bit in GPIO_IN_2 register shows the status of the GPIO11 signal. Write 1 to clear interrupt.
1	GPIO10_INT	R/W1C	0h	Latched status bit indicating that GPIO10 has pending interrupt. GPIO10_IN bit in GPIO_IN_2 register shows the status of the GPIO10 signal. Write 1 to clear interrupt.
0	GPIO9_INT	R/W1C	0h	Latched status bit indicating that GPIO9 has pending interrupt. GPIO9_IN bit in GPIO_IN_2 register shows the status of the GPIO9 signal. Write 1 to clear interrupt.

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8.7.1.94 INT_GPIO1_8 Register (Offset = 64h) [Reset = 00h]

INT_GPIO1_8 is shown in Figure 8-153 and described in Table 8-118.

Return to the Table 8-23.

Figure 8-153. INT_GPIO1_8 Register

7	6	5	4	3	2	1	0
GPIO8_INT	GPIO7_INT	GPIO6_INT	GPIO5_INT	GPIO4_INT	GPIO3_INT	GPIO2_INT	GPIO1_INT
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-118. INT_GPIO1_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_INT	R/W1C	0h	Latched status bit indicating that GPIO8 has has pending interrupt. GPIO8_IN bit in GPIO_IN_1 register shows the status of the GPIO8 signal. Write 1 to clear interrupt.
6	GPIO7_INT	R/W1C	0h	Latched status bit indicating that GPIO7 has has pending interrupt. GPIO7_IN bit in GPIO_IN_1 register shows the status of the GPIO7 signal. Write 1 to clear interrupt.
5	GPIO6_INT	R/W1C	0h	Latched status bit indicating that GPIO6 has has pending interrupt. GPIO6_IN bit in GPIO_IN_1 register shows the status of the GPIO6 signal. Write 1 to clear interrupt.
4	GPIO5_INT	R/W1C	0h	Latched status bit indicating that GPIO5 has has pending interrupt. GPIO5_IN bit in GPIO_IN_1 register shows the status of the GPIO5 signal. Write 1 to clear interrupt.
3	GPIO4_INT	R/W1C	0h	Latched status bit indicating that GPIO4 has has pending interrupt. GPIO4_IN bit in GPIO_IN_1 register shows the status of the GPIO4 signal. Write 1 to clear interrupt.
2	GPIO3_INT	R/W1C	0h	Latched status bit indicating that GPIO3 has has pending interrupt. GPIO3_IN bit in GPIO_IN_1 register shows the status of the GPIO3 signal. Write 1 to clear interrupt.
1	GPIO2_INT	R/W1C	0h	Latched status bit indicating that GPIO2 has pending interrupt. GPIO2_IN bit in GPIO_IN_1 register shows the status of the GPIO2 signal. Write 1 to clear interrupt.
0	GPIO1_INT	R/W1C	0h	Latched status bit indicating that GPIO1 has pending interrupt. GPIO1_IN bit in GPIO_IN_1 register shows the status of the GPIO1 signal. Write 1 to clear interrupt.

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8.7.1.95 INT_STARTUP Register (Offset = 65h) [Reset = 00h]

INT_STARTUP is shown in Figure 8-154 and described in Table 8-119.

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Figure 8-154. INT_STARTUP Register

7	6	5	4	3	2	1	0
RESERVED		SOFT_REBOOT_INT	FSD_INT	RESERVED	RTC_INT	ENABLE_INT	NPWRON_START_INT
R/W-0h		R/W1C-0h	R/W1C-0h	R/W-0h	R-0h	R/W1C-0h	R/W1C-0h

Table 8-119. INT_STARTUP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	SOFT_REBOOT_INT	R/W1C	0h	Latched status bit indicating that soft reboot event has been detected. Write 1 to clear.
4	FSD_INT	R/W1C	0h	Latched status bit indicating that PMIC has started from NO_SUPPLY or BACKUP state (first supply dectection). Write 1 to clear.
3	RESERVED	R/W	0h	
2	RTC_INT	R	0h	Latched status bit indicating that RTC_STATUS register has pending interrupt. This bit is cleared automatically when ALARM and TIMER interrupts are cleared.
1	ENABLE_INT	R/W1C	0h	Latched status bit indicating that ENABLE pin active event has been detected. Write 1 to clear.
0	NPWRON_START_INT	R/W1C	0h	Latched status bit indicating that NPWRON start-up event has been detected. Write 1 to clear.

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8.7.1.96 INT_MISC Register (Offset = 66h) [Reset = 00h]

INT_MISC is shown in Figure 8-155 and described in Table 8-120.

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Figure 8-155. INT_MISC Register

7	6	5	4	3	2	1	0
RESERVED				TWARN_INT	RESERVED	EXT_CLK_INT	BIST_PASS_INT
R/W-0h				R/W1C-0h	R/W-0h	R/W1C-0h	R/W1C-0h

Table 8-120. INT_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	TWARN_INT	R/W1C	0h	Latched status bit indicating that the die junction temperature has exceeded the thermal warning level. The actual status of the thermal warning is indicated by TWARN_STAT bit in STAT_MISC register. Write 1 to clear interrupt.
2	RESERVED	R/W	0h	
1	EXT_CLK_INT	R/W1C	0h	Latched status bit indicating that external clock is not valid. Internal clock is automatically taken into use. Write 1 to clear.
0	BIST_PASS_INT	R/W1C	0h	Latched status bit indicating that BIST has been completed. Write 1 to clear interrupt.

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8.7.1.97 INT_MODERATE_ERR Register (Offset = 67h) [Reset = 00h]

INT_MODERATE_ERR is shown in Figure 8-156 and described in Table 8-121.

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Figure 8-156. INT_MODERATE_ERR Register

7	6	5	4	3	2	1	0
NRSTOUT_READBACK_INT	NINT_READBACK_INT	NPWRON_LONG_INT	SPMI_ERR_INT	RECOV_CNT_INT	REG_CRC_ERR_INT	BIST_FAIL_INT	TSD_ORD_INT
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-121. INT_MODERATE_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NRSTOUT_READBACK_INT	R/W1C	0h	Latched status bit indicating that NRSTOUT readback error has been detected. Write 1 to clear interrupt.
6	NINT_READBACK_INT	R/W1C	0h	Latched status bit indicating that NINT readback error has been detected. Write 1 to clear interrupt.
5	NPWRON_LONG_INT	R/W1C	0h	Latched status bit indicating that NPWRON long press has been detected. Write 1 to clear.
4	SPMI_ERR_INT	R/W1C	0h	Latched status bit indicating that the SPMI communication interface has detected an error. Write 1 to clear interrupt.
3	RECOV_CNT_INT	R/W1C	0h	Latched status bit indicating that RECOV_CNT has reached the limit (RECOV_CNT_THR). Write 1 to clear.
2	REG_CRC_ERR_INT	R/W1C	0h	Latched status bit indicating that the register CRC checking has detected an error. Write 1 to clear interrupt.
1	BIST_FAIL_INT	R/W1C	0h	Latched status bit indicating that the LBIST or ABIST has detected an error. Write 1 to clear interrupt.
0	TSD_ORD_INT	R/W1C	0h	Latched status bit indicating that the die junction temperature has exceeded the thermal level causing a sequenced shutdown. The regulators have been disabled. The regulators cannot be enabled if this bit is active. The actual status of the temperature is indicated by TSD_ORD_STAT bit in STAT_MODERATE_ERR register. Write 1 to clear interrupt.

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8.7.1.98 INT_SEVERE_ERR Register (Offset = 68h) [Reset = 00h]

INT_SEVERE_ERR is shown in Figure 8-157 and described in Table 8-122.

Return to the Table 8-23.

Figure 8-157. INT_SEVERE_ERR Register

7	6	5	4	3	2	1	0
RESERVED					PFSM_ERR_INT	VCCA_OVP_INT	TSD_IMM_INT
R/W-0h					R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-122. INT_SEVERE_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	PFSM_ERR_INT	R/W1C	0h	Latched status bit indicating that the PFSM sequencer has detected an error. Write 1 to clear interrupt.
1	VCCA_OVP_INT	R/W1C	0h	Latched status bit indicating that the VCCA input voltage has exceeded the over-voltage threshold level causing an immediate shutdown. The regulators have been disabled. Write 1 to clear interrupt.
0	TSD_IMM_INT	R/W1C	0h	Latched status bit indicating that the die junction temperature has exceeded the thermal level causing an immediate shutdown. The regulators have been disabled. The regulators cannot be enabled if this bit is active. The actual status of the temperature is indicated by TSD_IMM_STAT bit in THER_CLK_STATUS register. Write 1 to clear interrupt.

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8.7.1.99 INT_FSM_ERR Register (Offset = 69h) [Reset = 00h]

INT_FSM_ERR is shown in Figure 8-158 and described in Table 8-123.

Return to the Table 8-23.

Figure 8-158. INT_FSM_ERR Register

7	6	5	4	3	2	1	0
WD_INT	ESM_INT	READBACK_ERR_INT	COMM_ERR_INT	SOC_PWR_ERR_INT	MCU_PWR_ERR_INT	ORD_SHUTDOWN_INT	IMM_SHUTDOWN_INT
R-0h	R-0h	R-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-123. INT_FSM_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_INT	R	0h	Interrupt indicating that WD_ERR_STATUS register has pending interrupt. This bit is cleared automatically when WD_RST_INT, WD_FAIL_INT and WD_LONGWIN_TIMEOUT_INT are cleared.
6	ESM_INT	R	0h	Interrupt indicating that INT_ESM has pending interrupt. This bit is cleared automatically when INT_ESM register is cleared to 0x00.
5	READBACK_ERR_INT	R	0h	Interrupt indicating that INT_READBACK_ERR has pending interrupt. This bit is cleared automatically when INT_READBACK_ERR register is cleared to 0x00.
4	COMM_ERR_INT	R	0h	Interrupt indicating that INT_COMM_ERR has pending interrupt. The reason for the interrupt is indicated in INT_COMM_ERR register. This bit is cleared automatically when INT_COMM_ERR register is cleared to 0x00.
3	SOC_PWR_ERR_INT	R/W1C	0h	Latched status bit indicating that SOC power error has been detected. Write 1 to clear.
2	MCU_PWR_ERR_INT	R/W1C	0h	Latched status bit indicating that MCU power error has been detected. Write 1 to clear.
1	ORD_SHUTDOWN_INT	R/W1C	0h	Latched status bit indicating that orderly shutdown has been detected. Write 1 to clear.
0	IMM_SHUTDOWN_INT	R/W1C	0h	Latched status bit indicating that immediate shutdown has been detected. Write 1 to clear.

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8.7.1.100 INT_COMM_ERR Register (Offset = 6Ah) [Reset = 00h]

INT_COMM_ERR is shown in Figure 8-159 and described in Table 8-124.

Return to the Table 8-23.

Figure 8-159. INT_COMM_ERR Register

7	6	5	4	3	2	1	0
I2C2_ADR_ERR_INT	RESERVED	I2C2_CRC_ERR_INT	RESERVED	COMM_ADR_ERR_INT	RESERVED	COMM_CRC_ERR_INT	COMM_FRM_ERR_INT
R/W1C-0h	R/W-0h	R/W1C-0h	R/W-0h	R/W1C-0h	R/W-0h	R/W1C-0h	R/W1C-0h

Table 8-124. INT_COMM_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C2_ADR_ERR_INT	R/W1C	0h	Latched status bit indicating that I2C2 write to non-existing, protected or read-only register address has been detected. Write 1 to clear interrupt.
6	RESERVED	R/W	0h	
5	I2C2_CRC_ERR_INT	R/W1C	0h	Latched status bit indicating that I2C2 CRC error has been detected. Write 1 to clear interrupt.
4	RESERVED	R/W	0h	
3	COMM_ADR_ERR_INT	R/W1C	0h	Latched status bit indicating that I2C1/SPI write to non-existing, protected or read-only register address has been detected. Write 1 to clear interrupt.
2	RESERVED	R/W	0h	
1	COMM_CRC_ERR_INT	R/W1C	0h	Latched status bit indicating that I2C1/SPI CRC error has been detected. Write 1 to clear interrupt.
0	COMM_FRM_ERR_INT	R/W1C	0h	Latched status bit indicating that SPI frame error has been detected. Write 1 to clear interrupt.

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8.7.1.101 INT_READBACK_ERR Register (Offset = 6Bh) [Reset = 00h]

INT_READBACK_ERR is shown in Figure 8-160 and described in Table 8-125.

Return to the Table 8-23.

Figure 8-160. INT_READBACK_ERR Register

7	6	5	4	3	2	1	0
RESERVED				NRSTOUT_SOC_READBACK_INT	RESERVED		EN_DRV_READBACK_INT
R/W-0h				R/W1C-0h	R/W-0h		R/W1C-0h

Table 8-125. INT_READBACK_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	NRSTOUT_SOC_READBACK_INT	R/W1C	0h	Latched status bit indicating that NRSTOUT_SOC readback error has been detected. Write 1 to clear interrupt.
2-1	RESERVED	R/W	0h	
0	EN_DRV_READBACK_INT	R/W1C	0h	Latched status bit indicating that EN_DRV readback error has been detected. Write 1 to clear interrupt.

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8.7.1.102 INT_ESM Register (Offset = 6Ch) [Reset = 00h]

INT_ESM is shown in Figure 8-161 and described in Table 8-126.

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Figure 8-161. INT_ESM Register

7	6	5	4	3	2	1	0
RESERVED		ESM_MCU_RST_INT	ESM_MCU_FAIL_INT	ESM_MCU_PIN_INT	ESM_SOC_RST_INT	ESM_SOC_FAIL_INT	ESM_SOC_PIN_INT
R/W-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-126. INT_ESM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	ESM_MCU_RST_INT	R/W1C	0h	Latched status bit indicating that MCU ESM reset has been detected. Write 1 to clear interrupt.
4	ESM_MCU_FAIL_INT	R/W1C	0h	Latched status bit indicating that MCU ESM fail has been detected. Write 1 to clear interrupt.
3	ESM_MCU_PIN_INT	R/W1C	0h	Latched status bit indicating that MCU ESM fault has been detected. Write 1 to clear interrupt.
2	ESM_SOC_RST_INT	R/W1C	0h	Latched status bit indicating that SOC ESM reset has been detected. Write 1 to clear interrupt.
1	ESM_SOC_FAIL_INT	R/W1C	0h	Latched status bit indicating that SOC ESM fail has been detected. Write 1 to clear interrupt.
0	ESM_SOC_PIN_INT	R/W1C	0h	Latched status bit indicating that SOC ESM fault has been detected. Write 1 to clear interrupt.

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8.7.1.103 STAT_BUCK1_2 Register (Offset = 6Dh) [Reset = 00h]

STAT_BUCK1_2 is shown in Figure 8-162 and described in Table 8-127.

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Figure 8-162. STAT_BUCK1_2 Register

7	6	5	4	3	2	1	0
BUCK2_ILIM_STAT	RESERVED	BUCK2_UV_STAT	BUCK2_OV_STAT	BUCK1_ILIM_STAT	RESERVED	BUCK1_UV_STAT	BUCK1_OV_STAT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-127. STAT_BUCK1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK2_ILIM_STAT	R	0h	Status bit indicating that BUCK2 output current is above current limit level.
6	RESERVED	R	0h	
5	BUCK2_UV_STAT	R	0h	Status bit indicating that BUCK2 output voltage is below under-voltage threshold.
4	BUCK2_OV_STAT	R	0h	Status bit indicating that BUCK2 output voltage is above over-voltage threshold.
3	BUCK1_ILIM_STAT	R	0h	Status bit indicating that BUCK1 output current is above current limit level.
2	RESERVED	R	0h	
1	BUCK1_UV_STAT	R	0h	Status bit indicating that BUCK1 output voltage is below under-voltage threshold.
0	BUCK1_OV_STAT	R	0h	Status bit indicating that BUCK1 output voltage is above over-voltage threshold.

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8.7.1.104 STAT_BUCK3_4 Register (Offset = 6Eh) [Reset = 00h]

STAT_BUCK3_4 is shown in Figure 8-163 and described in Table 8-128.

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Figure 8-163. STAT_BUCK3_4 Register

7	6	5	4	3	2	1	0
BUCK4_ILIM_STAT	RESERVED	BUCK4_UV_STAT	BUCK4_OV_STAT	BUCK3_ILIM_STAT	RESERVED	BUCK3_UV_STAT	BUCK3_OV_STAT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-128. STAT_BUCK3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK4_ILIM_STAT	R	0h	Status bit indicating that BUCK4 output current is above current limit level.
6	RESERVED	R	0h	
5	BUCK4_UV_STAT	R	0h	Status bit indicating that BUCK4 output voltage is below under-voltage threshold.
4	BUCK4_OV_STAT	R	0h	Status bit indicating that BUCK4 output voltage is above over-voltage threshold.
3	BUCK3_ILIM_STAT	R	0h	Status bit indicating that BUCK3 output current is above current limit level.
2	RESERVED	R	0h	
1	BUCK3_UV_STAT	R	0h	Status bit indicating that BUCK3 output voltage is below under-voltage threshold.
0	BUCK3_OV_STAT	R	0h	Status bit indicating that BUCK3 output voltage is above over-voltage threshold.

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8.7.1.105 STAT_BUCK5 Register (Offset = 6Fh) [Reset = 00h]

STAT_BUCK5 is shown in Figure 8-164 and described in Table 8-129.

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Figure 8-164. STAT_BUCK5 Register

7	6	5	4	3	2	1	0
RESERVED				BUCK5_ILIM_STAT	RESERVED	BUCK5_UV_STAT	BUCK5_OV_STAT
R-0h				R-0h	R-0h	R-0h	R-0h

Table 8-129. STAT_BUCK5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	BUCK5_ILIM_STAT	R	0h	Status bit indicating that BUCK5 output current is above current limit level.
2	RESERVED	R	0h	
1	BUCK5_UV_STAT	R	0h	Status bit indicating that BUCK5 output voltage is below under-voltage threshold.
0	BUCK5_OV_STAT	R	0h	Status bit indicating that BUCK5 output voltage is above over-voltage threshold.

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8.7.1.106 STAT_LDO1_2 Register (Offset = 70h) [Reset = 00h]

STAT_LDO1_2 is shown in Figure 8-165 and described in Table 8-130.

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Figure 8-165. STAT_LDO1_2 Register

7	6	5	4	3	2	1	0
LDO2_ILIM_STAT	RESERVED	LDO2_UV_STAT	LDO2_OV_STAT	LDO1_ILIM_STAT	RESERVED	LDO1_UV_STAT	LDO1_OV_STAT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-130. STAT_LDO1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO2_ILIM_STAT	R	0h	Status bit indicating that LDO2 output current is above current limit level.
6	RESERVED	R	0h	
5	LDO2_UV_STAT	R	0h	Status bit indicating that LDO2 output voltage is below under-voltage threshold.
4	LDO2_OV_STAT	R	0h	Status bit indicating that LDO2 output voltage is above over-voltage threshold.
3	LDO1_ILIM_STAT	R	0h	Status bit indicating that LDO1 output current is above current limit level.
2	RESERVED	R	0h	
1	LDO1_UV_STAT	R	0h	Status bit indicating that LDO1 output voltage is below under-voltage threshold.
0	LDO1_OV_STAT	R	0h	Status bit indicating that LDO1 output voltage is above over-voltage threshold.

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8.7.1.107 STAT_LDO3_4 Register (Offset = 71h) [Reset = 00h]

STAT_LDO3_4 is shown in Figure 8-166 and described in Table 8-131.

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Figure 8-166. STAT_LDO3_4 Register

7	6	5	4	3	2	1	0
LDO4_ILIM_STAT	RESERVED	LDO4_UV_STAT	LDO4_OV_STAT	LDO3_ILIM_STAT	RESERVED	LDO3_UV_STAT	LDO3_OV_STAT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-131. STAT_LDO3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4_ILIM_STAT	R	0h	Status bit indicating that LDO4 output current is above current limit level.
6	RESERVED	R	0h	
5	LDO4_UV_STAT	R	0h	Status bit indicating that LDO4 output voltage is below under-voltage threshold.
4	LDO4_OV_STAT	R	0h	Status bit indicating that LDO4 output voltage is above over-voltage threshold.
3	LDO3_ILIM_STAT	R	0h	Status bit indicating that LDO3 output current is above current limit level.
2	RESERVED	R	0h	
1	LDO3_UV_STAT	R	0h	Status bit indicating that LDO3 output voltage is below under-voltage threshold.
0	LDO3_OV_STAT	R	0h	Status bit indicating that LDO3 output voltage is above over-voltage threshold.

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8.7.1.108 STAT_VMON Register (Offset = 72h) [Reset = 00h]

STAT_VMON is shown in Figure 8-167 and described in Table 8-132.

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Figure 8-167. STAT_VMON Register

7	6	5	4	3	2	1	0
RESERVED						VCCA_UV_STAT	VCCA_OV_STAT
R-0h						R-0h	R-0h

Table 8-132. STAT_VMON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	VCCA_UV_STAT	R	0h	Status bit indicating that VCCA input voltage is below under-voltage level.
0	VCCA_OV_STAT	R	0h	Status bit indicating that VCCA input voltage is above over-voltage level.

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8.7.1.109 STAT_STARTUP Register (Offset = 73h) [Reset = 00h]

STAT_STARTUP is shown in Figure 8-168 and described in Table 8-133.

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Figure 8-168. STAT_STARTUP Register

7	6	5	4	3	2	1	0
RESERVED						ENABLE_STAT	RESERVED
R-0h						R-0h	R-0h

Table 8-133. STAT_STARTUP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	ENABLE_STAT	R	0h	Status bit indicating nPWRON / EN pin status
0	RESERVED	R	0h	

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8.7.1.110 STAT_MISC Register (Offset = 74h) [Reset = 00h]

STAT_MISC is shown in Figure 8-169 and described in Table 8-134.

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Figure 8-169. STAT_MISC Register

7	6	5	4	3	2	1	0
RESERVED				TWARN_STAT	RESERVED	EXT_CLK_STAT	RESERVED
R-0h				R-0h	R-0h	R-0h	R-0h

Table 8-134. STAT_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	TWARN_STAT	R	0h	Status bit indicating that die junction temperature is above the thermal warning level.
2	RESERVED	R	0h	
1	EXT_CLK_STAT	R	0h	Status bit indicating that external clock is not valid.
0	RESERVED	R	0h	

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8.7.1.111 STAT_MODERATE_ERR Register (Offset = 75h) [Reset = 00h]

STAT_MODERATE_ERR is shown in Figure 8-170 and described in Table 8-135.

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Figure 8-170. STAT_MODERATE_ERR Register

7	6	5	4	3	2	1	0
RESERVED							TSD_ORD_STAT
R-0h							R-0h

Table 8-135. STAT_MODERATE_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	TSD_ORD_STAT	R	0h	Status bit indicating that the die junction temperature is above the thermal level causing a sequenced shutdown.

8.7.1.112 STAT_SEVERE_ERR Register (Offset = 76h) [Reset = 00h]

STAT_SEVERE_ERR is shown in Figure 8-171 and described in Table 8-136.

Return to the Table 8-23.

Figure 8-171. STAT_SEVERE_ERR Register

7	6	5	4	3	2	1	0
RESERVED						VCCA_OVP_STAT	TSD_IMM_STAT
R-0h						R-0h	R-0h

Table 8-136. STAT_SEVERE_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	VCCA_OVP_STAT	R	0h	Status bit indicating that the VCCA voltage is above overvoltage protection level.
0	TSD_IMM_STAT	R	0h	Status bit indicating that the die junction temperature is above the thermal level causing an immediate shutdown.

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8.7.1.113 STAT_READBACK_ERR Register (Offset = 77h) [Reset = 00h]

STAT_READBACK_ERR is shown in Figure 8-172 and described in Table 8-137.

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Figure 8-172. STAT_READBACK_ERR Register

7	6	5	4	3	2	1	0
RESERVED				NRSTOUT_SOC_READBACK_STAT	NRSTOUT_READBACK_STAT	NINT_READBACK_STAT	EN_DRV_READBACK_STAT
R-0h				R-0h	R-0h	R-0h	R-0h

Table 8-137. STAT_READBACK_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	NRSTOUT_SOC_READBACK_STAT	R	0h	Status bit indicating that NRSTOUT_SOC pin output is high and device is driving it low.
2	NRSTOUT_READBACK_STAT	R	0h	Status bit indicating that NRSTOUT pin output is high and device is driving it low.
1	NINT_READBACK_STAT	R	0h	Status bit indicating that NINT pin output is high and device is driving it low.
0	EN_DRV_READBACK_STAT	R	0h	Status bit indicating that EN_DRV pin output is different than driven.

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8.7.1.114 PGOOD_SEL_1 Register (Offset = 78h) [Reset = 00h]

PGOOD_SEL_1 is shown in Figure 8-173 and described in Table 8-138.

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Figure 8-173. PGOOD_SEL_1 Register

7	6	5	4	3	2	1	0
PGOOD_SEL_BUCK4		PGOOD_SEL_BUCK3		PGOOD_SEL_BUCK2		PGOOD_SEL_BUCK1	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 8-138. PGOOD_SEL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PGOOD_SEL_BUCK4	R/W	0h	PGOOD signal source control from BUCK4 (Default from NVM memory) 0h = Masked 1h = Powergood threshold voltage 2h = Powergood threshold voltage AND current limit 3h = Powergood threshold voltage AND current limit
5-4	PGOOD_SEL_BUCK3	R/W	0h	PGOOD signal source control from BUCK3 (Default from NVM memory) 0h = Masked 1h = Powergood threshold voltage 2h = Powergood threshold voltage AND current limit 3h = Powergood threshold voltage AND current limit
3-2	PGOOD_SEL_BUCK2	R/W	0h	PGOOD signal source control from BUCK2 (Default from NVM memory) 0h = Masked 1h = Powergood threshold voltage 2h = Powergood threshold voltage AND current limit 3h = Powergood threshold voltage AND current limit
1-0	PGOOD_SEL_BUCK1	R/W	0h	PGOOD signal source control from BUCK1 (Default from NVM memory) 0h = Masked 1h = Powergood threshold voltage 2h = Powergood threshold voltage AND current limit 3h = Powergood threshold voltage AND current limit

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8.7.1.115 PGOOD_SEL_2 Register (Offset = 79h) [Reset = 00h]

PGOOD_SEL_2 is shown in Figure 8-174 and described in Table 8-139.

Return to the Table 8-23.

Figure 8-174. PGOOD_SEL_2 Register

7	6	5	4	3	2	1	0
RESERVED						PGOOD_SEL_BUCK5	
R/W-0h						R/W-0h	

Table 8-139. PGOOD_SEL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1-0	PGOOD_SEL_BUCK5	R/W	0h	PGOOD signal source control from BUCK5 (Default from NVM memory) 0h = Masked 1h = Powergood threshold voltage 2h = Powergood threshold voltage AND current limit 3h = Powergood threshold voltage AND current limit

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8.7.1.116 PGOOD_SEL_3 Register (Offset = 7Ah) [Reset = 00h]

PGOOD_SEL_3 is shown in Figure 8-175 and described in Table 8-140.

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Figure 8-175. PGOOD_SEL_3 Register

7	6	5	4	3	2	1	0
PGOOD_SEL_LDO4		PGOOD_SEL_LDO3		PGOOD_SEL_LDO2		PGOOD_SEL_LDO1	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 8-140. PGOOD_SEL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PGOOD_SEL_LDO4	R/W	0h	PGOOD signal source control from LDO4 (Default from NVM memory) 0h = Masked 1h = Powergood threshold voltage 2h = Powergood threshold voltage AND current limit 3h = Powergood threshold voltage AND current limit
5-4	PGOOD_SEL_LDO3	R/W	0h	PGOOD signal source control from LDO3 (Default from NVM memory) 0h = Masked 1h = Powergood threshold voltage 2h = Powergood threshold voltage AND current limit 3h = Powergood threshold voltage AND current limit
3-2	PGOOD_SEL_LDO2	R/W	0h	PGOOD signal source control from LDO2 (Default from NVM memory) 0h = Masked 1h = Powergood threshold voltage 2h = Powergood threshold voltage AND current limit 3h = Powergood threshold voltage AND current limit
1-0	PGOOD_SEL_LDO1	R/W	0h	PGOOD signal source control from LDO1 (Default from NVM memory) 0h = Masked 1h = Powergood threshold voltage 2h = Powergood threshold voltage AND current limit 3h = Powergood threshold voltage AND current limit

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8.7.1.117 PGOOD_SEL_4 Register (Offset = 7Bh) [Reset = 00h]

PGOOD_SEL_4 is shown in Figure 8-176 and described in Table 8-141.

Return to the Table 8-23.

Figure 8-176. PGOOD_SEL_4 Register

7	6	5	4	3	2	1	0
PGOOD_WINDOW	PGOOD_POL	PGOOD_SEL_NRSTOUT_SOC	PGOOD_SEL_NRSTOUT	PGOOD_SEL_TDIE_WARN	RESERVED		PGOOD_SEL_VCCA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

Table 8-141. PGOOD_SEL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PGOOD_WINDOW	R/W	0h	Type of voltage monitoring for PGOOD signal: (Default from NVM memory) 0h = Only undervoltage is monitored 1h = Both undervoltage and overvoltage are monitored
6	PGOOD_POL	R/W	0h	PGOOD signal polarity select: (Default from NVM memory) 0h = PGOOD signal is high when monitored inputs are valid 1h = PGOOD signal is low when monitored inputs are valid
5	PGOOD_SEL_NRSTOUT_SOC	R/W	0h	PGOOD signal source control from nRSTOUT_SOC pin: (Default from NVM memory) 0h = Masked 1h = nRSTOUT_SOC pin low state forces PGOOD signal to low
4	PGOOD_SEL_NRSTOUT	R/W	0h	PGOOD signal source control from nRSTOUT pin: (Default from NVM memory) 0h = Masked 1h = nRSTOUT pin low state forces PGOOD signal to low
3	PGOOD_SEL_TDIE_WARN	R/W	0h	PGOOD signal source control from thermal warning (Default from NVM memory) 0h = Masked 1h = Thermal warning affecting to PGOOD signal
2-1	RESERVED	R/W	0h	
0	PGOOD_SEL_VCCA	R/W	0h	PGOOD signal source control from VCCA monitoring (Default from NVM memory) 0h = Masked 1h = VCCA OV/UV threshold affecting PGOOD signal

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8.7.1.118 PLL_CTRL Register (Offset = 7Ch) [Reset = 00h]

PLL_CTRL is shown in Figure 8-177 and described in Table 8-142.

Return to the Table 8-23.

Figure 8-177. PLL_CTRL Register

7	6	5	4	3	2	1	0
RESERVED						EXT_CLK_FREQ	
R/W-0h						R/W-0h	

Table 8-142. PLL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1-0	EXT_CLK_FREQ	R/W	0h	Frequency of the external clock (SYNCCLKIN): See electrical specification for input clock frequency tolerance. (Default from NVM memory) 0h = 1.1 MHz 1h = 2.2 MHz 2h = 4.4 MHz 3h = Reserved

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8.7.1.119 CONFIG_1 Register (Offset = 7Dh) [Reset = C0h]

CONFIG_1 is shown in Figure 8-178 and described in Table 8-143.

Return to the Table 8-23.

Figure 8-178. CONFIG_1 Register

7	6	5	4	3	2	1	0
NSLEEP2_MASK	NSLEEP1_MASK	EN_ILIM_FSM_CTRL	I2C2_HS	I2C1_HS	RESERVED	TSD_ORD_LEVEL	TWARN_LEVEL
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-143. CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NSLEEP2_MASK	R/W	1h	Masking for NSLEEP2 pin(s) and NSLEEP2B bit: (Default from NVM memory) 0h = NSLEEP2(B) affects FSM state transitions. 1h = NSLEEP2(B) does not affect FSM state transitions.
6	NSLEEP1_MASK	R/W	1h	Masking for NSLEEP1 pin(s) and NSLEEP1B bit: (Default from NVM memory) 0h = NSLEEP1(B) affects FSM state transitions. 1h = NSLEEP1(B) does not affect FSM state transitions.
5	EN_ILIM_FSM_CTRL	R/W	0h	(Default from NVM memory) 0h = Buck/LDO regulators ILIM interrupts do not affect FSM triggers. 1h = Buck/LDO regulators ILIM interrupts affect FSM triggers.
4	I2C2_HS	R/W	0h	Select I2C2 speed (input filter) (Default from NVM memory) 0h = Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode controller code. 1h = Forced to Hs-mode
3	I2C1_HS	R/W	0h	Select I2C1 speed (input filter) (Default from NVM memory) 0h = Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode controller code. 1h = Forced to Hs-mode
2	RESERVED	R/W	0h	
1	TSD_ORD_LEVEL	R/W	0h	Thermal shutdown threshold level. (Default from NVM memory) 0h = 140C 1h = 145C
0	TWARN_LEVEL	R/W	0h	Thermal warning threshold level. (Default from NVM memory) 0h = 130C 1h = 140C

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8.7.1.120 CONFIG_2 Register (Offset = 7Eh) [Reset = 00h]

CONFIG_2 is shown in Figure 8-179 and described in Table 8-144.

Return to the Table 8-23.

Figure 8-179. CONFIG_2 Register

7	6	5	4	3	2	1	0
BB_EOC_RDY	RESERVED			BB_VEOC		BB_ICHR	BB_CHARGER_EN
R-0h	R/W-0h			R/W-0h		R/W-0h	R/W-0h

Table 8-144. CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BB_EOC_RDY	R	0h	Backup end of charge indication 0h = Charging active or not enabled 1h = Charger has reached termination voltage set by BB_VEOC register
6-4	RESERVED	R/W	0h	
3-2	BB_VEOC	R/W	0h	End of charge voltage for backup battery charger: (Default from NVM memory) 0h = 2.5V 1h = 2.8V 2h = 3.0V 3h = 3.3V
1	BB_ICHR	R/W	0h	Backup battery charging current: (Default from NVM memory) 0h = 100uA 1h = 500uA
0	BB_CHARGER_EN	R/W	0h	Backup battery charging: 0h = Disabled 1h = Enabled

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8.7.1.121 ENABLE_DRV_REG Register (Offset = 80h) [Reset = 00h]

ENABLE_DRV_REG is shown in Figure 8-180 and described in Table 8-145.

Return to the Table 8-23.

Figure 8-180. ENABLE_DRV_REG Register

7	6	5	4	3	2	1	0
RESERVED							ENABLE_DRV
R/W-0h							R/W-0h

Table 8-145. ENABLE_DRV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	ENABLE_DRV	R/W	0h	Control for EN_DRV pin: FORCE_EN_DRV_LOW must be 0 to control EN_DRV pin. Otherwise EN_DRV pin is low. 0h = Low 1h = High

8.7.1.122 MISC_CTRL Register (Offset = 81h) [Reset = 00h]

MISC_CTRL is shown in Figure 8-181 and described in Table 8-146.

Return to the Table 8-23.

Figure 8-181. MISC_CTRL Register

7	6	5	4	3	2	1	0
SYNCCLKOUT_FREQ_SEL		SEL_EXT_CLK	AMUXOUT_EN	CLKMON_EN	LPM_EN	NRSTOUT_SOC	NRSTOUT
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-146. MISC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SYNCCLKOUT_FREQ_SEL	R/W	0h	SYNCCLKOUT enable/frequency select: 0h = SYNCCLKOUT off 1h = 1.1 MHz 2h = 2.2 MHz 3h = 4.4 MHz
5	SEL_EXT_CLK	R/W	0h	Selection of external clock: 0h = Forced to internal RC oscillator. 1h = Automatic external clock used when available, interrupt is generated if the external clock is expected (SEL_EXT_CLK = 1), but it is not available or the clock frequency is not within the valid range.
4	AMUXOUT_EN	R/W	0h	Control bandgap voltage to AMUXOUT pin. 0h = Disabled 1h = Enabled
3	CLKMON_EN	R/W	0h	Control of internal clock monitoring. 0h = Disabled 1h = Enabled
2	LPM_EN	R/W	0h	Low power mode control. LPM_EN sets device in a low power mode. Intended use case is for the PFSM to set LPM_EN upon entering a deep sleep state. The end objective is to disable the digital oscillator to reduce power consumption. The following functions are disabled when LPM_EN=1. -TSD cycling of all sensors/thresholds -regmap/SRAM CRC continuous checking -SPMI WD NVM_ID request/response polling -Disable clock monitoring 0h = Low power mode disabled 1h = Low power mode enabled
1	NRSTOUT_SOC	R/W	0h	Control for nRSTOUT_SOC signal: 0h = Low 1h = High
0	NRSTOUT	R/W	0h	Control for nRSTOUT signal: 0h = Low 1h = High

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8.7.1.123 ENABLE_DRV_STAT Register (Offset = 82h) [Reset = 08h]

ENABLE_DRV_STAT is shown in Figure 8-182 and described in Table 8-147.

Return to the Table 8-23.

Figure 8-182. ENABLE_DRV_STAT Register

7	6	5	4	3	2	1	0
RESERVED			SPMI_LPM_EN	FORCE_EN_DRV_LOW	NRSTOUT_SOC_IN	NRSTOUT_IN	EN_DRV_IN
R/W-0h			R/W-0h	R/W-1h	R-0h	R-0h	R-0h

Table 8-147. ENABLE_DRV_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	SPMI_LPM_EN	R/W	0h	This bit is read/write for PFSM and read-only for I2C/SPI SPMI low power mode control. SPMI_LPM_EN sets SPMI in a low power mode which stops SPMI WD (Bus heartbeat). PMICs enters SPMI_LPM_EN=1 at similar times to prevent SPMI WD failures. Therefore to mitigate clock variations, setting SPMI_LPM_EN=1 must be done early in the sequence. The following functions are disabled when SPMI_LPM_EN=1. -SPMI WD NVM_ID request/response polling 0h = SPMI low power mode disabled 1h = SPMI low power mode enabled
3	FORCE_EN_DRV_LOW	R/W	1h	This bit is read/write for PFSM and read-only for I2C/SPI 0h = ENABLE_DRV bit can be written by I2C/SPI 1h = ENABLE_DRV bit is forced low and cannot be written high by I2C/SPI
2	NRSTOUT_SOC_IN	R	0h	Level of NRSTOUT_SOC pin: 0h = Low 1h = High
1	NRSTOUT_IN	R	0h	Level of NRSTOUT pin: 0h = Low 1h = High
0	EN_DRV_IN	R	0h	Level of EN_DRV pin: 0h = Low 1h = High

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8.7.1.124 RECOV_CNT_REG_1 Register (Offset = 83h) [Reset = 00h]

RECOV_CNT_REG_1 is shown in Figure 8-183 and described in Table 8-148.

Return to the Table 8-23.

Figure 8-183. RECOV_CNT_REG_1 Register

7	6	5	4	3	2	1	0
RESERVED				RECOV_CNT			
R-0h				R-0h			

Table 8-148. RECOV_CNT_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-0	RECOV_CNT	R	0h	Recovery counter status. Counter value is incremented each time PMIC goes through warm reset.

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8.7.1.125 RECOV_CNT_REG_2 Register (Offset = 84h) [Reset = 00h]

RECOV_CNT_REG_2 is shown in Figure 8-184 and described in Table 8-149.

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Figure 8-184. RECOV_CNT_REG_2 Register

7	6	5	4	3	2	1	0
RESERVED			RECOV_CNT_CLR	RECOV_CNT_THR			
R/W-0h			R/WSelfClrF-0h	R/W-0h			

Table 8-149. RECOV_CNT_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	RECOV_CNT_CLR	R/WSelfClrF	0h	Recovery counter clear. Write 1 to clear the counter. This bit is automatically set back to 0.
3-0	RECOV_CNT_THR	R/W	0h	Recovery counter threshold value for immediate power-down of all supply rails. (Default from NVM memory)

8.7.1.126 FSM_I2C_TRIGGERS Register (Offset = 85h) [Reset = 00h]

FSM_I2C_TRIGGERS is shown in Figure 8-185 and described in Table 8-150.

Return to the Table 8-23.

Figure 8-185. FSM_I2C_TRIGGERS Register

7	6	5	4	3	2	1	0
TRIGGER_I2C_7	TRIGGER_I2C_6	TRIGGER_I2C_5	TRIGGER_I2C_4	TRIGGER_I2C_3	TRIGGER_I2C_2	TRIGGER_I2C_1	TRIGGER_I2C_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/WSelfClrF-0h	R/WSelfClrF-0h	R/WSelfClrF-0h	R/WSelfClrF-0h

Table 8-150. FSM_I2C_TRIGGERS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TRIGGER_I2C_7	R/W	0h	Trigger for PFSM program.
6	TRIGGER_I2C_6	R/W	0h	Trigger for PFSM program.
5	TRIGGER_I2C_5	R/W	0h	Trigger for PFSM program.
4	TRIGGER_I2C_4	R/W	0h	Trigger for PFSM program.
3	TRIGGER_I2C_3	R/WSelfClrF	0h	Trigger for PFSM program. This bit is automatically cleared. Writing this bit 1 creates PFSM trigger pulse.
2	TRIGGER_I2C_2	R/WSelfClrF	0h	Trigger for PFSM program. This bit is automatically cleared. Writing this bit 1 creates PFSM trigger pulse.
1	TRIGGER_I2C_1	R/WSelfClrF	0h	Trigger for PFSM program. This bit is automatically cleared. Writing this bit 1 creates PFSM trigger pulse.
0	TRIGGER_I2C_0	R/WSelfClrF	0h	Trigger for PFSM program. This bit is automatically cleared. Writing this bit 1 creates PFSM trigger pulse.

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8.7.1.127 FSM_NSLEEP_TRIGGERS Register (Offset = 86h) [Reset = 00h]

FSM_NSLEEP_TRIGGERS is shown in Figure 8-186 and described in Table 8-151.

Return to the Table 8-23.

Figure 8-186. FSM_NSLEEP_TRIGGERS Register

7	6	5	4	3	2	1	0
RESERVED						NSLEEP2B	NSLEEP1B
R/W-0h						R/W-0h	R/W-0h

Table 8-151. FSM_NSLEEP_TRIGGERS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	NSLEEP2B	R/W	0h	Parallel register bit for NSLEEP2 function: 0h = NSLEEP2 low 1h = NSLEEP2 high
0	NSLEEP1B	R/W	0h	Parallel register bit for NSLEEP1 function: 0h = NSLEEP1 low 1h = NSLEEP1 high

8.7.1.128 BUCK_RESET_REG Register (Offset = 87h) [Reset = 00h]

BUCK_RESET_REG is shown in Figure 8-187 and described in Table 8-152.

Return to the Table 8-23.

Figure 8-187. BUCK_RESET_REG Register

7	6	5	4	3	2	1	0
RESERVED			BUCK5_RESET	BUCK4_RESET	BUCK3_RESET	BUCK2_RESET	BUCK1_RESET
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-152. BUCK_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	BUCK5_RESET	R/W	0h	Reset signal for Buck logic. Warning: This bit is for debug only. DO NOT SET THIS BIT TO "1" DURING DEVICE OPERATION.
3	BUCK4_RESET	R/W	0h	Reset signal for Buck logic. Warning: This bit is for debug only. DO NOT SET THIS BIT TO "1" DURING DEVICE OPERATION.
2	BUCK3_RESET	R/W	0h	Reset signal for Buck logic. Warning: This bit is for debug only. DO NOT SET THIS BIT TO "1" DURING DEVICE OPERATION.
1	BUCK2_RESET	R/W	0h	Reset signal for Buck logic. Warning: This bit is for debug only. DO NOT SET THIS BIT TO "1" DURING DEVICE OPERATION.
0	BUCK1_RESET	R/W	0h	Reset signal for Buck logic. Warning: This bit is for debug only. DO NOT SET THIS BIT TO "1" DURING DEVICE OPERATION.

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8.7.1.129 SPREAD_SPECTRUM_1 Register (Offset = 88h) [Reset = 00h]

SPREAD_SPECTRUM_1 is shown in Figure 8-188 and described in Table 8-153.

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Figure 8-188. SPREAD_SPECTRUM_1 Register

7	6	5	4	3	2	1	0
RESERVED					SS_EN	SS_DEPTH	
R/W-0h					R/W-0h	R/W-0h	

Table 8-153. SPREAD_SPECTRUM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	SS_EN	R/W	0h	Spread spectrum enable. (Default from NVM memory) 0h = Spread spectrum disabled 1h = Spread spectrum enabled
1-0	SS_DEPTH	R/W	0h	Spread spectrum modulation depth. (Default from NVM memory) 0h = No modulation 1h = +/- 6.3% 2h = +/- 8.4% 3h = RESERVED

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8.7.1.130 FREQ_SEL Register (Offset = 8Ah) [Reset = 00h]

FREQ_SEL is shown in Figure 8-189 and described in Table 8-154.

Return to the Table 8-23.

Figure 8-189. FREQ_SEL Register

7	6	5	4	3	2	1	0
RESERVED			BUCK5_FREQ_SEL	BUCK4_FREQ_SEL	BUCK3_FREQ_SEL	BUCK2_FREQ_SEL	BUCK1_FREQ_SEL
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-154. FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	BUCK5_FREQ_SEL	R/W	0h	Buck5 switching frequency: This bit is Read/Write or Read-Only for I2C/SPI access depending on NVM configuration. See Technical Reference Manual / User's Guide for details. (Default from NVM memory) 0h = 2.2 MHz 1h = 4.4 MHz
3	BUCK4_FREQ_SEL	R/W	0h	Buck4 switching frequency: This bit is Read/Write or Read-Only for I2C/SPI access depending on NVM configuration. See Technical Reference Manual / User's Guide for details. (Default from NVM memory) 0h = 2.2 MHz 1h = 4.4 MHz
2	BUCK3_FREQ_SEL	R/W	0h	Buck3 switching frequency: This bit is Read/Write or Read-Only for I2C/SPI access depending on NVM configuration. See Technical Reference Manual / User's Guide for details. (Default from NVM memory) 0h = 2.2 MHz 1h = 4.4 MHz
1	BUCK2_FREQ_SEL	R/W	0h	Buck2 switching frequency: This bit is Read/Write or Read-Only for I2C/SPI access depending on NVM configuration. See Technical Reference Manual / User's Guide for details. (Default from NVM memory) 0h = 2.2 MHz 1h = 4.4 MHz
0	BUCK1_FREQ_SEL	R/W	0h	Buck1 switching frequency: This bit is Read/Write or Read-Only for I2C/SPI access depending on NVM configuration. See Technical Reference Manual / User's Guide for details. (Default from NVM memory) 0h = 2.2 MHz 1h = 4.4 MHz

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8.7.1.131 FSM_STEP_SIZE Register (Offset = 8Bh) [Reset = 00h]

FSM_STEP_SIZE is shown in Figure 8-190 and described in Table 8-155.

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Figure 8-190. FSM_STEP_SIZE Register

7	6	5	4	3	2	1	0
RESERVED			PFSM_DELAY_STEP				
R/W-0h			R/W-0h				

Table 8-155. FSM_STEP_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-0	PFSM_DELAY_STEP	R/W	0h	Step size for PFSM sequence counter. Step size is 50ns * $2^{PFSM_DELAY_STEP}$. (Default from NVM memory)

8.7.1.132 LDO_RV_TIMEOUT_REG_1 Register (Offset = 8Ch) [Reset = 00h]

LDO_RV_TIMEOUT_REG_1 is shown in Figure 8-191 and described in Table 8-156.

Return to the Table 8-23.

Figure 8-191. LDO_RV_TIMEOUT_REG_1 Register

7	6	5	4	3	2	1	0
LDO2_RV_TIMEOUT				LDO1_RV_TIMEOUT			
R/W-0h				R/W-0h			

Table 8-156. LDO_RV_TIMEOUT_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LDO2_RV_TIMEOUT	R/W	0h	LDO residual voltage check timeout select. (Default from NVM memory) 0h = 0.5ms 1h = 1ms 2h = 1.5ms 3h = 2ms 4h = 2.5ms 5h = 3ms 6h = 3.5ms 7h = 4ms 8h = 2ms 9h = 4ms Ah = 6ms Bh = 8ms Ch = 10ms Dh = 12ms Eh = 14ms Fh = 16ms
3-0	LDO1_RV_TIMEOUT	R/W	0h	LDO residual voltage check timeout select. (Default from NVM memory) 0h = 0.5ms 1h = 1ms 2h = 1.5ms 3h = 2ms 4h = 2.5ms 5h = 3ms 6h = 3.5ms 7h = 4ms 8h = 2ms 9h = 4ms Ah = 6ms Bh = 8ms Ch = 10ms Dh = 12ms Eh = 14ms Fh = 16ms

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8.7.1.133 LDO_RV_TIMEOUT_REG_2 Register (Offset = 8Dh) [Reset = 00h]

LDO_RV_TIMEOUT_REG_2 is shown in Figure 8-192 and described in Table 8-157.

Return to the Table 8-23.

Figure 8-192. LDO_RV_TIMEOUT_REG_2 Register

7	6	5	4	3	2	1	0
LDO4_RV_TIMEOUT				LDO3_RV_TIMEOUT			
R/W-0h				R/W-0h			

Table 8-157. LDO_RV_TIMEOUT_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LDO4_RV_TIMEOUT	R/W	0h	LDO residual voltage check timeout select. (Default from NVM memory) 0h = 0.5ms 1h = 1ms 2h = 1.5ms 3h = 2ms 4h = 2.5ms 5h = 3ms 6h = 3.5ms 7h = 4ms 8h = 2ms 9h = 4ms Ah = 6ms Bh = 8ms Ch = 10ms Dh = 12ms Eh = 14ms Fh = 16ms
3-0	LDO3_RV_TIMEOUT	R/W	0h	LDO residual voltage check timeout select. (Default from NVM memory) 0h = 0.5ms 1h = 1ms 2h = 1.5ms 3h = 2ms 4h = 2.5ms 5h = 3ms 6h = 3.5ms 7h = 4ms 8h = 2ms 9h = 4ms Ah = 6ms Bh = 8ms Ch = 10ms Dh = 12ms Eh = 14ms Fh = 16ms

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8.7.1.134 USER_SPARE_REGS Register (Offset = 8Eh) [Reset = 00h]

USER_SPARE_REGS is shown in Figure 8-193 and described in Table 8-158.

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Figure 8-193. USER_SPARE_REGS Register

7	6	5	4	3	2	1	0
RESERVED				USER_SPARE_4	USER_SPARE_3	USER_SPARE_2	USER_SPARE_1
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-158. USER_SPARE_REGS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	USER_SPARE_4	R/W	0h	(Default from NVM memory)
2	USER_SPARE_3	R/W	0h	(Default from NVM memory)
1	USER_SPARE_2	R/W	0h	(Default from NVM memory)
0	USER_SPARE_1	R/W	0h	(Default from NVM memory)

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8.7.1.135 ESM_MCU_START_REG Register (Offset = 8Fh) [Reset = 00h]

ESM_MCU_START_REG is shown in Figure 8-194 and described in Table 8-159.

Return to the Table 8-23.

Figure 8-194. ESM_MCU_START_REG Register

7	6	5	4	3	2	1	0
RESERVED							ESM_MCU_START
R/W-0h							R/W-0h

Table 8-159. ESM_MCU_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	ESM_MCU_START	R/W	0h	Control bit to start the ESM_MCU: 0h = ESM_MCU not started. Device clears ENABLE_DRV bit when bit ESM_MCU_EN=1 1h = ESM_MCU started.

8.7.1.136 ESM_MCU_DELAY1_REG Register (Offset = 90h) [Reset = 00h]

ESM_MCU_DELAY1_REG is shown in Figure 8-195 and described in Table 8-160.

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Figure 8-195. ESM_MCU_DELAY1_REG Register

7	6	5	4	3	2	1	0
ESM_MCU_DELAY1							
R/W-0h							

Table 8-160. ESM_MCU_DELAY1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ESM_MCU_DELAY1	R/W	0h	These bits configure the duration of the ESM_MCU delay-1 time-interval (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_MCU_START=0.

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8.7.1.137 ESM_MCU_DELAY2_REG Register (Offset = 91h) [Reset = 00h]

ESM_MCU_DELAY2_REG is shown in Figure 8-196 and described in Table 8-161.

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Figure 8-196. ESM_MCU_DELAY2_REG Register

7	6	5	4	3	2	1	0
ESM_MCU_DELAY2							
R/W-0h							

Table 8-161. ESM_MCU_DELAY2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ESM_MCU_DELAY2	R/W	0h	These bits configure the duration of the ESM_MCU delay-2 time-interval (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_MCU_START=0.

8.7.1.138 ESM_MCU_MODE_CFG Register (Offset = 92h) [Reset = 00h]

ESM_MCU_MODE_CFG is shown in Figure 8-197 and described in Table 8-162.

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Figure 8-197. ESM_MCU_MODE_CFG Register

7	6	5	4	3	2	1	0
ESM_MCU_MODE	ESM_MCU_EN	ESM_MCU_ENDRV	RESERVED	ESM_MCU_ERR_CNT_TH			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

Table 8-162. ESM_MCU_MODE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ESM_MCU_MODE	R/W	0h	This bit selects the mode for the ESM_MCU: These bits can be only be written when control bit ESM_MCU_START=0. 0h = Level Mode 1h = PWM Mode
6	ESM_MCU_EN	R/W	0h	ESM_MCU enable configuration bit: These bits can be only be written when control bit ESM_MCU_START=0. 0h = ESM_MCU disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt bits are cleared 1h = ESM_MCU enabled. MCU can set ENABLE_DRV bit to 1 if: - bit ESM_MCU_START=1, and - (ESM_MCU_FAIL_INT=0 or ESM_MCU_ENDRV=0), and - ESM_MCU_RST_INT=0, and - all other interrupt bits are cleared
5	ESM_MCU_ENDRV	R/W	0h	Configuration bit to select ENABLE_DRV clear on ESM-error for ESM_MCU: These bits can be only be written when control bit ESM_MCU_START=0. 0h = ENABLE_DRV not cleared when ESM_MCU_FAIL_INT=1 1h = ENABLE_DRV cleared when ESM_MCU_FAIL_INT=1
4	RESERVED	R/W	0h	
3-0	ESM_MCU_ERR_CNT_TH	R/W	0h	Configuration bits for the threshold of the ESM_MCU error-counter. The ESM_MCU starts the Error Handling Procedure (see Error Signal Monitor chapter) if ESM_MCU_ERR_CNT[4:0] > ESM_MCU_ERR_CNT_TH[3:0]. These bits can be only be written when control bit ESM_MCU_START=0.

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8.7.1.139 ESM_MCU_HMAX_REG Register (Offset = 93h) [Reset = 00h]

ESM_MCU_HMAX_REG is shown in Figure 8-198 and described in Table 8-163.

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Figure 8-198. ESM_MCU_HMAX_REG Register

7	6	5	4	3	2	1	0
ESM_MCU_HMAX							
R/W-0h							

Table 8-163. ESM_MCU_HMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ESM_MCU_HMAX	R/W	0h	These bits configure the the maximum high-pulse time-threshold (tHIGH_MAX_TH) for ESM_MCU (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_MCU_START=0.

8.7.1.140 ESM_MCU_HMIN_REG Register (Offset = 94h) [Reset = 00h]

ESM_MCU_HMIN_REG is shown in Figure 8-199 and described in Table 8-164.

Return to the Table 8-23.

Figure 8-199. ESM_MCU_HMIN_REG Register

7	6	5	4	3	2	1	0
ESM_MCU_HMIN							
R/W-0h							

Table 8-164. ESM_MCU_HMIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ESM_MCU_HMIN	R/W	0h	These bits configure the the minimum high-pulse time-threshold (tHIGH_MIN_TH) for ESM_MCU (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_MCU_START=0.

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8.7.1.141 ESM_MCU_LMAX_REG Register (Offset = 95h) [Reset = 00h]

ESM_MCU_LMAX_REG is shown in Figure 8-200 and described in Table 8-165.

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Figure 8-200. ESM_MCU_LMAX_REG Register

7	6	5	4	3	2	1	0
ESM_MCU_LMAX							
R/W-0h							

Table 8-165. ESM_MCU_LMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ESM_MCU_LMAX	R/W	0h	These bits configure the the maximum low-pulse time-threshold (tLOW_MAX_TH) for ESM_MCU (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_MCU_START=0.

8.7.1.142 ESM_MCU_LMIN_REG Register (Offset = 96h) [Reset = 00h]

ESM_MCU_LMIN_REG is shown in Figure 8-201 and described in Table 8-166.

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Figure 8-201. ESM_MCU_LMIN_REG Register

7	6	5	4	3	2	1	0
ESM_MCU_LMIN							
R/W-0h							

Table 8-166. ESM_MCU_LMIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ESM_MCU_LMIN	R/W	0h	These bits configure the the minimum low-pulse time-threshold (tLOW_MAX_TH) for ESM_MCU (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_MCU_START=0.

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8.7.1.143 ESM_MCU_ERR_CNT_REG Register (Offset = 97h) [Reset = 00h]

ESM_MCU_ERR_CNT_REG is shown in Figure 8-202 and described in Table 8-167.

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Figure 8-202. ESM_MCU_ERR_CNT_REG Register

7	6	5	4	3	2	1	0
RESERVED			ESM_MCU_ERR_CNT				
R-0h			R-0h				

Table 8-167. ESM_MCU_ERR_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	ESM_MCU_ERR_CNT	R	0h	Status bits to indicate the value of the ESM_MCU Error-Counter. The device clears these bits when ESM_MCU_START bit is 0, or when the device resets the MCU.

8.7.1.144 ESM_SOC_START_REG Register (Offset = 98h) [Reset = 00h]

ESM_SOC_START_REG is shown in Figure 8-203 and described in Table 8-168.

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Figure 8-203. ESM_SOC_START_REG Register

7	6	5	4	3	2	1	0
RESERVED							ESM_SOC_START
R/W-0h							R/W-0h

Table 8-168. ESM_SOC_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	ESM_SOC_START	R/W	0h	Control bit to start the ESM_SoC: 0h = ESM_SoC not started. Device clears ENABLE_DRV bit when bit ESM_SOC_EN=1 1h = ESM_SoC started

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8.7.1.145 ESM_SOC_DELAY1_REG Register (Offset = 99h) [Reset = 00h]

ESM_SOC_DELAY1_REG is shown in Figure 8-204 and described in Table 8-169.

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Figure 8-204. ESM_SOC_DELAY1_REG Register

7	6	5	4	3	2	1	0
ESM_SOC_DELAY1							
R/W-0h							

Table 8-169. ESM_SOC_DELAY1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ESM_SOC_DELAY1	R/W	0h	These bits configure the duration of the ESM_SoC delay-1 time-interval (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_SOC_START=0.

8.7.1.146 ESM_SOC_DELAY2_REG Register (Offset = 9Ah) [Reset = 00h]

ESM_SOC_DELAY2_REG is shown in Figure 8-205 and described in Table 8-170.

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Figure 8-205. ESM_SOC_DELAY2_REG Register

7	6	5	4	3	2	1	0
ESM_SOC_DELAY2							
R/W-0h							

Table 8-170. ESM_SOC_DELAY2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ESM_SOC_DELAY2	R/W	0h	These bits configure the duration of the ESM_SoC delay-2 time-interval (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_SOC_START=0.

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8.7.1.147 ESM_SOC_MODE_CFG Register (Offset = 9Bh) [Reset = 00h]

ESM_SOC_MODE_CFG is shown in Figure 8-206 and described in Table 8-171.

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Figure 8-206. ESM_SOC_MODE_CFG Register

7	6	5	4	3	2	1	0
ESM_SOC_MODE	ESM_SOC_EN	ESM_SOC_ENDRV	RESERVED	ESM_SOC_ERR_CNT_TH			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

Table 8-171. ESM_SOC_MODE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ESM_SOC_MODE	R/W	0h	This bit selects the mode for the ESM_SoC: These bits can be only be written when control bit ESM_SOC_START=0. 0h = Level Mode 1h = PWM Mode
6	ESM_SOC_EN	R/W	0h	ESM_SoC enable configuration bit: These bits can be only be written when control bit ESM_SOC_START=0. 0h = ESM_SoC disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt bits are cleared 1h = ESM_SoC enabled. MCU can set ENABLE_DRV bit to 1 if: - bit ESM_SOC_START=1, and - (ESM_SOC_FAIL_INT=0 or ESM_SOC_ENDRV=0), and - ESM_SOC_RST_INT=0, and - all other interrupt bits are cleared.
5	ESM_SOC_ENDRV	R/W	0h	Configuration bit to select ENABLE_DRV clear on ESM-error for ESM_SoC: These bits can be only be written when control bit ESM_SOC_START=0 0h = ENABLE_DRV not cleared when ESM_SOC_FAIL_INT=1 1h = ENABLE_DRV cleared when ESM_SOC_FAIL_INT=1.
4	RESERVED	R/W	0h	
3-0	ESM_SOC_ERR_CNT_TH	R/W	0h	Configuration bits for the threshold of the ESM_SoC error-counter The ESM_SoC starts the Error Handling Procedure (see Error Signal Monitor chapter) if ESM_SOC_ERR_CNT[4:0] > ESM_SOC_ERR_CNT_TH[3:0]. These bits can be only be written when control bit ESM_SOC_START=0.

8.7.1.148 ESM_SOC_HMAX_REG Register (Offset = 9Ch) [Reset = 00h]

ESM_SOC_HMAX_REG is shown in Figure 8-207 and described in Table 8-172.

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Figure 8-207. ESM_SOC_HMAX_REG Register

7	6	5	4	3	2	1	0
ESM_SOC_HMAX							
R/W-0h							

Table 8-172. ESM_SOC_HMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ESM_SOC_HMAX	R/W	0h	These bits configure the the maximum high-pulse time-threshold (tHIGH_MAX_TH) for ESM_SoC (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_SOC_START=0.

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8.7.1.149 ESM_SOC_HMIN_REG Register (Offset = 9Dh) [Reset = 00h]

ESM_SOC_HMIN_REG is shown in Figure 8-208 and described in Table 8-173.

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Figure 8-208. ESM_SOC_HMIN_REG Register

7	6	5	4	3	2	1	0
ESM_SOC_HMIN							
R/W-0h							

Table 8-173. ESM_SOC_HMIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ESM_SOC_HMIN	R/W	0h	These bits configure the the minimum high-pulse time-threshold (tHIGH_MIN_TH) for ESM_SoC (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_SOC_START=0.

8.7.1.150 ESM_SOC_LMAX_REG Register (Offset = 9Eh) [Reset = 00h]

ESM_SOC_LMAX_REG is shown in Figure 8-209 and described in Table 8-174.

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Figure 8-209. ESM_SOC_LMAX_REG Register

7	6	5	4	3	2	1	0
ESM_SOC_LMAX							
R/W-0h							

Table 8-174. ESM_SOC_LMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ESM_SOC_LMAX	R/W	0h	These bits configure the the maximum low-pulse time-threshold (tLOW_MAX_TH) for ESM_SoC (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_SOC_START=0.

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8.7.1.151 ESM_SOC_LMIN_REG Register (Offset = 9Fh) [Reset = 00h]

ESM_SOC_LMIN_REG is shown in Figure 8-210 and described in Table 8-175.

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Figure 8-210. ESM_SOC_LMIN_REG Register

7	6	5	4	3	2	1	0
ESM_SOC_LMIN							
R/W-0h							

Table 8-175. ESM_SOC_LMIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ESM_SOC_LMIN	R/W	0h	These bits configure the the minimum low-pulse time-threshold (tLOW_MAX_TH) for ESM_SoC (see Error Signal Monitor chapter). These bits can be only be written when control bit ESM_SOC_START=0.

8.7.1.152 ESM_SOC_ERR_CNT_REG Register (Offset = A0h) [Reset = 00h]

ESM_SOC_ERR_CNT_REG is shown in Figure 8-211 and described in Table 8-176.

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Figure 8-211. ESM_SOC_ERR_CNT_REG Register

7	6	5	4	3	2	1	0
RESERVED			ESM_SOC_ERR_CNT				
R-0h			R-0h				

Table 8-176. ESM_SOC_ERR_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	ESM_SOC_ERR_CNT	R	0h	Status bits to indicate the value of the ESM_SoC Error-Counter. The device clears these bits when ESM_SOC_START bit is 0, or when the device resets the SoC.

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8.7.1.153 REGISTER_LOCK Register (Offset = A1h) [Reset = 00h]

REGISTER_LOCK is shown in Figure 8-212 and described in Table 8-177.

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Figure 8-212. REGISTER_LOCK Register

7	6	5	4	3	2	1	0
RESERVED							REGISTER_LOCK_STATUS
R/W-0h							R/W-0h

Table 8-177. REGISTER_LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	REGISTER_LOCK_STATUS	R/W	0h	Unlocking registers: write 0x9B to this address. Locking registers: write anything else than 0x9B to this address. Written 8 bit data to this address is not stored, only lock status can be read. REGISTER_LOCK_STATUS bit shows the lock status: 0h = Registers are unlocked 1h = Registers are locked

8.7.1.154 MANUFACTURING_VER Register (Offset = A6h) [Reset = 00h]

MANUFACTURING_VER is shown in Figure 8-213 and described in Table 8-178.

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Figure 8-213. MANUFACTURING_VER Register

7	6	5	4	3	2	1	0
SILICON_REV							
R-0h							

Table 8-178. MANUFACTURING_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SILICON_REV	R	0h	SILICON_REV[7:6] - Reserved SILICON_REV[5:3] - ALR SILICON_REV[2:0] - Metal

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8.7.1.155 CUSTOMER_NVM_ID_REG Register (Offset = A7h) [Reset = 00h]

CUSTOMER_NVM_ID_REG is shown in Figure 8-214 and described in Table 8-179.

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Figure 8-214. CUSTOMER_NVM_ID_REG Register

7	6	5	4	3	2	1	0
CUSTOMER_NVM_ID							
R/W-0h							

Table 8-179. CUSTOMER_NVM_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOMER_NVM_ID	R/W	0h	Customer defined value if customer programmed part Same value as in TI_NVM_ID register if TI programmed part

8.7.1.156 SOFT_REBOOT_REG Register (Offset = ABh) [Reset = 00h]

SOFT_REBOOT_REG is shown in Figure 8-215 and described in Table 8-180.

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Figure 8-215. SOFT_REBOOT_REG Register

7	6	5	4	3	2	1	0
RESERVED							SOFT_REBOOT
R/W-0h							R/WSelfClrF-0h

Table 8-180. SOFT_REBOOT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	SOFT_REBOOT	R/WSelfClrF	0h	Write 1 to request a soft reboot. This bit is automatically cleared.

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8.7.1.157 RTC_SECONDS Register (Offset = B5h) [Reset = 00h]

RTC_SECONDS is shown in Figure 8-216 and described in Table 8-181.

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Figure 8-216. RTC_SECONDS Register

7	6	5	4	3	2	1	0
RESERVED	SECOND_1			SECOND_0			
R/W-0h	R/W-0h			R/W-0h			

Table 8-181. RTC_SECONDS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	SECOND_1	R/W	0h	Second digit of seconds (range is 0 up to 5)
3-0	SECOND_0	R/W	0h	First digit of seconds (range is 0 up to 9)

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8.7.1.158 RTC_MINUTES Register (Offset = B6h) [Reset = 00h]

RTC_MINUTES is shown in Figure 8-217 and described in Table 8-182.

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Figure 8-217. RTC_MINUTES Register

7	6	5	4	3	2	1	0
RESERVED	MINUTE_1			MINUTE_0			
R/W-0h	R/W-0h			R/W-0h			

Table 8-182. RTC_MINUTES Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	MINUTE_1	R/W	0h	Second digit of minutes (range is 0 up to 5)
3-0	MINUTE_0	R/W	0h	First digit of minutes (range is 0 up to 9)

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8.7.1.159 RTC_HOURS Register (Offset = B7h) [Reset = 00h]

RTC_HOURS is shown in Figure 8-218 and described in Table 8-183.

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Figure 8-218. RTC_HOURS Register

7	6	5	4	3	2	1	0
PM_NAM	RESERVED	HOUR_1		HOUR_0			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			

Table 8-183. RTC_HOURS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PM_NAM	R/W	0h	Only used in PM_AM mode (otherwise it is set to 0) 0h = AM 1h = PM
6	RESERVED	R/W	0h	
5-4	HOUR_1	R/W	0h	Second digit of hours(range is 0 up to 2)
3-0	HOUR_0	R/W	0h	First digit of hours (range is 0 up to 9)

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8.7.1.160 RTC_DAYS Register (Offset = B8h) [Reset = 00h]

RTC_DAYS is shown in Figure 8-219 and described in Table 8-184.

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Figure 8-219. RTC_DAYS Register

7	6	5	4	3	2	1	0
RESERVED		DAY_1		DAY_0			
R/W-0h		R/W-0h		R/W-0h			

Table 8-184. RTC_DAYS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-4	DAY_1	R/W	0h	Second digit of days (range is 0 up to 3)
3-0	DAY_0	R/W	0h	First digit of days (range is 0 up to 9)

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8.7.1.161 RTC_MONTHS Register (Offset = B9h) [Reset = 00h]

RTC_MONTHS is shown in Figure 8-220 and described in Table 8-185.

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Figure 8-220. RTC_MONTHS Register

7	6	5	4	3	2	1	0
RESERVED			MONTH_1	MONTH_0			
R/W-0h			R/W-0h	R/W-0h			

Table 8-185. RTC_MONTHS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	MONTH_1	R/W	0h	Second digit of months (range is 0 up to 1)
3-0	MONTH_0	R/W	0h	First digit of months (range is 0 up to 9)

8.7.1.162 RTC_YEARS Register (Offset = BAh) [Reset = 00h]

RTC_YEARS is shown in Figure 8-221 and described in Table 8-186.

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Figure 8-221. RTC_YEARS Register

7	6	5	4	3	2	1	0
YEAR_1				YEAR_0			
R/W-0h				R/W-0h			

Table 8-186. RTC_YEARS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	YEAR_1	R/W	0h	Second digit of years (range is 0 up to 9)
3-0	YEAR_0	R/W	0h	First digit of years (range is 0 up to 9)

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8.7.1.163 RTC_WEEKS Register (Offset = BBh) [Reset = 00h]

RTC_WEEKS is shown in Figure 8-222 and described in Table 8-187.

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Figure 8-222. RTC_WEEKS Register

7	6	5	4	3	2	1	0
RESERVED					WEEK		
R/W-0h					R/W-0h		

Table 8-187. RTC_WEEKS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2-0	WEEK	R/W	0h	First digit of day of the week (range is 0 up to 6)

8.7.1.164 ALARM_SECONDS Register (Offset = BCh) [Reset = 00h]

ALARM_SECONDS is shown in Figure 8-223 and described in Table 8-188.

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Figure 8-223. ALARM_SECONDS Register

7	6	5	4	3	2	1	0
RESERVED	ALR_SECOND_1			ALR_SECOND_0			
R/W-0h	R/W-0h			R/W-0h			

Table 8-188. ALARM_SECONDS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	ALR_SECOND_1	R/W	0h	Second digit of alarm programmation for seconds (range is 0 up to 5)
3-0	ALR_SECOND_0	R/W	0h	First digit of alarm programmation for seconds (range is 0 up to 9)

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8.7.1.165 ALARM_MINUTES Register (Offset = BDh) [Reset = 00h]

ALARM_MINUTES is shown in Figure 8-224 and described in Table 8-189.

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Figure 8-224. ALARM_MINUTES Register

7	6	5	4	3	2	1	0
RESERVED	ALR_MINUTE_1			ALR_MINUTE_0			
R/W-0h	R/W-0h			R/W-0h			

Table 8-189. ALARM_MINUTES Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	ALR_MINUTE_1	R/W	0h	Second digit of alarm programmation for minutes (range is 0 up to 5)
3-0	ALR_MINUTE_0	R/W	0h	First digit of alarm programmation for minutes (range is 0 up to 9)

8.7.1.166 ALARM_HOURS Register (Offset = BEh) [Reset = 00h]

ALARM_HOURS is shown in Figure 8-225 and described in Table 8-190.

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Figure 8-225. ALARM_HOURS Register

7	6	5	4	3	2	1	0
ALR_PM_NAM	RESERVED	ALR_HOUR_1		ALR_HOUR_0			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			

Table 8-190. ALARM_HOURS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ALR_PM_NAM	R/W	0h	Only used in PM_AM mode for alarm programmation (otherwise it is set to 0) 0h = AM 1h = PM
6	RESERVED	R/W	0h	
5-4	ALR_HOUR_1	R/W	0h	Second digit of alarm programmation for hours(range is 0 up to 2)
3-0	ALR_HOUR_0	R/W	0h	First digit of alarm programmation for hours (range is 0 up to 9)

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8.7.1.167 ALARM_DAYS Register (Offset = BFh) [Reset = 00h]

ALARM_DAYS is shown in Figure 8-226 and described in Table 8-191.

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Figure 8-226. ALARM_DAYS Register

7	6	5	4	3	2	1	0
RESERVED		ALR_DAY_1		ALR_DAY_0			
R/W-0h		R/W-0h		R/W-0h			

Table 8-191. ALARM_DAYS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-4	ALR_DAY_1	R/W	0h	Second digit of alarm programmation for days (range is 0 up to 3)
3-0	ALR_DAY_0	R/W	0h	First digit of alarm programmation for days (range is 0 up to 9)

8.7.1.168 ALARM_MONTHS Register (Offset = C0h) [Reset = 00h]

ALARM_MONTHS is shown in Figure 8-227 and described in Table 8-192.

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Figure 8-227. ALARM_MONTHS Register

7	6	5	4	3	2	1	0
RESERVED			ALR_MONTH_1	ALR_MONTH_0			
R/W-0h			R/W-0h	R/W-0h			

Table 8-192. ALARM_MONTHS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	ALR_MONTH_1	R/W	0h	Second digit of alarm programmation for months (range is 0 up to 1)
3-0	ALR_MONTH_0	R/W	0h	First digit of alarm programmation for months (range is 0 up to 9)

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8.7.1.169 ALARM_YEARS Register (Offset = C1h) [Reset = 00h]

ALARM_YEARS is shown in Figure 8-228 and described in Table 8-193.

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Figure 8-228. ALARM_YEARS Register

7	6	5	4	3	2	1	0
ALR_YEAR_1				ALR_YEAR_0			
R/W-0h				R/W-0h			

Table 8-193. ALARM_YEARS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ALR_YEAR_1	R/W	0h	Second digit of alarm programmation for years (range is 0 up to 9)
3-0	ALR_YEAR_0	R/W	0h	First digit of alarm programmation for years (range is 0 up to 9)

8.7.1.170 RTC_CTRL_1 Register (Offset = C2h) [Reset = 00h]

RTC_CTRL_1 is shown in Figure 8-229 and described in Table 8-194.

Return to the Table 8-23.

Figure 8-229. RTC_CTRL_1 Register

7	6	5	4	3	2	1	0
RTC_V_OPT	GET_TIME	SET_32_COUNTER	RESERVED	MODE_12_24	AUTO_COMP	ROUND_30S	STOP_RTC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-194. RTC_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RTC_V_OPT	R/W	0h	RTC date / time register selection: 0h = Read access directly to dynamic registers (RTC_SECONDS, RTC_MINUTES, RTC_HOURS, RTC_DAYS, RTC_MONTHS, RTC_YEAR, RTC_WEEKS) 1h = Read access to static shadowed registers: (see GET_TIME bit).
6	GET_TIME	R/W	0h	When writing a 1 into this register, the content of the dynamic registers (RTC_SECONDS, RTC_MINUTES, RTC_HOURS, RTC_DAYS, RTC_MONTHS, RTC_YEARS_ and RTC_WEEKS) is transferred into static shadowed registers. Each update of the shadowed registers needs to be done by re-asserting GET_TIME bit to 1 (i.e.: reset it to 0 and then rewrite it to 1) Note: Shadowed registers, linked to the GET_TIME feature, are a parallel set of calendar static registers, at the same I2C addresses as the dynamic registers. Note: The GET_TIME feature loads the RTC counter in the shadow registers and make the content of the shadow registers available and stable for reading. Note: The GET_TIME bit has to be set to 0 and again to 1 to get a new timing value. Note: If the time reading is done without GET_TIME, the read value comes directly from the RTC counter and software has to manage the counter change during the reading. Time reading remains always at the same address, with or without using the GET_TIME feature.
5	SET_32_COUNTER	R/W	0h	Note: This bit must only be used when the RTC is frozen. 0h = No action 1h = Set the 32kHz counter with RTC_COMP_MSB_REG/ RTC_COMP_LSB_REG value
4	RESERVED	R/W	0h	
3	MODE_12_24	R/W	0h	Note: It is possible to switch between the two modes at any time without disturbed the RTC, read or write are always performed with the current mode. 0h = 24 hours mode 1h = 12 hours mode (PM-AM mode)
2	AUTO_COMP	R/W	0h	AUTO_COMP 0h = No auto compensation 1h = Auto compensation enabled
1	ROUND_30S	R/W	0h	Note: This bit is a toggle bit, the micro-controller can only write one and RTC clears it. If the micro-controller sets the ROUND_30S bit and then read it, the micro-controller reads one until the rounding to the closest minute is performed at the next second. 0h = No update 1h = When a one is written, the time is rounded to the closest minute
0	STOP_RTC	R/W	0h	STOP_RTC 0h = RTC is frozen 1h = RTC is running

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8.7.1.171 RTC_CTRL_2 Register (Offset = C3h) [Reset = 00h]

RTC_CTRL_2 is shown in Figure 8-230 and described in Table 8-195.

Return to the Table 8-23.

Figure 8-230. RTC_CTRL_2 Register

7	6	5	4	3	2	1	0
FIRST_START UP_DONE	STARTUP_DEST		FAST_BIST	LP_STANDBY_ SEL	XTAL_SEL		XTAL_EN
R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h		R/W-0h

Table 8-195. RTC_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FIRST_STARTUP_DONE	R/W	0h	This bit controls if pre-configured NVM defaults are loaded to RTC domain reg bits during NVM read 0h = pre-configured NVM defaults are loaded to RTC domain bits 1h = pre-configured NVM defaults are not loaded to RTC domain bits
6-5	STARTUP_DEST	R/W	0h	FSM start-up destination select. (Default from NVM memory) 0h = STANDBY/LP_STANDBY based on LP_STANDBY_SEL 1h = Reserved 2h = MCU_ONLY 3h = ACTIVE
4	FAST_BIST	R/W	0h	FAST_BIST (Default from NVM memory) 0h = Logic and analog BIST is run at BOOT BIST. 1h = Only analog BIST is run at BOOT BIST.
3	LP_STANDBY_SEL	R/W	0h	Control to enter low power standby state: (Default from NVM memory) 0h = LDOINT is enabled in standby state. 1h = Low power standby state is used as standby state (LDOINT is disabled).
2-1	XTAL_SEL	R/W	0h	Crystal oscillator type select (Default from NVM memory) 0h = 6 pF 1h = 9 pF 2h = 12.5 pF 3h = Reserved
0	XTAL_EN	R/W	0h	Crystal oscillator enable. (Default from NVM memory) 0h = Crystal oscillator is disabled 1h = Crystal oscillator is enabled

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8.7.1.172 RTC_STATUS Register (Offset = C4h) [Reset = 80h]

RTC_STATUS is shown in Figure 8-231 and described in Table 8-196.

Return to the Table 8-23.

Figure 8-231. RTC_STATUS Register

7	6	5	4	3	2	1	0
POWER_UP	ALARM	TIMER	RESERVED			RUN	RESERVED
R/W1C-1h	R/W1C-0h	R/W1C-0h	R/W-0h			R-0h	R/W-0h

Table 8-196. RTC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	POWER_UP	R/W1C	1h	Indicates that a reset occurred (bit cleared to 0 by writing 1) and that RTC data are not valid anymore. Note: POWER_UP is set by a reset, is cleared by writing one in this bit. Note: The POWER_UP (RTC_STATUS) and RESET_STATUS (RTC_RESET_STATUS) register bits indicate the same information.
6	ALARM	R/W1C	0h	Indicates that an alarm interrupt has been generated (bit clear by writing 1).
5	TIMER	R/W1C	0h	Indicates that an timer interrupt has been generated (bit clear by writing 1).
4-2	RESERVED	R/W	0h	
1	RUN	R	0h	Note: This bit shows the real state of the RTC, indeed because of STOP_RTC (RTC_CTRL) signal was resynchronized on 32kHz clock, the action of this bit is delayed. 0h = RTC is frozen 1h = RTC is running
0	RESERVED	R/W	0h	

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8.7.1.173 RTC_INTERRUPTS Register (Offset = C5h) [Reset = 00h]

RTC_INTERRUPTS is shown in Figure 8-232 and described in Table 8-197.

Return to the Table 8-23.

Figure 8-232. RTC_INTERRUPTS Register

7	6	5	4	3	2	1	0
RESERVED				IT_ALARM	IT_TIMER	EVERY	
R/W-0h				R/W-0h	R/W-0h	R/W-0h	

Table 8-197. RTC_INTERRUPTS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	IT_ALARM	R/W	0h	Enable one interrupt when the alarm value is reached (TC ALARM registers: ALARM_SECONDS, ALARM_MINUTES, ALARM_HOURS, ALARM_DAYS, ALARM_MONTHS, ALARM_YEARS) by the TC registers NOTE: To prevent mis-firing of the ALARM interrupt, set the IT_ALARM = 0 prior to configuring the ALARM registers 0h = interrupt disabled 1h = interrupt enabled
2	IT_TIMER	R/W	0h	Enable periodic interrupt NOTE: To prevent mis-firing of the TIMER interrupt, set the IT_TIMER = 0 prior to configuring the periodic time value 0h = interrupt disabled 1h = interrupt enabled
1-0	EVERY	R/W	0h	Interrupt period 0h = every second 1h = every minute 2h = every hour 3h = every day

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8.7.1.174 RTC_COMP_LSB Register (Offset = C6h) [Reset = 00h]

RTC_COMP_LSB is shown in Figure 8-233 and described in Table 8-198.

Return to the Table 8-23.

Figure 8-233. RTC_COMP_LSB Register

7	6	5	4	3	2	1	0
COMP_LSB_RTC							
R/W-0h							

Table 8-198. RTC_COMP_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	COMP_LSB_RTC	R/W	0h	This register contains the number of 32kHz periods to be added into the 32kHz counter every hour [LSB]

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8.7.1.175 RTC_COMP_MSB Register (Offset = C7h) [Reset = 00h]

RTC_COMP_MSB is shown in Figure 8-234 and described in Table 8-199.

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Figure 8-234. RTC_COMP_MSB Register

7	6	5	4	3	2	1	0
COMP_MSB_RTC							
R/W-0h							

Table 8-199. RTC_COMP_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	COMP_MSB_RTC	R/W	0h	This register contains the number of 32kHz periods to be added into the 32kHz counter every hour [MSB]

8.7.1.176 RTC_RESET_STATUS Register (Offset = C8h) [Reset = 00h]

RTC_RESET_STATUS is shown in Figure 8-235 and described in Table 8-200.

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Figure 8-235. RTC_RESET_STATUS Register

7	6	5	4	3	2	1	0
RESERVED							RESET_STATUS_RTC
R/W-0h							R/W-0h

Table 8-200. RTC_RESET_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	RESET_STATUS_RTC	R/W	0h	This bit can only be set to one and is cleared when a manual reset or a POR (case of VOUT_LDO_RTC below the LDO_RTC POR level) occur. If this bit is reset it means that the RTC has lost its configuration. Note: The RESET_STATUS (RTC_RESET_STATUS) and POWER_UP (RTC_STATUS) register bits indicate the same information.

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8.7.1.177 SCRATCH_PAD_REG_1 Register (Offset = C9h) [Reset = 00h]

SCRATCH_PAD_REG_1 is shown in Figure 8-236 and described in Table 8-201.

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Figure 8-236. SCRATCH_PAD_REG_1 Register

7	6	5	4	3	2	1	0
SCRATCH_PAD_1							
R/W-0h							

Table 8-201. SCRATCH_PAD_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SCRATCH_PAD_1	R/W	0h	Scratchpad for temporary data storage. The register is reset only when VRTC is disabled. The data is maintained when VINT regulator is disabled, for example during LP_STANDBY state.

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8.7.1.178 SCRATCH_PAD_REG_2 Register (Offset = CAh) [Reset = 00h]

SCRATCH_PAD_REG_2 is shown in Figure 8-237 and described in Table 8-202.

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Figure 8-237. SCRATCH_PAD_REG_2 Register

7	6	5	4	3	2	1	0
SCRATCH_PAD_2							
R/W-0h							

Table 8-202. SCRATCH_PAD_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SCRATCH_PAD_2	R/W	0h	Scratchpad for temporary data storage. The register is reset only when VRTC is disabled. The data is maintained when VINT regulator is disabled, for example during LP_STANDBY state.

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8.7.1.179 SCRATCH_PAD_REG_3 Register (Offset = CBh) [Reset = 00h]

SCRATCH_PAD_REG_3 is shown in Figure 8-238 and described in Table 8-203.

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Figure 8-238. SCRATCH_PAD_REG_3 Register

7	6	5	4	3	2	1	0
SCRATCH_PAD_3							
R/W-0h							

Table 8-203. SCRATCH_PAD_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SCRATCH_PAD_3	R/W	0h	Scratchpad for temporary data storage. The register is reset only when VRTC is disabled. The data is maintained when VINT regulator is disabled, for example during LP_STANDBY state.

8.7.1.180 SCRATCH_PAD_REG_4 Register (Offset = CCh) [Reset = 00h]

SCRATCH_PAD_REG_4 is shown in Figure 8-239 and described in Table 8-204.

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Figure 8-239. SCRATCH_PAD_REG_4 Register

7	6	5	4	3	2	1	0
SCRATCH_PAD_4							
R/W-0h							

Table 8-204. SCRATCH_PAD_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SCRATCH_PAD_4	R/W	0h	Scratchpad for temporary data storage. The register is reset only when VRTC is disabled. The data is maintained when VINT regulator is disabled, for example during LP_STANDBY state.

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8.7.1.181 PFSM_DELAY_REG_1 Register (Offset = CDh) [Reset = 00h]

PFSM_DELAY_REG_1 is shown in Figure 8-240 and described in Table 8-205.

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Figure 8-240. PFSM_DELAY_REG_1 Register

7	6	5	4	3	2	1	0
PFSM_DELAY1							
R/W-0h							

Table 8-205. PFSM_DELAY_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PFSM_DELAY1	R/W	0h	Generic delay1 for PFSM use. The step size is defined by PFSM_DELAY_STEP bits. (Default from NVM memory)

8.7.1.182 PFSM_DELAY_REG_2 Register (Offset = CEh) [Reset = 00h]

PFSM_DELAY_REG_2 is shown in Figure 8-241 and described in Table 8-206.

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Figure 8-241. PFSM_DELAY_REG_2 Register

7	6	5	4	3	2	1	0
PFSM_DELAY2							
R/W-0h							

Table 8-206. PFSM_DELAY_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PFSM_DELAY2	R/W	0h	Generic delay2 for PFSM use. The step size is defined by PFSM_DELAY_STEP bits. (Default from NVM memory)

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8.7.1.183 PFSM_DELAY_REG_3 Register (Offset = CFh) [Reset = 00h]

PFSM_DELAY_REG_3 is shown in Figure 8-242 and described in Table 8-207.

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Figure 8-242. PFSM_DELAY_REG_3 Register

7	6	5	4	3	2	1	0
PFSM_DELAY3							
R/W-0h							

Table 8-207. PFSM_DELAY_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PFSM_DELAY3	R/W	0h	Generic delay3 for PFSM use. The step size is defined by PFSM_DELAY_STEP bits. (Default from NVM memory)

8.7.1.184 PFSM_DELAY_REG_4 Register (Offset = D0h) [Reset = 00h]

PFSM_DELAY_REG_4 is shown in Figure 8-243 and described in Table 8-208.

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Figure 8-243. PFSM_DELAY_REG_4 Register

7	6	5	4	3	2	1	0
PFSM_DELAY4							
R/W-0h							

Table 8-208. PFSM_DELAY_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PFSM_DELAY4	R/W	0h	Generic delay4 for PFSM use. The step size is defined by PFSM_DELAY_STEP bits. (Default from NVM memory)

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8.7.1.185 WD_ANSWER_REG Register (Offset = 401h) [Reset = 00h]

WD_ANSWER_REG is shown in Figure 8-244 and described in Table 8-209.

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Figure 8-244. WD_ANSWER_REG Register

7	6	5	4	3	2	1	0
WD_ANSWER							
R/W-0h							

Table 8-209. WD_ANSWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_ANSWER	R/W	0h	MCU answer byte. The MCU must write the expected reference Answer-x into this register. Each watchdog question requires four answer bytes: - Three answer bytes (Answer-3, Answer-2, Answer-1) must be written in Window-1. - The fourth (final) answer-byte (Answer-0) must be written in Window-2. The number of written answer bytes is tracked with the WD_ANSW_CNT counter in the WD_QUESTION_ANSW_CNT register. These bits only apply for Watchdog in Q&A mode.

8.7.1.186 WD_QUESTION_ANSW_CNT Register (Offset = 402h) [Reset = 30h]

WD_QUESTION_ANSW_CNT is shown in Figure 8-245 and described in Table 8-210.

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Figure 8-245. WD_QUESTION_ANSW_CNT Register

7	6	5	4	3	2	1	0
RESERVED		WD_ANSW_CNT		WD_QUESTION			
R-0h		R-3h		R-0h			

Table 8-210. WD_QUESTION_ANSW_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-4	WD_ANSW_CNT	R	3h	Current, received watchdog-answer count state. These bits only apply for Watchdog in Q&A mode.
3-0	WD_QUESTION	R	0h	Watchdog question. The MCU must read (or calculate) the current watchdog question value to generate correct answers. These bits only apply for Watchdog in Q&A mode.

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8.7.1.187 WD_WIN1_CFG Register (Offset = 403h) [Reset = 7Fh]

WD_WIN1_CFG is shown in Figure 8-246 and described in Table 8-211.

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Figure 8-246. WD_WIN1_CFG Register

7	6	5	4	3	2	1	0
RESERVED	WD_WIN1						
R/W-0h	R/W-7Fh						

Table 8-211. WD_WIN1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-0	WD_WIN1	R/W	7Fh	These bits are for programming the duration of Watchdog Window-1 (see Watchdoc chapter). These bits can be only be written when the watchdog is in the Long Window.

8.7.1.188 WD_WIN2_CFG Register (Offset = 404h) [Reset = 7Fh]

WD_WIN2_CFG is shown in Figure 8-247 and described in Table 8-212.

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Figure 8-247. WD_WIN2_CFG Register

7	6	5	4	3	2	1	0
RESERVED	WD_WIN2						
R/W-0h	R/W-7Fh						

Table 8-212. WD_WIN2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-0	WD_WIN2	R/W	7Fh	These bits are for programming the duration of Watchdog Window-2 (see Watchdog chapter). These bits can be only be written when the watchdog is in the Long Window.

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8.7.1.189 WD_LONGWIN_CFG Register (Offset = 405h) [Reset = FFh]

WD_LONGWIN_CFG is shown in Figure 8-248 and described in Table 8-213.

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Figure 8-248. WD_LONGWIN_CFG Register

7	6	5	4	3	2	1	0
WD_LONGWIN							
R/W-FFh							

Table 8-213. WD_LONGWIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_LONGWIN	R/W	FFh	These bits are for programming the duration of Watchdog Long Window (see Watchdog chapter). These bits can be only be written when the watchdog is in the Long Window. (Default from NVM memory)

8.7.1.190 WD_MODE_REG Register (Offset = 406h) [Reset = 02h]

WD_MODE_REG is shown in Figure 8-249 and described in Table 8-214.

Return to the Table 8-23.

Figure 8-249. WD_MODE_REG Register

7	6	5	4	3	2	1	0
RESERVED					WD_PWRHOLD	WD_MODE_SELECT	WD_RETURN_LONGWIN
R/W-0h					R/W-0h	R/W-1h	R/W-0h

Table 8-214. WD_MODE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	WD_PWRHOLD	R/W	0h	Device sets WD_PWRHOLD if hardware condition on pin DISABLE_WDOG (mapped to GPIO8 pin) is applied at start-up (see Watchdog chapter). MCU can write this bit to 1. MCU needs to clear this bit to get out of the Long Window: 0h = watchdog goes out of the Long Window and starts the first watchdog-sequence when the configured Long Window time-interval elapses 1h = watchdog stays in Long Window
1	WD_MODE_SELECT	R/W	1h	Watchdog mode-select: MCU can set this to required value only when watchdog is in the Long Window. 0h = Trigger Mode 1h = Q&A mode.
0	WD_RETURN_LONGWIN	R/W	0h	MCU can set this bit to put the watchdog from operating back to the Long Window (see Watchdog chapter): 0h = Watchdog continues operating 1h = Watchdog returns to Long-Window after completion of the current watchdog-sequence.

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8.7.1.191 WD_QA_CFG Register (Offset = 407h) [Reset = 0Ah]

WD_QA_CFG is shown in Figure 8-250 and described in Table 8-215.

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Figure 8-250. WD_QA_CFG Register

7	6	5	4	3	2	1	0
WD_QA_FDBK		WD_QA_LFSR		WD_QUESTION_SEED			
R/W-0h		R/W-0h		R/W-Ah			

Table 8-215. WD_QA_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_QA_FDBK	R/W	0h	Feedback configuration bits for the watchdog question. These bits control the sequence of the generated questions and respective reference answers (see Watchdog chapter). These bits are only used for the watchdog in Q&A mode. These bits can be only be written when the watchdog is in the Long Window.
5-4	WD_QA_LFSR	R/W	0h	LFSR-equation configuration bits for the watchdog question (see Watchdog chapter). These bits are only used for the watchdog in Q&A mode. These bits can be only be written when the watchdog is in the Long Window.
3-0	WD_QUESTION_SEED	R/W	Ah	The watchdog question-seed value (see Watchdog chapter). The MCU updates the question-seed value to generate a set of new questions. These bits can be only be written when the watchdog is in the Long Window.

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8.7.1.192 WD_ERR_STATUS Register (Offset = 408h) [Reset = 00h]

WD_ERR_STATUS is shown in Figure 8-251 and described in Table 8-216.

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Figure 8-251. WD_ERR_STATUS Register

7	6	5	4	3	2	1	0
WD_RST_INT	WD_FAIL_INT	WD_ANSW_ERR	WD_SEQ_ERR	WD_ANSW_EARLY	WD_TRIG_EARLY	WD_TIMEOUT	WD_LONGWIN_TIMEOUT_INT
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-216. WD_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_RST_INT	R/W1C	0h	Latched status bit to indicate that the device went through warm reset due to WD_FAIL_CNT[3:0] > (WD_FAIL_TH[2:0] + WD_RST_TH[2:0]). Write 1 to clear.
6	WD_FAIL_INT	R/W1C	0h	Latched status bit to indicate that the watchdog has cleared the ENABLE_DRV bit due to WD_FAIL_CNT[3:0] > WD_FAIL_TH[2:0]. Write 1 to clear.
5	WD_ANSW_ERR	R/W1C	0h	Latched status bit to indicate that the watchdog has detected an incorrect answer-byte. Write 1 to clear. This bit only applies for Watchdog in Q&A mode.
4	WD_SEQ_ERR	R/W1C	0h	Latched status bit to indicate that the watchdog has detected an incorrect sequence of the answer-bytes. Write 1 to clear. This bit only applies for Watchdog in Q&A mode.
3	WD_ANSW_EARLY	R/W1C	0h	Latched status bit to indicate that the watchdog has received the final answer-byte in Window-1. Write 1 to clear. This bit only applies for Watchdog in Q&A mode.
2	WD_TRIG_EARLY	R/W1C	0h	Latched status bit to indicate that the watchdog has received the watchdog-trigger in Window-1. Write 1 to clear. This bit only applies for Watchdog in Trigger mode.
1	WD_TIMEOUT	R/W1C	0h	Latched status bit to indicate that the watchdog has detected a time-out event in the started watchdog sequence. Write 1 to clear.
0	WD_LONGWIN_TIMEOUT_INT	R/W1C	0h	Latched status bit to indicate that device went through warm reset due to elapse of Long Window time-interval. Write 1 to clear interrupt.

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8.7.1.193 WD_THR_CFG Register (Offset = 409h) [Reset = FFh]

WD_THR_CFG is shown in Figure 8-252 and described in Table 8-217.

Return to the Table 8-23.

Figure 8-252. WD_THR_CFG Register

7	6	5	4	3	2	1	0
WD_RST_EN	WD_EN	WD_FAIL_TH			WD_RST_TH		
R/W-1h	R/W-1h	R/W-7h			R/W-7h		

Table 8-217. WD_THR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_RST_EN	R/W	1h	Watchdog reset configuration bit: This bit can be only be written when the watchdog is in the Long Window. 0h = No warm reset when WD_FAIL_CNT[3:0] > (WD_FAIL_TH[2:0] + WD_RST_TH[2:0]) 1h = Warm reset when WD_FAIL_CNT[3:0] > (WD_FAIL_TH[2:0] + WD_RST_TH[2:0]).
6	WD_EN	R/W	1h	Watchdog enable configuration bit: This bit can be only be written when the watchdog is in the Long Window. (Default from NVM memory) 0h = watchdog disabled. MCU can set ENABLE_DRV bit to 1 if all other interrupt status bits are cleared 1h = watchdog enabled. MCU can set ENABLE_DRV bit to 1 if: - watchdog is out of the Long Window - WD_FAIL_CNT[3:0] =< WD_FAIL_TH[2:0] - WD_FIRST_OK=1 - all other interrupt status bits are cleared.
5-3	WD_FAIL_TH	R/W	7h	Configuration bits for the 1st threshold of the watchdog fail counter: Device clears ENABLE_DRV bit when WD_FAIL_CNT[3:0] > WD_FAIL_TH[2:0]. These bits can be only be written when the watchdog is in the Long Window.
2-0	WD_RST_TH	R/W	7h	Configuration bits for the 2nd threshold of the watchdog fail counter: Device goes through warm reset when WD_FAIL_CNT[3:0] > (WD_FAIL_TH[2:0] + WD_RST_TH[2:0]). These bits can be only be written when the watchdog is in the Long Window.

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8.7.1.194 WD_FAIL_CNT_REG Register (Offset = 40Ah) [Reset = 20h]

WD_FAIL_CNT_REG is shown in Figure 8-253 and described in Table 8-218.

Return to the Table 8-23.

Figure 8-253. WD_FAIL_CNT_REG Register

7	6	5	4	3	2	1	0
RESERVED	WD_BAD_EVENT	WD_FIRST_OK	RESERVED	WD_FAIL_CNT			
R-0h	R-0h	R-1h	R-0h	R-0h			

Table 8-218. WD_FAIL_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	WD_BAD_EVENT	R	0h	Status bit to indicate that the watchdog has detected a bad event in the current watchdog sequence. The device clears this bit at the end of the watchdog sequence.
5	WD_FIRST_OK	R	1h	Status bit to indicate that the watchdog has detected a good event. The device clears this bit when the watchdog goes to the Long Window.
4	RESERVED	R	0h	
3-0	WD_FAIL_CNT	R	0h	Status bits to indicate the value of the Watchdog Fail Counter. The device clears these bits when the watchdog goes to the Long Window.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following sections provides more detail on the proper utilization of the PMIC. Each orderable part number has unique default non-volatile memory settings and the relevant user's guide for that orderable are available in the TPS6594-Q1 product folder . Reference these user's guides for specific application information. More generic topics and some examples are outlined here.

To help with new designs, a variety of tools and documents are available in the product folder. Some examples are:

- Evaluation module and user guide which allow testing of various orderable part numbers, including multi-PMIC operation
- GUI to communicate with the PMIC
- Schematic and layout checklist

9.2 Typical Application

The PMIC is generally used to power a processor. The number of regulators needed, the required sequencing, the load current requirements, and the voltage characteristics are all critical in determining the number of PMICs used in the system as well as the external components used with it. The following section provides a generic case. For specific cases, refer to the relevant user's guide based on the orderable part number.

9.2.1 Powering a Processor

In this example, a single PMIC is used to power a generic processor. For this case, the PMIC is used in 2+1+1+1 buck phase configuration where BUCK1 and BUCK2 are used in parallel to supply higher currents.

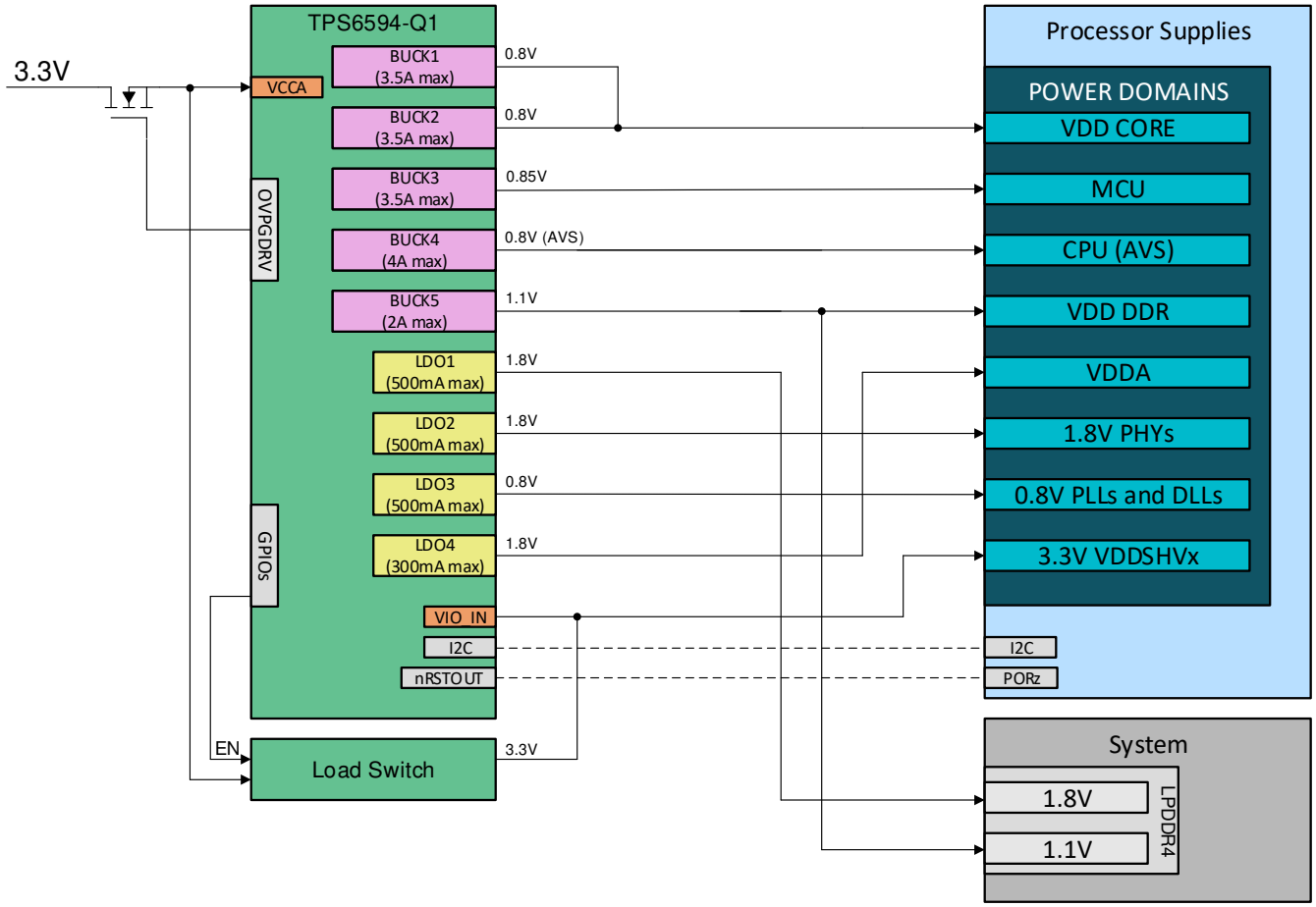

Figure 9-1. Example Power Map

9.2.1.1 Design Requirements

The design requirements for the sample processor in Figure 9-1 are outlined below:

- VDD CORE rail requires 0.8 V, 5 A
- MCU rail requires 0.85 V, 2 A
- CPU (AVS) rail requires 0.8 V, 3 A and the ability to support Adaptive Voltage Scaling
- LPDDR4 is used, which requires 1.1 V, 1 A and 1.8 V, 200 mA
- 1.8V PHYs and 0.8V PLLs and DLLs which are noise sensitive
- VDDA supplies the most noise sensitive components of the processor, requires 100 mA, and requires extra low noise
- Protection from 3.3 V overvoltage (functional safety variant only)

9.2.1.2 Detailed Design Procedure

Based on the above requirements, the PMIC has been configured with the connections outlined in Figure 9-1. BUCK1 and BUCK2 are used in multiphase operation to support the 5 A current. LDO2 and LDO3 are used to power 1.8 V PHYs and 0.8 V PLLs and DLLs because they are lower noise than a buck regulator and it isolates them from the noise of VDD CORE and the LPDDR4 1.8 V supply. LDO4 is used to power VDDA because it has better noise performance.

Using this configuration information, components can be chosen to use with the PMIC.

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9.2.1.2.1 VCCA, VSYS_SENSE, and OVPGDRV

The VCCA pin provides power to the LDOVINT regulator and other internal functions. It is always connected in parallel with the buck input pins (PVIN_Bx pins). The VSYS_SENSE pin and OVPGDRV pin protect the device from being damaged by an overvoltage event from the pre-regulator by disconnecting the low voltage VCCA-powered pins from VSYS. The VCCA pin can be connected to an optional 0.47-µF bypass capacitor close to the pin. For cases where the pre-regulator is not located near the device, place some additional bulk capacitance before the protection FET to stabilize the VSYS supply near the device.

For the input protection, the total amount of capacitance on the VSYS and VCCA node must be large enough to ensure that the voltage at the VCCA pin does not rise above 8 V before the PMIC disables the protection FET in case of pre-regulator high side FET short failure. For a system with 5 V input supply, the specified rise-time in the 6 V to 8 V range is equal or greater than 7-µs. For a system with 3.3 V input supply, the specified rise-time in the 4 V to 8 V range is equal or greater than 7-µs. The capacitance varies based on the pre-regulator inductor and the pre-regulator input filter and it is recommended to simulate this circuit to get an initial estimate on the required capacitance.

Choose a zener diode with a breakdown voltage less than the recommended maximum of the VSYS_SENSE pin (12 V maximum) and greater than the overvoltage detection voltage (VSYS_OVP_Rising of 6.2 V) at all times for proper protection. Choose the protection resistors values to assure that the voltage across the Zener diode remains within those two boundaries and that the current is not greater than the Zener diode maximum current for the full desired input voltage protection range. For increased reliability, two resistors with 90° physical orientation offset are recommended to reduce risk of a single point short resulting in IC damage.

Finally, choose the protection NMOS FET with sufficient current and voltage ratings for the application with minimal gate charge values. The turn-on and turn-off time of the protection FET is generally very fast relative to the detection time, so gate charge is not as critical as R_{DSON} in general. The components chosen for the evaluation module to cover a broad set of applications are shown in Table 9-1. To determine the required minimum FET $R_{DS(ON)}$, the maximum input current is first measured or calculated based on output current requirements multiplied by the duty cycle (V_{OUT} / V_{IN}) and then divided by the buck efficiency. Next, determine the $VCCA_{UV_TH}$ from the VCCA_PG_WINDOW. VCCA_UV_THR register setting. The $R_{DS(ON)}$ maximum must be less than the $VCCA_{UV_TH}$ minimum divided by the input current maximum to ensure that VCCA does not drop below $VCCA_{UV_TH}$ at maximum loading. From there, the second factor to consider is to minimize the Q_{GS} for faster FET turn off time.

For cases where input voltage protection is not required, ground VSYS_SENSE, float OVPGDRV, and the protection diode and FET are not needed.

Table 9-1. Recommended VCCA, VSYS_SENSE, and OVPGDRV Components

COMPONENT	MANUFACTURER	PART NUMBER	VALUE	EIA SIZE CODE	SIZE (mm)	USED for VALIDATION
Capacitor	Murata	GCM155C71A474KE36	0.47 µF, 10 V, X7R	0402	1.0 × 0.5	Yes
Capacitor	TDK	CGA2B3X7S1A474K050BB	0.47 µF, 10 V, X7R	0402	1.0 × 0.5	—
Zener Diode	ON Semiconductor	MM3Z10VST1G	10 V, 300 mW	SOD-323	2.5 × 1.25 × 0.9	Yes
Zener Diode	Vishay-Dale	BZX84B10-G3-08	10 V, 300 mW	SOT-23-3	3.1 × 2.6 × 1.15	—
Resistor(1)	Vishay-Dale	CRCW0402240RJNED	240 Ω	0402	1.0 × 0.5	Yes
NMOS FET	On Semiconductor	NVMFS4C05N	30 V, 4.0 mΩ, 127 A	—	5.15 × 6.15 × 1.0	Yes
NMOS FET	Diodes Incorporated	DMNH3010LK3	30 V, 11.5 mΩ, 50 A	—	6.70 × 10.41 × 2.39	—

(1) Two resistors are used in series to create an effective 480 Ω total resistance.

9.2.1.2.2 Internal LDOs

The internal LDOs, VOUT_LDOVINT and VOUT_LDOVRTC, require external 2.2 µF capacitors for stabilization. The recommended components are shown below.

Table 9-2. Recommended Internal LDO Components

COMPONENT	MANUFACTURER	PART NUMBER	VALUE	EIA SIZE CODE	SIZE (mm)	USED for VALIDATION
Capacitor	Murata	GCM188R70J225KE22	2.2 µF, 6.3 V, X7R	0603	1.6 × 0.8	—
Capacitor	TDK	CGA3E1X7S1C225M080AC	2.2 µF, 6.3 V, X7R	0603	1.6 × 0.8	—

9.2.1.2.3 Crystal Oscillator

A crystal oscillator can be used for application requiring a high accuracy real-time clock module. The OSC32KCAP pin is bypassed with a 100-nF bypass capacitor for noise rejection. For the OSC32KIN and OSC32KOUT pins, a simplified oscillator schematic is shown in Figure 9-2 to determine what external load capacitors are needed for the crystal.

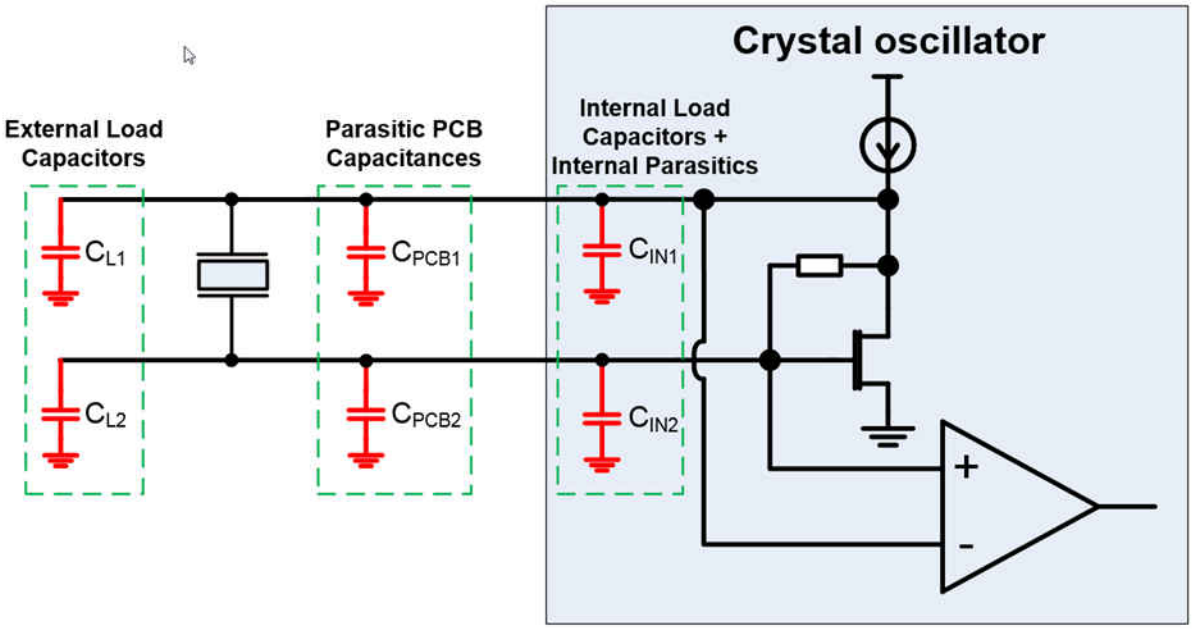

Figure 9-2. Crystal Oscillator Component Selection

C_{IN1} and C_{IN2} are both 12-pF for this device. C_{PCB1} and C_{PCB2} depend on the board but is generally around 1-pF. The crystal oscillator chosen must have a required load capacitance of either 6-pF, 9-pF, or 12.5-pF and the value of the XTAL_SEL bit in the RTC_CTRL_2 register must be updated based on the oscillator chosen. To achieve the required load capacitance (C_L) for the oscillator, Equation 26 is used. It assumes that the crystal series capacitance is negligible.

$$C_L = (C_{L1} + C_{PCB1} + C_{IN1}) \times (C_{L2} + C_{PCB2} + C_{IN2}) / ((C_{L1} + C_{PCB1} + C_{IN1}) + (C_{L2} + C_{PCB2} + C_{IN2})) \quad (26)$$

Assuming $C_{L1} = C_{L2}$, this simplifies to $C_{L1} = 2 \times C_L - C_{PCB} - C_{IN}$. Simplifying this into the standard capacitor values typically available results in the following general capacitor recommendations. If more precise matching is desired, complete the exercise without series capacitance neglected and with exact PCB parasitic capacitance. Too much capacitance results in a lower than expected oscillator frequency, while not enough capacitance has the opposite impact.

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Table 9-3. Approximate Crystal Oscillator Load Capacitors

Crystal C_L (pF)	Component $C_{L1} = C_{L2}$ (pF)
6	0
9	6
12.5	12.5

The recommended components using a 9-pF oscillator as an example are in Table 9-4. If an alternate load capacitance crystal is used, the values of the load capacitors must be adjusted to match based on the above.

Table 9-4. Recommended Crystal Oscillator Components for 9-pF Crystal

Component	MANUFACTURER	PART NUMBER	VALUE	EIA size code	SIZE (mm)	Used for Validation
Capacitor	Murata	GCM155R71C104JA55D	100-nF, 16-V, X7R	0402	1.0 x 0.5	Yes
Capacitor	TDK	CGA2B1X7R1C104K050BC	100-nF, 16-V, X7R	0402	1.0 x 0.5	-
Crystal	NDK	NX3215SD-32.768K-STD-MUS-6	32.768-kHz, ±20 ppm, 9-pF		3.2 x 1.5 x 0.9	Yes
Crystal	Abracon	ABS07AIG-32.768kHz-9-T	32.768-kHz, ±20 ppm, 9-pF		3.2 x 1.5 x 0.9	-
Capacitor	Murata	GCM1555C1H6R0CA16	6-pF, 50-V, C0G/NP0	0402	1.0 x 0.5	Yes
Capacitor	TDK	CGA2B2C0G1H060D050BA	6-pF, 50-V, C0G/NP0	0402	1.0 x 0.5	-

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9.2.1.2.4 Buck Input Capacitors

For optimal performance, every buck needs an input capacitor, and the capacitor value and voltage rating must be at least 10-µF, 10-V and must be placed as close to the buck input pins as possible. If the board size allows a larger foot print, a 22-µF, 10-V capacitor is recommended. See Table 9-5 for the recommended input capacitors, and the Section 11 for more information about component placement.

Table 9-5. Recommended Buck Input Capacitors

MANUFACTURER	PART NUMBER	VALUE	EIA size code	SIZE (mm)	Used for Validation
TDK	CGA4J1X7S1C106K125AC	10 µF, 16 V, X7R	0805	2.0 × 1.25 × 1.25	Yes
Murata	GCM21BR71A106KE22	10 µF, 10 V, X7R	0805	2.0 × 1.25 × 1.25	-

9.2.1.2.5 Buck Output Capacitors

The buck converters have seven potential NVM configurations which can impact the output capacitor selection. Refer the part number specific user's guide to identify which configuration applies to each buck regulator. The actual minimal capacitance requirements to achieve a specific accuracy or ripple target varies depending on the input voltage, output voltage, and load transient characteristics; some guidance, however, is provided below. The local output capacitors must be placed as close to the inductor as possible to minimize electromagnetic emissions. Every buck output requires a local output capacitor to form the capacitive part of the LC output filter. It is recommended to place all large capacitors near the inductor. See Section 11 for more information about component placement. Use ceramic local output capacitors, X7R or X7T types; do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to perform these functions. Minimum effective output capacitance (including the DC voltage roll-off, tolerances, aging and temperature effects) is defined in Electrical Characteristics table for different buck configurations. The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its R_{ESR}. The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the switching frequency of the part.

To achieve better ripple and transient performance, additional high pass filter caps are recommended to compensate for the parasitic impedance due to board routing and provide faster transient response to a load step. These caps are placed close to the point of load and are also the input capacitors of the load. These capacitors are referred to as POL caps later in this document. POL capacitor usage varies based on the application and generally follows the SoC or FPGA input capacitor requirements. Low ESL 3-terminal caps are recommended, as their high performance can help reduce the total number of capacitors required which simplifies board layout design and saves board area. They also help to reduce the total cost of the solution.

Note that the output capacitor may be the limiting factor in the output voltage ramp and the maximum total output capacitance listed in electrical characteristics must not be exceeded. At shutdown the output capacitors are discharged to 0.15-V level using forced-PWM operation. This discharge of the output capacitors can cause an increase of the input voltage if the load current is small and the output capacitor is large. Below 0.15-V level the output capacitor is discharged by the internal discharge resistor and with large capacitor more time is required to settle V_{OUT} down as a consequence of the increased time constant.

Figure 9-3 is an example power distribution network (PDN) of local and POL caps at the output of a buck for optimal ripple and transient performance. Table 9-6 lists the local and POL capacitors used to validate the buck transient and ripple performance specified in the parametric table for each of the seven configurations. Table 9-7 lists the actual capacitor part numbers used for the different use case tests, neglecting capacitors below 10-µF. It is recommended to simulate and validate that the capacitor network chosen for a particular design meets the desired requirements as these are provided as guidelines.

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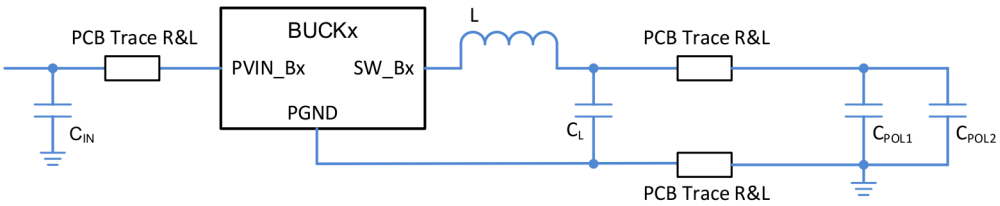

Figure 9-3. Example Power Distribution Network (PDN) of Local and POL Capacitors

Table 9-6. Local and POL Capacitors used for Buck Use Case Validation

Configuration	C_{OUT}	L	C_L / phase	R_{PCB} per phase[1]	L_{PCB} per phase[2]	C_{POL1} (total)	C_{POL2} (total)
4.4 MHz V_{OUT} Less than 1.9 V, Multiphase	Low	220 nH	47 µF × 2	8 mΩ	2.5 nH	10 µF × 4	
	High	220 nH	47 µF × 4	8 mΩ	2.5 nH	10 µF × 2	
4.4 MHz V_{OUT} Less than 1.9 V, Single Phase with high C_{OUT}	Low	220 nH	47 µF × 1	8 mΩ	2.5 nH	10 µF × 4	
	High	220 nH	47 µF × 4	8 mΩ	2.5 nH	10 µF × 2	
4.4 MHz V_{OUT} Less than 1.9 V, Single Phase with low C_{OUT}	Low	220 nH	22 µF × 1	8 mΩ	2.5 nH	10 µF × 2	
	High	220 nH	47 µF × 1	8 mΩ	2.5 nH	10 µF × 4	
4.4 MHz V_{OUT} Greater than 1.7 V, Single Phase Only (V_{IN} Greater than 4.5 V)	Low	470 nH	47 µF × 1	27 mΩ	6 nH	10 µF × 4	
	High	470 nH	47 µF × 2	27 mΩ	6 nH	10 µF × 2	
2.2 MHz Full V_{OUT} Range and V_{IN} Greater than 4.5 V, Single Phase Only	Low	1000 nH	47 µF × 3	8 mΩ	2.5 nH	10 µF × 4	
	High	1000 nH	47 µF × 3	8 mΩ	2.5 nH	10 µF × 4	680 µF × 1
2.2 MHz V_{OUT} Less than 1.9 V Multiphase or Single Phase	Low	470 nH	47 µF × 3	4.1 mΩ	1.3 nH	10 µF × 4	
	High	470 nH	47 µF × 3	4.1 mΩ	1.3 nH	10 µF × 4	680 µF × 1
2.2 MHz Full V_{OUT} and Full V_{IN} Range, Single Phase Only	Low	1000 nH	47 µF × 3	4.1 mΩ	1.3 nH	10 µF × 2	
	High	1000 nH	100 µF × 4	4.1 mΩ	1.3 nH	10 µF × 2	
DDR VTT Termination, 2.2 MHz Single Phase Only	-	470 nH	22 µF × 1	27 mΩ	6 nH	10 µF × 1 + 22 µF x 1	

1. R_{PCB} is the PCB wiring resistance between local and POL capacitors including both positive and negative paths. For multi-phase outputs the total resistance is divided by the number of phases.
2. L_{PCB} is the PCB wiring inductance between local and POL capacitors including both positive and negative paths. For multi-phase outputs the total inductance is divided by the number of phases.

Power input and output wiring parasitic resistance and inductance must be minimized.

Table 9-7. Recommended Buck Converter Output Capacitor Components

MANUFACTURER	PART NUMBER	VALUE	EIA Size Code	SIZE (mm)	Used for Validation
Murata	NFM15HC105D0G(1)	1 µF, 4 V, X7S	0402	1.0 × 0.5	Yes
TDK	YFF18AC0J105M(1)	1 µF, 6.3 V	0603	1.6 × 0.8	-
Murata	NFM18HC106D0G(1)	10 µF, 4 V, X7S	0603	1.6 × 0.8	Yes
TDK	YFF18AC0G475M(1)	4.7 µF, 6.3 V	0603	1.6 × 0.8	-
Murata	GCM31CR71A226KE02	22 µF, 10 V, X7R	1206	3.2 × 1.6	Yes
Murata	GCM21BD7CGA5L1X7R0J226MT0J226M	22 µF, 6.3 V, X7T	0805	2.0 × 1.25 × 1.25	-
TDK	CGA5L1X7R0J226MT	22 µF, 6.3 V, X7R	1206	3.2 × 1.6	-
TDK	CGA4J1X7T0J226MT	22 µF, 6.3 V, X7T	0805	2.0 × 1.25 × 1.25	-
Murata	GCM32ER70J476ME19	47 µF, 6.3 V, X7R	1210	3.2 × 2.5	Yes
Murata	GCM31CD70G476M	47 µF, 4 V, X7T	1206	3.2 × 1.6	-
TDK	CGA6P1X7S1A476MT	47 µF, 10 V, X7S	1210	3.2 × 2.5	-
TDK	CGA5L1X7T0G476MT	47 µF, 4 V, X7T	1206	3.2 × 1.6	-
Murata	GCM32ED70G107MEC4	100 µF, 4 V, X7S	1210	3.2 × 2.5	Yes
TDK	CGA6P1X7T0G107MT	100 µF, 4 V, X7T	1210	3.2 × 2.5	-
Kemet	T510X687K006ATA023(2)	680 µF, 6.3 V	2917	7.4 × 5.0	Yes

(1) Low ESL 3-terminal cap.
(2) Dependent on availability; may switch to 470 µF.

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9.2.1.2.6 Buck Inductors

Inductor must be chosen based on the buck configuration. See Table 9-6 for the appropriate nominal inductance.

Recommended inductors based on these requirements are shown below.

Table 9-8. Recommended Buck Converter Inductors

MANUFACTURER	PART NUMBER	VALUE	SIZE (mm)	Used for Validation
TDK	TFM322512ALMA1R0MTAA	1000 nH, 4 A Max, 150 °C	3.2 × 2.5 × 1.2	Yes
Murata	DFE322520FD-1R0M=P2	1000 nH, 4.1 A Max, 125 °C	3.2 x 2.5 x 2.0	-
TDK	TFM322512ALMAR47MTAA	470 nH, 5.3 A Max, 150 °C	3.2 × 2.5 × 1.2	Yes
TDK	TFM252012ALMAR47MTAA	470 nH, 4.9 A Max, 150 °C	2.5 x 2.0 x 1.2	-
Murata	DFE2HCAHR47MJ0	470 nH, 4.5 A Max, 150 °C	2.5 × 2.0 × 1.2	-
TDK	TFM322512ALMAR22MTAA	220 nH, 7.6 A Max, 150 °C	3.2 x 2.5 x 1.2	Yes
TDK	TFM201610ALMAR24MTAA	220 nH, 5 A Max, 150 °C	2.0 x 1.6 x 1.2	-
Murata	DFE2MCAHR24MJ0	240 nH, 4.2 A Max, 150 °C	2.0 x 1.6 x 1.2	-

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9.2.1.2.7 LDO Input Capacitors

All LDO inputs require an input decoupling capacitor to minimize input ripple voltage. Using a 2.2-µF capacitor for each LDO is recommended. Depending on the input voltage of the LDO, a 6.3-V, 10-V, or 16-V capacitor can be used. For optimal performance, the input capacitors must be placed as close to the LDO input pins as possible. See the Section 11 for more information about component placement. See Table 9-9 for the recommended input capacitors.

Table 9-9. Recommended LDO Input Capacitors(1)

MANUFACTURER	PART NUMBER	VALUE	EIA size code	SIZE (mm)	Used for Validation
TDK	CGA3E1X7S1C225M080AC	2.2-µF, 16-V, X7S	0603	1.6 x 0.8	Yes
Murata	GCM188R70J225KE22	2.2-µF, 16-V, X7R	0603	1.6 x 0.8	-

(1) Component minimum and maximum tolerance values are specified in the electrical parameters section of each IP.

9.2.1.2.8 LDO Output Capacitors

All LDO outputs require an output capacitor to hold up the output voltage during a load step or changes to the input voltage. Using a 2.2-µF capacitor for each LDO output is recommended. Note: this requirement excludes any capacitance seen at the load and only refers to the capacitance seen close to the device. Additional capacitance placed near the load can be supported, but the end application or system must be evaluated for stability. See Table 9-10 for the specific part number of the recommended output capacitors. For BOM optimization purposes, the same capacitor part number was used for LDO input and LDO output.

Table 9-10. Recommended LDO Output Capacitors

MANUFACTURER	PART NUMBER	VALUE	EIA size code	SIZE (mm)	Used for Validation
TDK	CGA3E1X7S1C225M080AC	2.2-µF, 16-V, X7S	0603	1.6 × 0.8	Yes
Murata	GCM188R70J225KE22	2.2-µF, 16-V, X7R	0603	1.6 × 0.8	—

9.2.1.2.9 Digital Signal Connections

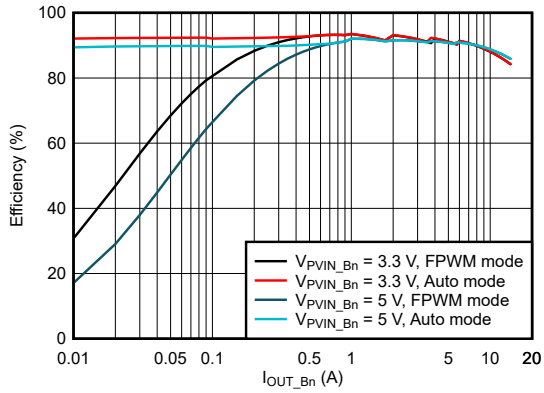
The VIO_IN pin requires a 0.47 µF bypass capacitor close to the pin. See Table 9-11 for the recommended bypass capacitors.

Table 9-11. Recommended VIO_IN Capacitor

Component	MANUFACTURER	PART NUMBER	VALUE	EIA size code	SIZE (mm)	Used for Validation
Capacitor	Murata	GCM155C71A474KE36	0.47 µF, 10 V, X7S	0402	1.0 x 0.5	Yes
Capacitor	TDK	CGA2B3X7S1A474K050BB	0.47 µF, 10 V, X7S	0402	1.0 x 0.5	-

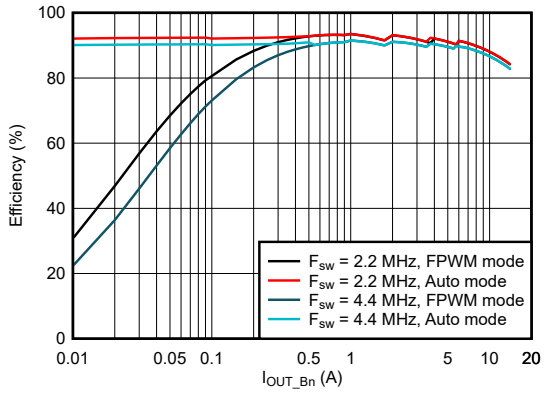
For I^2C pull-up resistor values, please refer to the I^2C standard for the chosen use-case (standard mode, Fast mode, Fast mode+, High-Speed mode with C_b = 100pF or 400pF)

9.2.2 Application Curves



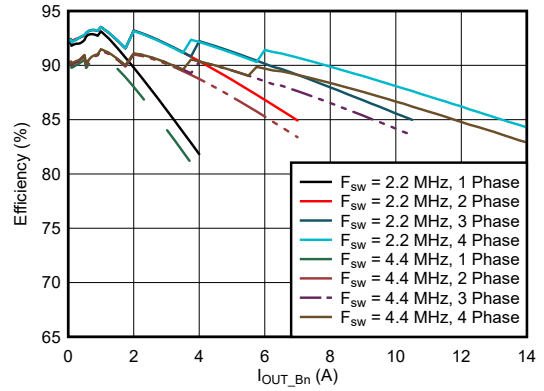
V_{VOUT_Bn} = 1.8 V Fsw = 2.2 MHz 4-Phase

Figure 9-4. BUCK Efficiency at 3.3 V or 5 V Input Voltage



V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1.8 V 4-Phase

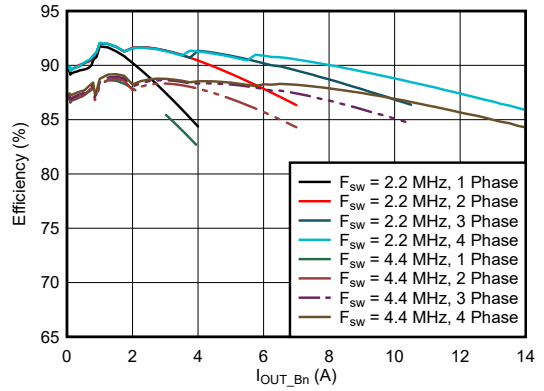
Figure 9-5. BUCK Efficiency with Fsw = 2.2 MHz or 4.4 MHz



Data valid for all bucks up to I_{OUT_Bn}

V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1.8 V Auto Mode

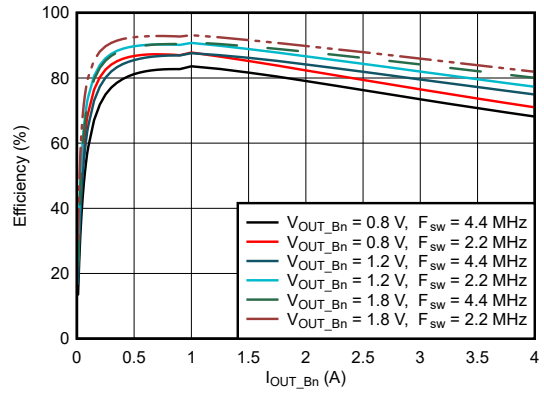
Figure 9-6. BUCK Efficiency in Varied Phase Configuration, 3.3 V Input



Data valid for all bucks up to I_{OUT_Bn}

V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1.8 V Auto Mode

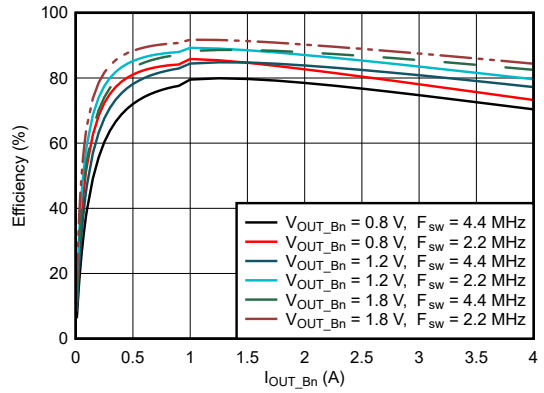
Figure 9-7. BUCK Efficiency in Varied Phase Configuration, 5 V Input



Data valid for all bucks up to I_{OUT_Bn}

V_{PVIN_Bn} = 3.3 V Single-Phase Forced-PWM Mode

Figure 9-8. BUCK Efficiency with different VOUT_Bn, 3.3 V Input



Data valid for all bucks up to I_{OUT_Bn}

V_{PVIN_Bn} = 5 V Single-Phase Forced-PWM Mode

Figure 9-9. BUCK Efficiency with different VOUT_Bn, 5 V Input

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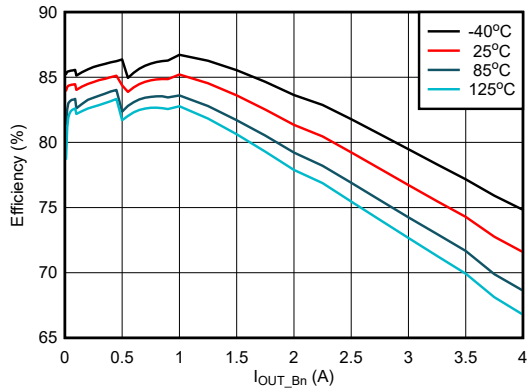
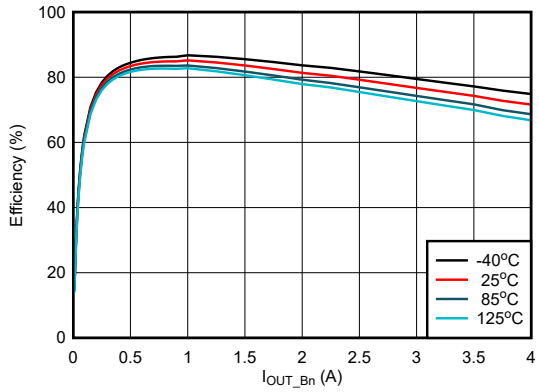
9.2.2 Application Curves (continued)



Data valid for all bucks up to I_{OUT_Bn}

V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V Single-Phase

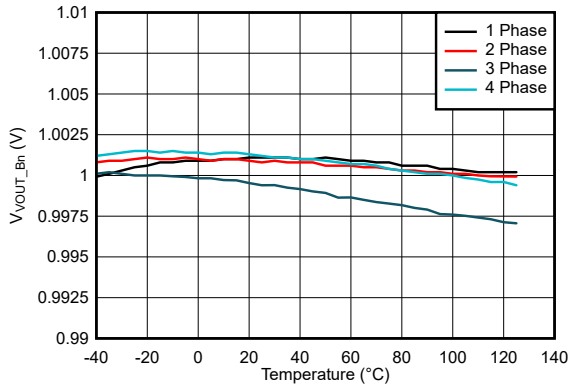
Figure 9-10. BUCK Efficiency at different T_A, Auto Mode



Data valid for all bucks up to I_{OUT_Bn}

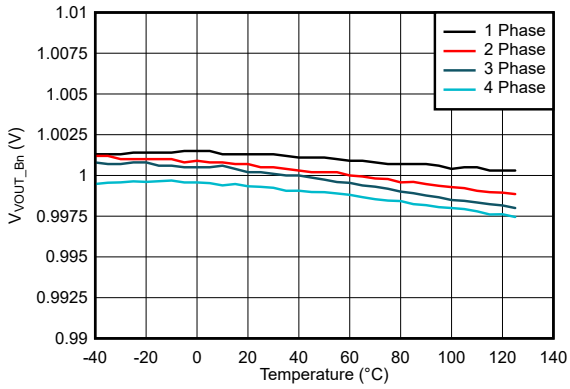
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V Single-Phase

Figure 9-11. BUCK Efficiency at different T_A, Forced-PWM Mode



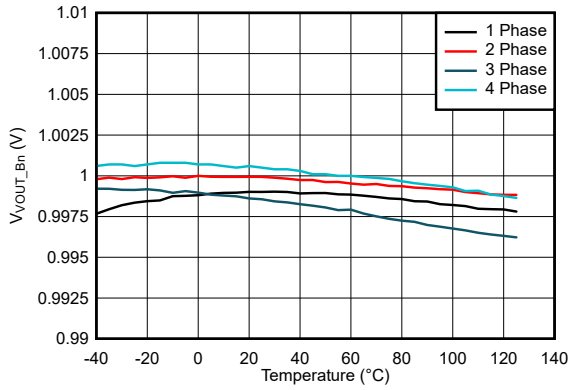
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-12. Buck Temperature Drift, Auto Mode, Fsw = 2.2 MHz



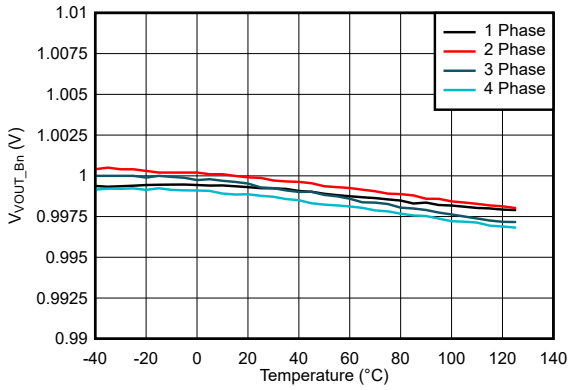
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-13. Buck Temperature Drift, Auto Mode, Fsw = 4.4 MHz



V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

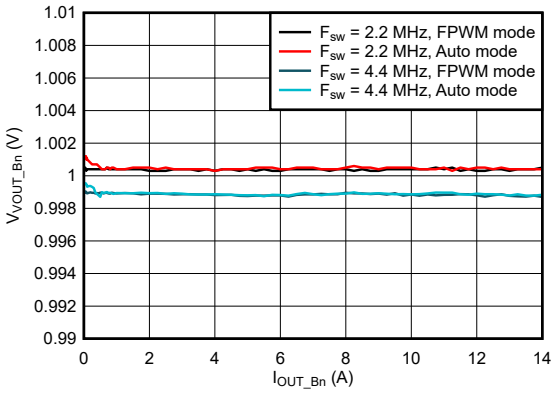
Figure 9-14. Buck Temperature Drift, Forced-PWM Mode, Fsw = 2.2 MHz



V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

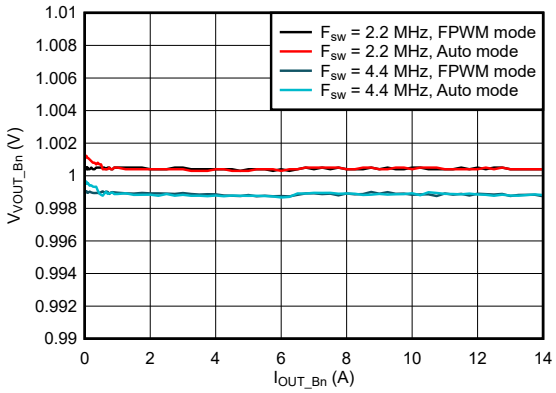
Figure 9-15. Buck Temperature Drift, Forced-PWM Mode, Fsw = 4.4 MHz

9.2.2 Application Curves (continued)



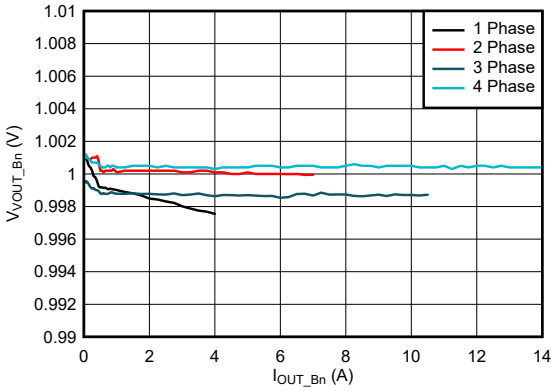
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V 4-Phase

Figure 9-16. Buck Load Regulation with 3.3 V Input



V_{PVIN_Bn} = 5 V V_{VOUT_Bn} = 1 V 4-Phase

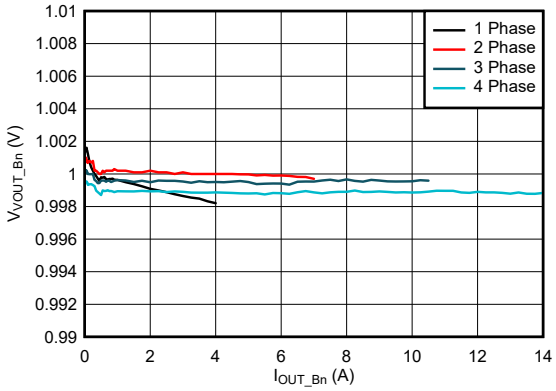
Figure 9-17. Buck Load Regulation with 5 V Input



Data valid for all bucks up to I_{OUT_Bn}

V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V Auto Mode

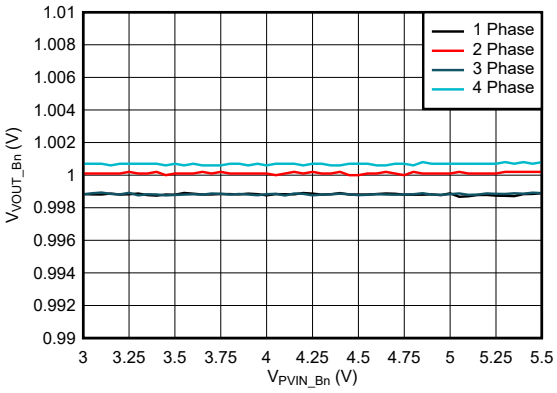
Figure 9-18. Buck Load Regulation, with Fsw = 2.2 MHz



Data valid for all bucks up to I_{OUT_Bn}

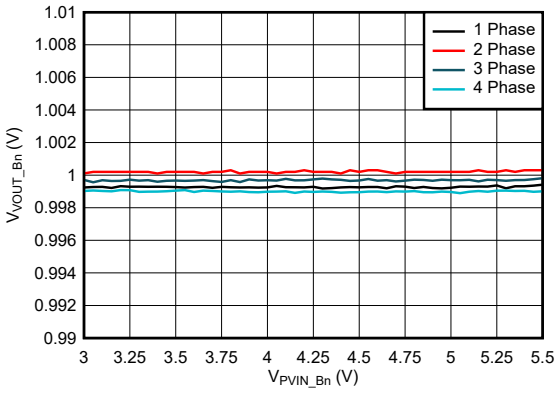
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V Auto Mode

Figure 9-19. Buck Load Regulation, with Fsw = 4.4 MHz



V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V Auto Mode

Figure 9-20. Buck Line Regulation, with Fsw = 2.2 MHz



V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V Auto Mode

Figure 9-21. Buck Line Regulation, with Fsw = 4.4 MHz

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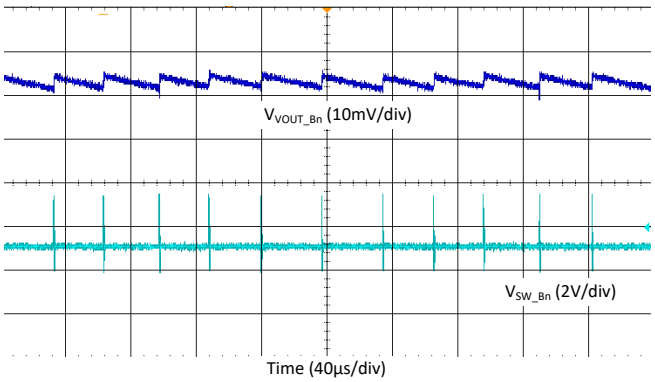
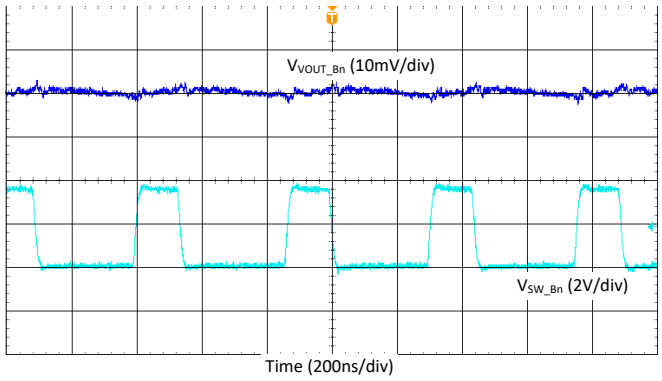
9.2.2 Application Curves (continued)



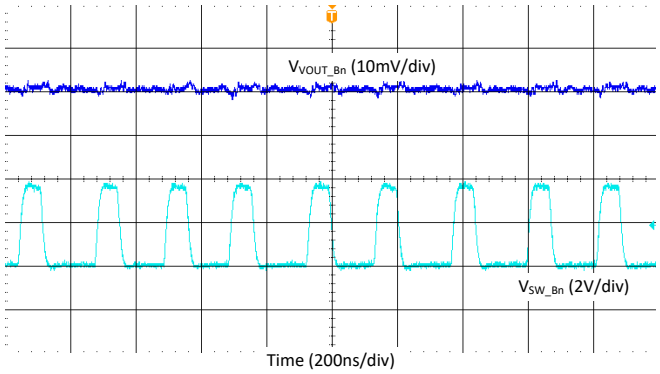
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 10 mA

Figure 9-22. Buck Output Ripple - Single Phase, Auto Mode



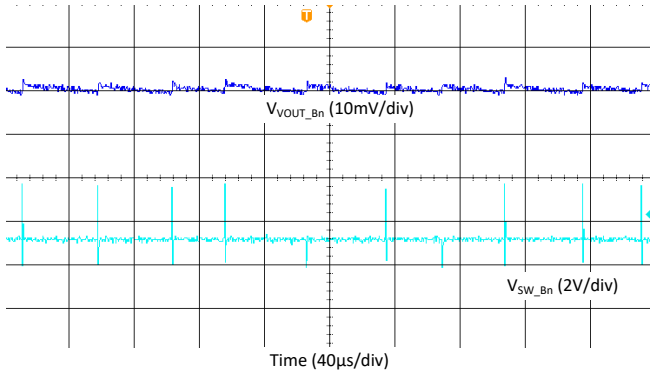
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 200 mA

Figure 9-23. Buck Output Ripple - Single Phase, Fsw = 2.2 MHz, Forced-PWM Mode



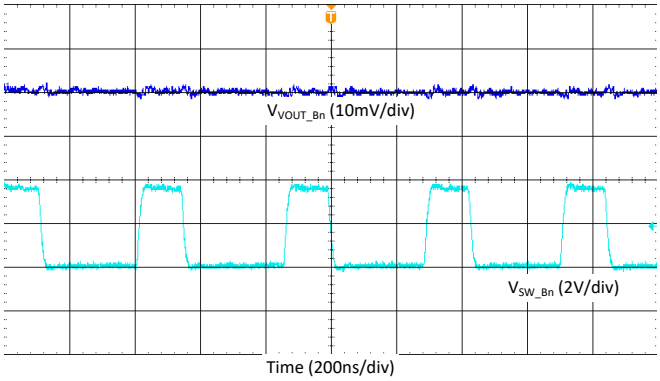
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 200 mA

Figure 9-24. Buck Output Ripple - Single Phase, Fsw = 4.4 MHz, Forced-PWM Mode



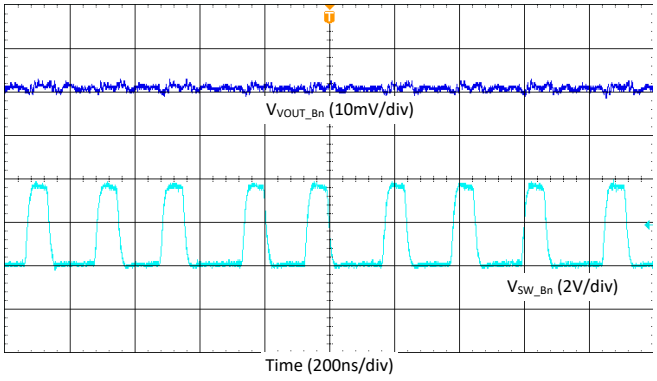
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 10 mA

Figure 9-25. Buck Output Ripple - 2-Phase, Auto Mode



V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 200 mA

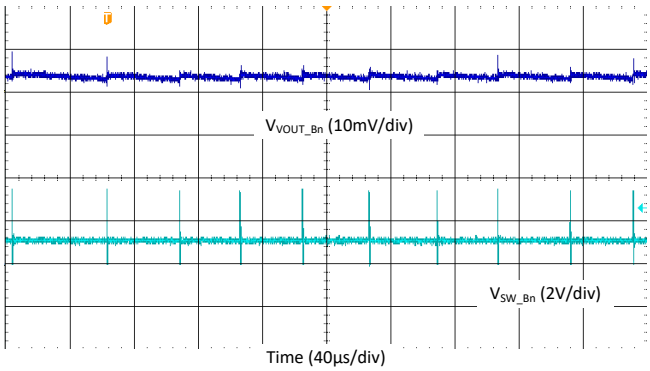
Figure 9-26. Buck Output Ripple - 2-Phase, Fsw = 2.2 MHz, Forced-PWM Mode



V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 200 mA

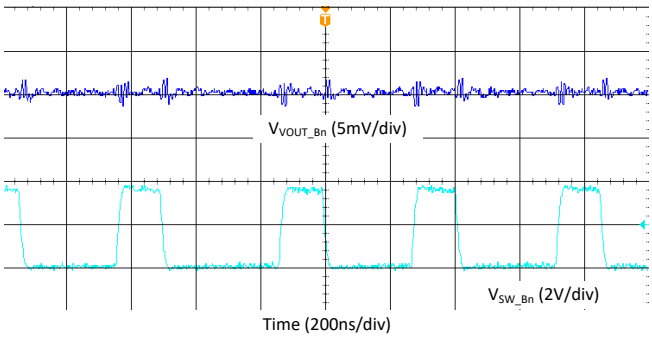
Figure 9-27. Buck Output Ripple - 2-Phase, Fsw = 4.4 MHz, Forced-PWM Mode

9.2.2 Application Curves (continued)



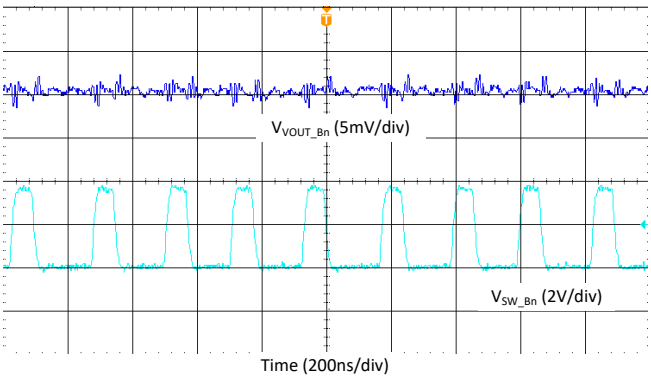
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 10 mA

Figure 9-28. Buck Output Ripple - 3-Phase, Auto Mode



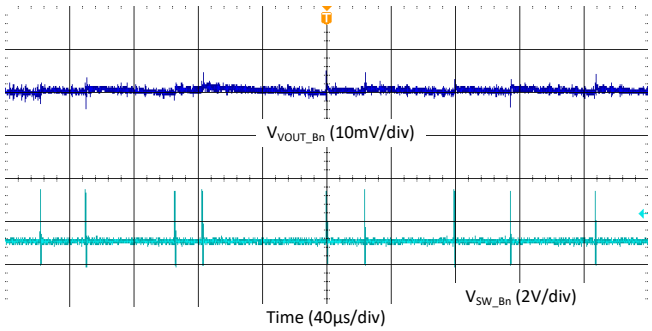
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 200 mA

Figure 9-29. Buck Output Ripple - 3-Phase, Fsw = 2.2 MHz, Forced-PWM Mode



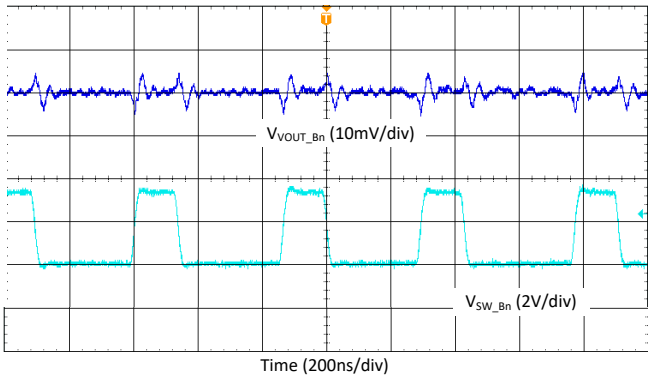
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 200 mA

Figure 9-30. Buck Output Ripple - 3-Phase, Fsw = 4.4 MHz, Forced-PWM Mode



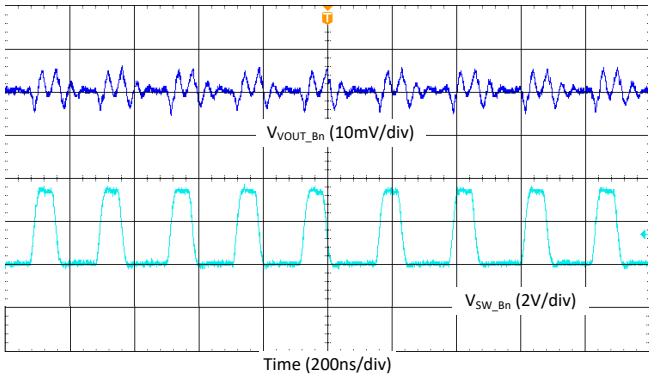
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 10 mA

Figure 9-31. Buck Output Ripple - 4-Phase, Auto Mode



V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 200 mA

Figure 9-32. Buck Output Ripple - 4-Phase, Fsw = 2.2 MHz, Forced-PWM Mode



V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 200 mA

Figure 9-33. Buck Output Ripple - 4-Phase, Fsw = 4.4 MHz, Forced-PWM Mode

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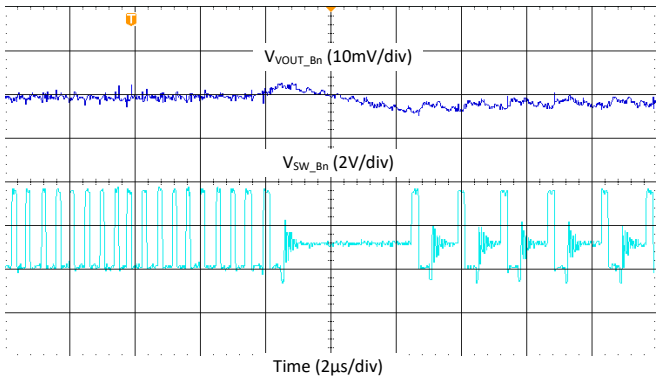
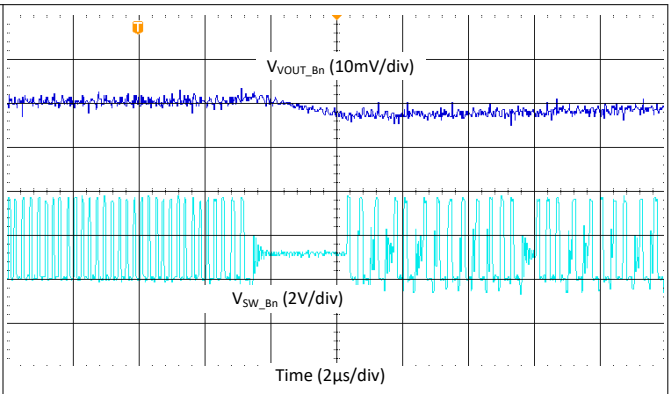
9.2.2 Application Curves (continued)



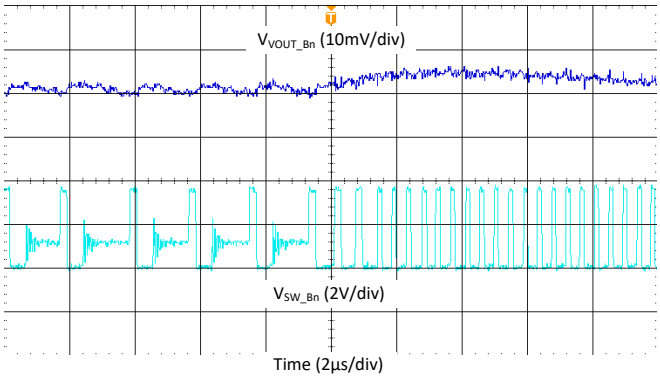
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 200 mA

Figure 9-34. Buck Transient from PWM mode to PFM mode, 2.2 MHz, Single Phase



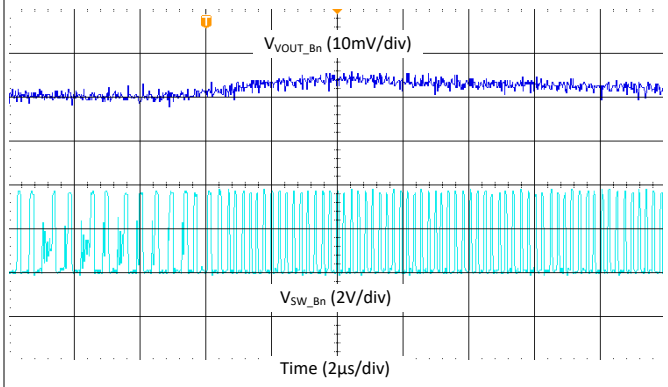
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 200 mA

Figure 9-35. Buck Transient from PWM mode to PFM mode, 4.4 MHz, Single Phase



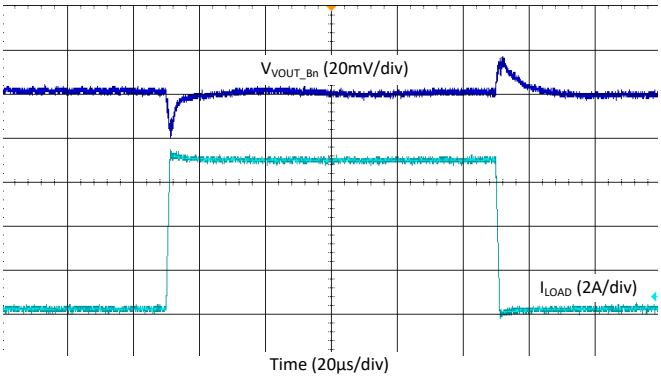
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 200 mA

Figure 9-36. Buck Transient from PFM mode to PWM mode, 2.2 MHz, Single Phase



V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V I_{LOAD} = 200 mA

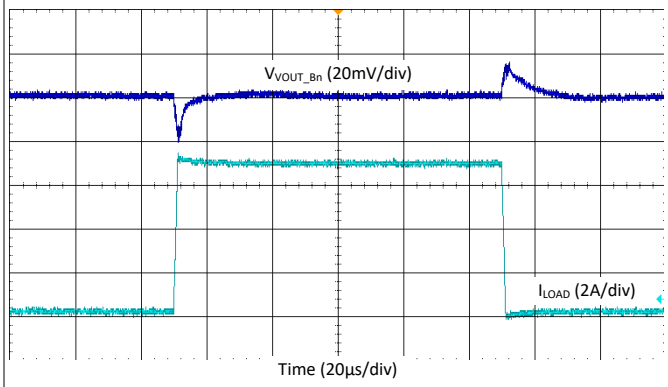
Figure 9-37. Buck Transient from PFM mode to PWM mode, 4.4 MHz, Single Phase



I_{LOAD} = 0.1 A → 7 A → 0.1 A, T_R = T_F = 1 µs

V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-38. Buck Load Step Transient - 4-Phase, 2.2 MHz, Auto Mode

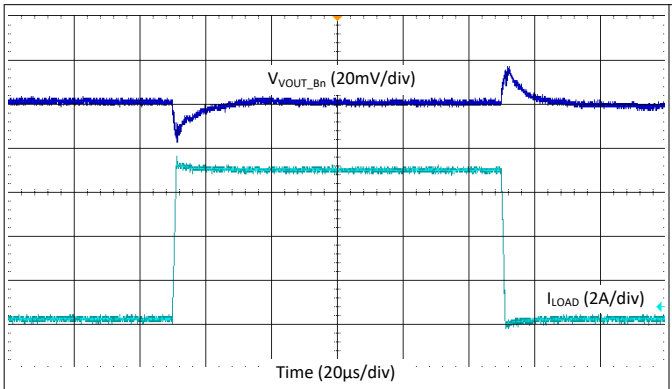


I_{LOAD} = 0.1 A → 7 A → 0.1 A, T_R = T_F = 1 µs

V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

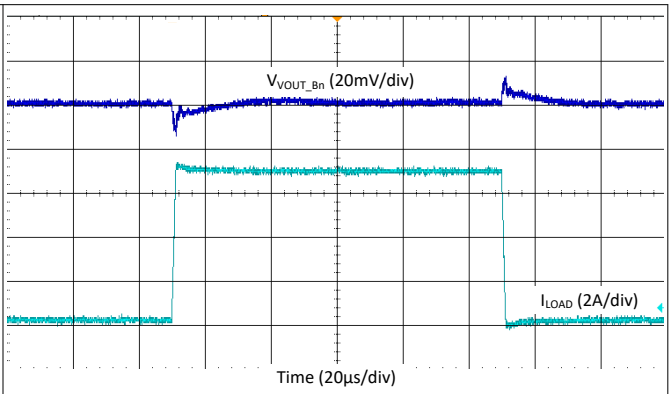
Figure 9-39. Buck Load Step Transient - 4-Phase, 4.4 MHz, Auto Mode

9.2.2 Application Curves (continued)



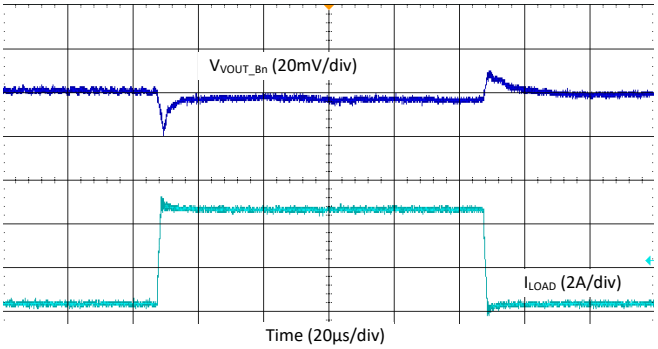
I_{LOAD} = 0.1 A → 7 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-40. Buck Load Step Transient - 4-Phase, 2.2 MHz, Forced-PWM Mode



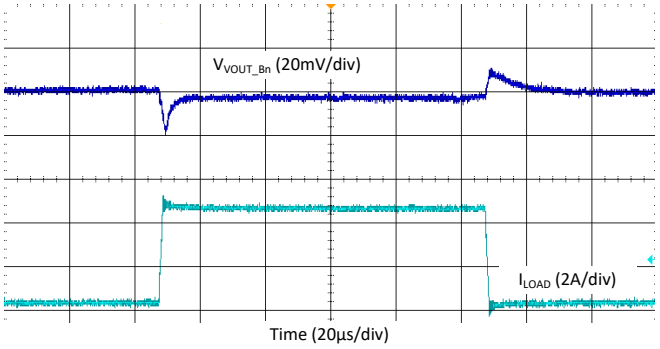
I_{LOAD} = 0.1 A → 7 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-41. Buck Load Step Transient - 4-Phase, 4.4 MHz, Forced-PWM Mode



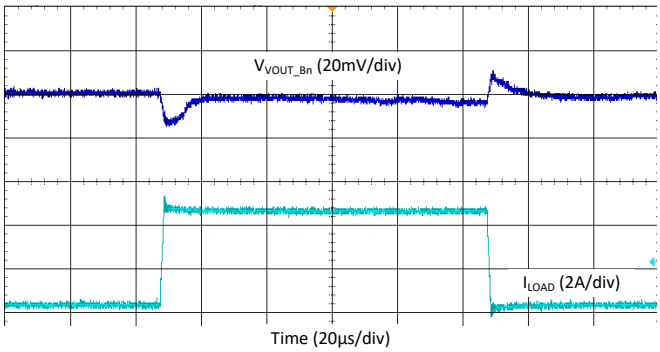
I_{LOAD} = 0.1 A → 5.25 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-42. Buck Load Step Transient - 3-Phase, 2.2 MHz, Auto Mode



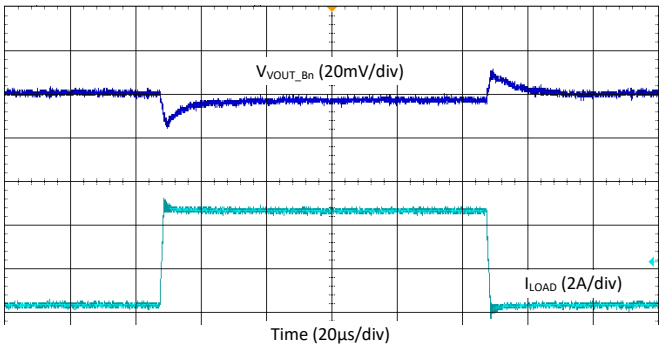
I_{LOAD} = 0.1 A → 5.25 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-43. Buck Load Step Transient - 3-Phase, 4.4 MHz, Auto Mode



I_{LOAD} = 0.1 A → 5.25 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-44. Buck Load Step Transient - 3-Phase, 2.2 MHz, Forced-PWM Mode



I_{LOAD} = 0.1 A → 5.25 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-45. Buck Load Step Transient - 3-Phase, 4.4 MHz, Forced-PWM Mode

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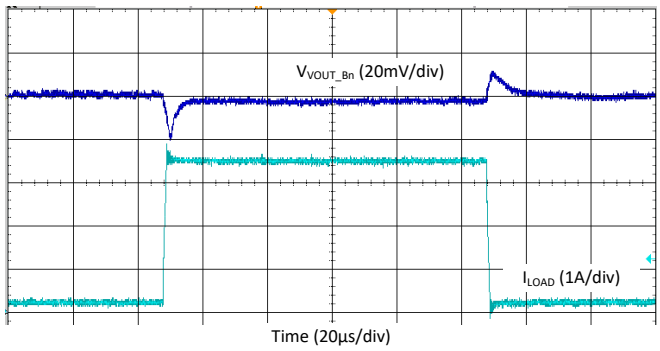
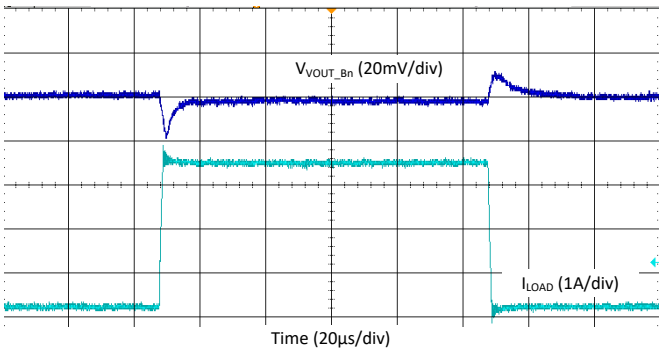
9.2.2 Application Curves (continued)



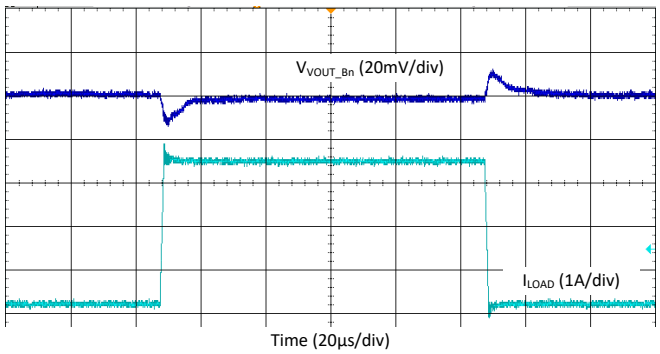
I_{LOAD} = 0.1 A → 3.5 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-46. Buck Load Step Transient - 2-Phase, 2.2 MHz, Auto Mode



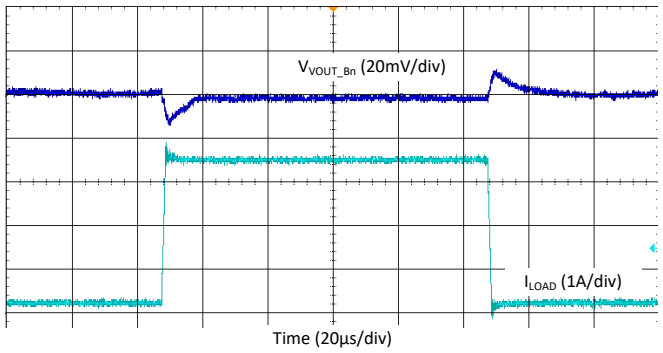
I_{LOAD} = 0.1 A → 3.5 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-47. Buck Load Step Transient - 2-Phase, 4.4 MHz, Auto Mode



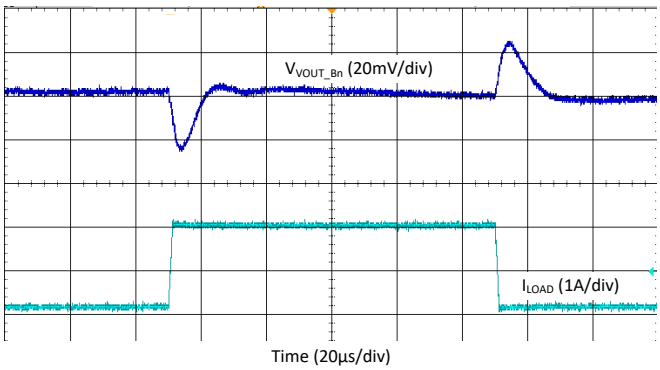
I_{LOAD} = 0.1 A → 3.5 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-48. Buck Load Step Transient - 2-Phase, 2.2 MHz, Forced-PWM Mode



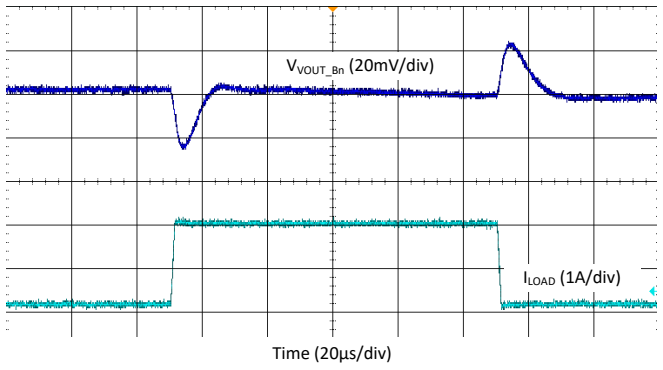
I_{LOAD} = 0.1 A → 3.5 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-49. Buck Load Step Transient - 2-Phase, 4.4 MHz, Forced-PWM Mode



I_{LOAD} = 0.1 A → 2 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

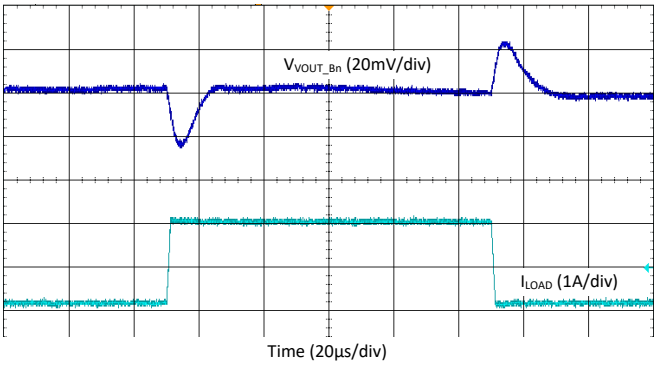
Figure 9-50. Buck Load Step Transient - Buck4, 2.2 MHz, Auto Mode



I_{LOAD} = 0.1 A → 2 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

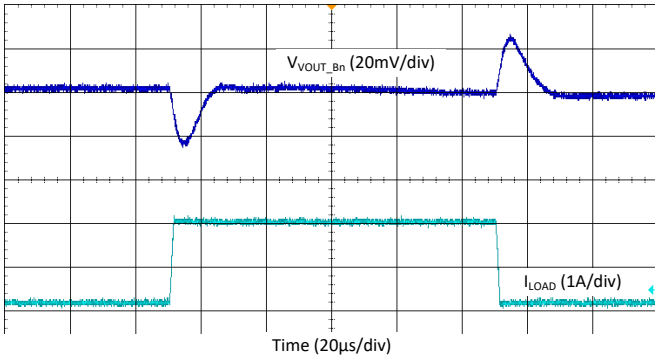
Figure 9-51. Buck Load Step Transient - Buck4, 4.4 MHz, Auto Mode

9.2.2 Application Curves (continued)



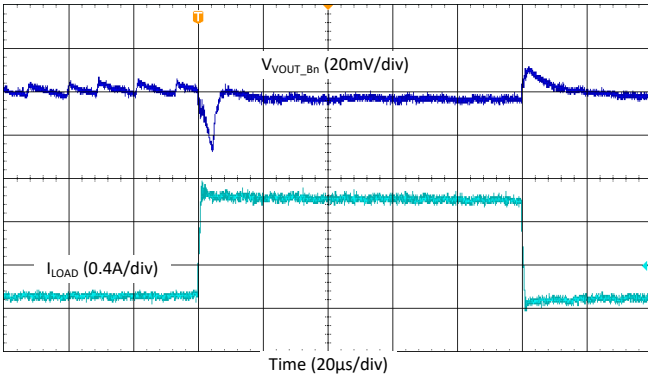
I_{LOAD} = 0.1 A → 2 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-52. Buck Load Step Transient - Buck4, 2.2 MHz, Forced-PWM Mode



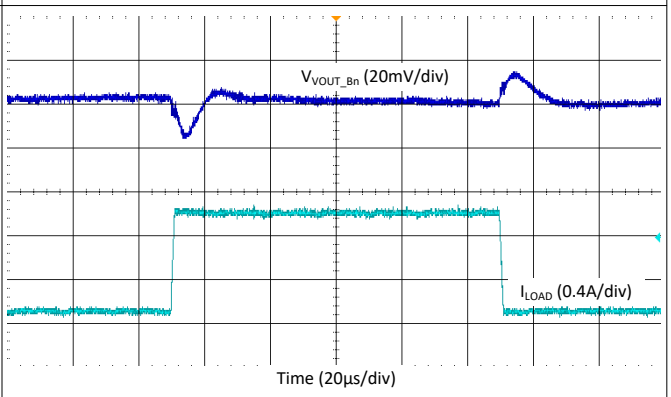
I_{LOAD} = 0.1 A → 2 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-53. Buck Load Step Transient - Buck4, 4.4 MHz, Forced-PWM Mode



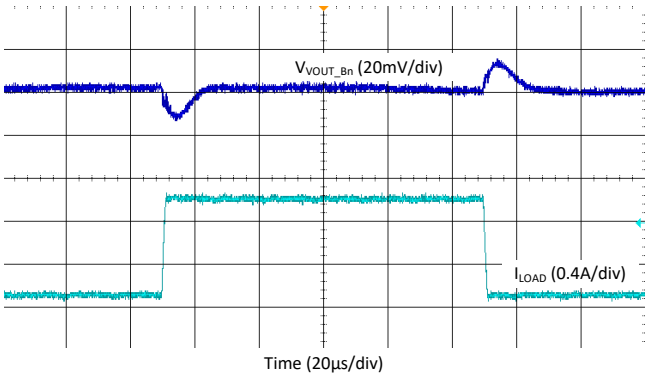
I_{LOAD} = 0.1 A → 1 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-54. Buck Load Step Transient - Buck5, 2.2 MHz, Auto Mode



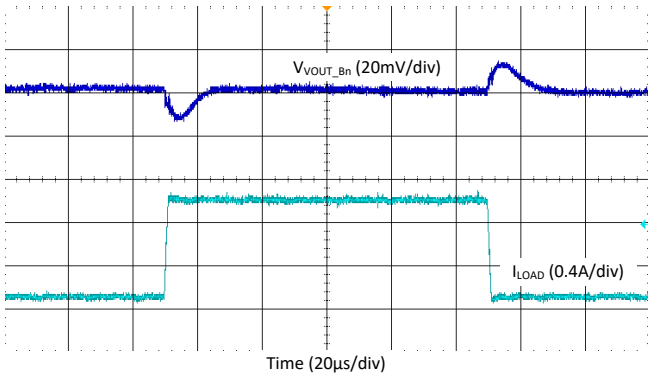
I_{LOAD} = 0.1 A → 1 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-55. Buck Load Step Transient - Buck5, 4.4 MHz, Auto Mode



I_{LOAD} = 0.1 A → 1 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-56. Buck Load Step Transient - Buck5, 2.2 MHz, Forced-PWM Mode



I_{LOAD} = 0.1 A → 1 A → 0.1 A, T_R = T_F = 1 µs
V_{PVIN_Bn} = 3.3 V V_{VOUT_Bn} = 1 V

Figure 9-57. Buck Load Step Transient - Buck5, 4.4 MHz, Forced-PWM Mode

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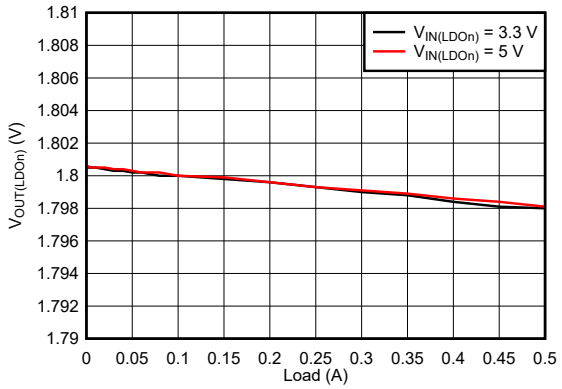
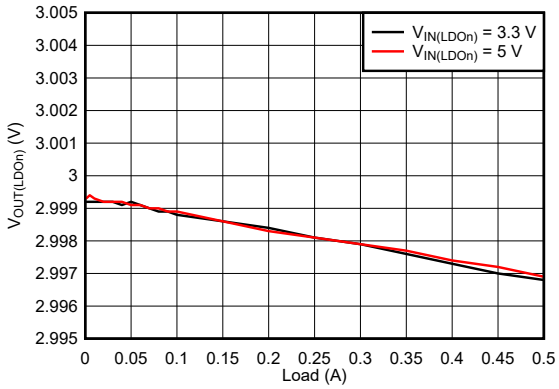
9.2.2 Application Curves (continued)



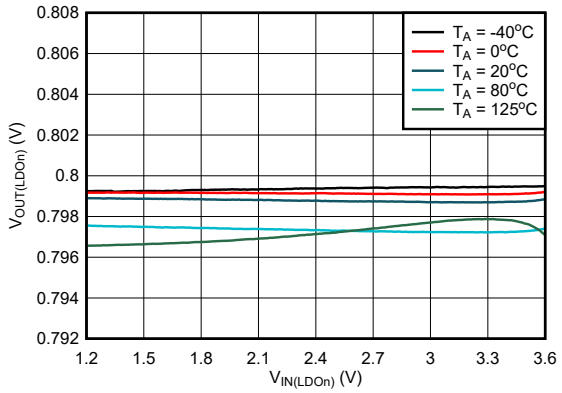
$V_{IN(LDOn)}$ = 3.3 V $V_{OUT(LDOn)}$ = 1.8 V

Figure 9-58. LDO1/2/3 Load Regulation, Vout = 1.8 V



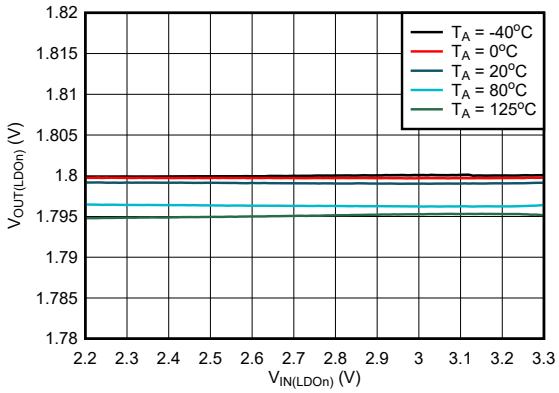
$V_{IN(LDOn)}$ = 3.3 V $V_{OUT(LDOn)}$ = 3.0 V

Figure 9-59. LDO1/2/3 Load Regulation, Vout = 3 V



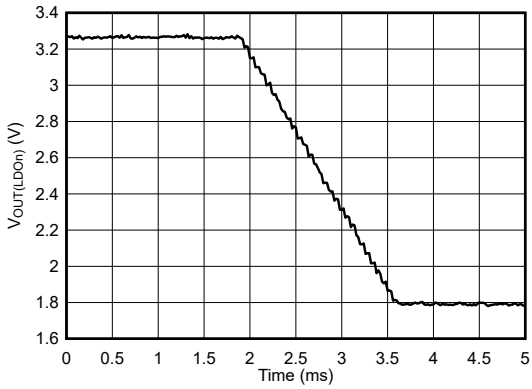
$V_{OUT(LDOn)}$ = 0.8 V $I_{OUT(LDOn)}$ = 500 mA

Figure 9-60. LDO1/2/3 Line Regulation over Temperature, Vout = 0.8 V



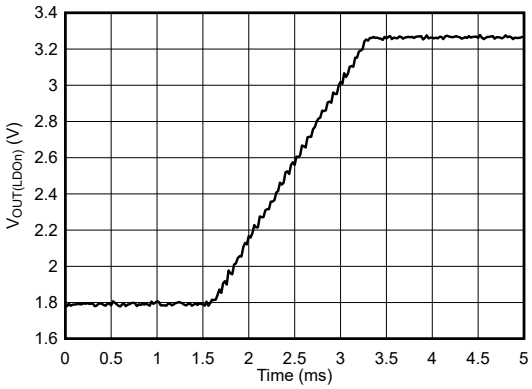
$V_{OUT(LDOn)}$ = 1.8 V $I_{OUT(LDOn)}$ = 50 mA

Figure 9-61. LDO1/2/3 Line Regulation over Temperature, Vout = 1.8 V



$V_{IN(LDOn)}$ = 3.3 V $I_{OUT(LDOn)}$ = 50 mA

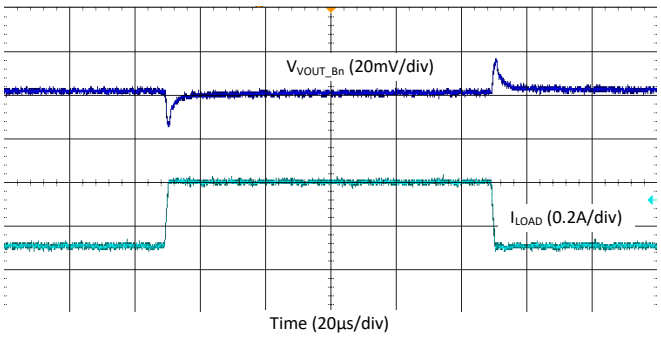
Figure 9-62. LDO1/2/3 Transition from 3.3 V in Bypass Mode to 1.8 V Linear Mode



$V_{IN(LDOn)}$ = 3.3 V $I_{OUT(LDOn)}$ = 50 mA

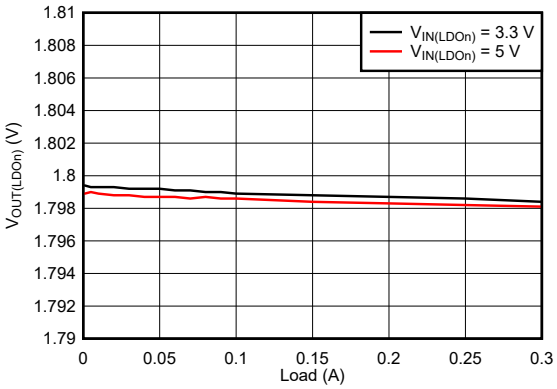
Figure 9-63. LDO1/2/3 Transition from 1.8 V in Linear Mode to 3.3 V in Bypass Mode

9.2.2 Application Curves (continued)



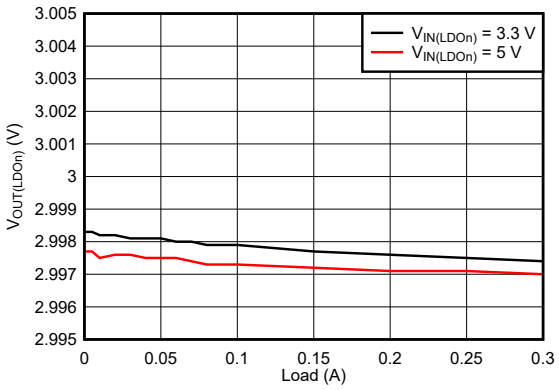
I_{LOAD} = 0.1 A → 0.4 A → 0.1 A, T_R = T_F = 1 µs
$V_{IN(LDOn)}$ = 3.3 V
$V_{OUT(LDOn)}$ = 1 V

Figure 9-64. LDO1/2/3 Load Step Transient



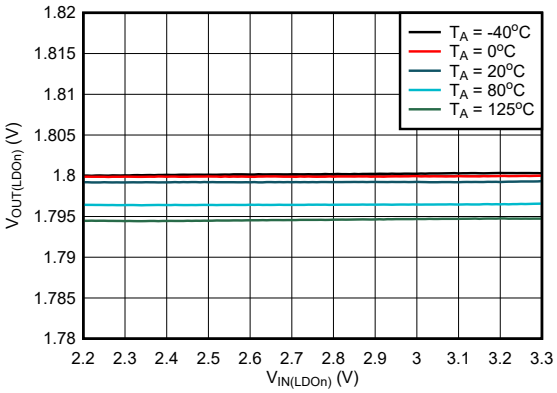
$V_{IN(LDO4)}$ = 3.3 V
$V_{OUT(LDO4)}$ = 1.8 V

Figure 9-65. LDO4 Load Regulation, Vout = 1.8 V



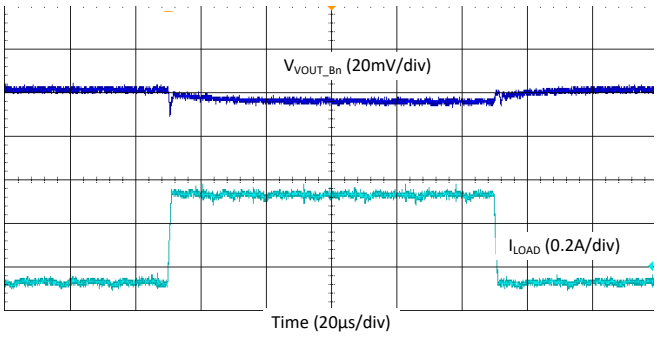
$V_{IN(LDO4)}$ = 3.3 V
$V_{OUT(LDO4)}$ = 3.0 V

Figure 9-66. LDO4 Load Regulation, Vout = 3 V



$V_{OUT(LDO4)}$ = 1.8 V
$I_{OUT(LDO4)}$ = 300 mA

Figure 9-67. LDO4 Line Regulation over Temperature, Vout = 1.8 V



I_{LOAD} = 0.1 A → 0.4 A → 0.1 A, T_R = T_F = 1 µs
$V_{IN(LDO4)}$ = 3.3 V
$V_{OUT(LDO4)}$ = = 1 V

Figure 9-68. LDO4 Load Step Transient

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10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3.0 V and 5.5 V. This input supply must be well regulated and can withstand maximum input current and keep a stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail must be low enough that the input current transient does not cause too high drop in the device supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

The high frequency and large switching currents of the TPS6594-Q1 device make the choice of layout important. Good power supply results only occur when care is given to correct design and layout. Layout affects noise pickup and generation and can cause a good design to perform with less-than-expected results.

With a range of buck output currents from a few milliampere to 10 A and over, good power supply layout is much more difficult than most general PCB design. Use the following steps as a reference to ensure the buck regulators are stable and maintain correct voltage and current regulation across its intended operating voltage and current range.

1. Place C_{IN} as close as possible to the PVIN_Bx pin and the PGND/Thermal Pad. Route the V_{IN} trace wide and thick to avoid IR drops. The DCR of the trace from the source to the pin must be less than 2 mΩ. The trace between the positive node of the input capacitor and the PVIN_Bx pins of the device, as well as the trace between the negative node of the input capacitor and PGND/Thermal Pad, must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The inductance of the connection is the most important parameter of a local decoupling capacitor — parasitic inductance on these traces must be kept as small as possible for correct device operation. The parasitic inductance can be reduced by using a ground plane as close as possible to top layer by using thin dielectric layer between top layer and ground plane.
2. The output filter, consisting of C_{OUT} and L, converts the switching signal at SW_Bx to the noiseless output voltage. It must be placed as close as possible to the device keeping the switch node small, for best EMI behavior. Note that the PVIN_Bx pin is directly adjacent to the SW_Bx pin. The inductor and capacitor placement must be made as close as possible without compromising PVIN_Bx. Route the traces between the output capacitors of the device and the load direct and wide to avoid losses due to the IR drop.
3. Input for analog blocks (VCCA and REFGND1/2) must be isolated from noisy signals. Connect VCCA directly to a quiet system voltage node and REFGND1/2 to a quiet ground point where no IR drop occurs. Place the decoupling capacitor as close as possible to the VCCA pin.
4. If the processor load supports remote voltage sensing, connect the feedback pins FB_Bx of the device to the respective sense pins on the processor. If the processor does not support remote voltage sensing, then connect the FB_Bx pin to a representative load capacitor. With differential feedback, also connect the negative feedback pin to the negative terminal of the same load capacitor. The minimum recommended trace width is 6 mils. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND, PVIN_Bx, and SW_Bx, as well as high bandwidth signals such as the I^2C. Avoid capacitive and inductive coupling by keeping the sense lines short, direct, and close to each other. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible. Running the signal as a differential pair is recommended. If series resistors are used for load current measurement, place them after connection of the voltage feedback.
5. PGND, PVIN_Bx and SW_Bx must be routed on thick layers. They must not surround inner signal layers, which are not able to withstand interference from noisy PGND, PVIN_Bx and SW_Bx.

For the LDO regulators, the feedback connection is internal. Therefore, it is important to keep the PCB resistance between LDO output and target load in the range of the acceptable voltage drop for LDOs. Similar to the buck regulators, the input capacitor at the PVIN_LDOx pins and the VCCA pin must be placed as close as possible to the PMIC. The impedance from the source of the PVIN_LDOx pins and the VCCA pin must be low and the DCR less than 2 mΩ. The output capacitor at the VOUT_LDOx, VOUT_LDOVINT and VOUT_LDOVRTC pins must be as close (0.5mm) to the PMIC as possible. The ground connection of these

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capacitors, especially for the capacitor at the VOUT_LDOVINT pin, must have a low impedance of less than 2 mΩ to the ground (Thermal Pad) of the TPS6594-Q1. For the ground connection of this capacitor at the VOUT_LDOVINT pin, use multiple vias (at least three) directly at the ground landing pad of the capacitor. See illustration below:

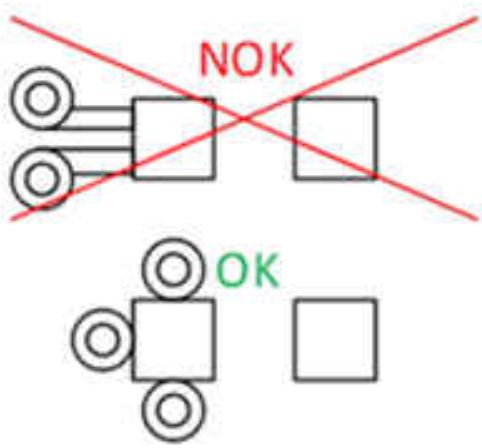

Figure 11-1. Ground connection of capacitor at VOUT_LDOVINT pin

Due to the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent parameters, such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide and thick power traces come with the ability to sink dissipated heat. The capability to sink dissipated heat can be improved further on multi-layer PCB designs with vias to different planes. Improved heat-sinking capability results in reduced junction-to-ambient ($R_{\theta JA}$) and junction-to-board ($R_{\theta JB}$) thermal resistances and thereby reduces the device junction temperature, T_J. TI strongly recommends to perform a careful system-level 2D or full 3D dynamic thermal analysis at the beginning product design process, by using a thermal modeling analysis software.

Overall recommendation for the PCB is to use at least 12 layers with 60 to 90 mil thickness, and with following weights for the Copper layers:

- 0.5oz for signal layers
- at least 1.5oz for top layer and other plane layers

A more complete list of layout recommendations can be found in the Schematic and layout checklist.

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11.2 Layout Example

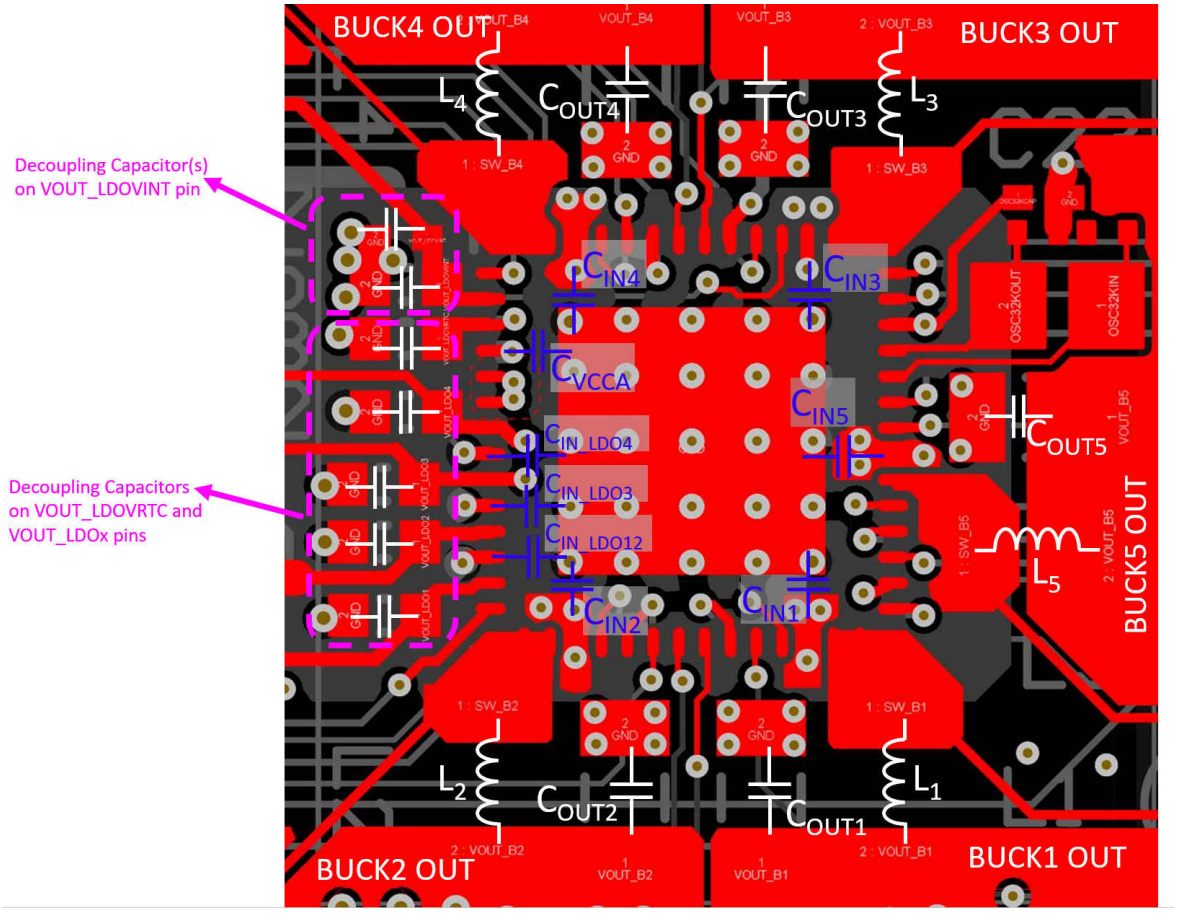

Figure 11-2. Example PMIC Layout

This example shows a top and bottom layout of the key power components and the crystal oscillator based on the EVM. Most of the digital routing is neglected in this image, see the EVM design files EVM design files for full details. The highest priority must be on the buck input capacitors, followed by the inductors, and the output capacitor on the VOUT_LDOVINT pin. Ensure that there are sufficient vias for high current pathways.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Device Nomenclature

The following acronyms and terms are used in this data sheet. For a detailed list of terms, acronyms, and definitions, see the *TI glossary*.

ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
APE	Application Processor Engine
AVS	Adaptive Voltage Scaling
DVS	Dynamic Voltage Scaling
GPIO	General-Purpose Input and Output
LDO	Low-Dropout voltage linear regulator
PM	Power Management
PMIC	Power-Management Integrated Circuit
PSRR	Power Supply Rejection Ratio
RTC	Real-Time Clock
NA	Not Applicable
NVM	Non-Volatile Memory
ESR	Equivalent Series Resistance
DCR	DC Resistance of an inductor
PDN	Power Delivery Network
PMU	Power Management Unit
PFM	Pulse Frequency Modulation
PWM	Pulse Width Modulation
EMC	Electromagnetic Compatibility
PLL	Phase Locked Loop
SPI	Serial Peripheral Interface
SPMI	System Power Management Interface
I^2C	Inter-Integrated Circuit
PFSM	Pre-configured Finite State Machine
UV	Undervoltage
OV	Overvoltage
RV	Residual Voltage
POR	Power On Reset
UVLO	Undervoltage Lockout
OVP	Overvoltage Protection

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EPC	Embedded Power Controller
FSD	First Supply Detection
ESM	Error Signal Monitor
MCU	Micro Controller Unit
SoC	System on Chip
BIST	Built-In Self-Test
ABIST	Analog Built-In Self-Test
LBIST	Logic Built-In Self-Test
CRC	Cyclic Redundancy Check
VMON	Voltage Monitor
PGOOD	Power Good (signal which indicates that the monitored power supply rail(s) is (are) in range)

12.3 Documentation Support

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65940400RWERQ1	ACTIVE	VQFNP	RWE	56	2000	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS6594 0400-Q1	Samples
TPS65941111RWERQ1	ACTIVE	VQFNP	RWE	56	2000	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	TPS6594 1111-Q1	Samples
TPS65941120RWERQ1	ACTIVE	VQFNP	RWE	56	2000	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	TPS6594 1120-Q1	Samples
TPS65941212RWERQ1	ACTIVE	VQFNP	RWE	56	2000	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	TPS6594 1212-Q1	Samples
TPS65941213RWERQ1	ACTIVE	VQFNP	RWE	56	2000	RoHS & Green	Call TI | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	TPS6594 1213-Q1	Samples
TPS65941319RWERQ1	ACTIVE	VQFNP	RWE	56	2000	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	TPS6594 1319-Q1	Samples
TPS6594133ARWERQ1	ACTIVE	VQFNP	RWE	56	2000	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS6594 133A-Q1	Samples
TPS6594141BRWERQ1	ACTIVE	VQFNP	RWE	56	2000	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	TPS6594 141B-Q1	Samples
TPS65941421RWERQ1	ACTIVE	VQFNP	RWE	56	2000	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	TPS6594 1421-Q1	Samples
TPS65941515RWERQ1	ACTIVE	VQFNP	RWE	56	2000	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS6594 1515-Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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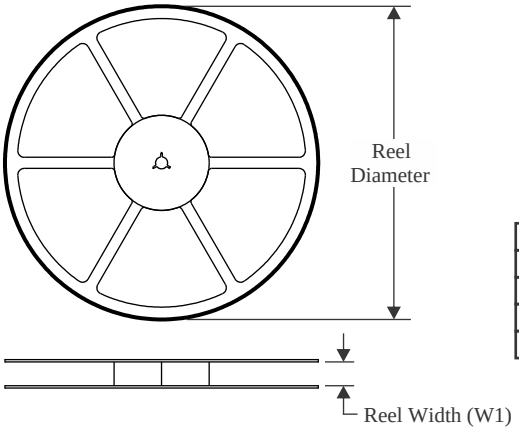
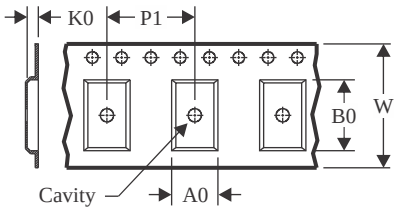
TAPE AND REEL INFORMATION

REEL DIMENSIONS

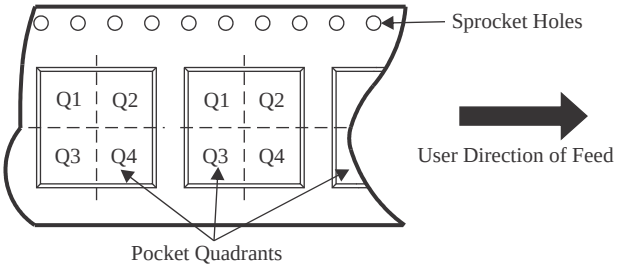


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

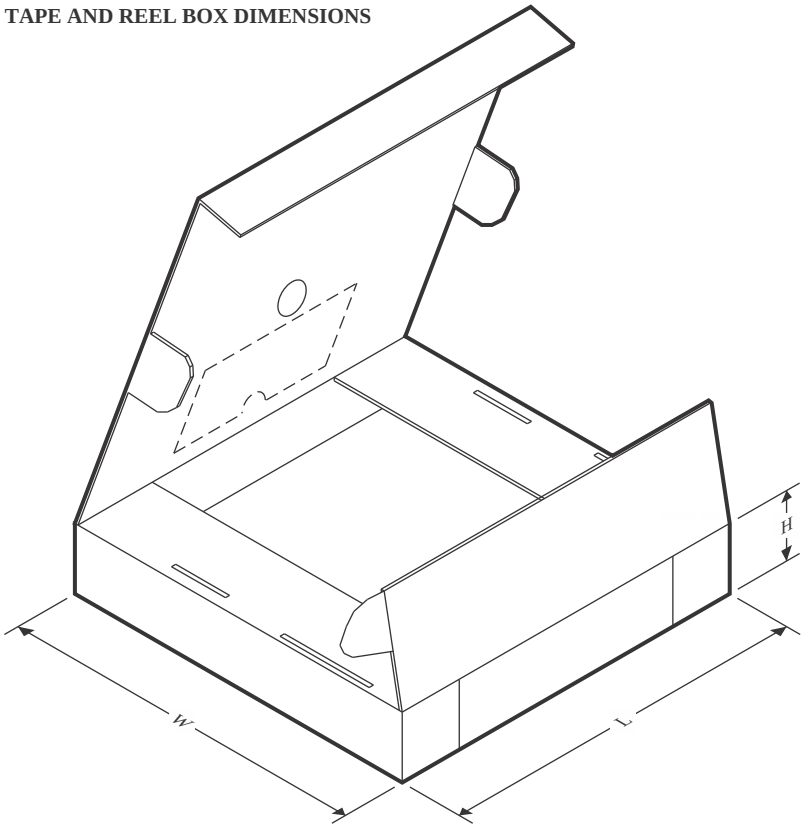
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65941120RWERQ1	VQFNP	RWE	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
TPS65941319RWERQ1	VQFNP	RWE	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
TPS65941421RWERQ1	VQFNP	RWE	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65941120RWERQ1	VQFNP	RWE	56	2000	350.0	350.0	43.0
TPS65941319RWERQ1	VQFNP	RWE	56	2000	350.0	350.0	43.0
TPS65941421RWERQ1	VQFNP	RWE	56	2000	350.0	350.0	43.0

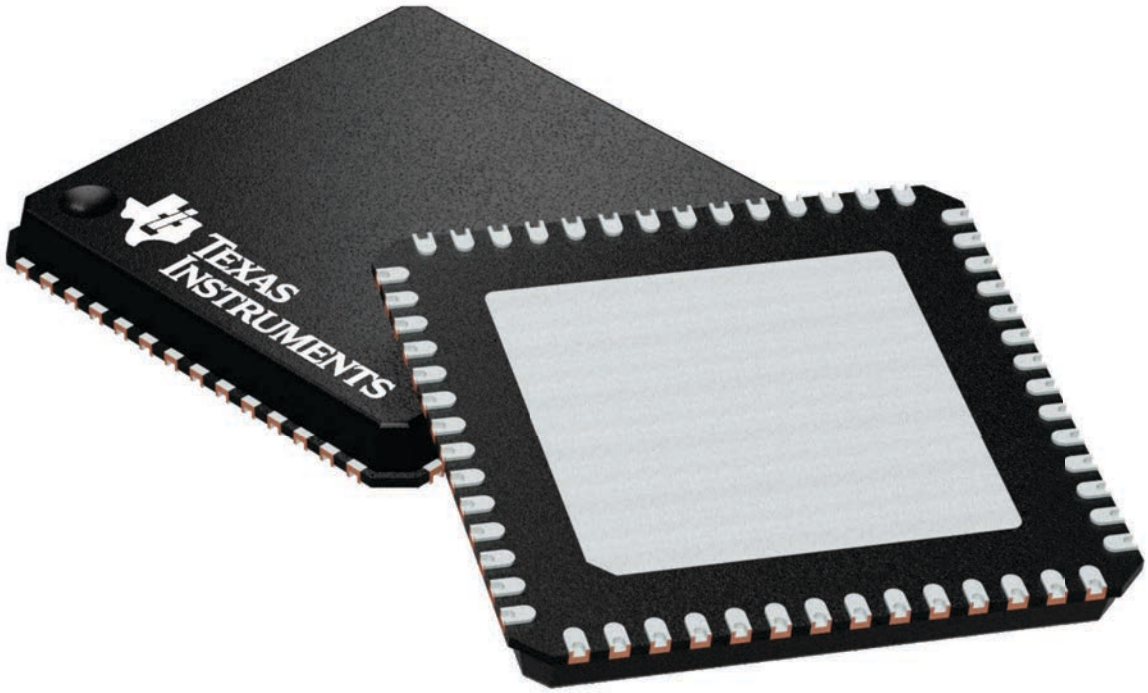
GENERIC PACKAGE VIEW

RWE 56

VQFNP - 0.9 mm max height

8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

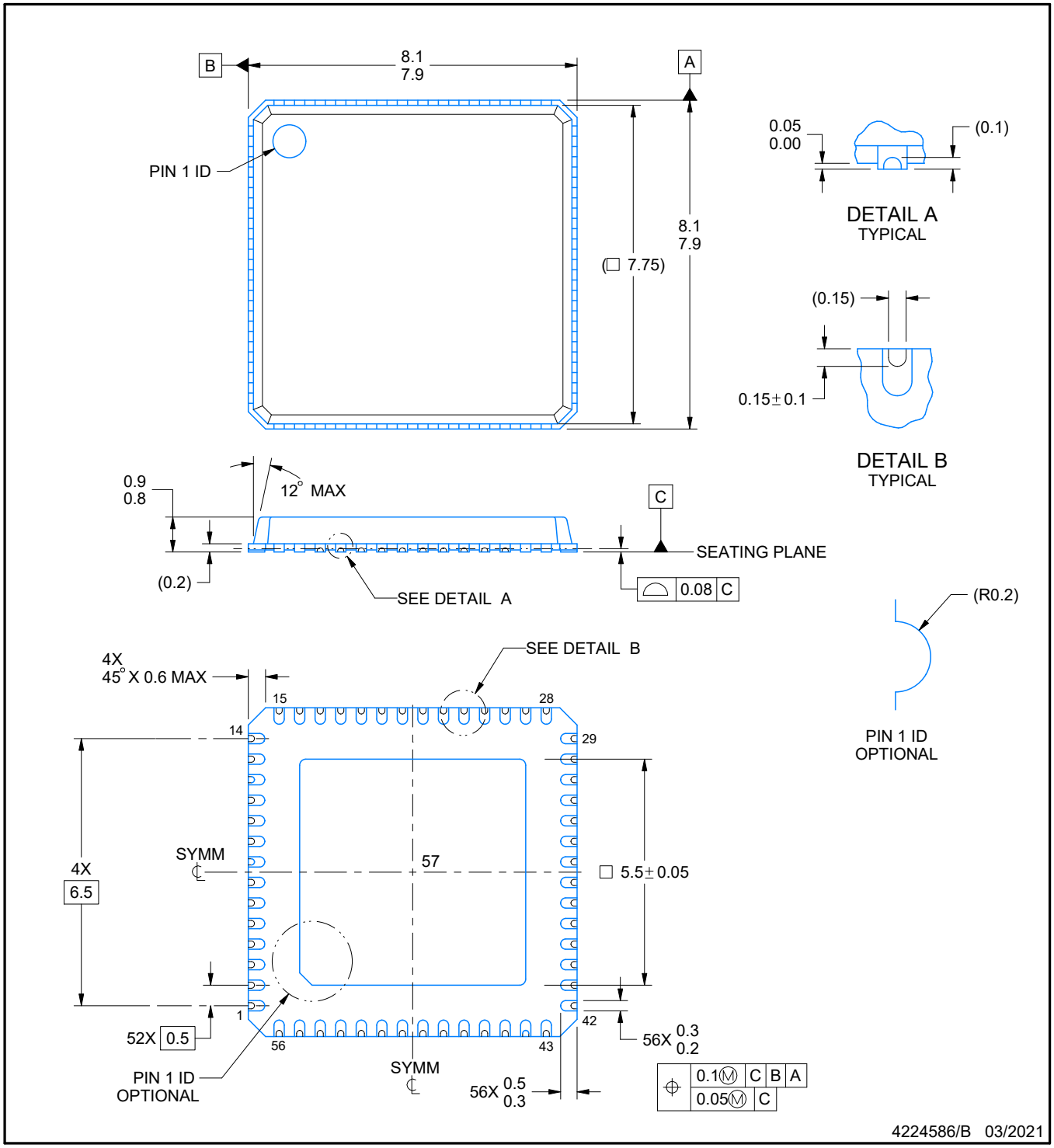
4224587/A

PACKAGE OUTLINE

RWE0056C

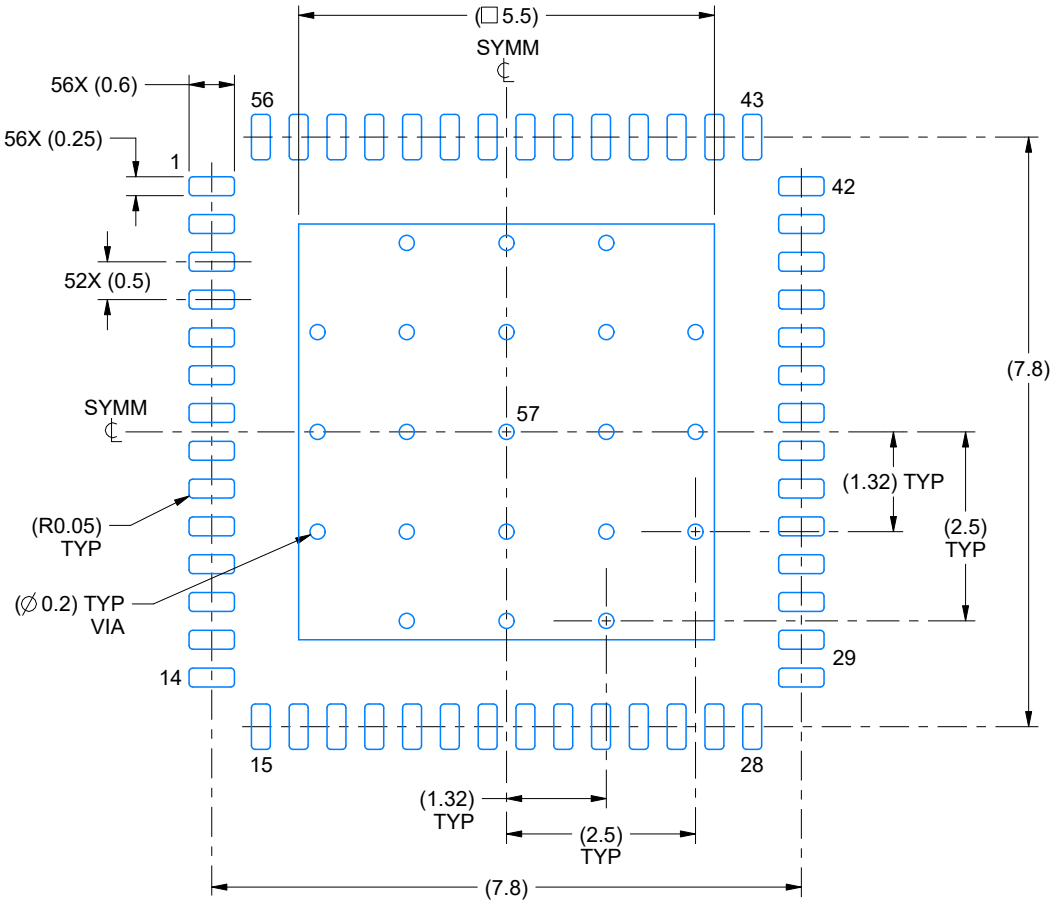
VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

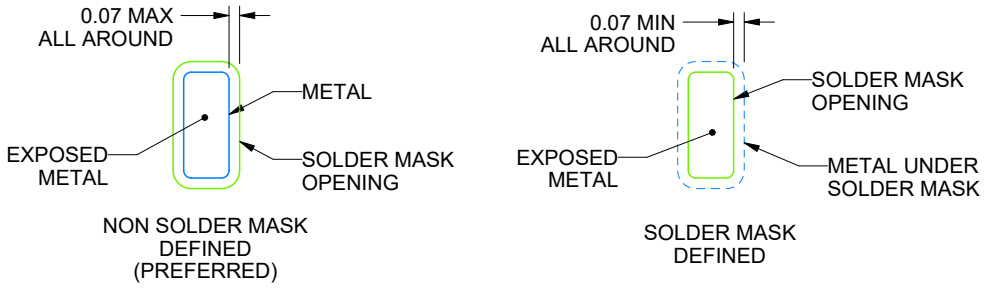


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



SOLDER MASK DETAILS

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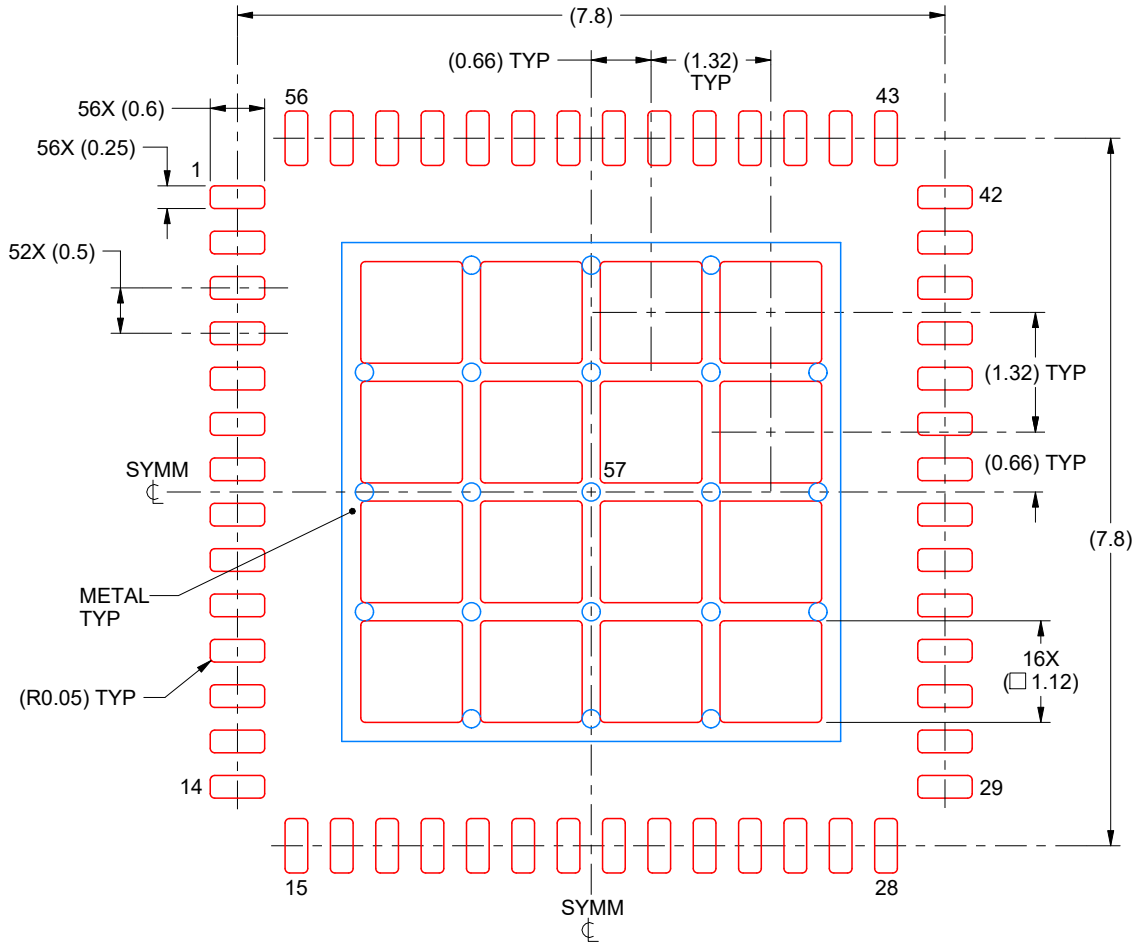
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 57:
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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