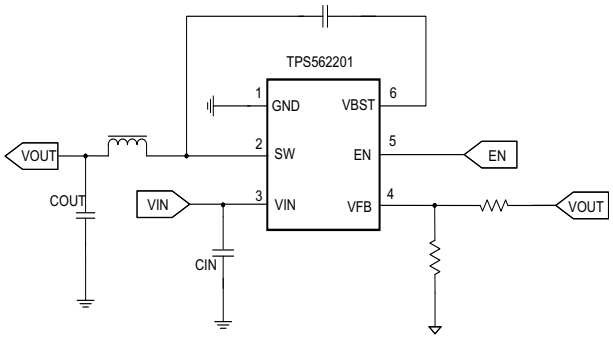
TPS56220x 4.5V to 17V Input, 2A Synchronous Step-Down Voltage Regulator in SOT-23

1 Features

- TPS562201 and TPS562208 2A converter integrated 140mΩ and 84mΩ FETs
- D-CAP2™ control scheme with fast transient response
- Input voltage range: 4.5V to 17V
- Output voltage range: 0.76V to 7V
- Pulse-skip mode (TPS562201) or continuous current mode (TPS562208)
- 580kHz switching frequency
- Low shutdown current less than 20µA
- 2% feedback voltage accuracy (25°C)
- Start-up from prebiased output voltage
- Cycle-by-cycle overcurrent limit
- Hiccup-mode overcurrent protection
- Non-latch UVP and TSD protections
- Fixed soft start: 1.0ms
- Create a custom design using the TPS56220x with the WEBENCH® Power Designer

2 Applications

- Digital TV power supply
- High definition Blu-ray™ disc players
- Networking home terminal
- Digital set-top box (STB)
- Surveillance



Simplified Schematic

3 Description

The TPS562201 and TPS562208 are simple, easy-to-use, 2A synchronous step-down converters in SOT-23 package.

The devices are designed to operate with minimum external component counts and also designed to achieve low standby current.

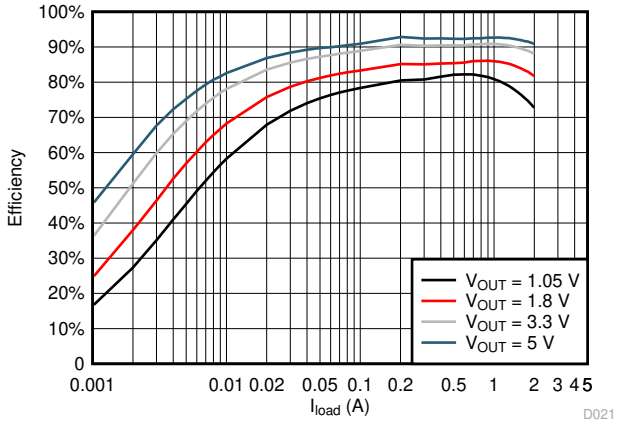
These switch mode power supply (SMPS) devices employ D-CAP2 control scheme providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

The TPS562201 operates in pulse skip mode, which maintains high efficiency during light load operation. The TPS562201 and TPS562208 are available in a 6-pin 1.6mm × 2.9 mm SOT (DDC) package and specified from a –40°C to 125°C junction temperature.

Device Information

PART NUMBER	MODE	PACKAGE(1)	PACKAGE SIZE(2)
TPS562201	ECO	DDC (SOT, 6)	1.6mm × 2.9mm
TPS562208	FCCM		

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPS562201 Efficiency

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4 Pin Configuration and Functions

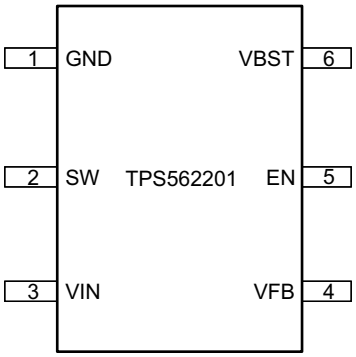


Figure 4-1. 6-Pin SOT DDC Package (Top View)

Table 4-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
GND	1	Ground pin source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET
VFB	4	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	Enable input control. Active high and must be pulled up to enable the device
VBST	6	Supply input for the high-side NFET gate drive circuit. Connect a 0.1-µF capacitor between VBST and SW pins.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN, EN	–0.3	19	V
	VBST	–0.3	25	V
	VBST (10-ns transient)	–0.3	27	V
	VBST (vs SW)	–0.3	6	V
	VFB	–0.3	6	V
	SW	–2	19	V
	SW (10 ns transient)	–3.5	21	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage		4.5	17	V
V_I	Input voltage	VBST	–0.1	23	V
		VBST (10-ns transient)	–0.1	26	
		VBST(vs SW)	–0.1	5.5	
		EN	–0.1	17	
		VFB	–0.1	5.5	
		SW	–1.8	17	
		SW (10 ns transient)	–3.5	20	
T_J	Operating junction temperature		–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS562201 and TPS562208 DDC (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	°C/W

THERMAL METRIC(1)		TPS562201 and TPS562208 DDC (SOT) 6 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	16.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

T_J = –40°C to 125°C, V = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{VIN}	Operating – non-switching supply current	V_{IN} current, EN = 5 V, VFB = 0.9 V	TPS562201		120	200	µA
			TPS562208		350	500	
I_{VINSDN}	Shutdown supply current	V_{IN} current, EN = 0 V			8	20	µA
LOGIC THRESHOLD							
V_{ENH}	EN high-level input voltage			1.6			V
V_{ENL}	EN low-level input voltage					0.8	V
R_{EN}	EN pin resistance to GND	V_{EN} = 1.5 V		600	1500	2400	kΩ
I_{EN}	EN pulldown current	V_{EN} = 1.5 V			1		µA
VFB VOLTAGE AND DISCHARGE RESISTANCE							
V_{FBTH}	VFB threshold voltage (1)	V_O = 1.05 V, I_O = 10 mA, Eco-mode operation			774		mV
	VFB threshold voltage	V_O = 1.05 V, continuous mode operation		749	768	787	mV
I_{VFB}	VFB input current	V_{FB} = 0.8 V			0	±0.1	µA
MOSFET							
$R_{DS(on)h}$	High-side switch resistance	T_A = 25°C, V_{BST} – SW = 5 V			140		mΩ
$R_{DS(on)l}$	Low-side switch resistance	T_A = 25°C			84		mΩ
CURRENT LIMIT							
I_{ocl}	Current limit	DC current, V_{OUT} = 1.05 V, L1 = 2.2 µH		2.4	3.2	4.0	A
THERMAL SHUTDOWN							
T_{SDN}	Thermal shutdown threshold(1)	Shutdown temperature			160		°C
		Hysteresis			25		
ON-TIME TIMER CONTROL							
$t_{OFF(MIN)}$	Minimum off time	VFB = 0.5 V			220	310	ns
SOFT START							
t_{ss}	Soft-start time	Internal soft-start time			1.0		ms
Frequency							
F_{sw}	Switching frequency	V_{IN} = 12 V, V_O = 1.05 V, FCCM mode			580		kHz
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION							
V_{UVP}	Output UVP threshold	Hiccup detect (H > L)			65%		
T_{HICCUP_WAIT}	Hiccup wait time				1.2		ms
T_{HICCUP_RE}	Hiccup time before restart				10		ms
UVLO							
UVLO	UVLO threshold	Wake up VIN voltage			3.8	4.3	V
		Shut down VIN voltage		3.3	3.4		
		Hysteresis VIN voltage			0.4		

(1) Not production tested

5.6 Typical Characteristics

V_{IN} = 12 V (unless otherwise noted)

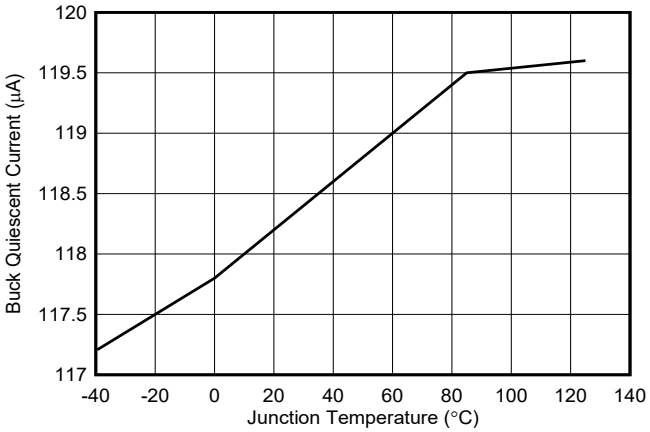


Figure 5-1. TPS562201 Supply Current vs Junction Temperature

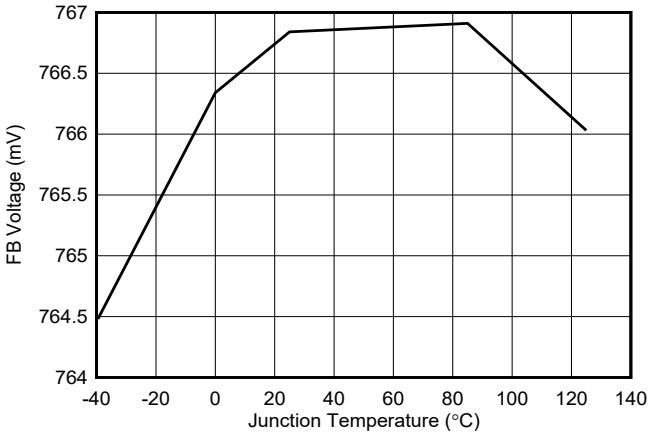


Figure 5-2. VFB Voltage vs Junction Temperature

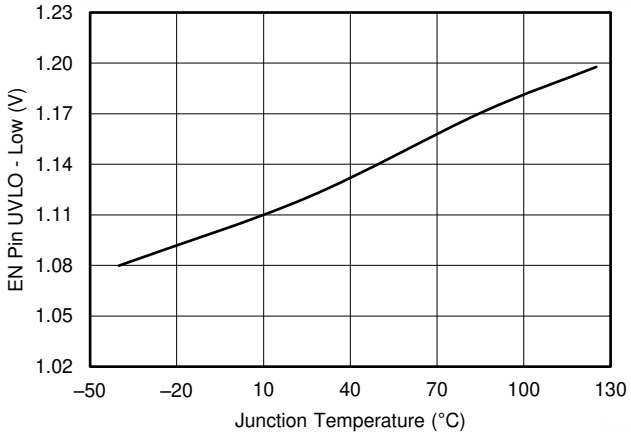


Figure 5-3. EN Pin UVLO Low Voltage vs Junction Temperature

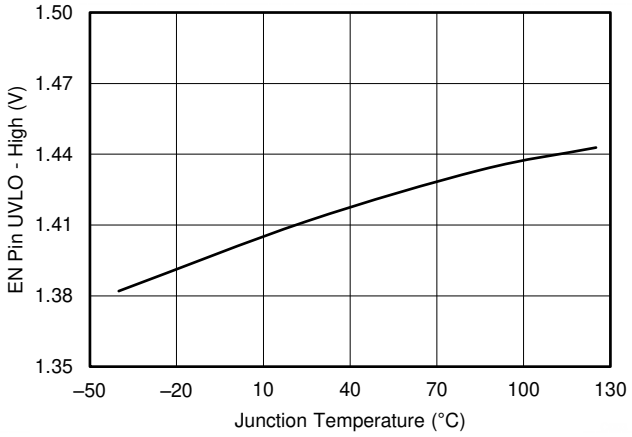


Figure 5-4. EN Pin UVLO High Voltage vs Junction Temperature

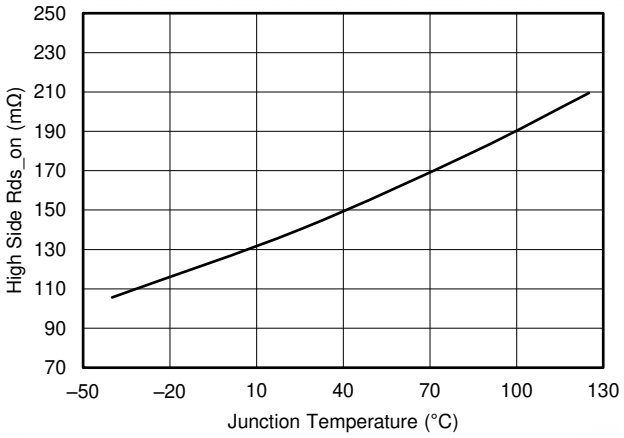


Figure 5-5. High-Side R_{ds-on} vs Junction Temperature

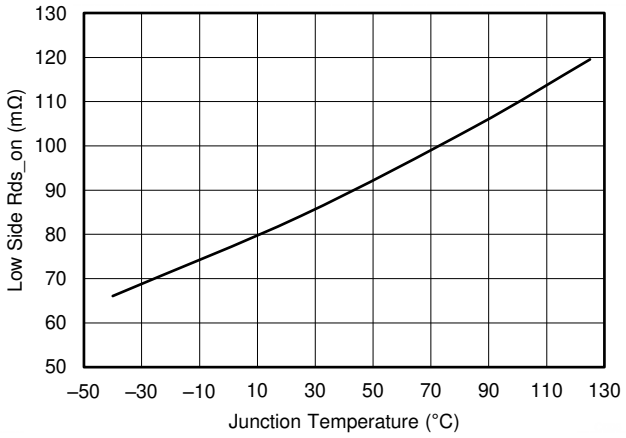


Figure 5-6. Low-Side R_{ds-on} vs Junction Temperature

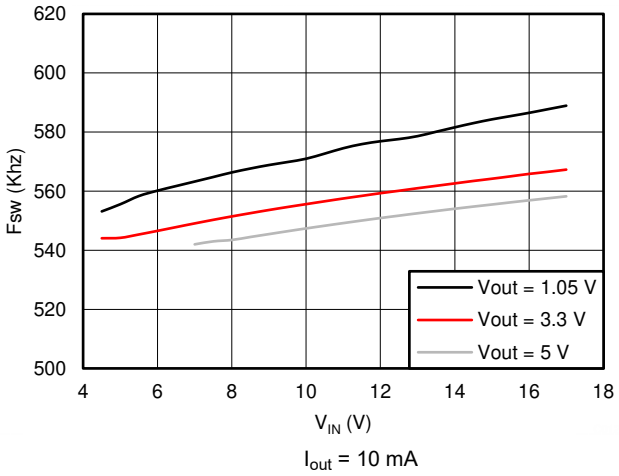


Figure 5-7. TPS562208 Switching Frequency vs Input Voltage

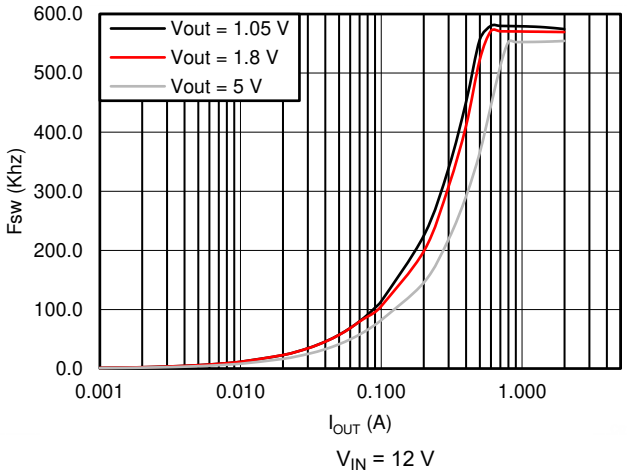


Figure 5-8. TPS562201 Switching Frequency vs Output Current

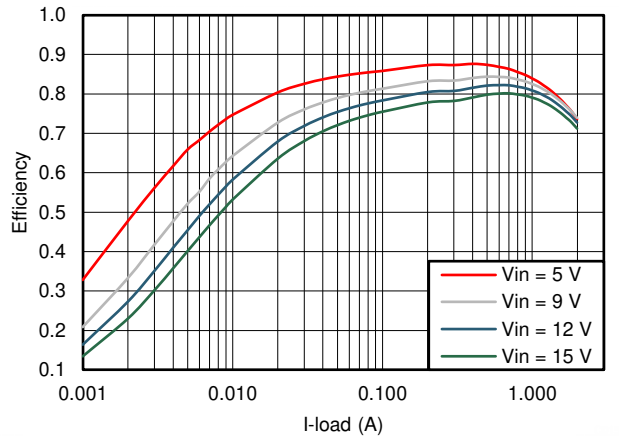


Figure 5-9. TPS562201 V_{OUT} = 1.05 V Efficiency, L = 2.2 µH

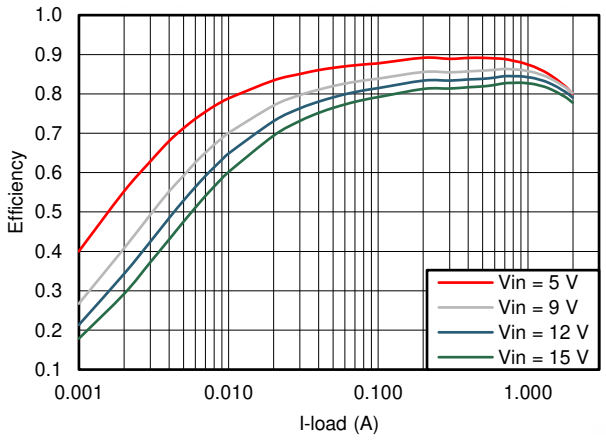


Figure 5-10. TPS562201 V_{OUT} = 1.5 V Efficiency, L = 2.2 µH

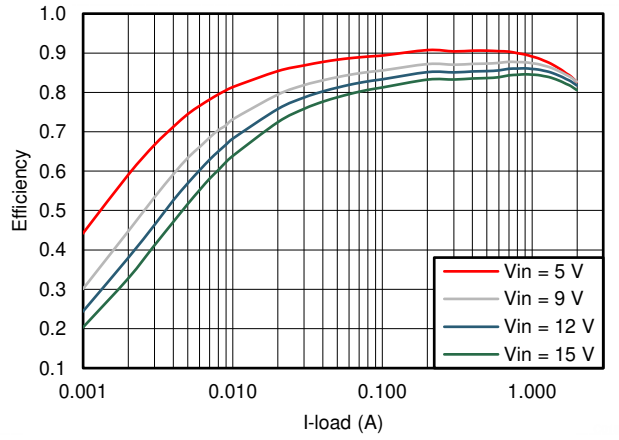


Figure 5-11. TPS562201 V_{OUT} = 1.8 V Efficiency, L = 2.2 µH

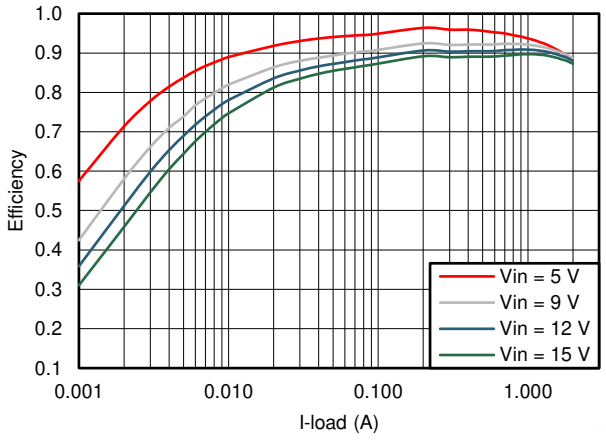


Figure 5-12. TPS562201 V_{OUT} = 3.3 V Efficiency, L = 3.3 µH

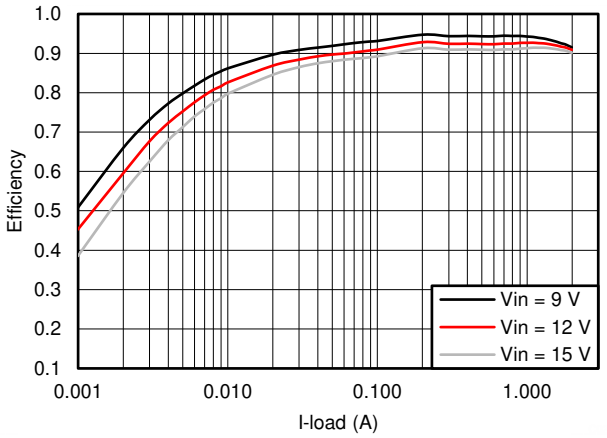


Figure 5-13. TPS562201 V_{OUT} = 5 V Efficiency, L = 3.3 µH

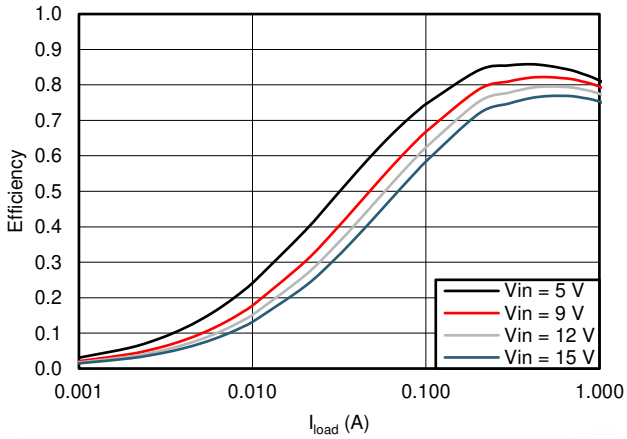


Figure 5-14. TPS562208 V_{OUT} = 1.05 V Efficiency, L = 2.2 µH

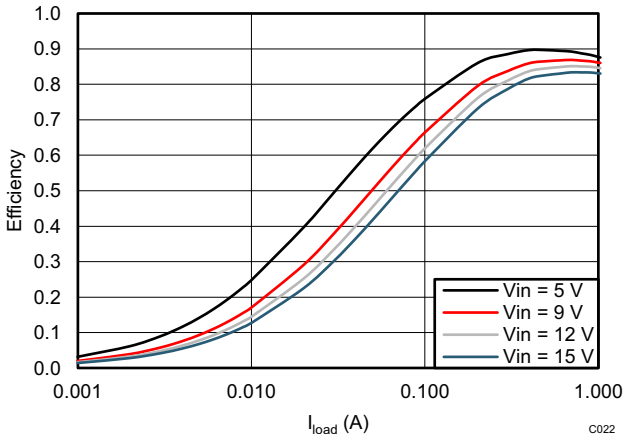


Figure 5-15. TPS562208 V_{OUT} = 1.5 V Efficiency, L = 2.2 µH

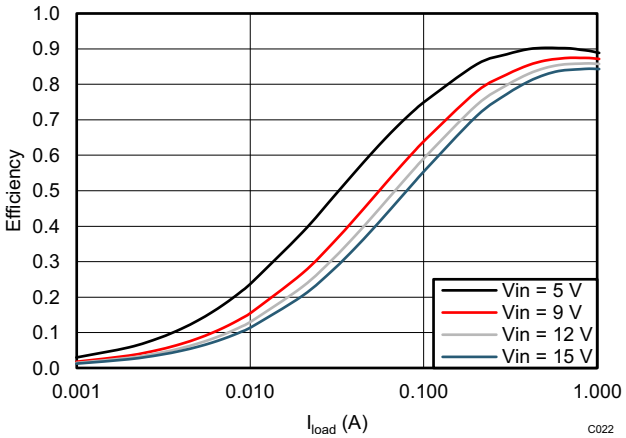


Figure 5-16. TPS562208 V_{OUT} = 1.8 V Efficiency, L = 2.2 µH

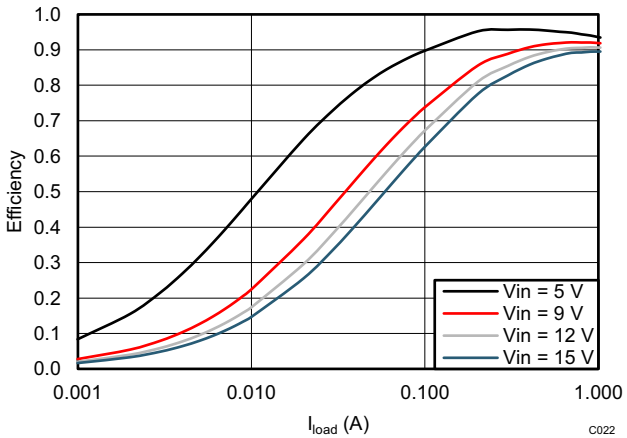


Figure 5-17. TPS562208 V_{OUT} = 3.3 V Efficiency, L = 2.2 µH

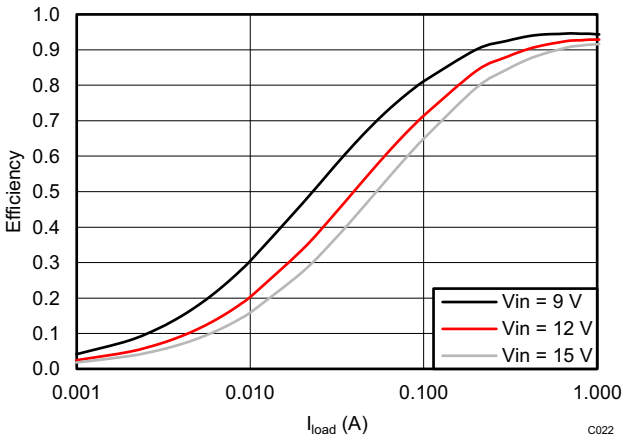


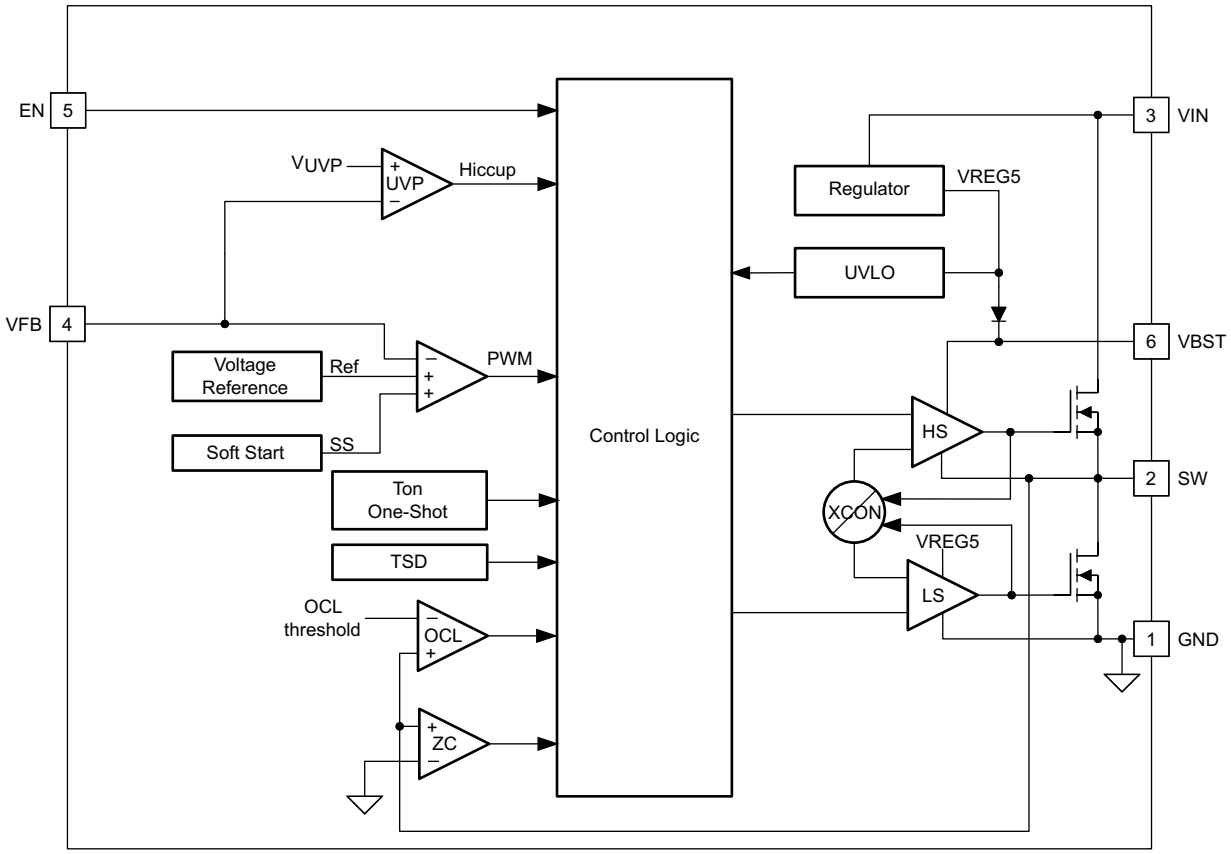
Figure 5-18. TPS562208 V_{OUT} = 5 V Efficiency, L = 3.3 µH

6 Detailed Description

6.1 Overview

The TPS562201 and TPS562208 are 2-A synchronous step-down converters. The proprietary D-CAP2 control scheme supports low-ESR output capacitors, such as specialty polymer capacitors and multi-layer ceramic capacitors, without complex external compensation circuits. The fast transient response of D-CAP2 control scheme can reduce the output capacitance required to meet a specific level of performance.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS562201 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 control scheme. The D-CAP2 control scheme combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set proportional to the converter input voltage, V_{IN}, and inversely proportional to the output voltage, V_O, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 control scheme.

6.3.2 Pulse Skip Control (TPS562201)

The TPS562201 and TPS562208 are designed with Advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually

comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

6.3.3 Soft Start and Pre-Biased Soft Start

The TPS562201 and TPS562208 have an internal 1.0-ms soft start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator. If the output capacitor is pre-biased at start-up, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage, VFB. This scheme ensures that the converters ramp up smoothly into regulation point.

6.3.4 Current Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by V_{in}, V_{out}, the on-time, and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current, I_{out}. If the monitored current is above the OCL level, the converter keeps the low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter. This can cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it, then the device will shut down after the UVP delay time (typically 256 µs) and restart after the hiccup time (typically 10 ms).

When the overcurrent condition is removed, the output voltage returns to the regulated value.

6.3.5 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

6.3.6 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 160°C), the device is shut off. This is a non-latch protection.

6.4 Device Functional Modes

6.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS562200 can operate in their normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS562208 operates at a quasi-fixed frequency of 580 kHz.

6.4.2 Eco-mode Operation

When the TPS562201 and TPS562208 are in the normal CCM operating mode and the switch current falls to 0 A, the TPS562200 begins operating in pulse skipping Eco-mode. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the Eco-mode threshold voltage. As the output current decreases, the perceived time between switching pulses increases.

6.4.3 Standby Operation

When the TPS562201 and TPS562208 are operating in either normal CCM or Eco-mode, they can be placed in standby by asserting the EN pin low.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The devices are typical step-down DC-DC converters. It typically uses to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 2 A. The following design procedure can be used to select component values for the TPS562201 and TPS562208. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

7.2 Typical Application

The application schematic in Figure 7-1 was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

Figure 7-1 shows the TPS562201 and TPS562208 4.5-V to 17-V Input, 1.05-V output converter schematics.

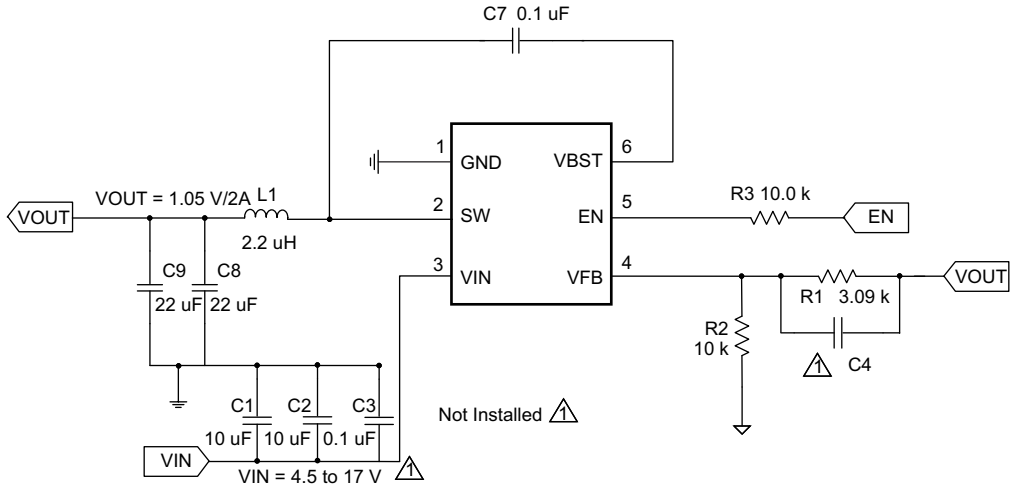


Figure 7-1. TPS562201 and TPS562208 1.05-V/2-A Reference Design

7.2.1 Design Requirements

Table 7-1 shows the design parameters.

Table 7-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 17 V
Output voltage	1.05 V
Transient response, 1.5-A load step	ΔVout = ±5%
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	2A
Operating frequency	580 kHz

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS56220x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using Equation 2 to calculate VOUT.

To improve efficiency at very light loads, consider using larger value resistors. Too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.768 \times \left(1 + \frac{R1}{R2}\right) \tag{2}$$

7.2.2.3 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{3}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 control scheme introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 7-2.

Table 7-2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)			C8 + C9 (µF)
			MIN	TYP	MAX	
1	3.09	10.0	2.2	2.2	4.7	20 to 68
1.05	3.74	10.0	2.2	2.2	4.7	20 to 68
1.2	5.76	10.0	2.2	2.2	4.7	20 to 68
1.5	9.53	10.0	2.2	2.2	4.7	20 to 68
1.8	13.7	10.0	2.2	2.2	4.7	20 to 68
2.5	22.6	10.0	3.3	3.3	4.7	20 to 68
3.3	33.2	10.0	3.3	3.3	4.7	20 to 68

Table 7-2. Recommended Component Values (continued)

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)			C8 + C9 (µF)
			MIN	TYP	MAX	
5	54.9	10.0	3.3	4.7	4.7	20 to 68
6.5	75	10.0	3.3	4.7	4.7	20 to 68

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using Equation 4, Equation 5, and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 580 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

$$II_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{4}$$

$$II_{PEAK} = I_O + \frac{II_{P-P}}{2} \tag{5}$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} II_{P-P}^2} \tag{6}$$

For this design example, the calculated peak current is 3.5 A and the calculated RMS current is 3.01 A. The inductor used is a WE 744311330 with a peak current rating of 11 A and an RMS current rating of 6.5 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS562201 and TPS562208 are intended for use with ceramic or other low-ESR capacitors. Recommended values range from 20 µF to 68 µF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \tag{7}$$

For this design, two TDK C3216X5R0J226M 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4 A.

7.2.2.4 Input Capacitor Selection

The TPS562201 and TPS562208 require an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

7.2.2.5 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

7.2.3 Application Curves

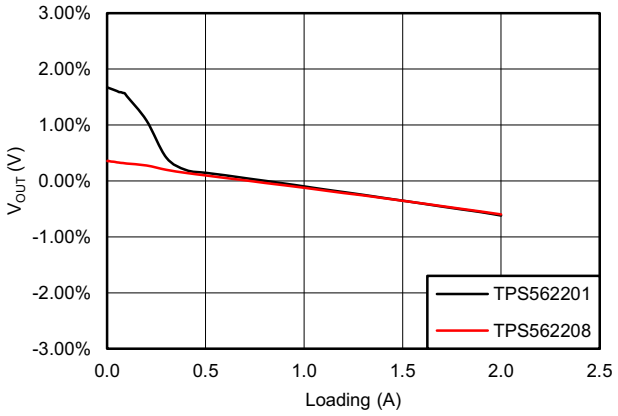


Figure 7-2. Load Regulation, V_{IN} = 5 V

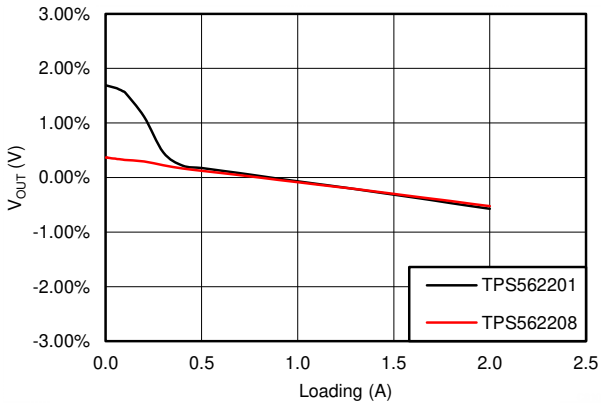
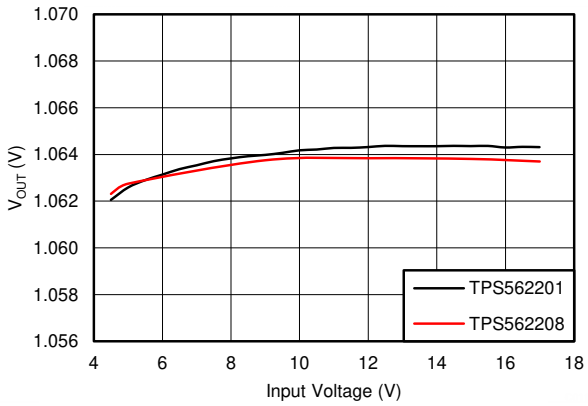


Figure 7-3. Load Regulation V_{IN} = 12 V



TPS562201: I_{out} = 1 A
TPS562208: I_{out} = 10 mA

Figure 7-4. Line Regulation

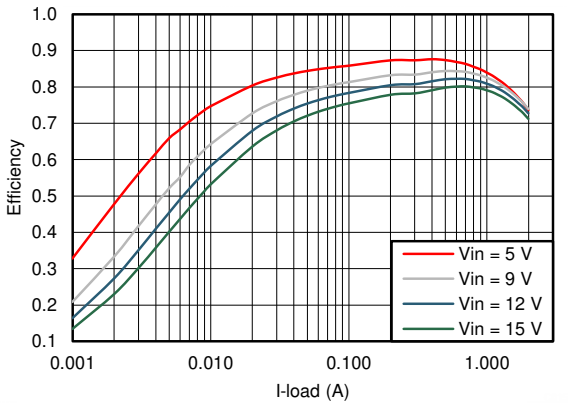
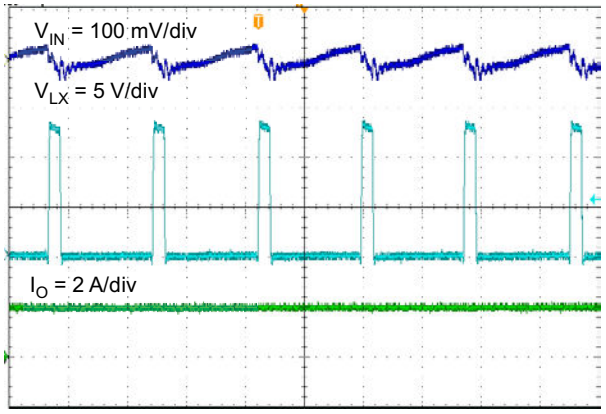
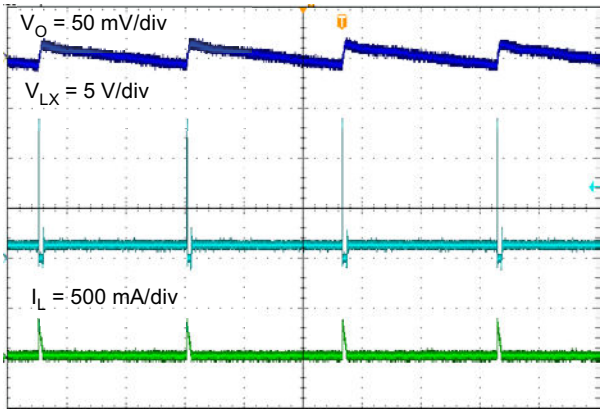


Figure 7-5. TPS562201 Efficiency, V_{OUT} = 1.05 V



800 ns/div

Figure 7-6. TPS562201 Input Voltage Ripple



20 ns/div

Figure 7-7. TPS562201 Output Voltage Ripple, I_{OUT} = 10 mA

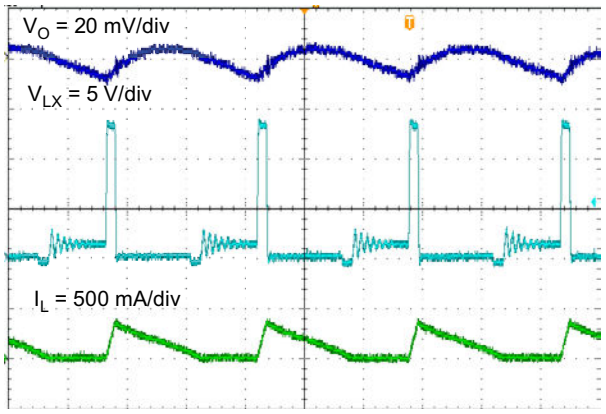


Figure 7-8. TPS562201 Output Voltage Ripple, I_{OUT} = 0.25 A

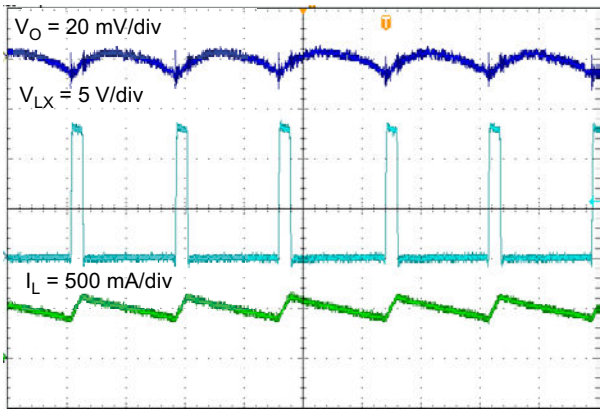


Figure 7-9. TPS562201 Output Voltage Ripple, I_{OUT} = 2 A

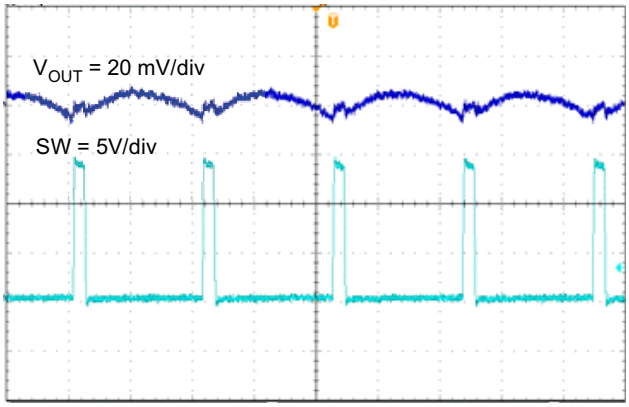


Figure 7-10. TPS562208 Output Voltage Ripple, I_{OUT} = 0 A

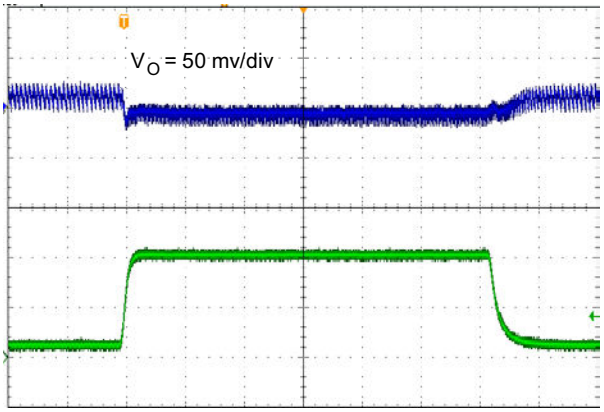


Figure 7-11. TPS562201 Transient Response, 0.1 to 1.5 A

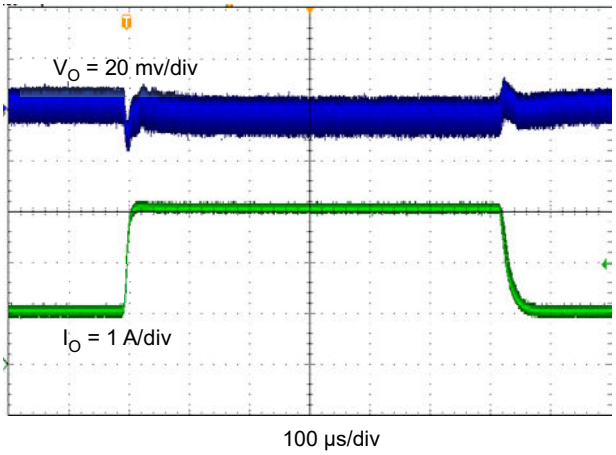


Figure 7-12. TPS562201 Transient Response, 0.75 to 2.25 A

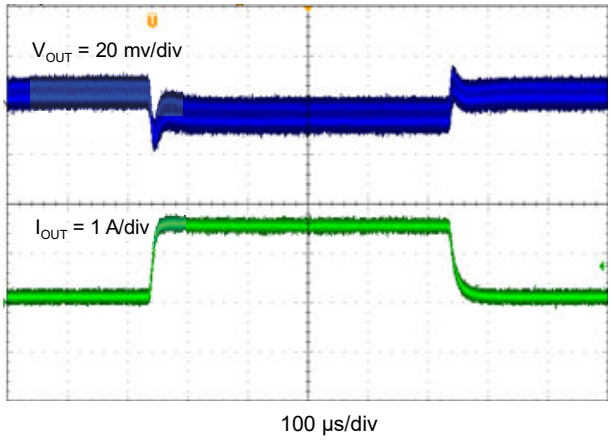


Figure 7-13. TPS562208 Transient Response 0.1 to 2 A

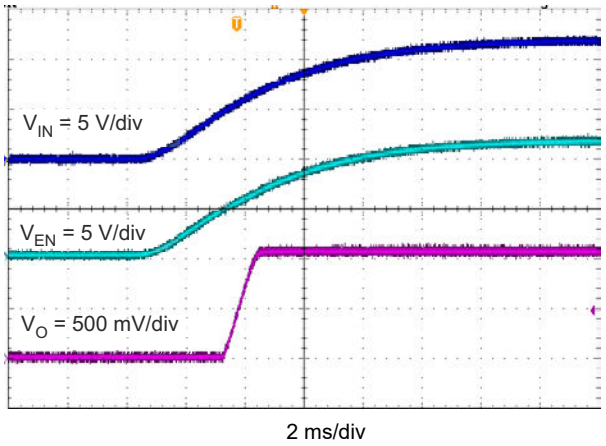


Figure 7-14. TPS562201 Start-Up Relative to V_I

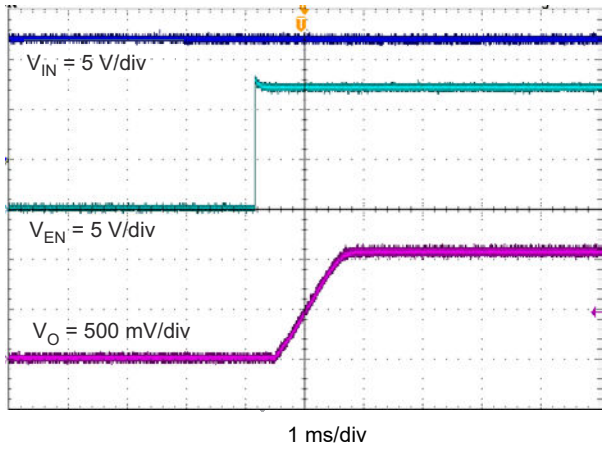


Figure 7-15. TPS562201 Start-Up Relative to EN

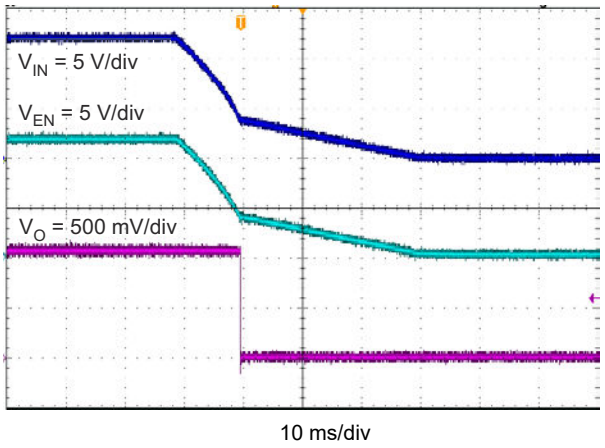


Figure 7-16. TPS562201 Shutdown Relative to V_I

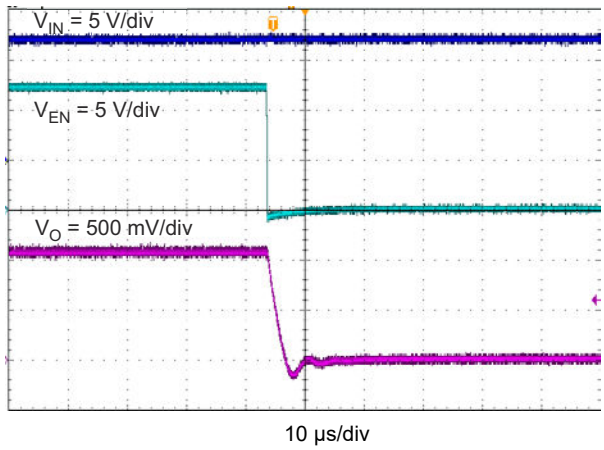


Figure 7-17. TPS562201 Shutdown Relative to EN

7.3 Power Supply Recommendations

The TPS562201 and TPS562208 are designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is V_O / 0.75.

7.4 Layout

7.4.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.

10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

7.4.2 Layout Example

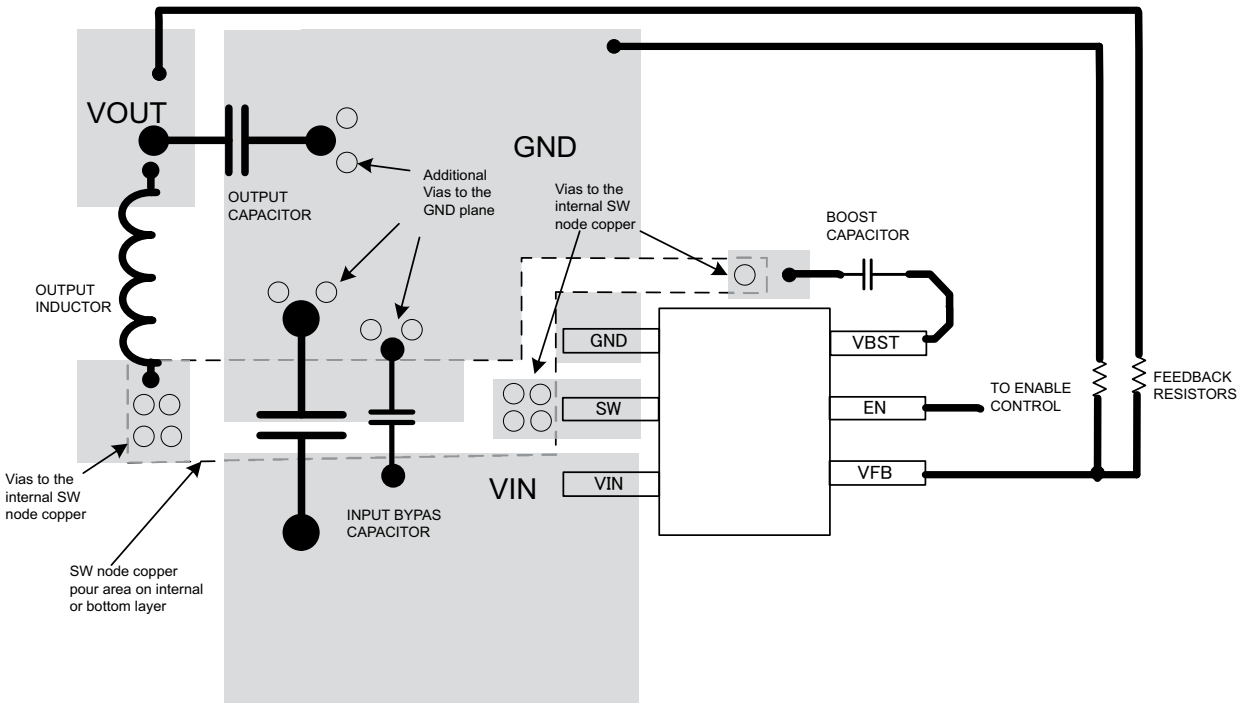


Figure 7-18. TPS562201 and TPS562208 Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS56220x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2020) to Revision C (April 2024)	Page
• Updated trademark information	1
• Added WEBENCH information throughout the document	1
• Changed low shutdown current from less than 10µA to less than 20µA	1
• Updated the document title	1
• Updated *Device Information* table format	1
• Changed VBST (vs SW) and VFB MAX from 6.5 to 6	4
• Changed Human-body model (HBM) value from 3000 to 2000	4
• Changed VBST (vs SW) MAX from 6.0 to 5.5	4
• Updated specifications in the *Electrical Characteristics* table	5
• Updated Figure 5-1 and Figure 5-2	6
• Updated the *Current Protection* section	10

Changes from Revision A (December 2017) to Revision B (September 2020)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document.	1
• Changed to 'TPS562201' from 'TPS563201' in "TPS562201 Efficiency"	1
• Changed 'TPS563201' to 'TPS562201' in "TPS562201 Supply Current vs Junction Temperature"	6
• Changed to 'TPS562208' from 'TPS563208' and 'TPS562201' from 'TPS563208' in "Line Regulation"	15
• Changed to 'TPS562201' from 'TPS563201' in "TPS562201 Efficiency, V_{OUT} = 1.05 V"	15

Changes from Revision * (December 2015) to Revision A (December 2017)	Page
• Deleted the OVP comparator from the block diagram.	9

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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