TEXAS INSTRUMENTS

INA200, INA201, INA202

SBOS374E – NOVEMBER 2006 – REVISED SEPTEMBER 2017

INA20x High-Side Measurement Current-Shunt Monitor With Open-Drain Comparator and Reference

1 Features

- Complete Current Sense Solution
- Three Gain Options Available:
  - INA200 = 20 V/V
  - INA201 = 50 V/V
  - INA202 = 100 V/V
- 0.6-V Internal Voltage Reference
- Internal Open-Drain Comparator
- Latching Capability on Comparator
- Common-Mode Range: –16 V to 80 V
- High Accuracy: 3.5% Maximum Error Over Temperature
- Bandwidth: 500 kHz (INA200)
- Quiescent Current: 1800 μA (Maximum)
- Packages: SOIC-8, VSSOP-8

2 Applications

- Notebook Computers
- Cell Phones
- Telecom Equipment
- Automotive
- Power Management
- Battery Chargers
- Welding Equipment

3 Description

The INA200, INA201, and INA202 devices are high-side current-shunt monitors with voltage output and integrated comparator. The INA20x devices can sense drops across shunts at common-mode voltages from –16 V to 80 V. The INA20x series is available with three output voltage scales: 20 V/V, 50 V/V, and 100 V/V, with a bandwidth up to 500-kHz.

The INA200, INA201, and INA202 devices incorporate an open-drain comparator and internal reference providing a 0.6-V threshold. External dividers set the current trip point. The comparator includes a latching capability, that can be made transparent by grounding (or leaving open) the $\overline{\text{RESET}}$ pin.

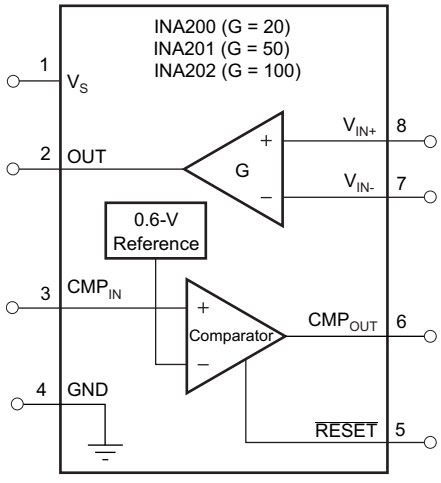
The INA200, INA201, and INA202 devices operate from a single 2.7-V to 18-V supply, drawing a maximum of 1800 μA of supply current. Package options include the very small VSSOP-8 and the SOIC-8. All versions are specified over the extended operating temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA200 INA201 INA202	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2015) to Revision E — **Page**

- Reformatted *Thermal Information* table note ... 4
- Corrected typo in *Voltage Output* section in *Electrical Characteristics* table ... 6
- Added text to *Comparator* subsection in *Feature Description* section ... 14
- Added Figure 31 to *Feature Description* section ... 18
- Added *Output vs Supply Ramp Considerations* subsection in *Feature Description* section ... 23
- Added Figure 36, Figure 37, and Figure 38 ... 23

Changes from Revision C (October 2010) to Revision D — **Page**

- Added *ESD Ratings* table, *Thermal Information* table, Feature Description section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4

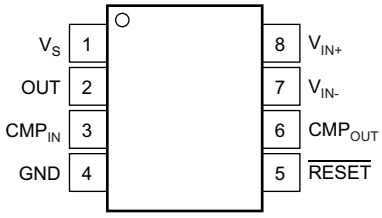
Changes from Revision B (October, 2007) to Revision C — **Page**

- Revised front-page figure ... 1
- Changed title of data sheet ... 1
- Updated document format to current standards ... 1

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5 Pin Configuration and Functions

DGK and D Packages
8-Pin VSSOP and SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CMP_{IN}	3	Analog input	Comparator input
CMP_{OUT}	6	Analog output	Comparator output
GND	4	Analog	Ground
OUT	2	Analog output	Output voltage
$\overline{RESET}$	5	Analog input	Comparator reset pin, active low
V_{IN-}	7	Analog input	Connect to shunt low side
V_{IN+}	8	Analog input	Connect to shunt high side
V_S	1	Analog	Power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S		2.7	18	V
Current-shunt monitor analog inputs, V_{IN+}, V_{IN-}	Differential (V_{IN+}) – (V_{IN-})	–18	18	V
	Common-mode(2)	–16	80	V
Comparator analog input and reset pins(2)		GND – 0.3	(V_S) + 0.3	V
Analog output, OUT(2)		GND – 0.3	(V_S) + 0.3	V
Comparator output, OUT(2)		GND – 0.3	18	V
Input current into any pin(2)			5	mA
Operating temperature		–55	150	°C
Junction temperature		–65	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This voltage may exceed the ratings shown if the current at that pin is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	–16	12	80	V
V_S	Operating supply voltage	2.7	12	18	V
T_A	Operating free-air temperature	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA20x		UNIT
		D (SOIC)	DGK (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.5	162.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.4	37.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.7	82.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.8	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.9	81.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics: Current-Shunt Monitor

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S, and CMP_{IN} = GND, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{SENSE}	Full-scale sense input voltage	$V_{SENSE} = V_{IN+} - V_{IN-}$		0.15	$(V_S - 0.25)$ / Gain	V
V_{CM}	Common-mode input range	T_A = –40°C to 125°C	–16		80	V
CMR	Common-mode rejection	V_{IN+} = –16 V to 80 V	80	100		dB
		V_{IN+} = 12 V to 80 V, T_A = –40°C to 125°C	100	123		dB
V_{OS}	Offset voltage, RTI(1)	T_A = 25°C		±0.5	±2.5	mV
		T_A = 25°C to 125°C			±3	mV
		T_A = –40°C to 25°C			±3.5	mV
dV_{OS}/dT	Offset voltage, RTI, vs temperature	T_{MIN} to T_{MAX}, T_A = –40°C to 125°C		5		µV/°C
PSR	Offset voltage, RTI, vs power supply	V_{OUT} = 2 V, V_{IN+} = 18 V, 2.7 V, T_A = –40°C to 125°C		2.5	100	µV/V
I_B	Input bias current, V_{IN-} pin	T_A = –40°C to 125°C		±9	±16	µA

(1) Offset is extrapolated from measurements of the output at 20-mV and 100-mV V_{SENSE}.

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Electrical Characteristics: Current-Shunt Monitor (continued)

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S, and CMP_{IN} = GND, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT (V_{SENSE} ≥ 20 mV)							
G	Gain	INA200			20		V/V
		INA201			50		V/V
		INA202			100		V/V
	Gain error	V_{SENSE} = 20 mV to 100 mV			±0.2%	±1%	
		V_{SENSE} = 20 mV to 100 mV, T_A = –40°C to 125°C				±2%	
	Total output error(2)	V_{SENSE} = 120 mV, V_S = 16 V			±0.75%	±2.2%	
		V_{SENSE} = 120 mV, V_S = 16 V, T_A = –40°C to 125°C				±3.5%	
	Nonlinearity error(3)	V_{SENSE} = 20 mV to 100 mV			±0.002%		
R_O	Output impedance				1.5		Ω
	Maximum capacitive load	No sustained oscillation			10		nF
OUTPUT (V_{SENSE} < 20 mV)(4)							
	Output	INA200, INA201, INA202	–16 V ≤ V_{CM} < 0 V		300		mV
		INA200	0 V ≤ V_{CM} ≤ V_S, V_S = 5 V			0.4	V
		INA201	0 V ≤ V_{CM} ≤ V_S, V_S = 5 V			1	V
		INA202	0 V ≤ V_{CM} ≤ V_S, V_S = 5 V			2	V
		INA200, INA201, INA202	V_S < V_{CM} ≤ 80 V		300		mV
VOLTAGE OUTPUT(5)							
	Output swing to the positive rail	$V_{IN–}$ = 11 V, V_{IN+} = 12 V, T_A = –40°C to 125°C			(V_s) – 0.15	(V_s) – 0.25	V
	Output swing to GND(6)	$V_{IN–}$ = 0 V, V_{IN+} = –0.5 V, T_A = –40°C to 125°C			(GND) + 0.004	(GND) + 0.05	V
FREQUENCY RESPONSE							
BW	Bandwidth	INA200	C_{LOAD} = 5 pF		500		kHz
		INA201	C_{LOAD} = 5 pF		300		kHz
		INA202	C_{LOAD} = 5 pF		200		kHz
	Phase margin	C_{LOAD} < 10 nF			40		°C
SR	Slew rate				1		V/µs
	Settling time (1%)	V_{SENSE} = 10 mV_{PP} to 100 mV_{PP}, C_{LOAD} = 5 pF			2		µs
NOISE, RTI							
	Voltage noise density				40		nV/√Hz

(2) Total output error includes effects of gain error and V_{OS}.
(3) Linearity is best fit to a straight line.
(4) For details on this region of operation, see *Accuracy Variations* section in *Device Functional Modes*.
(5) See Figure 8.
(6) Specified by design.

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6.6 Electrical Characteristics: Comparator

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, and $R_{PULL-UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
	Threshold	T_A = 25°C	590	608	620	mV
		T_A = –40°C to 125°C	586		625	mV
	Hysteresis(1)	T_A = –40°C to 85°C		–8		mV
INPUT BIAS CURRENT(2)						
	Input bias current, CMP_{in} PIN			0.005	10	nA
	Input bias current, CMP_{in} PIN, vs temperature	T_A = –40°C to 125°C			15	nA
INPUT VOLTAGE RANGE						
	Input voltage range, CMP_{in} PIN		0 V to V_S – 1.5 V			V
OUTPUT (OPEN-DRAIN)						
	Large-signal differential voltage gain	CMP V_{OUT} 1 V to 4 V, R_L ≥ 15 kΩ connected to 5 V		200		V/mV
I_{LKG}	High-level leakage current(3)(4)	V_{ID} = 0.4 V, V_{OH} = V_S		0.0001	1	µA
V_{OL}	Low-level output voltage(3)	V_{ID} = –0.6 V, I_{OL} = 2.35 mA		220	300	mV
RESPONSE TIME						
	Response time(5)	R_L to 5 V, C_L = 15 pF, 100-mV Input Step with 5-mV overdrive		1.3		µs
$\overline{\text{RESET}}$						
	$\overline{\text{RESET}}$ threshold(6)			1.1		V
	Logic input impedance			2		MΩ
	Minimum $\overline{\text{RESET}}$ pulse width			1.5		µs
	$\overline{\text{RESET}}$ propagation delay			3		µs

(1) Hysteresis refers to the threshold (the threshold specification applies to a rising edge of a noninverting input) of a falling edge on the noninverting input of the comparator; refer to Figure 1.
(2) Specified by design.
(3) V_{ID} refers to the differential voltage at the comparator inputs.
(4) Open-drain output can be pulled to the range of 2.7 to 18 V, regardless of V_S.
(5) The comparator response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.
(6) The $\overline{\text{RESET}}$ input has an internal 2 MΩ (typical) pull-down. Leaving $\overline{\text{RESET}}$ open results in a LOW state, with transparent comparator operation.

6.7 Electrical Characteristics: General

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S, and CMP_{IN} = 1 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Operating power supply	T_A = –40°C to 125°C	2.7		18	V
I_Q	Quiescent current	V_{OUT} = 2 V		1350	1800	µA
		V_{SENSE} = 0 mV, T_A = –40°C to 125°C			1850	µA
	Comparator power-on reset threshold(1)			1.5		V
TEMPERATURE						
	Specified temperature		–40		125	°C
	Operating temperature		–55		150	°C
	Storage temperature		–65		150	°C
θ_{JA}	Thermal resistance	VSSOP-8 Surface-Mount		200		°C/W
		SOIC-8		150		°C/W

(1) The INA200, INA201, and INA202 are designed to power-up with the comparator in a defined reset state as long as $\overline{\text{RESET}}$ is open or grounded. The comparator is in reset as long as the power supply is below the voltage shown here. The comparator assumes a state based on the comparator input above this supply voltage. If $\overline{\text{RESET}}$ is high at power-up, the comparator output comes up high and requires a reset to assume a low state, if appropriate.

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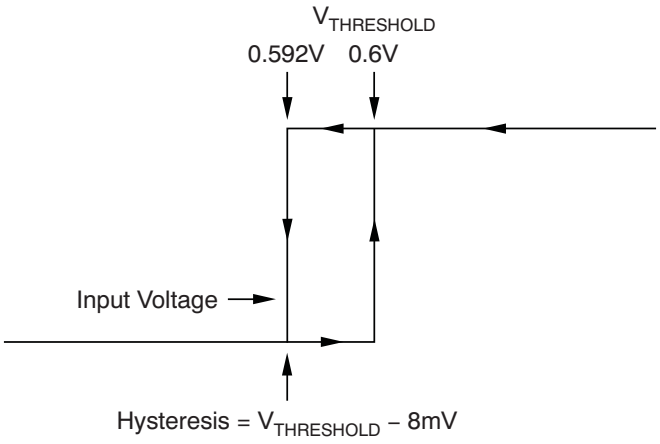


Figure 1. Typical Comparator Hysteresis

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6.8 Typical Characteristics

at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV, (unless otherwise noted)

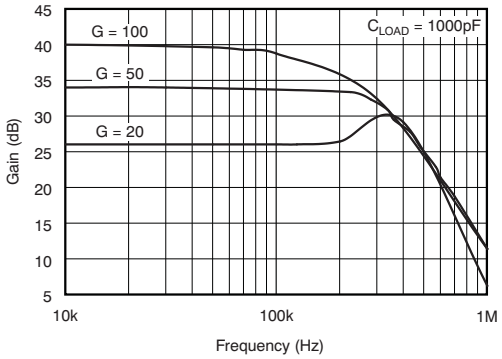


Figure 2. Gain vs Frequency

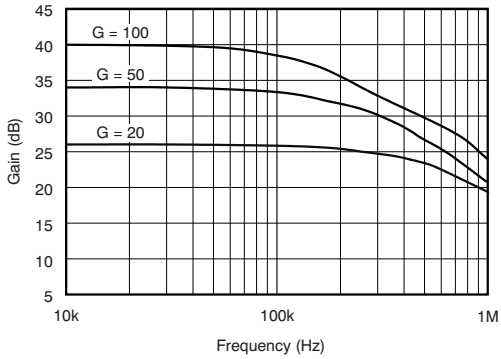


Figure 3. Gain vs Frequency

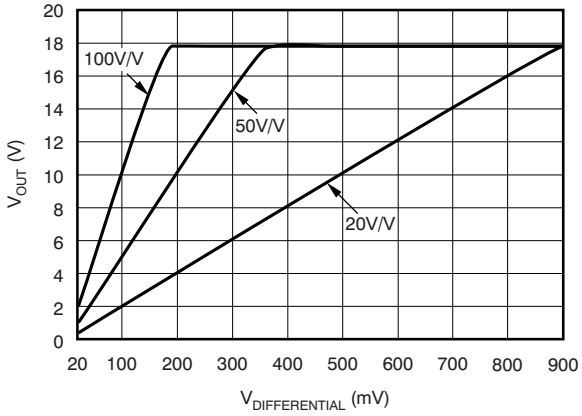


Figure 4. Gain Plot

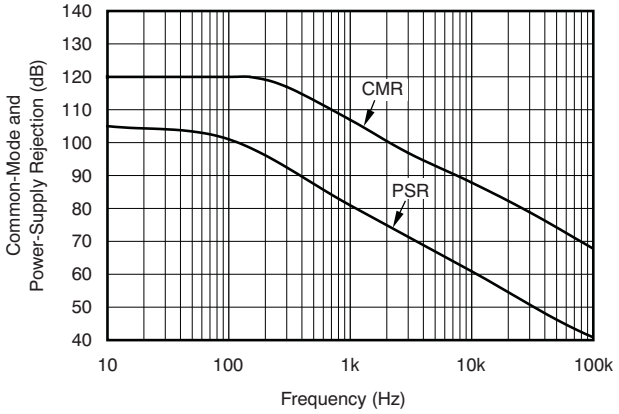


Figure 5. Common-Mode and Power-Supply Rejection vs Frequency

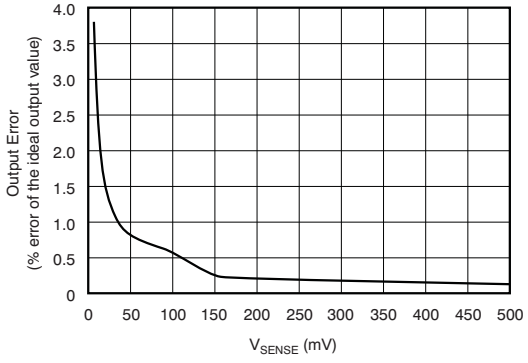


Figure 6. Output Error vs V_{SENSE}

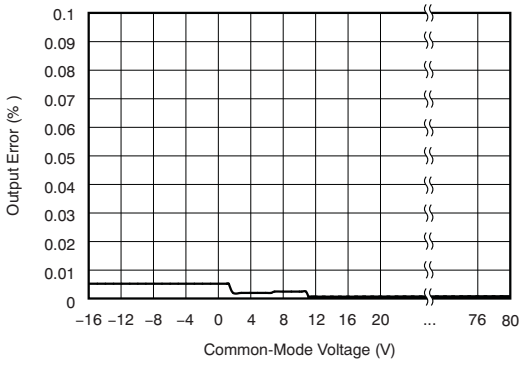


Figure 7. Output Error vs Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV, (unless otherwise noted)

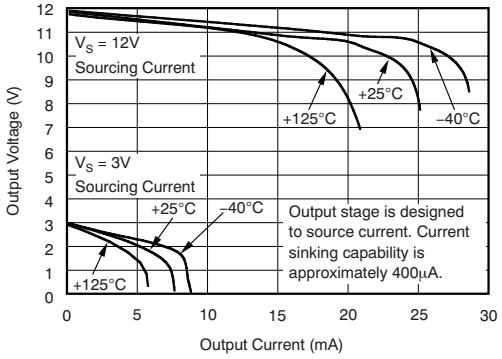


Figure 8. Positive Output Voltage Swing vs Output Current

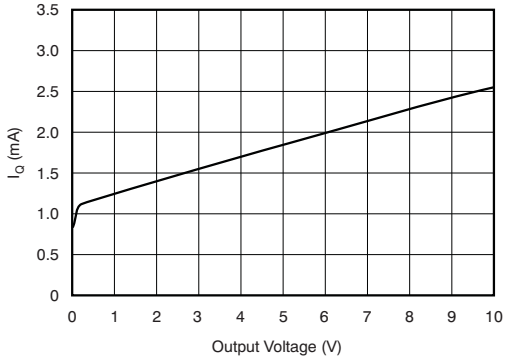


Figure 9. Quiescent Current vs Output Voltage

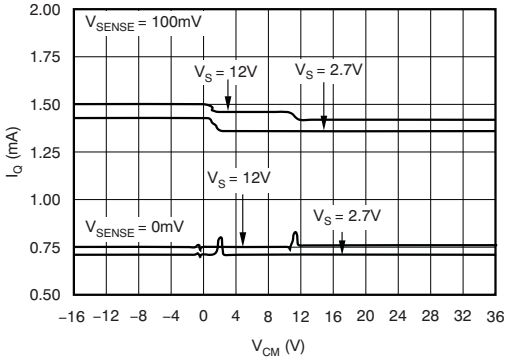


Figure 10. Quiescent Current vs Common-Mode Voltage

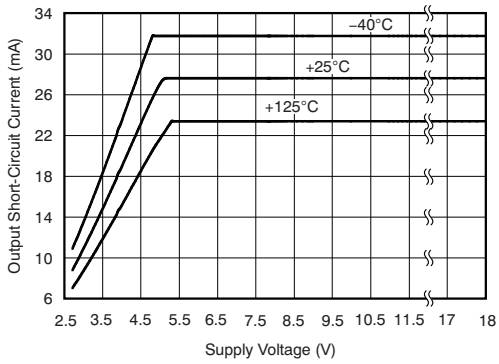


Figure 11. Output Short-Circuit Current vs Supply Voltage

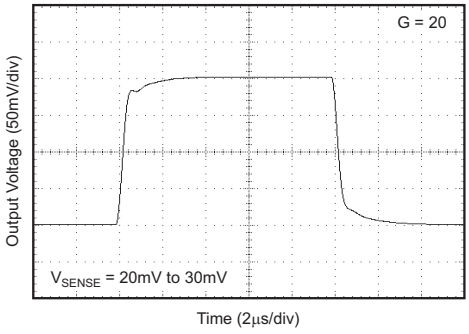


Figure 12. Step Response

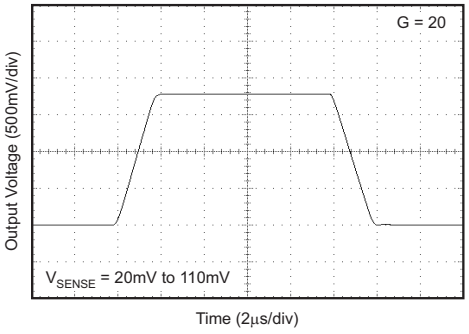


Figure 13. Step Response

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV, (unless otherwise noted)

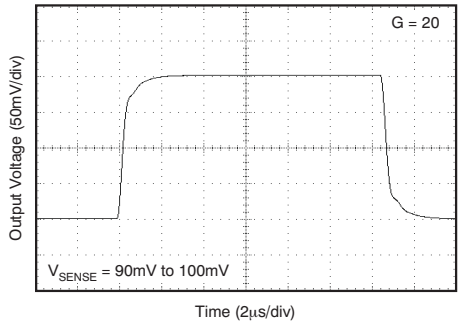


Figure 14. Step Response

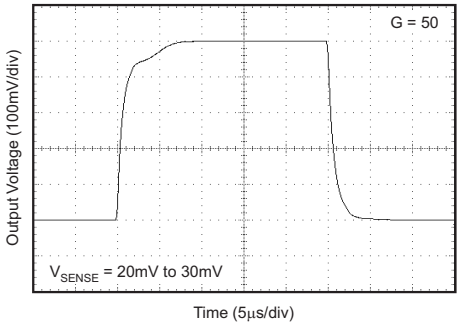


Figure 15. Step Response

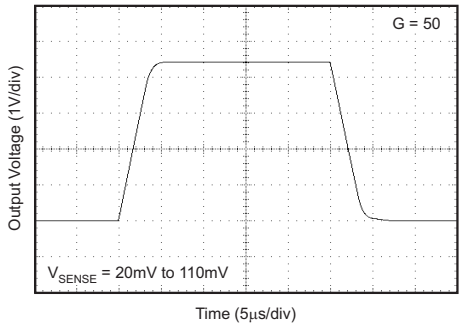


Figure 16. Step Response

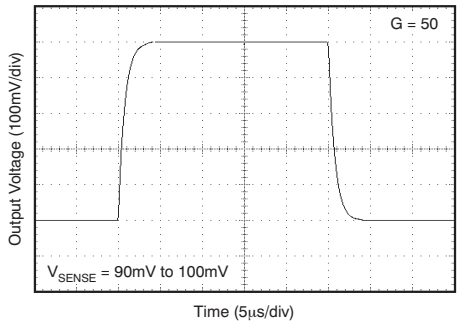


Figure 17. Step Response

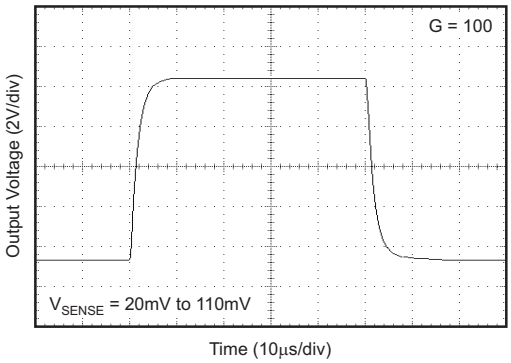


Figure 18. Step Response

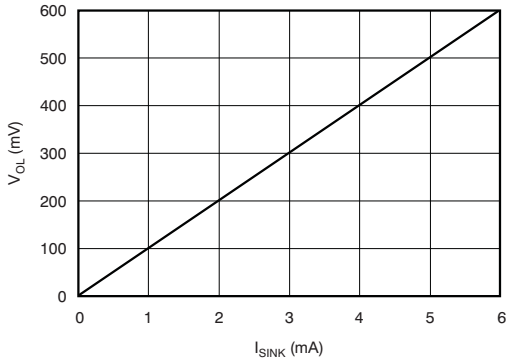


Figure 19. Comparator V_{OL} vs I_{SINK}

Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV, (unless otherwise noted)

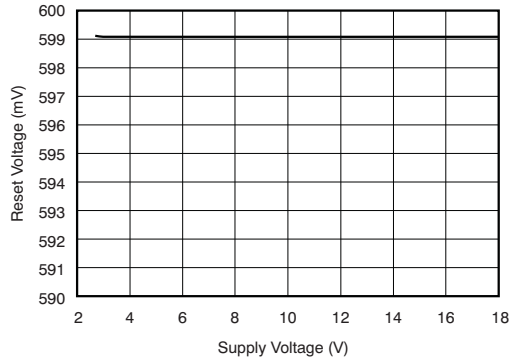


Figure 20. Comparator Trip Point vs Supply Voltage

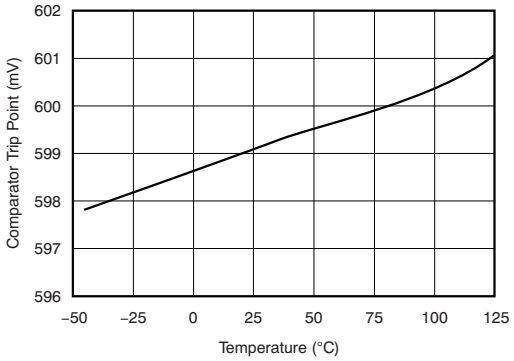


Figure 21. Comparator Trip Point vs Temperature

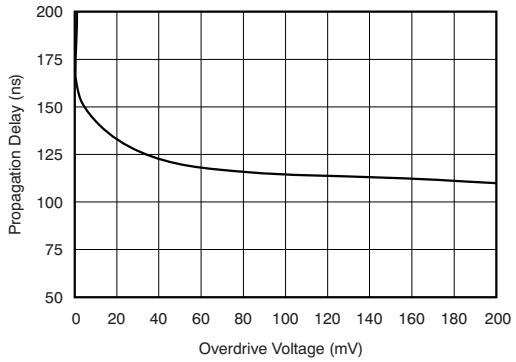


Figure 22. Comparator Propagation Delay vs Overdrive Voltage

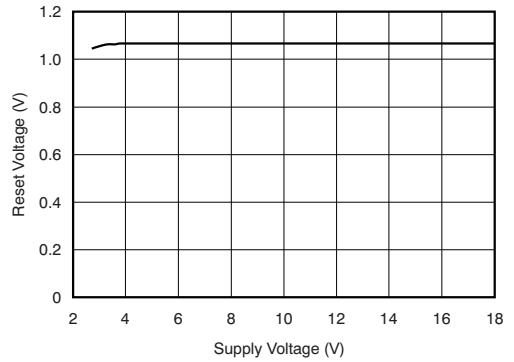


Figure 23. Comparator Reset Voltage vs Supply Voltage

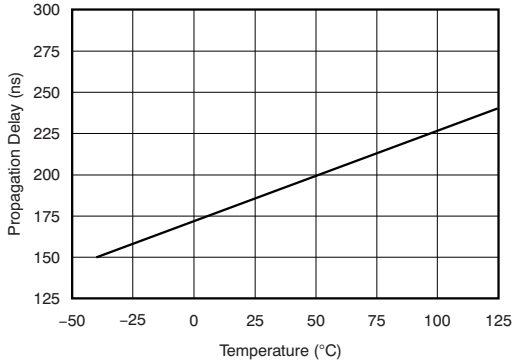


Figure 24. Comparator Propagation Delay vs Temperature

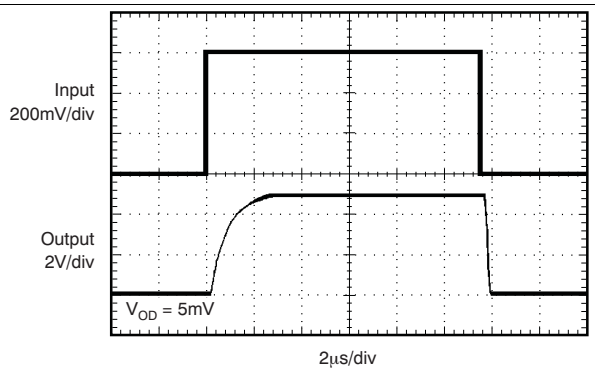


Figure 25. Comparator Propagation Delay

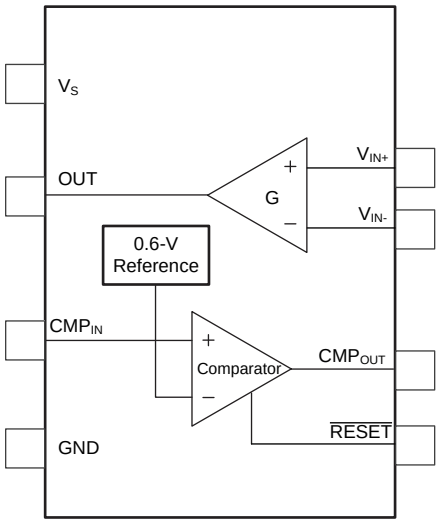
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7 Detailed Description

7.1 Overview

The INA200, INA201, and INA202 devices are high-side current-shunt monitors with voltage output. The INA20x devices can sense drops across shunts at common-mode voltages from –16 V to 80 V. The INA200–INA202 devices are available with three output voltage scales: 20 V/V, 50 V/V, and 100 V/V, with up to 500-kHz bandwidth. The INA200, INA201, and INA202 devices incorporate an open-drain comparator and internal reference providing a 0.6-V threshold. External dividers set the current trip point. The comparator includes a latching capability, that can be made transparent by grounding (or leaving open) the $\overline{\text{RESET}}$ pin. The INA200, INA201, and INA202 devices operate from a single 2.7 to 18-V supply, drawing a maximum of 1800 μA of supply current. Package options include the very small MSOP-8 and the SO-8. All versions are specified over the extended operating temperature range of –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Basic Connections

Figure 26 shows the basic connections of the INA20x devices. The input pins (V_{IN+} and $V_{IN–}$) must be connected as closely as possible with Kelvin connections to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

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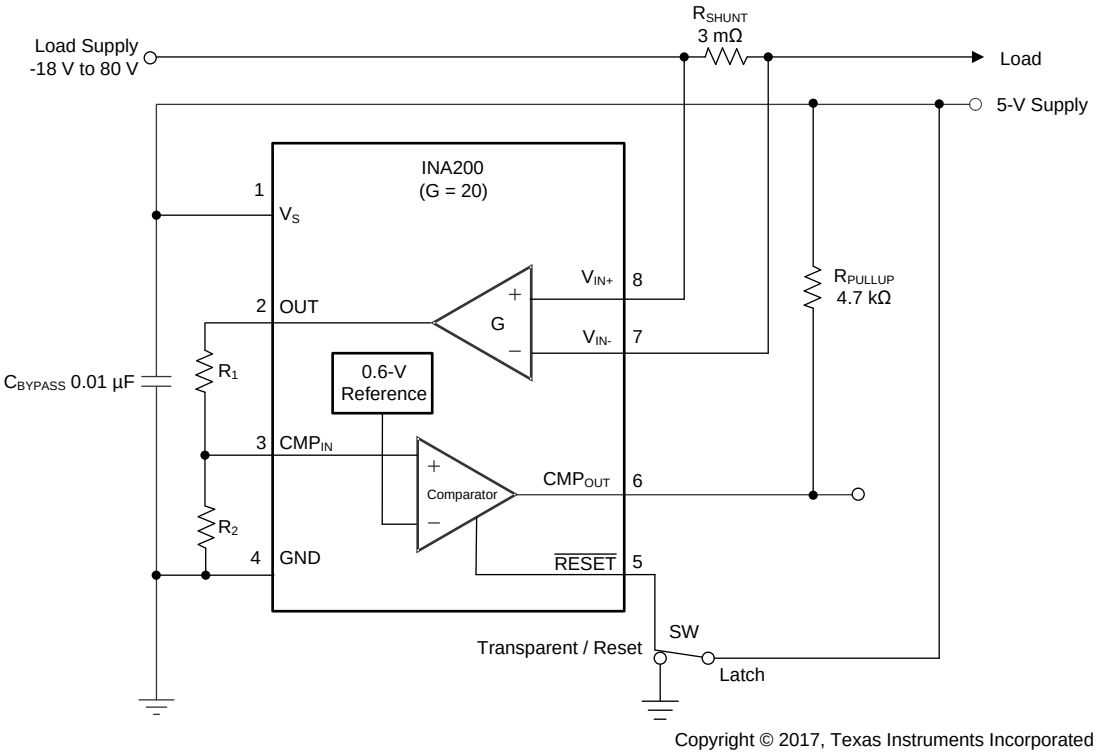


Figure 26. INA200 Basic Connections

7.3.2 Selecting R_S

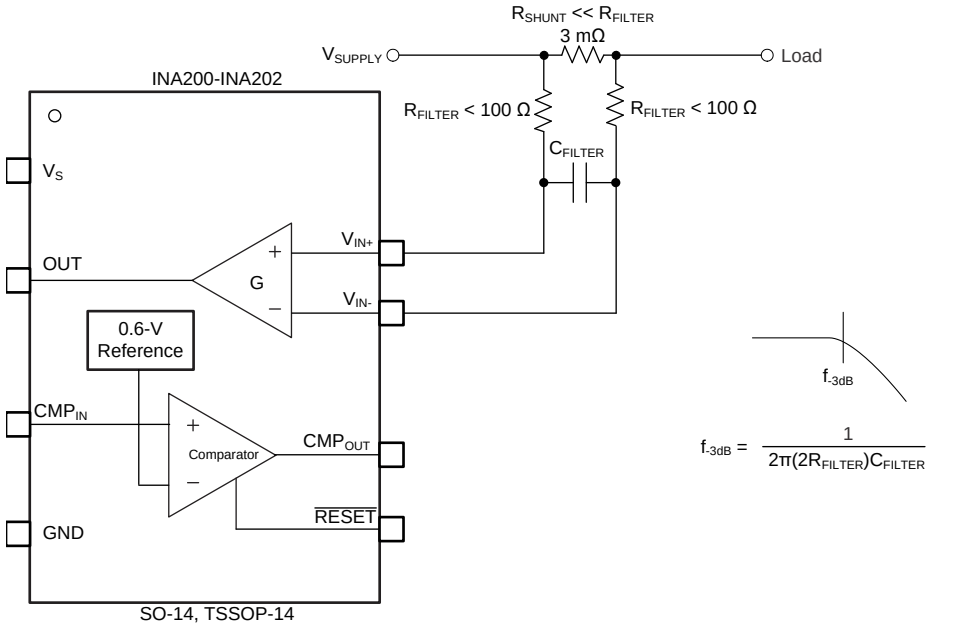
The selected value for the shunt resistor, R_S, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_S provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_S minimize voltage loss in the supply line. For most applications, using an R_S value that provides a full-scale shunt voltage range of 50 mV to 100 mV results in the best performance. Maximum input voltage for accurate measurements is 500 mV, but output voltage is limited by supply.

7.3.3 Comparator

The INA200, INA201, and INA202 devices incorporate an open-drain comparator. This comparator typically has 2 mV of offset and a 1.3-µs (typical) response time. The output of the comparator latches and is reset through the $\overline{\text{RESET}}$ pin; see Figure 28.

When V_s and $\overline{\text{RESET}}$ are different, TI recommends adding a low-pass filter (LPF) on the $\overline{\text{RESET}}$ pin to avoid comparator behavior inconsistent with the data sheet. For instance, with a 12-V supply and a 3.3-V RESET, a rise time of 400 ns is appropriate. Similarly, with an 18-V supply and a 2.7-V RESET, a 1-µs rise time is appropriate; see Figure 31.

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Figure 27. Input Filter (Gain Error: 1.5% to 2.8%)

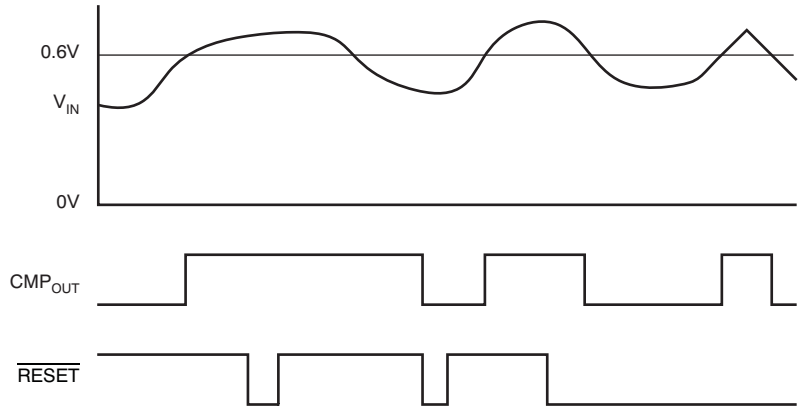
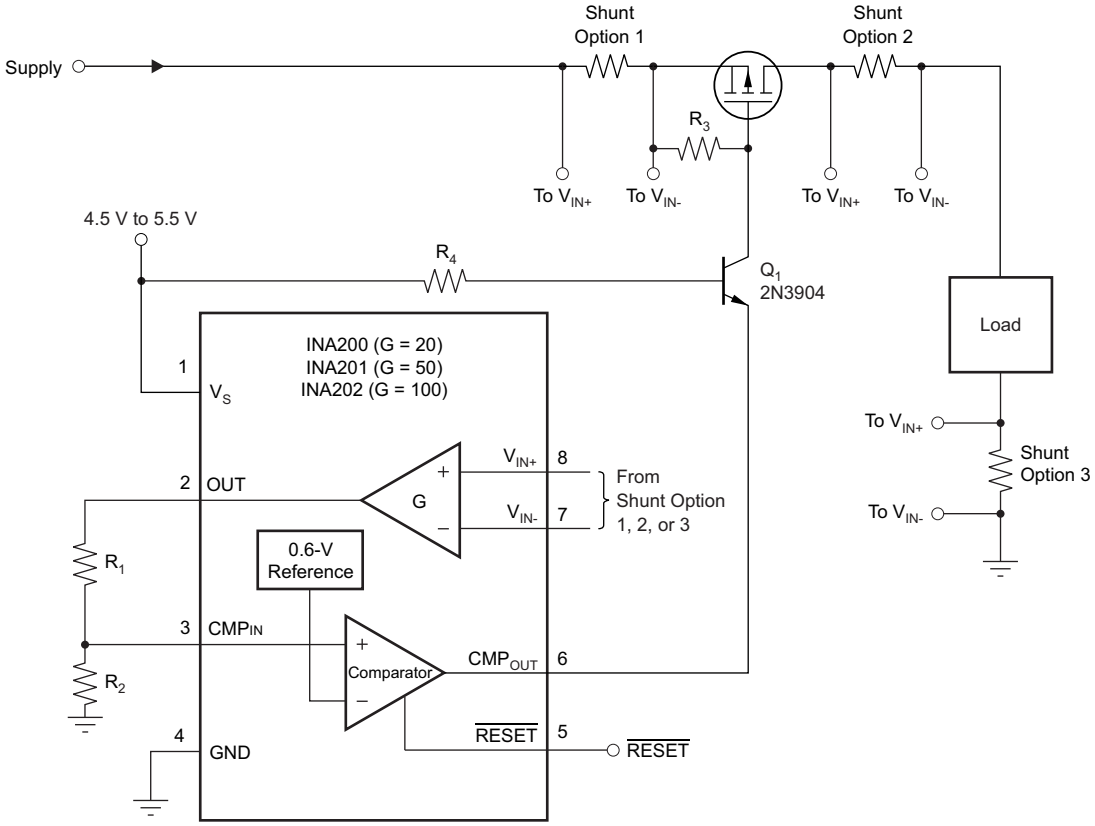


Figure 28. Comparator Latching Capability

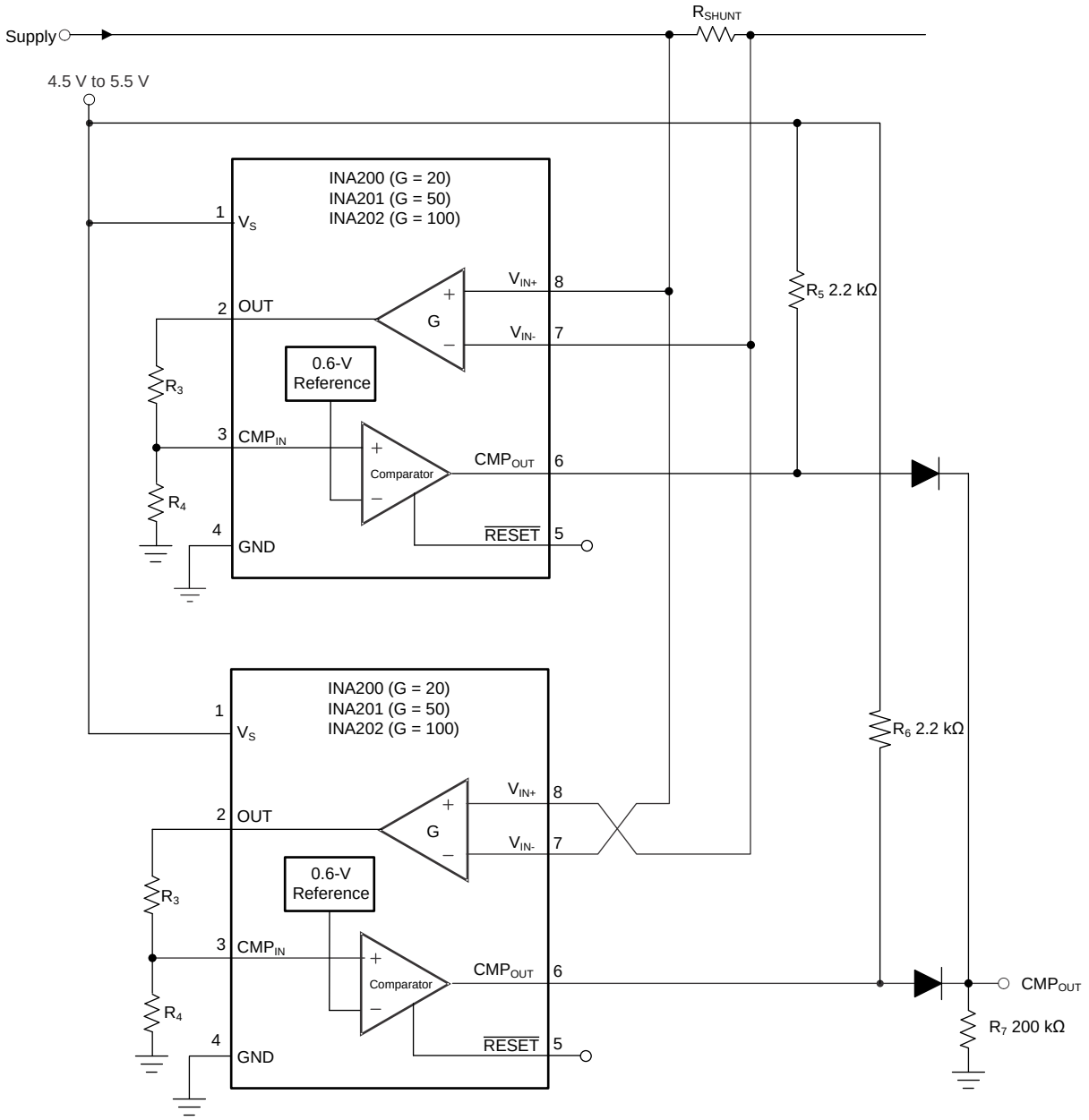


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(1) Q1 cascodes the comparator output to drive a high-side FET (the 2N3904) shown is good up to 60 V. The shunt can be located in any one of the three locations shown. The latching capability must be used in shutdown applications to prevent oscillation at the trip point.

Figure 29. High-Side Switch Overcurrent Shutdown

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(1) It is possible to set different limits for each direction.

Figure 30. Bidirectional Overcurrent Comparator

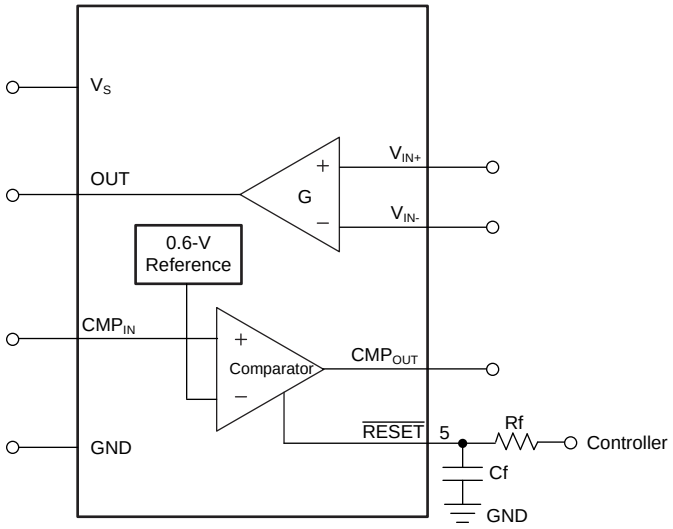


Figure 31. Filter on $\overline{\text{RESET}}$ Pin

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7.4 Device Functional Modes

7.4.1 Input Filtering

An obvious and straightforward location for filtering is at the output of the INA20x series; however, this location negates the advantage of the low output impedance of the internal buffer. The only other option for filtering is at the input pins of the INA20x devices, which is complicated by the internal 5 kΩ + 30% input impedance. This is shown in Figure 27. Using the lowest possible resistor values minimizes the initial shift in gain and effects of tolerance. The effect on initial gain is shown in Equation 1:

$$\text{Gain Error \%} = 100 - \left(100 \times \frac{5\text{k}\Omega}{5\text{k}\Omega + R_{FILT}}\right) \quad (1)$$

Total effect on gain error can be calculated by replacing the 5-kΩ term with 5 kΩ – 30%, (or 3.5 kΩ) or 5 kΩ + 30% (or 6.5 kΩ). The tolerance extremes of R_{FILT} can be inserted into the equation. If a pair of 100-Ω 1% resistors are used on the inputs, the initial gain error equals 1.96%. Worst-case tolerance conditions always occur at the lower excursion of the internal 5-kΩ resistor (3.5 kΩ), and the higher excursion of R_{FILT} – 3% in this case.

The specified accuracy of the INA20x devices must then be combined in addition to these tolerances. While this discussion treated accuracy worst-case conditions by combining the extremes of the resistor values, it is appropriate to use geometric mean or root sum square calculations to total the effects of accuracy variations.

7.4.2 Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage

The accuracy of the INA200, INA201, and INA202 current shunt monitors is a function of two main variables: V_{SENSE} ($V_{IN+} – V_{IN–}$), common-mode voltage, (V_{CM}), relative to the supply voltage (V_S). V_{CM} is expressed as ($V_{IN+} + V_{IN–}$) / 2; however, in practice, V_{CM} is seen as the voltage at V_{IN+} because the voltage drop across V_{SENSE} is typically small.

This section addresses the accuracy of these specific operating regions:

- Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$
- Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$
- Low V_{SENSE} Case 1: $V_{SENSE} < 20$ mV, $–16\text{ V} \leq V_{CM} < 0$
- Low V_{SENSE} Case 2: $V_{SENSE} < 20$ mV, $0\text{ V} \leq V_{CM} \leq V_S$
- Low V_{SENSE} Case 3: $V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

7.4.2.1 Normal Case 1: $V_{SENSE} \geq 20$ mv, $V_{CM} \geq V_S$

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by Equation 2.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100\text{mV} - 20\text{mV}}$$

where

- V_{OUT1} = output voltage with V_{SENSE} = 100 mV
- V_{OUT2} = output voltage with V_{SENSE} = 20 mV (2)

Then the offset voltage is measured at V_{SENSE} = 100 mV, and referred to the input (RTI) of the current shunt monitor, as shown in *Electrical Characteristics: Current-Shunt Monitor*.

$$V_{OS}\text{RTI (Referred-To-Input)} = \left(\frac{V_{OUT1}}{G}\right) - 100\text{mV} \quad (3)$$

In the *Typical Characteristics*, *Figure 7* shows the highest accuracy for the this region of operation. In this plot, V_S = 12 V. For $V_{CM} \geq 12$ V, the output error is at the minimum value. This case creates the $V_{SENSE} \geq 20$-mV output specifications in *Electrical Characteristics: Current-Shunt Monitor* .

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Device Functional Modes (continued)

7.4.2.2 Normal Case 2: $V_{SENSE} \geq 20$ mv, $V_{CM} < V_S$

This region of operation is less accurate than normal case 1 as a result of the common-mode operating area in which the part functions, as shown in the *Figure 7* curve (Figure 7). As noted, for this graph V_S = 12 V; for V_{CM} < 12 V, the output error increases as V_{CM} decreases to less than 12 V, with a typical maximum error of 0.005% at the most negative V_{CM} = –16 V.

7.4.2.3 Low V_{SENSE} Case 1: $V_{SENSE} < 20$ mV, $-16\ V \leq V_{CM} < 0$ and Low V_{SENSE} Case 3: $V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

Although the INA200 family of devices are not designed for accurate operation in these regions, some applications are exposed to these conditions. For example, when monitoring power supplies that are switched on and off while V_S is still applied to the INA20x devices, it is important to know what the behavior of the devices is in these regions.

As V_{SENSE} approaches 0 mV, in these V_{CM} regions, the accuracy of the device output degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of V_{OUT} = 300 mV for V_{SENSE} = 0 mV. As V_{SENSE} approaches 20 mV, V_{OUT} returns to the expected output value with accuracy as shown in *Electrical Characteristics: Current-Shunt Monitor*. Figure 32 shows this effect using the INA202 (gain = 100).

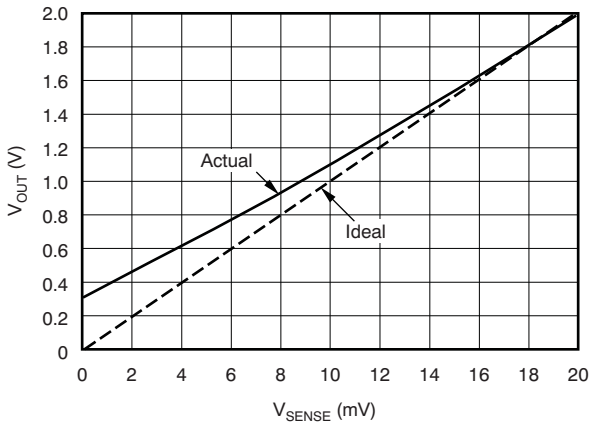


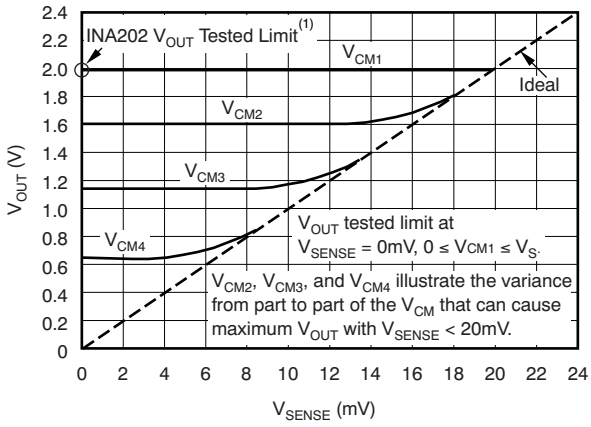
Figure 32. Example For Low V_{SENSE} Cases 1 and 3 (INA202, Gain = 100)

7.4.2.4 Low V_{SENSE} Case 2: $V_{SENSE} < 20$ mV, $0\ V \leq V_{CM} \leq V_S$

This region of operation is the least accurate for the INA20x family. To achieve the wide input common-mode voltage range, these devices use two op amp front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is low. Within this region, V_{OUT} approaches voltages close to linear operation levels for normal case 2. This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0 V. Within this region, as V_{SENSE} approaches 20 mV, device operation is closer to that is described in normal case 2. Figure 33 shows this behavior for the INA202. The V_{OUT} maximum peak for this case is tested by maintaining a constant V_S, setting V_{SENSE} equal to 0 mV and sweeping V_{CM} from 0 V to V_S. The exact V_{CM} at which V_{OUT} peaks during this test varies from device to device, but the V_{OUT} maximum peak is tested to be less than the specified V_{OUT} tested limit.

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Device Functional Modes (continued)



NOTE: (1) INA200 V_{OUT} Tested Limit = 0.4V. INA201 V_{OUT} Tested Limit = 1V.

Figure 33. Example For Low V_{SENSE} Case 2 (INA202, Gain = 100)

7.4.3 Transient Protection

The –16 to 80 V common-mode range of the INA20x devices is ideal for withstanding automotive fault conditions ranging from 12-V battery reversal up to 80-V transients, since no additional protective components are required up to those levels. In the event that the INA20x devices are exposed to transients on the inputs in excess of their ratings, then external transient absorption with semiconductor transient absorbers (such as Zeners) are required. TI does not recommend using MOVs or VDRs, except when they are used in addition to a semiconductor transient absorber. Select the transient absorber so the absorber does not allow the INA20x devices to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance and additional voltage due to transient absorber dynamic impedance). Despite the use of internal Zener-type ESD protection, the INA20x devices do not lend themselves to using external resistors in series with the inputs since the internal gain resistors can vary up to ±30%. (If gain accuracy is not important, then resistors can be added in series with the INA200, INA201, and INA202 inputs with two equal resistors on each input.)

7.4.4 Output Voltage Range

The output of the INA20x devices is accurate within the output voltage swing range set by the power supply pin (V_S.) This performance is best illustrated when using the INA202 (a gain of 100 version), where a 100-mV full-scale input from the shunt resistor requires an output voltage swing of 10 V, and a power-supply voltage sufficient to achieve 10 V on the output.

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8 Application and Implementation

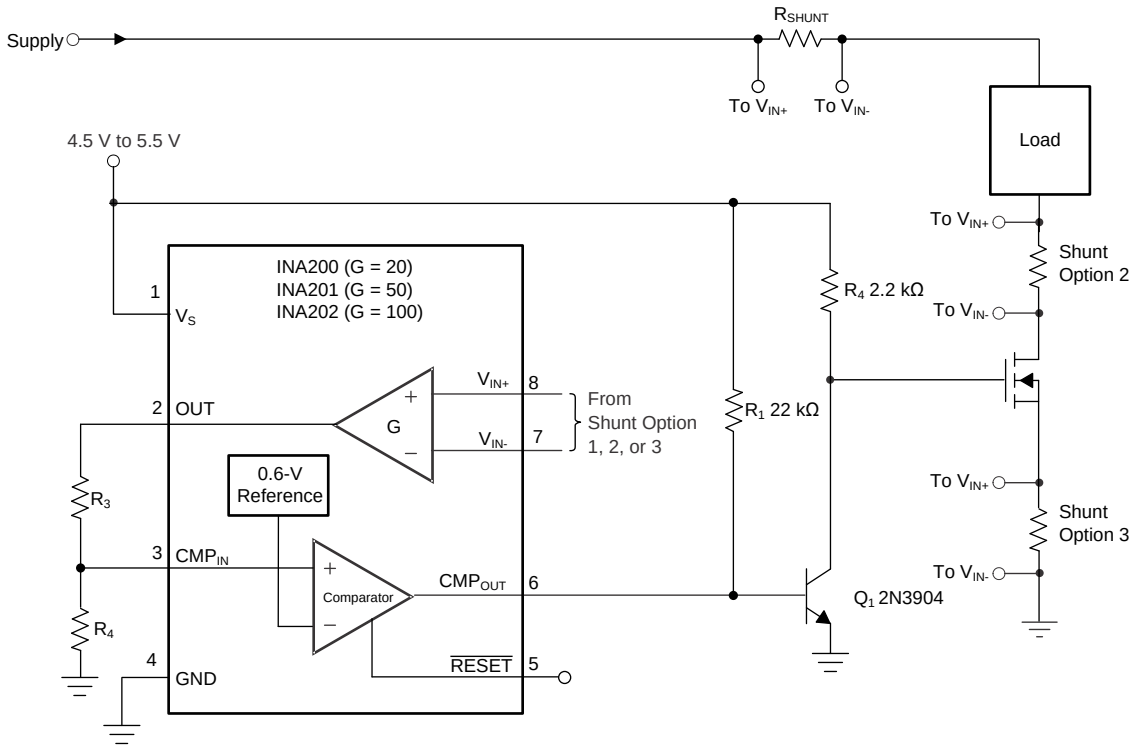
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA20x series is designed to enable simple configuration for detecting overcurrent conditions and current monitoring in an application. This device is individually targeted towards overcurrent detection of a single threshold. However, this device can pair with additional devices and circuitry to create more complex monitoring functional blocks.

8.2 Typical Application



(1) In this case, Q inverts the comparator output.

Figure 34. Low-Side Switch Overcurrent Shutdown

8.2.1 Design Requirements

The device measures current through a resistive shunt with current flowing in one direction that enables detection of an overcurrent event only when the differential input voltage exceeds the threshold limit. When the current reaches the set limit of the divider R_1 / R_2, the output of CMP_{OUT} transitions high, which turns Q1 on, pulls the gate of the pass-FET low, and turns off the flow off current.

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Typical Application (continued)

8.2.2 Detailed Design Procedure

Figure 34 shows the basic connections of the device. The input terminals (IN+ and IN –) must be connected as closely as possible to the current-sensing resistor to minimize any resistance in series with the shunt resistance. Additional resistance between the current-sensing resistor and input terminals results in errors in the measurement. When input current flows through this external input resistance, the voltage developed across the shunt resistor differs from the voltage reaching the input terminals.

Use the gain of the INA20x and shunt value to calculate the OUT voltage for the desired trip current. Configure R1 and R2 so that the current trip point is equal to the 0.6-V reference voltage.

8.2.3 Application Curve

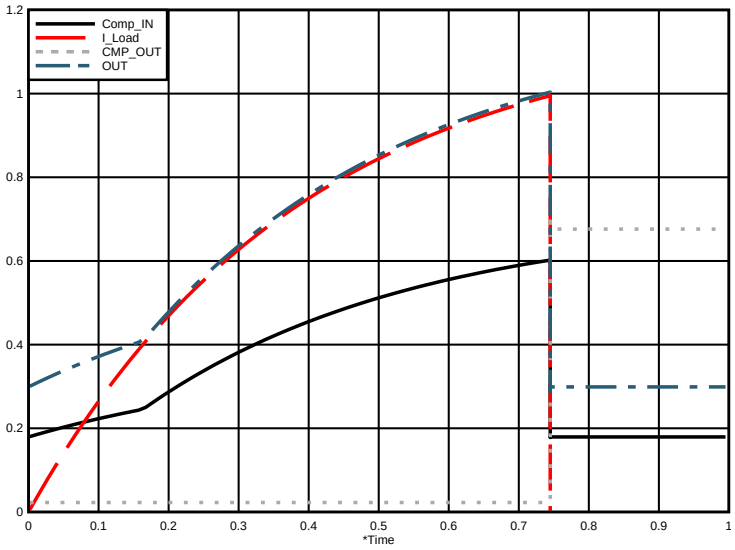


Figure 35. Low-Side Switch Overcurrent Shutdown Response

9 Power Supply Recommendations

The input circuitry of the INA20x devices can accurately measure beyond the power-supply voltage, V_S. For example, the V_S power supply is 5 V, whereas the load power-supply voltage is up to 80 V. However, the output voltage range of the OUT pin is limited by the voltages on the power supply pin.

9.1 Output vs Supply Ramp Considerations

Figure 36, Figure 37, and Figure 38 show the typical output voltages for high and low-side configurations with the given ramp supply voltage. These fluctuations on the output during power-up may require a controller to incorporate a blanking time to disregard the artifacts.

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Output vs Supply Ramp Considerations (continued)

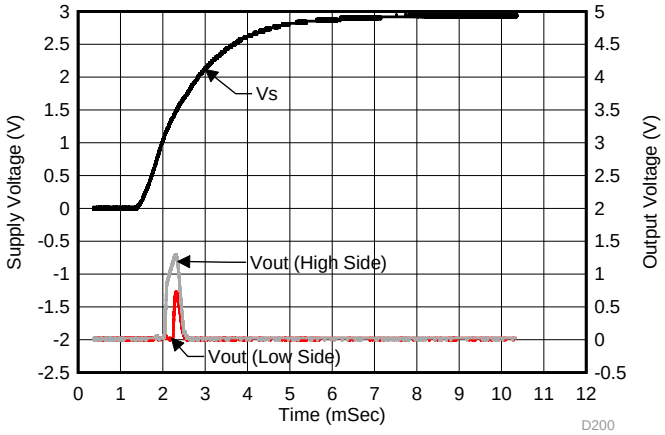


Figure 36. Analog Output vs Supply Ramp (INA200)

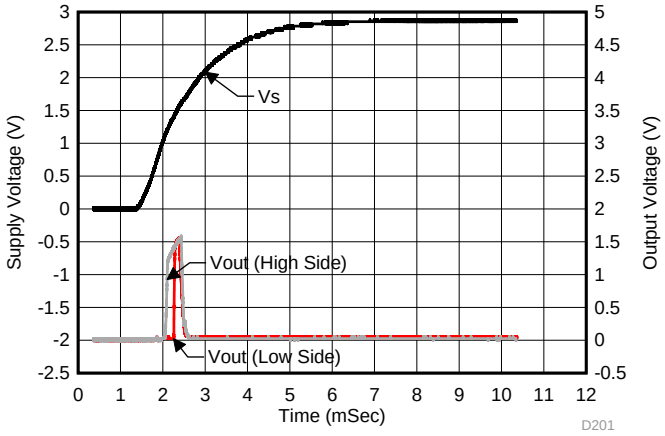


Figure 37. Analog Output vs Supply Ramp (INA201)

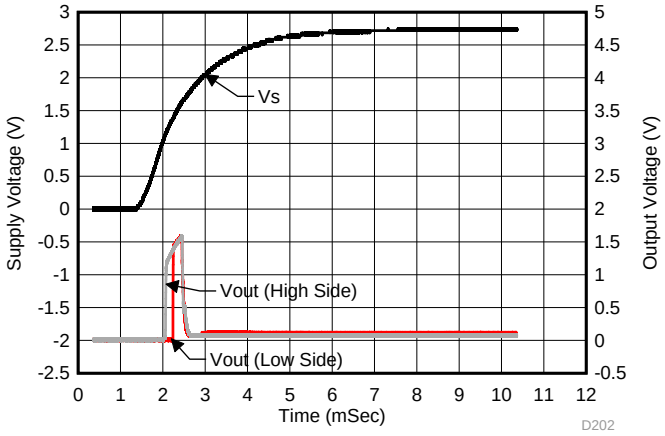


Figure 38. Analog Output vs Supply Ramp (INA202)

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10 Layout

10.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very-low-ohmic value of the current resistor, any additional high-current carrying impedance causes significant measurement errors.
- The power-supply bypass capacitor must be placed as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 μF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

10.2 Layout Example

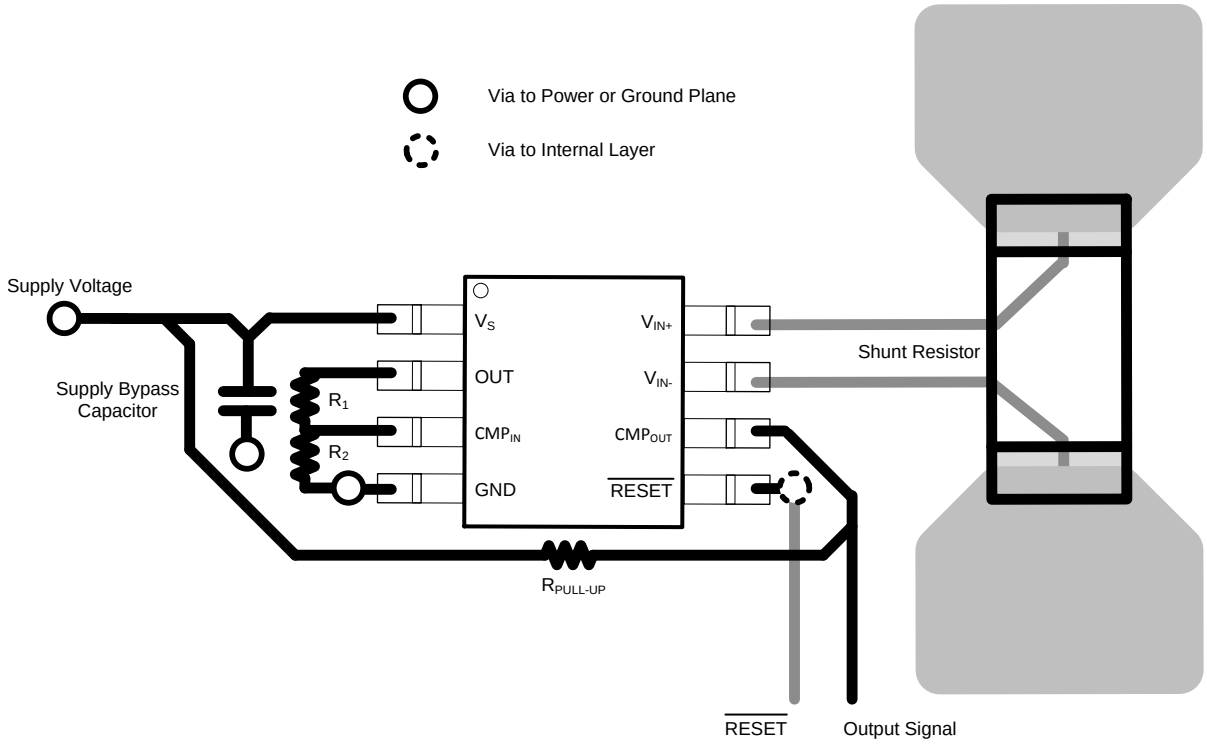


Figure 39. INA20x Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA200	Click here	Click here	Click here	Click here	Click here
INA201	Click here	Click here	Click here	Click here	Click here
INA202	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA200AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 200A	Samples
INA200AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BQH	Samples
INA200AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BQH	Samples
INA200AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 200A	Samples
INA201AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 201A	Samples
INA201AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | NIPDAUAG | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQJ	Samples
INA201AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI | NIPDAUAG | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQJ	Samples
INA201AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 201A	Samples
INA202AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 202A	Samples
INA202AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQL	Samples
INA202AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI | NIPDAUAG | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQL	Samples
INA202AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 202A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA200, INA201, INA202 :

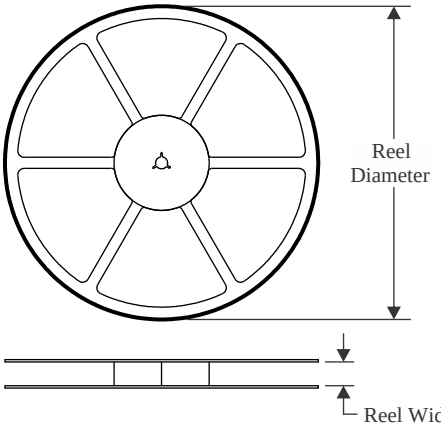
- Automotive : INA200-Q1, INA201-Q1, INA202-Q1

NOTE: Qualified Version Definitions:

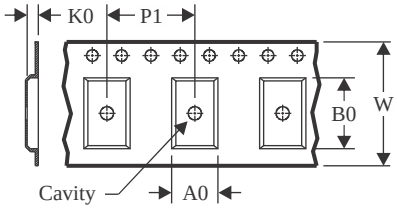
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

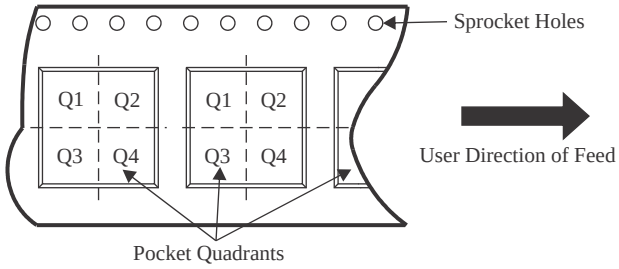


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

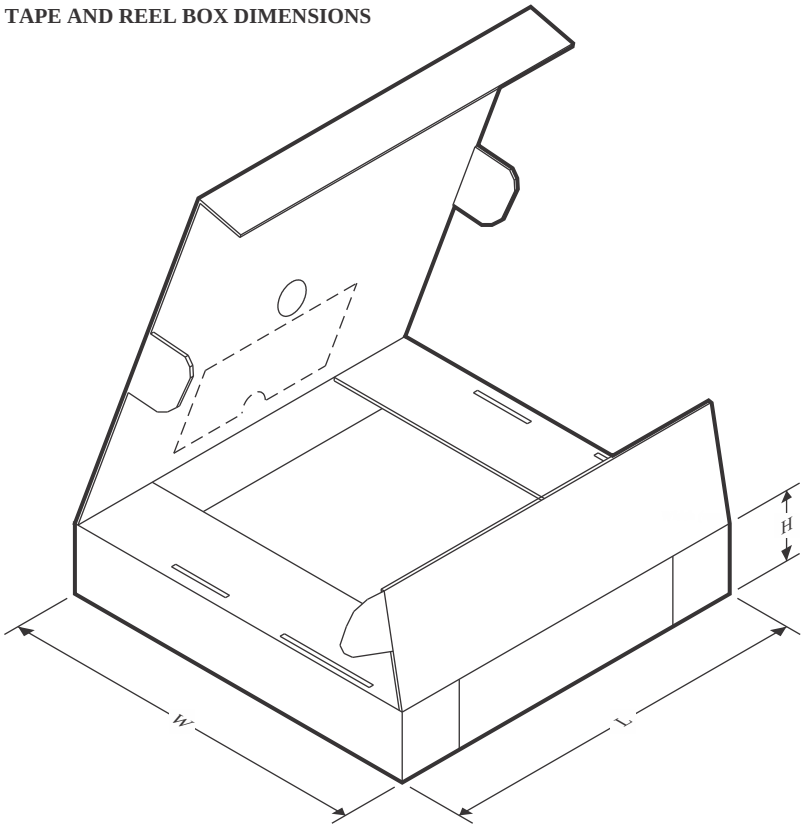
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA200AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA200AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA200AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA201AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA201AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA201AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA201AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA202AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA202AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA202AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

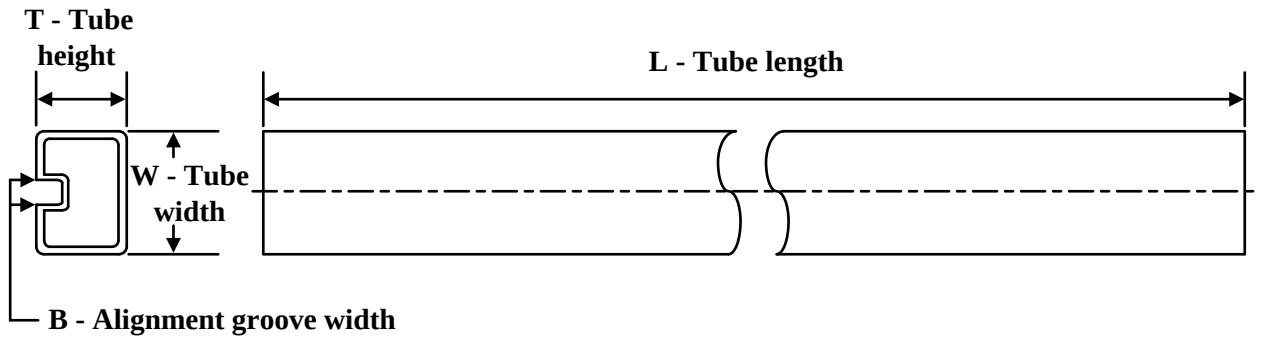
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

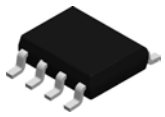
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA200AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA200AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA200AIDR	SOIC	D	8	2500	367.0	367.0	35.0
INA201AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA201AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
INA201AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA201AIDR	SOIC	D	8	2500	356.0	356.0	35.0
INA202AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
INA202AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA202AIDR	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA200AID	D	SOIC	8	75	506.6	8	3940	4.32
INA201AID	D	SOIC	8	75	506.6	8	3940	4.32
INA202AID	D	SOIC	8	75	506.6	8	3940	4.32

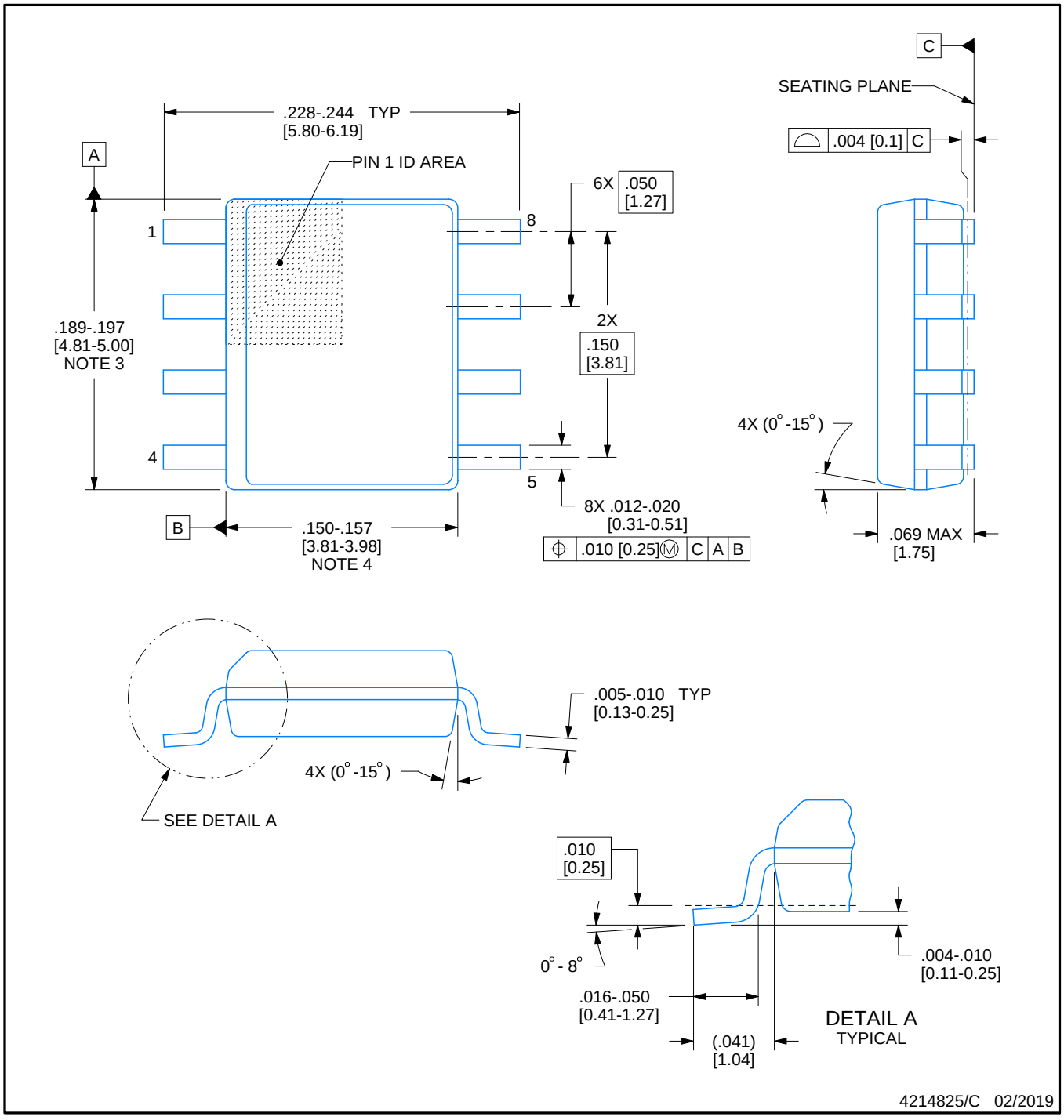


PACKAGE OUTLINE

D0008A

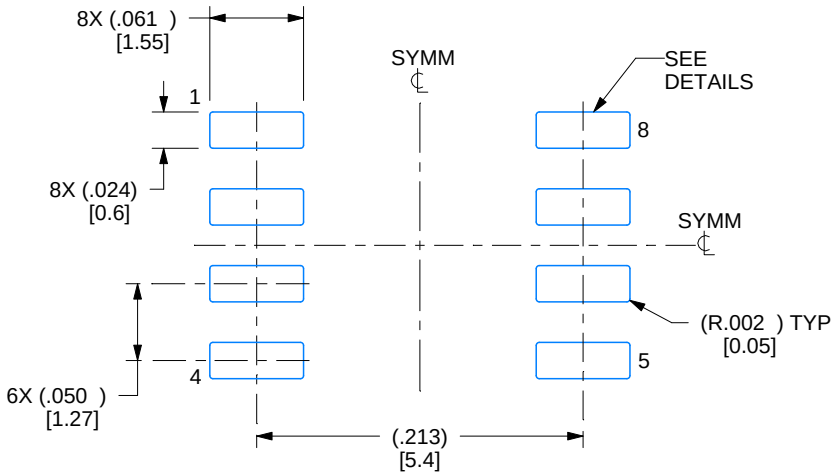
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

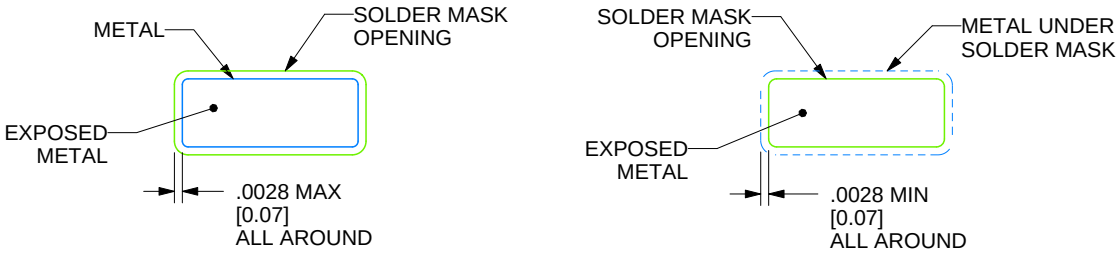


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

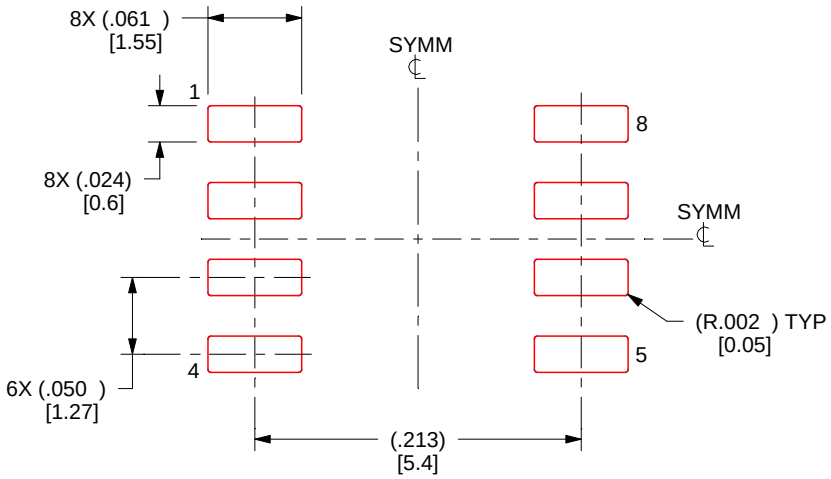
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



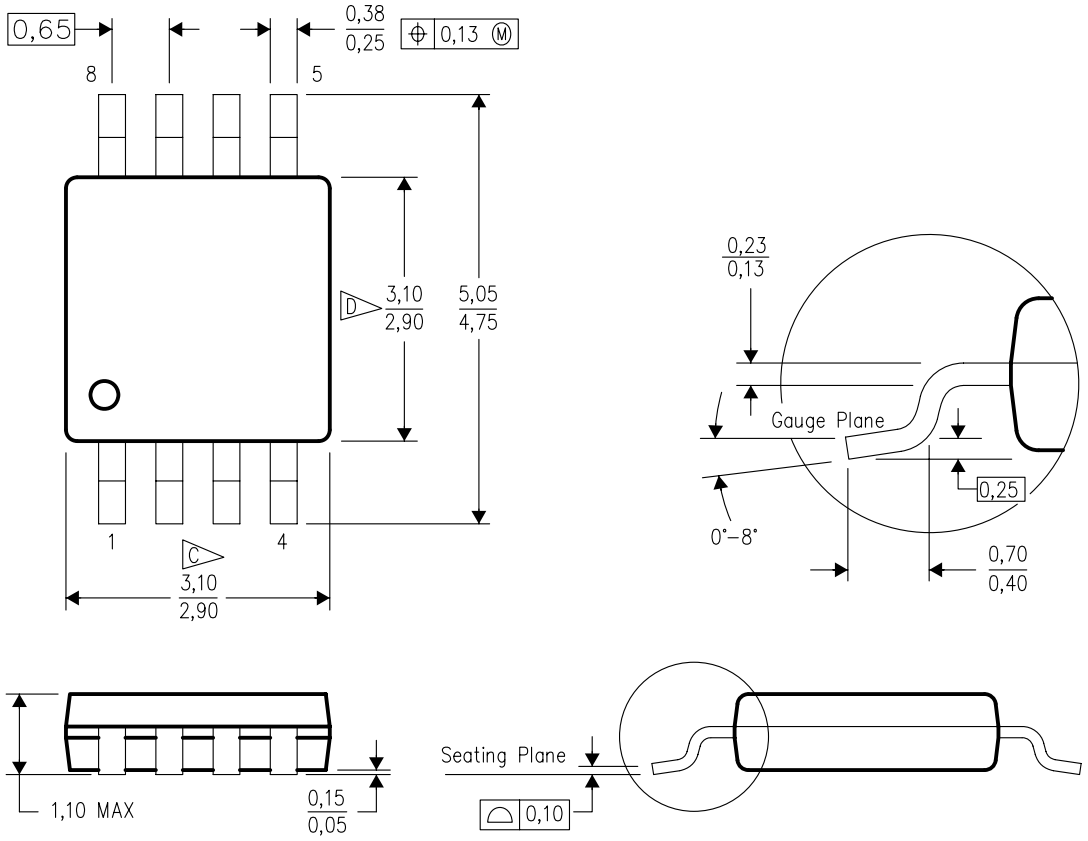
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

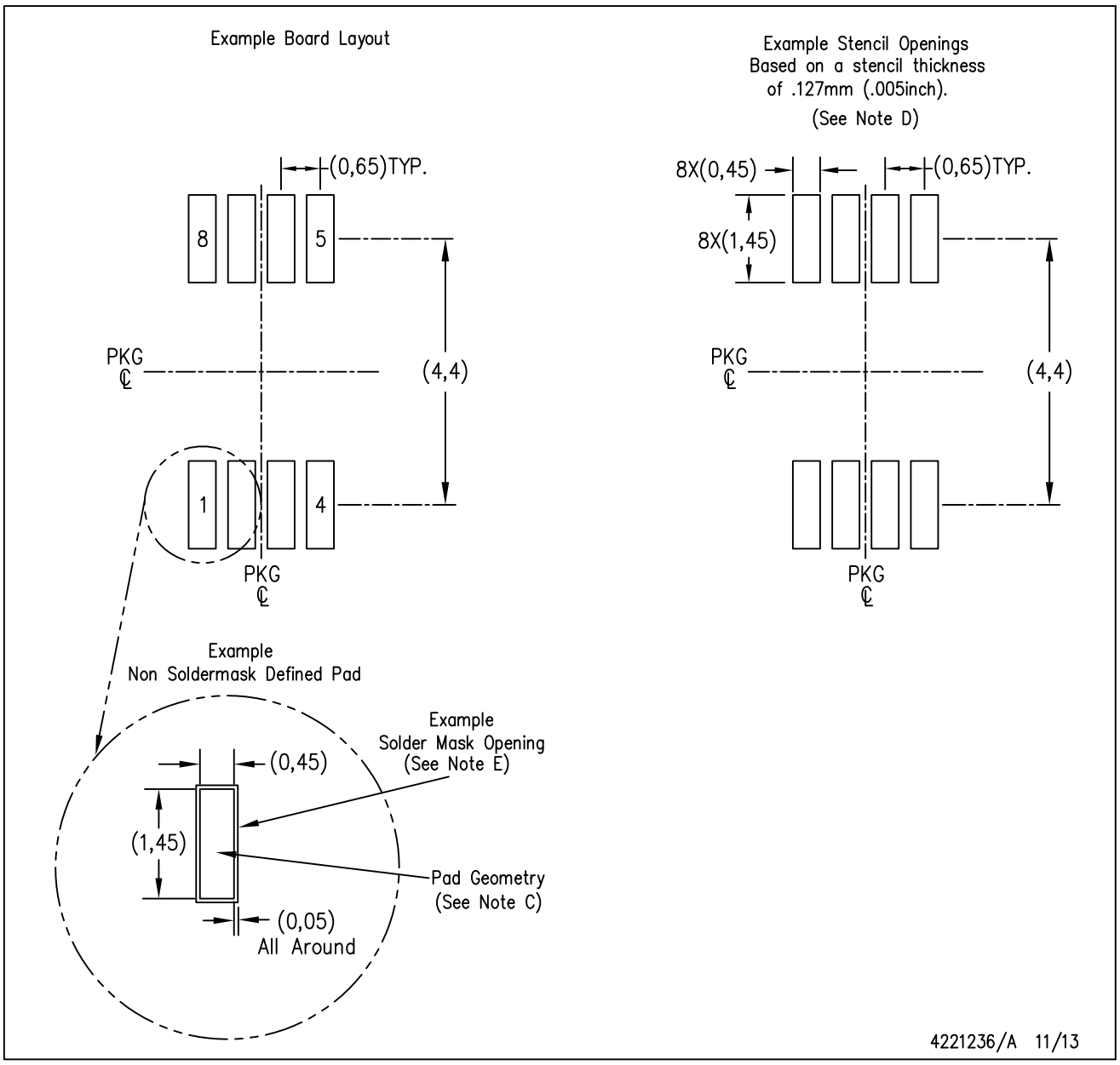
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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