AM273x Sitara™ Microcontrollers

1 Features

Processor Cores:

- Dual-core Arm® Cortex®-R5F MCU subsystem operating up to 400 MHz, highly-integrated for real-time processing
  - Dual-core Arm® Cortex®-R5F cluster supports dual-core and single-core operation
  - 32KB I-Cache and 32KB D-Cache per R5F core with SECDED ECC on all memories
  - Single-core: 128KB TCM per cluster (128KB TCM per R5F core)
  - Dual-core: 128KB TCM per cluster (64KB TCM per R5F core)
- C66x DSP core
  - Single core, 32-bit, floating point DSP
  - Operating at 450 MHz (14.4 GMAC)

Memory subsystem:

- Up to 5.0 MB On Chip RAM (OCSRAM)
  - Memory space sharable between DSP, MCU, and shared L3
  - 3.5625MB shared L3 memory
  - 960KB dedicated to Main subsystem
  - 384KB dedicated to DSP subsystem
- External Memory Interfaces (EMIF)
  - QSPI interface operating up to 67 MHz

System on Chip (SoC) Services and Architecture:

- 12x EDMA for various subsystems, MCU, DSP and Accelerator cores
- 5x Real-Time Interrupt (RTI) modules
- Mailbox system for Interprocessor Communication (IPC)
- JTAG/Trace interfaces for device debugging
- Clock source
  - 40.0 MHz crystal with internal oscillator
  - Supports external oscillator at 40/50 MHz
  - Supports externally driven clock (Square/Sine) at 40/50 MHz

High-speed Serial Interfaces:

- 10/100 Mbps Ethernet (RGMII/RMII/MII)
- Input: 2x 4-lane MIPI D-PHY CSI 2.0 Data
- Output: 4-lane Aurora/LVDS

General Connectivity Peripherals:

- General Purpose Analog to Digital Converters (GPADC)
  - 1x 9-channel ADC supporting up to 625 Ksps
- Digital Connectivity
  - 4x Serial Peripheral Interface (SPI) controllers operating up to 25 MHz
  - 3x Inter-Integrated Circuit (I2C) ports
  - 4x Universal Asynchronous Receiver-Transmitters (UART)
  - 3x Multi-channel Audio Serail Port (McASP)
  - Audio Tracking Logic (ATL)

Industrial and control interfaces:

- 3x Enhanced Pulse-Width Modulator (ePWM)
- 1x Enhanced Capture Module (eCAP)
- 2x Modular Controller Area Network (MCAN) modules with CAN-FD support

Power Management:

- Recommend LP87745-Q1 Power Management ICs (PMIC)
- Simplified power sequencing and reduced number of power supply rails
- Dual voltage digital I/O supporting 3.3V and 1.8V operation

Security:

- Device Security
  - Programmable embedded Hardware Security Module (HSM)
  - Secure authenticated and encrypted boot support
  - Customer programmable root keys, symmetric keys (256 bit), Asymmetric keys (up to RSA-4K or ECC-512) with Key revocation capability
  - Crypto hardware accelerators - PKA with ECC, AES (up to 256 bit), TRNG/DRBG

Functional Safety:

- Functional Safety Quality Managed
  - Documentation will be available to aid ISO 26262 functional safety system design
- AEC-Q100 Qualified
- Operating Conditions
  - Extended automotive grade temperature range supported
  - Extended industrial grade temperature range supported

Package options:

- ZCE (285-pin) nFBGA package 13mm x 13mm, 0.65 mm pitch
- NZN (225-pin) nFBGA package 13mm x 13mm, 0.80 mm pitch

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

2 Applications

- Robotics
- Factory automation safety guards
- Building automation
- Automotive audio
- Traffic monitoring
- Machine vision
- Avionics
- Industrial transport

3 Description

The AM273x family of microcontrollers are highly-integrated, high-performance microcontrollers based on the Arm Cortex-R5F and a C66x floating-point DSP cores. The device enables original equipment manufacturers (OEM) and original design manufacturers (ODM) to quickly bring to market devices with robust software support, rich user interfaces, and high performance. The device offers the maximum flexibility of a fully integrated, mixed processor design.

With an integrated Hardware Security Module (HSM), functional safety support built in, large, integrated RAM on die, and a wide temperature range, the AM273x offers a safe, secure and cost effective design for many industrial and automotive applications.

The AM273x device is provided as part of a complete platform including hardware reference designs, software drivers, DSP library, sample software configurations/applications, API guide, and user documentation.

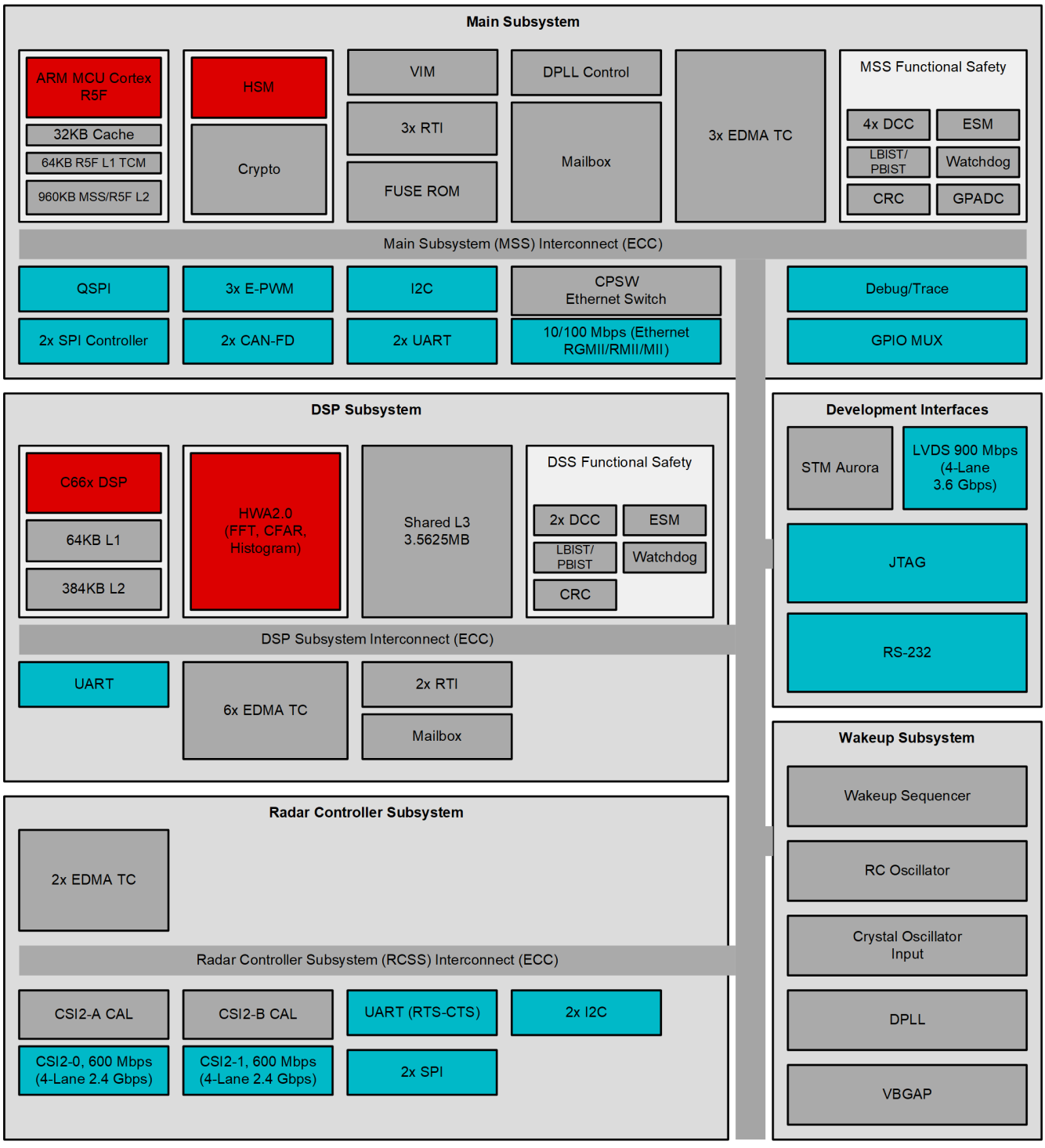
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE
AM2732ADRFGAZCER	285-Pin NFBGA	13.0 mm x 13.0 mm
AM2732CDRFHAZCER	285-Pin NFBGA	13.0 mm x 13.0 mm
AM2732ADRFGQZCERQ1	285-Pin NFBGA	13.0 mm x 13.0 mm
AM2732CDRFHQZCERQ1	285-Pin NFBGA	13.0 mm x 13.0 mm
AM2732CMSFHQNZNRQ1	225-Pin NFBGA	13.0 mm x 13.0 mm
AM2731CLSFHQNZNRQ1	225-Pin NFBGA	13.0 mm x 13.0 mm
AM2731CASFHQNZNRQ1	225-Pin NFBGA	13.0 mm x 13.0 mm
AM2731CNSFHQNZNRQ1	225-Pin NFBGA	13.0 mm x 13.0 mm

(1) For more information, see Section 11.

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3.1 Functional Block Diagram



Denotes associated peripheral interface

Note: For additional information on supported subsystems and peripherals please see the device comparison table in the datasheet.

Figure 3-1. AM273x Functional Block Diagram

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4 Device Comparison

Table 4-1. Device Comparison

FUNCTION	AM2732	AM2732-Q1	AM2731	AM2731-Q1
On-chip memory	Up to 3.5625 MB		Up to 2 MB	
PROCESSORS				
MCU Arm Cortex (R5F)	2x		1x	
DSP (C66x)	1x			
RADAR FEATURES				
Hardware Accelerator 2.0	Yes			
PERIPHERALS				
Ethernet Interface RGMII, RMII, MII (10/100 ONLY)	Yes			
Serial Peripheral Interface (SPI) ports	4			
Quad Serial Peripheral Interface (QSPI)	1			
Inter-Integrated Circuit (I^2C) Interface	3			
Modular Controller Area Network (MCAN) modules with CAN-FD	2			
Universal Asynchronous Receiver-Transmitters (UART)	4			
Enhanced Pulse-Width Modulator (ePWM)	3			
Enhanced Capture Module (eCAP)	Yes			
MCASP	3x			
Hardware in Loop (HIL/DMM)	Yes			
General Purpose ADC (9 Channels)	Yes			
4-lane Aurora/LVDS Debug(1)	Yes		No	
4-lane MIPI D-PHY CSI2.0 Receiver (CSI2_RX0 and CSI2_RX1)(1)	2x		No	
JTAG/Trace	Yes			
Package(2)	ZCE, NZN		NZN	
Junction Temperature(3)	Extended Industrial -40 C to 105 C			
	Extended Automotive -40 C to 140 C			

(1) Only available in ZCE package variants
(2) Supports Features R in Table 9-1
(3) See the Section 6.1

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4.1 Related Products

Sitara™ processors Broad family of scalable processors based on Arm® Cortex® cores with flexible accelerators, peripherals, connectivity and unified software support – perfect for sensors to servers. Sitara™ processors have the reliability needed for use in industrial applications.

AM273x Sitara™ microcontrollers AM273x microcontrollers enable industrial Ethernet networks, robust operation with extensive ECC on memories, and enhanced security features.

Sitara™ processors - Evaluation Modules TI provides Evaluation Modules (EVM) are also provided to help kick-start product development. See the AM273x GP EVM for more information.

Products to complete your design Review products that are frequently purchased or used in conjunction with this product to complete your design. See the following:

- 4x 5-A (20-A) multiphase buck converter PMIC with functional safety features for automotive SoCs LP87745-Q1
- Extended temperature, robust low-latency gigabit Ethernet PHY transceiver DP83867E
- Automotive high-speed CAN transceiver TCAN1044-Q1

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5 Terminal Configuration and Functions

5.1 Pin Diagram

Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

The diagrams in this section are used in conjunction with the other Terminal Configuration and Functions tables to locate signal names and ball grid numbers.

5.1.1 AM273x ZCE Pin Diagram

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Figure 5-1 shows the ball locations for the 285-ball NanoFree™ ball grid array (NFBGA) package.

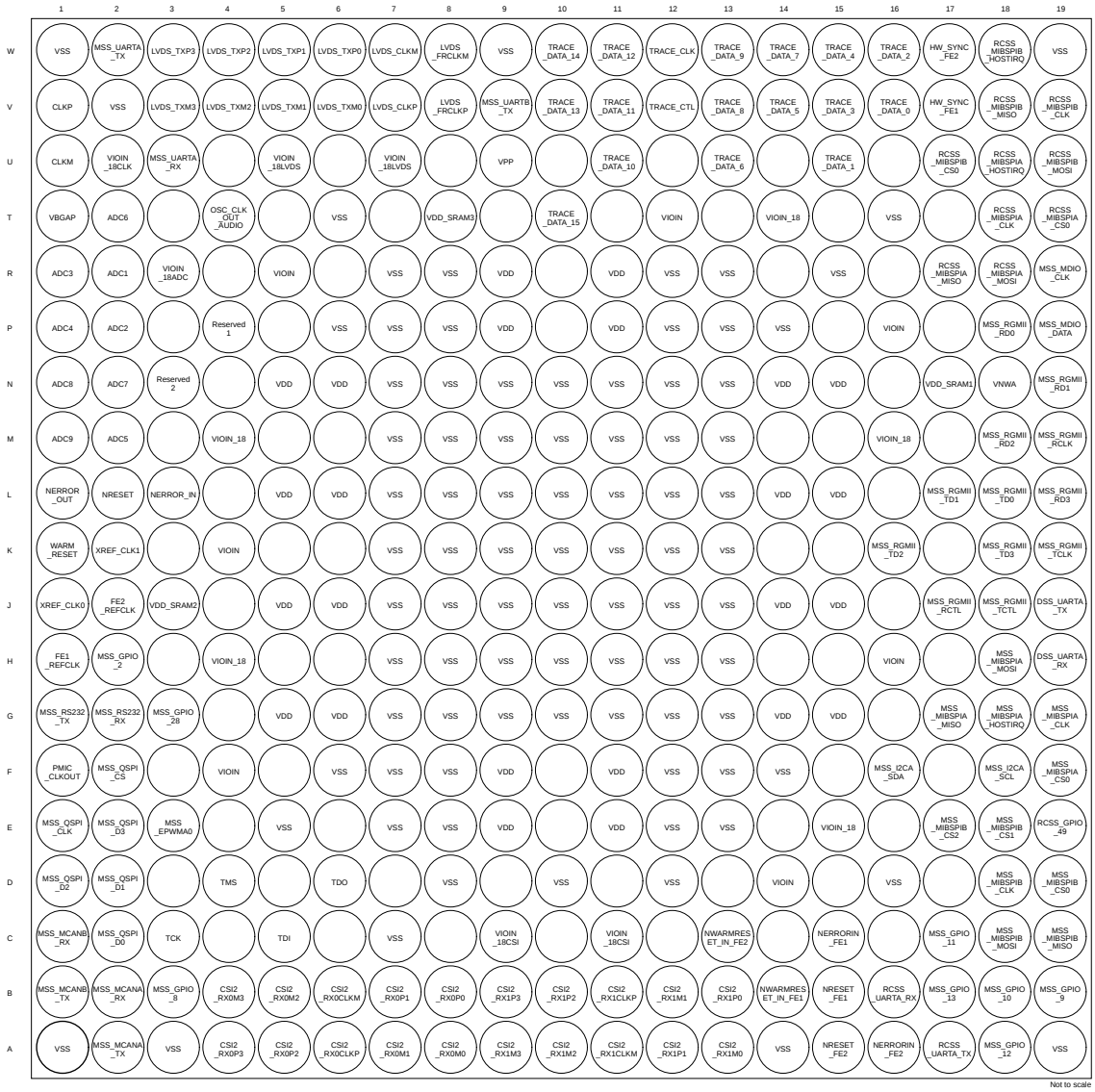


Figure 5-1. ZCE ZCE0285A Pin Diagram (Bottom View)

5.1.2 AM273x NZN Pin Diagram

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Figure 5-2 shows the ball locations for the 225-ball NanoFree™ ball grid array (NFBGA) package.

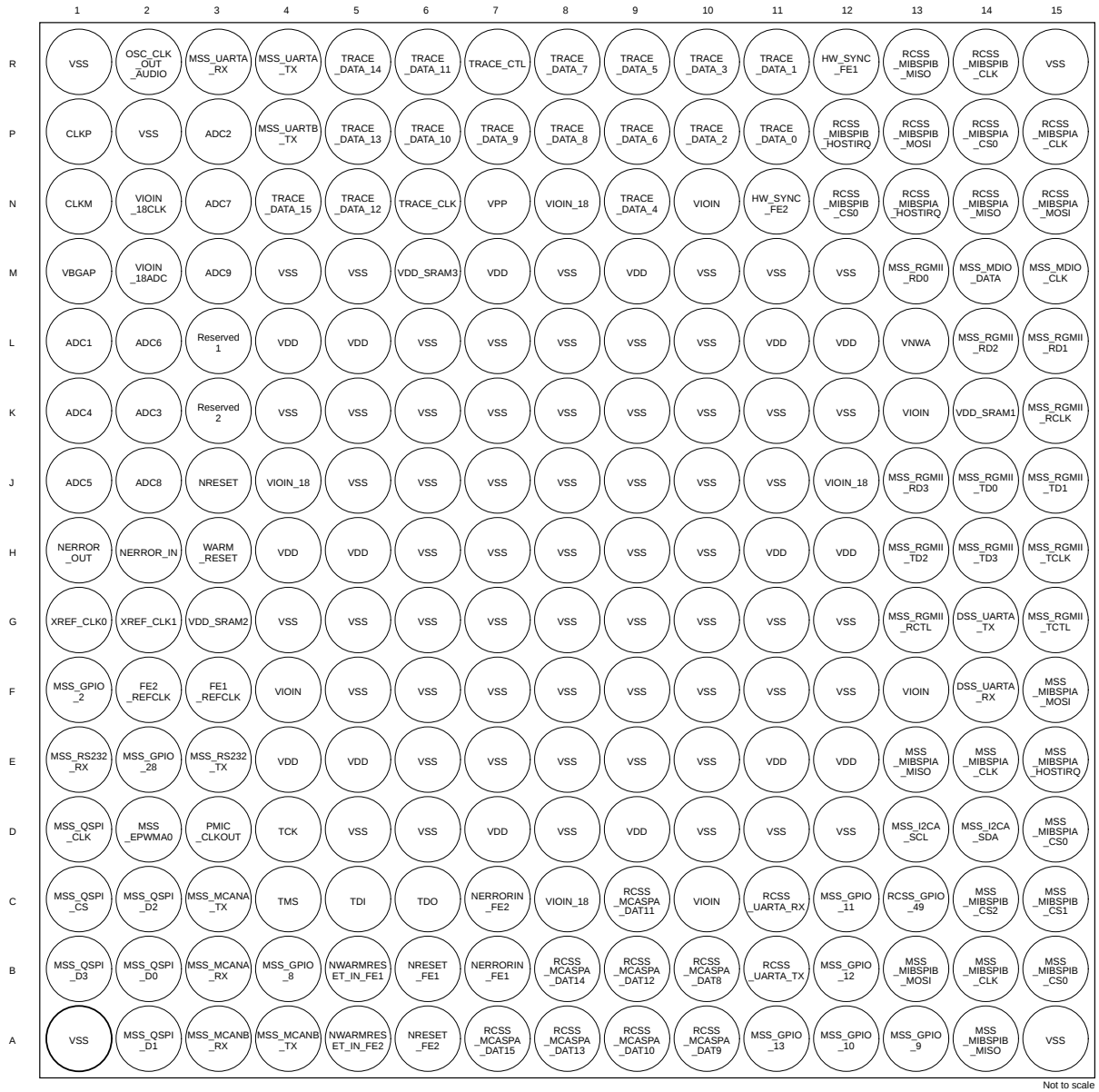


Figure 5-2. NZN NZN0225A Pin Diagram (Bottom View)

5.2 Pin Attributes (AM273x ZCE, NZN Packages)

The following list describes the contents of each column in the *Pin Attributes* table:

1. **BALL NUMBER:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **BALL NAME:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **SIGNAL NAME:** Signal name(s) of all dedicated and pin multiplexed signal functions associated with a ball.

Note

The *Pin Attributes* table, defines the pin multiplexed signal functions implemented at the pin and does not define secondary multiplexing of signal functions implemented in device subsystems. Secondary multiplexing of signal functions are not described in this table. For more information on seconadry multiplexed signal functions, see the respective peripheral chapter of the device TRM.

4. **PIN CONTROL REGISTER:** Name of pin control register. Reference the device Technical Reference Manual.
5. **PIN CONTROL ADDRESS:**Address of pin control register. Reference the device Technical Reference Manual.
6. **MUX MODE:** The MUXMODE value associated with each pin multiplexed signal function:
   a. MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.

Note

The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when MCU_PORz is deasserted.

   b. MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only valid values of MUXMODE should be used.
   c. Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz_OUT. These input signal functions are fixed to their respective pins and are not programmable via MUXMODE.
   d. An empty box or "-" means Not Applicable.
7. **TYPE:** Signal type and direction:
   - I = Input
   - O = Output
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - PWR = Power
   - GND = Ground
   - CAP = LDO Capacitor.

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8. **DSIS:** The deselected input state (DSIS) indicates the state driven to the subsystem input (logic "0", logic "1", or "pad" level) when the pin multiplexed signal function is not selected by MUXMODE.
   - 0: Logic 0 driven to the subsystem input.
   - 1: Logic 1 driven to the subsystem input.
   - pad: Logic state of the pad is driven to the subsystem input.
   - An empty box or "-" means Not Applicable.
9. **BALL STATE DURING RESET (RX/TX/PULL):** State of the terminal while MCU_PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is disabled.
     - On: The input buffer is enabled.
   - TX (Output buffer)
     - Off: The output buffer is disabled.
     - Low: The output buffer is enabled and drives V_{OL}.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned off.
     - Up: Internal pull-up resistor is turned on.
     - Down: Internal pull-down resistor is turned on.
   - An empty box or "-" means Not Applicable.
10. **BALL STATE AFTER RESET (RX/TX/PULL):** State of the terminal after MCU_PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
    - RX (Input buffer)
      - Off: The input buffer is disabled.
      - On: The input buffer is enabled.
    - TX (Output buffer)
      - Off: The output buffer is disabled.
      - SS: The subsystem selected with MUXMODE determines the output buffer state.
    - PULL (Internal pull resistors)
      - Off: Internal pull resistors are turned off.
      - Up: Internal pull-up resistor is turned on.
      - Down: Internal pull-down resistor is turned on.
    - An empty box or "-" means Not Applicable.
11. **MUX MODE AFTER RESET:** The value found in this column defines the default pin multiplexed signal function after MCU_PORz is deasserted. An empty box means Not Applicable.
12. **I/O VOLTAGE VALUE**: This column describes I/O operating voltage options of the respective power supply, when applicable. An empty box or "-" means Not Applicable.

    For more information, see valid operating voltage range(s) defined for each power supply in *Recommended Operating Conditions*.
13. **POWER DOMAIN:** The power supply of the associated I/O, when applicable. An empty box or "-" means this description is not applicable.

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14. **HYS:** Indicates if the input buffer associated with this I/O has hysteresis:
    - Yes: With hysteresis
    - No: Without hysteresis
    - An empty box or "-" means Not Applicable.

    For more information, see the hysteresis values in *Electrical Characteristics*.
15. **BUFFER TYPE:** This column defines the buffer type associated with a terminal. This information can be used to determine which Electrical Characteristics table is applicable.

    An empty box or "-" means Not Applicable.

    For electrical characteristics, refer to the appropriate buffer type table in *Electrical Characteristics*.
16. **PULL UP/DOWN TYPE:** Indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
    - PU: Internal pull-up
    - PD: Internal pull-down
    - PU/PD: Internal pull-up and pull-down
    - An empty box or "-" means No internal pull.

Note

Configuring two pins to the same pin multiplexed signal function is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration.

Note

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This should be avoided.

Table 5-1. Pin Attributes (ZCE, NZN Packages)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
R2	L1	ADC1	ADC1			0	I					1.8V	VIN_18ADC			ADC
P2	P3	ADC2	ADC2			0	I					1.8V	VIN_18ADC			ADC
R1	K2	ADC3	ADC3			0	I					1.8V	VIN_18ADC			ADC
P1	K1	ADC4	ADC4			0	I					1.8V	VIN_18ADC			ADC
M2	J1	ADC5	ADC5			0	I					1.8V	VIN_18ADC			ADC

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
T2	L2	ADC6	ADC6			0	I					1.8V	VIN_18ADC			ADC
N2	N3	ADC7	ADC7			0	I					1.8V	VIN_18ADC			ADC
N1	J2	ADC8	ADC8			0	I					1.8V	VIN_18ADC			ADC
M1	M3	ADC9	ADC9			0	I					1.8V	VIN_18ADC			ADC
U1	N1	CLKM	CLKM			0	I					1.8V	VIN_18CLK			Clock Subsystem
V1	P1	CLKP	CLKP			0	I					1.8V	VIN_18CLK			Clock Subsystem
B6		CSI2_RX0CLKM	CSI2_RX0CLKM				I						VIN_18CSI			MIPI D-PHY
A6		CSI2_RX0CLKP	CSI2_RX0CLKP				I						VIN_18CSI			MIPI D-PHY
A8		CSI2_RX0M0	CSI2_RX0M0				I						VIN_18CSI			MIPI D-PHY
A7		CSI2_RX0M1	CSI2_RX0M1				I						VIN_18CSI			MIPI D-PHY
B5		CSI2_RX0M2	CSI2_RX0M2				I						VIN_18CSI			MIPI D-PHY
B4		CSI2_RX0M3	CSI2_RX0M3				I						VIN_18CSI			MIPI D-PHY
B8		CSI2_RX0P0	CSI2_RX0P0				I						VIN_18CSI			MIPI D-PHY
B7		CSI2_RX0P1	CSI2_RX0P1				I						VIN_18CSI			MIPI D-PHY
A5		CSI2_RX0P2	CSI2_RX0P2				I						VIN_18CSI			MIPI D-PHY
A4		CSI2_RX0P3	CSI2_RX0P3				I						VIN_18CSI			MIPI D-PHY
A11		CSI2_RX1CLKM	CSI2_RX1CLKM				I						VIN_18CSI			MIPI D-PHY
B11		CSI2_RX1CLKP	CSI2_RX1CLKP				I						VIN_18CSI			MIPI D-PHY
A13		CSI2_RX1M0	CSI2_RX1M0				I						VIN_18CSI			MIPI D-PHY
B12		CSI2_RX1M1	CSI2_RX1M1				I						VIN_18CSI			MIPI D-PHY
A10		CSI2_RX1M2	CSI2_RX1M2				I						VIN_18CSI			MIPI D-PHY
A9		CSI2_RX1M3	CSI2_RX1M3				I						VIN_18CSI			MIPI D-PHY

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
B13		CSI2_RX1P0	CSI2_RX1P0				I						VIN_18CSI			MIPI D-PHY
A12		CSI2_RX1P1	CSI2_RX1P1				I						VIN_18CSI			MIPI D-PHY
B10		CSI2_RX1P2	CSI2_RX1P2				I						VIN_18CSI			MIPI D-PHY
B9		CSI2_RX1P3	CSI2_RX1P3				I						VIN_18CSI			MIPI D-PHY
H19	F14	DSS_UARTA_RX	RCSS_GPIO_47	PADDD_CFG_REG	0x020C0144	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			DSS_UARTA_RX			1	IO	Pad								
			RCSS_UARTA_TX			5	O	Pad								
			MSS_UARTA_TX			6	IO	Pad								
J19	G14	DSS_UARTA_TX	RCSS_GPIO_46	PADDC_CFG_REG	0x020C0140	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_CPTS0_HW1TSPUSH			1	I	Pad								
			DSS_UARTA_TX			4	IO	Pad								
			RCSS_UARTA_RX			5	I	Pad								
			MSS_UARTA_RX			6	IO	Pad								
H1	F3	FE1_REFCLK	MSS_GPIO_13	PADAB_CFG_REG	0x020C0004	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_GPIO_0			1	IO	Pad								
			PMIC_CLKOUT			2	O	Pad								
			MSS_EPWM_TZ2			3	I	Pad								
			MSS_EPWMA1			10	O	Pad								
			MSS_EPWMB0			11	O	Pad								
J2	F2	FE2_REFCLK	MSS_GPIO_16	PADAC_CFG_REG	0x020C0008	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_GPIO_1			1	IO	Pad								
			MSS_EPWM_TZ1			3	I	Pad								
			DMM_MUX_IN			12	I	Pad								
			MSS_MIBSPIB_CS1			13	IO	Pad								
			MSS_MIBSPIB_CS2			14	IO	Pad								
			MSS_EPWMA_SYNCI			15	I	Pad								
V17	R12	HW_SYNC_FE1	RCSS_GPIO_42	PADCY_CFG_REG	0x020C0130	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_CPTS0_TS_GENF			1	O	Pad								
			RCSS_MCASPC_DAT3			4	IO	Pad								
W17	N11	HW_SYNC_FE2	RCSS_GPIO_43	PADCZ_CFG_REG	0x020C0134	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_CPTS0_TS_COMP			1	O	Pad								
			RCSS_MCASPC_DAT2			4	IO	Pad								
W7		LVDS_CLKM	LVDS_CLKM				O									LVDS
V7		LVDS_CLKP	LVDS_CLKP				O									LVDS
W8		LVDS_FRCLKM	LVDS_FRCLKM				O									LVDS

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
V8		LVDS_FRCLKP	LVDS_FRCLKP				O									LVDS
V6		LVDS_TXM0	LVDS_TXM0				O									LVDS
V5		LVDS_TXM1	LVDS_TXM1				O									LVDS
V4		LVDS_TXM2	LVDS_TXM2				O									LVDS
V3		LVDS_TXM3	LVDS_TXM3				O									LVDS
W6		LVDS_TXP0	LVDS_TXP0				O									LVDS
W5		LVDS_TXP1	LVDS_TXP1				O									LVDS
W4		LVDS_TXP2	LVDS_TXP2				O									LVDS
W3		LVDS_TXP3	LVDS_TXP3				O									LVDS
E3	D2	MSS_EPWMA0	MSS_GPIO_25	PADAY_CFG_REG	0x020C0060	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MCU_CLKOUT			1	O	Pad								
			MSS_EPWMA0			12	O	Pad								
			OBS_CLKOUT			15	O	Pad								
H2	F1	MSS_GPIO_2	MSS_GPIO_26	PADAZ_CFG_REG	0x020C0064	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_GPIO_2			1	IO	Pad								
			MSS_UARTB_TX			7	IO	Pad								
			RCSS_GPIO_34			8	IO	Pad								
			PMIC_CLKOUT			10	O	Pad								
			MSS_EPWM_TZ0			14	I	Pad								
B3	B4	MSS_GPIO_8	MSS_GPIO_8	PADDM_CFG_REG	0x020C0168	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_EPWMA_SYNCO			2	O	Pad								
			MSS_EPWMB_SYNCI			3	I	Pad								
			MSS_EPWMC0			4	O	Pad								
			RCSS_I2CB_SCL			5	IO	Pad								
			MSS_UARTA_TX			6	IO	Pad								
			MSS_CPTS0_TS_SYNC			7	O	Pad								
			RCSS_ECAPA_SYNCOUT			8	O	Pad								
			RCSS_GPIO_40			12	IO	Pad								
B19	A13	MSS_GPIO_9	MSS_GPIO_9	PADDN_CFG_REG	0x020C016C	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_UARTA_TX			2	O	Pad								
			MSS_EPWMB_SYNCO			3	O	Pad								
			MSS_EPWMA1			4	O	Pad								
			DSS_UARTA_TX			6	IO	Pad								
			MSS_CPTS0_HW2TSPUSH			7	I	Pad								
			RCSS_MCASPA_AHCLKX			8	IO	Pad								
			RCSS_ATL_CLK0			11	IO	Pad								
			RCSS_GPIO_41			12	IO	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
B18	A12	MSS_GPIO_10	MSS_GPIO_10	PADDO_CFG_REG	0x020C0170	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_UARTA_RX			2	I	Pad								
			MSS_EPWMC_SYNCI			3	I	Pad								
			MSS_EPWMB1			4	O	Pad								
			DSS_UARTA_RX			6	IO	Pad								
			MSS_CPTS0_HW1TSPUSH			7	I	Pad								
			RCSS_MCASPA_ACLKX			8	IO	Pad								
			RCSS_GPIO_42			12	IO	Pad								
C17	C12	MSS_GPIO_11	MSS_GPIO_11	PADDP_CFG_REG	0x020C0174	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_UARTA_RTS			2	O	Pad								
			MSS_EPWMC_SYNCO			3	O	Pad								
			MSS_EPWMC1			4	O	Pad								
			MSS_I2CA_SDA			5	IO	Pad								
			MSS_UARTB_TX			6	IO	Pad								
			RCSS_MCASPA_FSX			8	IO	Pad								
			RCSS_GPIO_43			12	IO	Pad								
A18	B12	MSS_GPIO_12	MSS_GPIO_12	PADDQ_CFG_REG	0x020C0178	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_I2CA_SCL			1	IO	Pad								
			RCSS_UARTA_CTS			2	I	Pad								
			RCSS_ECAPA_CAPIN_PWMO			4	IO	Pad								
			MSS_CPTS0_TS_GENF			5	O	Pad								
			MSS_UARTB_RX			6	IO	Pad								
			RCSS_ECAPA_CAPIN_PWMO			7	IO	Pad								
			RCSS_MCASPA_ACLKR			8	IO	Pad								
			MSS_RS232_RX			11	IO	Pad								
			RCSS_GPIO_44			12	IO	Pad								
B17	A11	MSS_GPIO_13	MSS_GPIO_13	PADDR_CFG_REG	0x020C017C	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_I2CA_SDA			1	IO	Pad								
			MSS_CPTS0_TS_COMP			2	O	Pad								
			RCSS_UARTA_TX			4	O	Pad								
			MSS_UARTA_TX			5	IO	Pad								
			MSS_UARTB_TX			6	IO	Pad								
			DSS_UARTA_TX			7	IO	Pad								
			RCSS_MCASPA_FSR			8	IO	Pad								
			MSS_RS232_TX			11	IO	Pad								
			RCSS_GPIO_45			12	IO	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
G3	E2	MSS_GPIO_28	MSS_GPIO_28	PADBB_CFG_REG	0x020C006C	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			SYNC_IN			1	I	Pad								
			RCSS_MCASPB_AHCLKR			3	IO	Pad								
			MSS_UARTB_RX			6	IO	Pad								
			DMM_MUX_IN			7	I	Pad								
			DSS_UARTA_RX			8	IO	Pad								
F18	D13	MSS_I2CA_SCL	RCSS_GPIO_51	PADBZ_CFG_REG	0x020C00CC	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_RXER			1	I	Pad								
			MSS_RMII_RXER			2	I	Pad								
			MSS_I2CA_SCL			3	IO	Pad								
			RCSS_MCASPA_DAT1			4	IO	Pad								
			MSS_EPWMC1			6	O	Pad								
F16	D14	MSS_I2CA_SDA	RCSS_GPIO_50	PADBY_CFG_REG	0x020C00C8	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_CRS			1	I	Pad								
			MSS_RMII_CRS_DV			2	I	Pad								
			MSS_I2CA_SDA			3	IO	Pad								
			RCSS_MCASPA_DAT2			4	IO	Pad								
			MSS_EPWMB1			6	O	Pad								
B2	B3	MSS_MCANA_RX	MSS_GPIO_3	PADAF_CFG_REG	0x020C0014	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_MIBSPIA_CLK			1	IO	Pad								
			RCOSC_CLK			2	O	Pad								
			MSS_MCANB_RX			6	I	Pad								
			DSS_UARTA_TX			7	IO	Pad								
			MSS_MCANA_RX			9	I	Pad								
A2	C3	MSS_MCANA_TX	MSS_GPIO_30	PADAG_CFG_REG	0x020C0018	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_MIBSPIA_CS0			1	IO	Pad								
			RCOSC_CLK			2	O	Pad								
			MSS_MCANB_TX			6	O	Pad								
			MSS_MCANA_TX			9	O	Pad								
C1	A3	MSS_MCANB_RX	MSS_GPIO_19	PADAD_CFG_REG	0x020C000C	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_MIBSPIA_MOSI			1	IO	Pad								
			MSS_MCANA_RX			2	I	Pad								
			DSS_UARTA_TX			8	IO	Pad								
			MSS_MCANB_RX			9	I	Pad								
			MSS_I2CA_SCL			10	IO	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
B1	A4	MSS_MCANB_TX	MSS_GPIO_20	PADAE_CFG_REG	0x020C0010	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_MIBSPIA_MISO			1	IO	Pad								
			MSS_MCANA_TX			2	O	Pad								
			MSS_MCANB_TX			9	O	Pad								
			MSS_I2CA_SDA			10	IO	Pad								
R19	M15	MSS_MDIO_CLK	MSS_GPIO_31	PADCN_CFG_REG	0x020C0104	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_MDIO_CLK			1	O	Pad								
			RCSS_MCASPB_DAT1			4	IO	Pad								
P19	M14	MSS_MDIO_DATA	MSS_GPIO_30	PADCM_CFG_REG	0x020C0100	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_MDIO_DATA			1	IO	Pad								
			RCSS_MCASPB_DAT0			4	IO	Pad								
G19	E14	MSS_MIBSPIA_CLK	MSS_GPIO_5	PADDJ_CFG_REG	0x020C015C	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_CPTS0_TS_COMP			2	O	Pad								
			MSS_EPWMB1			3	O	Pad								
			RCSS_ECAPA_CAPIN_PWMO			4	IO	Pad								
			RCSS_I2CA_SDA			5	IO	Pad								
			MSS_UARTB_TX			6	IO	Pad								
			MSS_MIBSPIA_CLK			10	IO	Pad								
			RCSS_GPIO_37			12	IO	Pad								
F19	D15	MSS_MIBSPIA_CS0	MSS_GPIO_6	PADDK_CFG_REG	0x020C0160	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_EPWMA_SYNCI			1	I	Pad								
			MSS_EPWMA0			4	O	Pad								
			RCSS_I2CA_SCL			5	IO	Pad								
			MSS_UARTB_RX			6	IO	Pad								
			MSS_CPTS0_TS_GENF			7	O	Pad								
			MSS_MIBSPIA_CS0			10	IO	Pad								
			RCSS_GPIO_38			12	IO	Pad								
G18	E15	MSS_MIBSPIA_HOSTIRQ	MSS_GPIO_7	PADDL_CFG_REG	0x020C0164	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_EPWMA_SYNCO			1	O	Pad								
			MSS_EPWMC1			2	O	Pad								
			MSS_EPWMB0			4	O	Pad								
			RCSS_I2CB_SDA			5	IO	Pad								
			MSS_UARTA_RX			6	IO	Pad								
			MSS_CPTS0_TS_COMP			7	O	Pad								
			RCSS_ECAPA_SYNCIN			8	I	Pad								
			MSS_MIBSPIA_HOSTIRQ			10	O	Pad								
			RCSS_GPIO_39			12	IO	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
G17	E13	MSS_MIBSPIA_MISO	MSS_GPIO_4	PADDI_CFG_REG	0x020C0158	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_CPTS0_TS_GENF			2	O	Pad								
			RCSS_ATL_CLK1			3	IO	Pad								
			RCSS_I2CB_SCL			4	IO	Pad								
			MSS_EPWMB1			5	O	Pad								
			MSS_EPWMB0			6	O	Pad								
			OBS_CLKOUT			8	O	Pad								
			RCSS_UARTA_CTS			9	I	Pad								
			MSS_MIBSPIA_MISO			10	IO	Pad								
			RCSS_GPIO_36			12	IO	Pad								
H18	F15	MSS_MIBSPIA_MOSI	MSS_GPIO_3	PADDH_CFG_REG	0x020C0154	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			OBS_CLKOUT			1	O	Pad								
			RCSS_ATL_CLK0			2	IO	Pad								
			RCSS_I2CB_SDA			4	IO	Pad								
			MSS_EPWMA1			5	O	Pad								
			RCSS_UARTA_RTS			9	O	Pad								
			MSS_MIBSPIA_MOSI			10	IO	Pad								
			RCSS_GPIO_35			12	IO	Pad								
D18	B14	MSS_MIBSPIB_CLK	MSS_GPIO_5	PADAJ_CFG_REG	0x020C0024	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_MIBSPIB_CLK			1	IO	Pad								
			MSS_UARTA_RX			2	IO	Pad								
			MSS_EPWMC0			3	O	Pad								
			MSS_UARTB_TX			6	IO	Pad								
			MSS_MCANA_RX			8	I	Pad								
D19	B15	MSS_MIBSPIB_CS0	MSS_GPIO_4	PADAK_CFG_REG	0x020C0028	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_MIBSPIB_CS0			1	IO	Pad								
			MSS_UARTA_TX			2	IO	Pad								
			MSS_UARTB_TX			6	IO	Pad								
			MSS_MCANA_TX			9	O	Pad								
E18	C15	MSS_MIBSPIB_CS1	MSS_GPIO_12	PADAA_CFG_REG	0x020C0000	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MIBSPIA_HOSTIRQ			1	O	Pad								
			MSS_MIBSPIB_CS1			6	IO	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
E17	C14	MSS_MIBSPIB_CS2	MSS_GPIO_29	PADBC_CFG_REG	0x020C0070	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCOSC_CLK			2	O	Pad								
			DMM_MUX_IN			9	I	Pad								
			MSS_MIBSPIB_CS1			10	IO	Pad								
			MSS_MIBSPIB_CS2			11	IO	Pad								
			MSS_EPWMB0			12	O	Pad								
			MSS_EPWMB1			13	O	Pad								
C19	A14	MSS_MIBSPIB_MISO	MSS_GPIO_22	PADAI_CFG_REG	0x020C0020	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_MIBSPIB_MISO			1	IO	Pad								
			MSS_I2CA_SCL			2	IO	Pad								
			MSS_EPWMB0			3	O	Pad								
			DSS_UARTA_TX			6	IO	Pad								
			MSS_MCANB_TX			7	O	Pad								
C18	B13	MSS_MIBSPIB_MOSI	MSS_GPIO_21	PADAH_CFG_REG	0x020C001C	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_MIBSPIB_MOSI			1	IO	Pad								
			MSS_I2CA_SDA			2	IO	Pad								
			MSS_EPWMA0			3	O	Pad								
			MSS_MCANB_RX			7	I	Pad								
E1	D1	MSS_QSPI_CLK	MSS_GPIO_7	PADAP_CFG_REG	0x020C003C	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_QSPI_CLK			1	IO	Pad								
			MSS_MIBSPIB_CLK			2	IO	Pad								
			DSS_UARTA_TX			6	IO	Pad								
F2	C1	MSS_QSPI_CS	MSS_GPIO_6	PADAQ_CFG_REG	0x020C0040	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_QSPI_CS			1	O	Pad								
			MSS_MIBSPIB_CS0			2	IO	Pad								
C2	B2	MSS_QSPI_D0	MSS_GPIO_8	PADAL_CFG_REG	0x020C002C	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_QSPI_D0			1	IO	Pad								
			MSS_MIBSPIB_MISO			2	IO	Pad								
D2	A2	MSS_QSPI_D1	MSS_GPIO_9	PADAM_CFG_REG	0x020C0030	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_QSPI_D1			1	I	Pad								
			MSS_MIBSPIB_MOSI			2	IO	Pad								
			MSS_MIBSPIB_CS2			8	IO	Pad								
D1	C2	MSS_QSPI_D2	MSS_GPIO_10	PADAN_CFG_REG	0x020C0034	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_QSPI_D2			1	I	Pad								
			MSS_MCANA_TX			8	O	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
E2	B1	MSS_QSPI_D3	MSS_GPIO_11	PADAO_CFG_REG	0x020C0038	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_QSPI_D3			1	I	Pad								
			MSS_MCANA_RX			8	I	Pad								
M19	K15	MSS_RGMII_RCLK	RCSS_GPIO_59	PADCH_CFG_REG	0x020C00EC	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_RXCLK			1	I	Pad								
			MSS_RGMII_RCLK			3	I	Pad								
			RCSS_MCASPB_AHCLKR			4	IO	Pad								
			RCSS_I2CA_SCL			5	IO	Pad								
J17	G13	MSS_RGMII_RCTL	RCSS_GPIO_53	PADCB_CFG_REG	0x020C00D4	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_RXDV			1	I	Pad								
			MSS_RGMII_RCTL			3	I	Pad								
			RCSS_MCASPA_FSR			4	IO	Pad								
			MSS_UARTB_RX			5	IO	Pad								
			MSS_EPWMB0			6	O	Pad								
P18	M13	MSS_RGMII_RD0	RCSS_GPIO_63	PADCL_CFG_REG	0x020C00FC	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_RXD0			1	I	Pad								
			MSS_RMII_RXD0			2	I	Pad								
			MSS_RGMII_RD0			3	I	Pad								
			RCSS_MCASPB_FSR			4	IO	Pad								
N19	L15	MSS_RGMII_RD1	RCSS_GPIO_62	PADCK_CFG_REG	0x020C00F8	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_RXD1			1	I	Pad								
			MSS_RMII_RXD1			2	I	Pad								
			MSS_RGMII_RD1			3	I	Pad								
			RCSS_MCASPB_ACLKR			4	IO	Pad								
M18	L14	MSS_RGMII_RD2	RCSS_GPIO_61	PADCJ_CFG_REG	0x020C00F4	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_RXD2			1	I	Pad								
			MSS_RGMII_RD2			3	I	Pad								
			RCSS_MCASPB_FSX			4	IO	Pad								
			RCSS_I2CB_SCL			5	IO	Pad								
L19	J13	MSS_RGMII_RD3	RCSS_GPIO_60	PADCI_CFG_REG	0x020C00F0	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_RXD3			1	I	Pad								
			MSS_RGMII_RD3			3	I	Pad								
			RCSS_MCASPB_ACLKX			4	IO	Pad								
			RCSS_I2CB_SDA			5	IO	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
K19	H15	MSS_RGMII_TCLK	RCSS_GPIO_58	PADCG_CFG_REG	0x020C00E8	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_RXD3			1	I	Pad								
			MSS_RGMII_RD3			3	I	Pad								
			RCSS_MCASPB_ACLKX			4	IO	Pad								
			RCSS_I2CB_SDA			5	IO	Pad								
J18	G15	MSS_RGMII_TCTL	RCSS_GPIO_52	PADCA_CFG_REG	0x020C00D0	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_TXEN			1	O	Pad								
			MSS_RMII_TXEN			2	O	Pad								
			MSS_RGMII_TCTL			3	O	Pad								
			RCSS_MCASPA_DAT0			4	IO	Pad								
			MSS_EPWMA0			6	O	Pad								
L18	J14	MSS_RGMII_TD0	RCSS_GPIO_57	PADCF_CFG_REG	0x020C00E4	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_TXD0			1	O	Pad								
			MSS_RMII_TXD0			2	O	Pad								
			MSS_RGMII_TD0			3	O	Pad								
			RCSS_MCASPA_AHCLKX			4	IO	Pad								
L17	J15	MSS_RGMII_TD1	RCSS_GPIO_56	PADCE_CFG_REG	0x020C00E0	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_TXD1			1	O	Pad								
			MSS_RMII_TXD1			2	O	Pad								
			MSS_RGMII_TD1			3	O	Pad								
			RCSS_MCASPA_ACLKX			4	IO	Pad								
K16	H13	MSS_RGMII_TD2	RCSS_GPIO_55	PADCD_CFG_REG	0x020C00DC	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_TXD2			1	O	Pad								
			MSS_RGMII_TD2			3	O	Pad								
			RCSS_MCASPA_FSX			4	IO	Pad								
K18	H14	MSS_RGMII_TD3	RCSS_GPIO_54	PADCC_CFG_REG	0x020C00D8	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_TXD3			1	O	Pad								
			MSS_RGMII_TD3			3	O	Pad								
			RCSS_MCASPA_ACLKR			4	IO	Pad								
			MSS_UARTB_TX			5	IO	Pad								
			MSS_EPWMC0			6	O	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
G2	E1	MSS_RS232_RX	MSS_GPIO_15	PADBD_CFG_REG	0x020C0074	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_RS232_RX			1	IO	Pad								
			MSS_UARTA_RX			2	IO	Pad								
			MSS_UARTB_RX			7	IO	Pad								
			MSS_MCANA_RX			8	I	Pad								
			MSS_I2CA_SCL			9	IO	Pad								
			MSS_EPWMB0			10	O	Pad								
			MSS_EPWMB1			11	O	Pad								
			MSS_EPWMC0			12	O	Pad								
G1	E3	MSS_RS232_TX	MSS_GPIO_14	PADBE_CFG_REG	0x020C0078	0	IO	Pad	Off / Off / Off	Off / Off / Off	1	1.8V/3.3V	VIOIN	Yes	PU/PD (No Pull)	LVCMOS
			MSS_RS232_TX			1	IO	Pad								
			MSS_UARTA_TX			5	IO	Pad								
			MSS_UARTB_TX			6	IO	Pad								
			MSS_MCANA_TX			10	O	Pad								
			MSS_I2CA_SDA			11	IO	Pad								
			MSS_EPWMA0			12	O	Pad								
			MSS_EPWMA1			13	O	Pad								
			NDMM_EN			14	O	Pad								
			MSS_EPWMB0			15	O	Pad								
U3	R3	MSS_UARTA_RX	RCSS_GPIO_44	PADDA_CFG_REG	0x020C0138	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_CPTS0_TS_SYNC			1	O	Pad								
			MSS_UARTB_TX			4	IO	Pad								
			MSS_UARTA_RX			5	IO	Pad								
			DSS_UARTA_TX			6	IO	Pad								
W2	R4	MSS_UARTA_TX	RCSS_GPIO_45	PADDB_CFG_REG	0x020C013C	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			MSS_CPTS0_HW2TSPUSH			1	I	Pad								
			MSS_UARTB_RX			4	IO	Pad								
			MSS_UARTA_TX			5	IO	Pad								
			DSS_UARTA_RX			6	IO	Pad								
V9	P4	MSS_UARTB_TX	MSS_GPIO_0	PADDE_CFG_REG	0x020C0148	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			DSS_UARTA_TX			1	IO	Pad								
			MSS_EPWMB_SYNCI			3	I	Pad								
			MSS_UARTA_TX			5	IO	Pad								
			MSS_UARTB_TX			6	IO	Pad								
			RCSS_GPIO_32			12	IO	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
C15	B7	NERRORIN_FE1	MSS_GPIO_16	PADDU_CFG_REG	0x020C0188	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_MCASPA_DAT10			7	IO	Pad								
			RCSS_MCASPA_DAT2			8	IO	Pad								
			RCSS_GPIO_48			12	IO	Pad								
A16	C7	NERRORIN_FE2	MSS_GPIO_17	PADDV_CFG_REG	0x020C018C	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_MCASPA_DAT11			7	IO	Pad								
			RCSS_MCASPA_DAT3			8	IO	Pad								
			RCSS_GPIO_49			12	IO	Pad								
L3	H2	NERROR_IN	NERROR_IN	PADAR_CFG_REG	0x020C0044	0	I	Pad	Off / Off / Off	Off / NA / Up	0	1.8V/3.3V	VIOIN	Yes	Pull Disabled	LVCMOS
L1	H1	NERROR_OUT	NERROR_OUT	PADAT_CFG_REG	0x020C004C	0	IO	Pad	Off / Off / Off	Off / NA / Off	0	1.8V/3.3V	VIOIN	Yes	Pull Disabled	LVCMOS
L2	J3	NRESET	NRESET			0	I					1.8V/3.3V	VIOIN	Yes	PU/PD	LVCMOS
B15	B6	NRESET_FE1	MSS_GPIO_18	PADDW_CFG_REG	0x020C0190	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_MCASPA_DAT12			7	IO	Pad								
			RCSS_MCASPA_DAT4			8	IO	Pad								
			RCSS_GPIO_50			12	IO	Pad								
A15	A6	NRESET_FE2	MSS_GPIO_19	PADDX_CFG_REG	0x020C0194	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_I2CA_SDA			3	IO	Pad								
			RCSS_MCASPA_DAT13			7	IO	Pad								
			RCSS_MCASPA_DAT5			8	IO	Pad								
			RCSS_GPIO_51			12	IO	Pad								
B14	B5	NWARMRESET_IN_FE1	MSS_GPIO_20	PADDY_CFG_REG	0x020C0198	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_I2CA_SCL			3	IO	Pad								
			RCSS_MCASPA_DAT14			7	IO	Pad								
			RCSS_MCASPA_DAT6			8	IO	Pad								
			RCSS_GPIO_52			12	IO	Pad								
C13	A5	NWARMRESET_IN_FE2	MSS_GPIO_21	PADDZ_CFG_REG	0x020C019C	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_ECAPA_CAPIN_PWMO			4	IO	Pad								
			RCSS_MCASPA_DAT15			7	IO	Pad								
			RCSS_MCASPA_DAT7			8	IO	Pad								
			RCSS_GPIO_53			12	IO	Pad								
T4	R2	OSC_CLK_OUT_AUDIO	OSCCLKOUT			0	O					1.8V	VIN_18CLK			Clock Subsystem Output

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
F1	D3	PMIC_CLKOUT	MSS_GPIO_27	PADBA_CFG_REG	0x020C0068	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			PMIC_CLKOUT			1	O	Pad								
			OBS_CLKOUT			2	O	Pad								
			MSS_EPWMA1			11	O	Pad								
			MSS_EPWMB0			12	O	Pad								
E19	C13	RCSS_GPIO_49	RCSS_GPIO_49	PADBX_CFG_REG	0x020C00C4	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_MII_COL			1	I	Pad								
			MSS_RMII_REFCLK			2	IO	Pad								
			RCSS_MCASPA_DAT3			4	IO	Pad								
			MSS_EPWMA1			6	O	Pad								
	B10	RCSS_MCASPA_DAT8	MSS_GPIO_22	PADEA_CFG_REG	0x020C01A0	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_UARTA_RX			1	IO	Pad								
			MSS_GPIO_0			2	IO	Pad								
			RCSS_ECAPA_SYNCIN			4	I	Pad								
			RCSS_I2CA_SDA			5	IO	Pad								
			RCSS_MCASPA_DAT8			8	IO	Pad								
			RCSS_GPIO_54			12	IO	Pad								
	A10	RCSS_MCASPA_DAT9	MSS_GPIO_23	PADEB_CFG_REG	0x020C01A4	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_UARTA_TX			1	IO	Pad								
			MSS_GPIO_1			2	IO	Pad								
			RCSS_ECAPA_SYNCOUT			4	O	Pad								
			RCSS_I2CA_SCL			5	IO	Pad								
			RCSS_MCASPA_DAT9			8	IO	Pad								
			RCSS_GPIO_55			12	IO	Pad								
	A9	RCSS_MCASPA_DAT10	MSS_GPIO_24	PADEC_CFG_REG	0x020C01A8	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_UARTB_TX			1	IO	Pad								
			MSS_GPIO_2			2	IO	Pad								
			RCSS_ECAPA_CAPIN_PWMO			4	IO	Pad								
			RCSS_I2CB_SDA			5	IO	Pad								
			RCSS_MCASPA_DAT10			8	IO	Pad								
			RCSS_GPIO_56			12	IO	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
	C9	RCSS_MCASPA_DAT11	MSS_GPIO_25	PADED_CFG_REG	0x020C01AC	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_UARTB_RX			1	IO	Pad								
			MSS_GPIO_3			2	IO	Pad								
			RCSS_ECAPA_SYNCIN			4	I	Pad								
			RCSS_I2CB_SCL			5	IO	Pad								
			RCSS_MCASPA_DAT11			8	IO	Pad								
			RCSS_GPIO_57			12	IO	Pad								
	B9	RCSS_MCASPA_DAT12	MSS_GPIO_26	PADEE_CFG_REG	0x020C01B0	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_UARTA_RTS			1	IO	Pad								
			MSS_GPIO_4			2	IO	Pad								
			RCSS_ECAPA_SYNCOUT			4	O	Pad								
			RCSS_ECAPA_CAPIN_PWMO			5	IO	Pad								
			RCSS_MCASPA_DAT12			8	IO	Pad								
			RCSS_GPIO_58			12	IO	Pad								
	A8	RCSS_MCASPA_DAT13	MSS_GPIO_27	PADEF_CFG_REG	0x020C01B4	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_UARTA_CTS			1	I	Pad								
			MSS_GPIO_9			2	IO	Pad								
			DSS_UARTA_RX			3	IO	Pad								
			RCSS_MCASPA_DAT13			8	IO	Pad								
			RCSS_GPIO_59			12	IO	Pad								
	B8	RCSS_MCASPA_DAT14	MSS_GPIO_28	PADEG_CFG_REG	0x020C01B8	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_UARTA_TX			1	O	Pad								
			MSS_GPIO_10			2	IO	Pad								
			MSS_I2CA_SDA			5	IO	Pad								
			RCSS_MCASPA_DAT14			8	IO	Pad								
			RCSS_GPIO_60			12	IO	Pad								
	A7	RCSS_MCASPA_DAT15	MSS_GPIO_29	PADEH_CFG_REG	0x020C01BC	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_UARTA_RX			1	I	Pad								
			MSS_GPIO_11			2	IO	Pad								
			MSS_I2CA_SCL			5	IO	Pad								
			RCSS_MCASPA_DAT15			8	IO	Pad								
			RCSS_GPIO_61			12	IO	Pad								
T18	P15	RCSS_MIBSPIA_CLK	RCSS_GPIO_34	PADCQ_CFG_REG	0x020C0110	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			RCSS_MIBSPIA_CLK			1	IO	Pad								
			RCSS_I2CB_SDA			2	IO	Pad								
			MSS_MIBSPIA_CLK			5	IO	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
T19	P14	RCSS_MIBSPIA_CS0	RCSS_GPIO_35	PADCR_CFG_REG	0x020C0114	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			RCSS_MIBSPIA_CS0			1	IO	Pad								
			RCSS_I2CB_SCL			2	IO	Pad								
			MSS_MIBSPIA_CS0			5	IO	Pad								
U18	N13	RCSS_MIBSPIA_HOSTIRQ	RCSS_GPIO_36	PADCS_CFG_REG	0x020C0118	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_MIBSPIA_CS1			1	IO	Pad								
			MSS_GPIO_2			2	IO	Pad								
			MSS_GPIO_8			3	IO	Pad								
			MSS_MIBSPIA_HOSTIRQ			5	O	Pad								
			MSS_MIBSPIB_CS2			6	IO	Pad								
			RCSS_GPIO_34			7	IO	Pad								
			RCSS_GPIO_40			10	IO	Pad								
R17	N14	RCSS_MIBSPIA_MISO	RCSS_GPIO_33	PADCP_CFG_REG	0x020C010C	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			RCSS_MIBSPIA_MISO			1	IO	Pad								
			RCSS_I2CA_SCL			2	IO	Pad								
			MSS_MIBSPIA_MISO			5	IO	Pad								
R18	N15	RCSS_MIBSPIA_MOSI	RCSS_GPIO_32	PADCO_CFG_REG	0x020C0108	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			RCSS_MIBSPIA_MOSI			1	IO	Pad								
			RCSS_I2CA_SDA			2	IO	Pad								
			MSS_MIBSPIA_MOSI			5	IO	Pad								
V19	R14	RCSS_MIBSPIB_CLK	RCSS_GPIO_39	PADCV_CFG_REG	0x020C0124	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			RCSS_MIBSPIB_CLK			1	IO	Pad								
			RCSS_I2CB_SDA			2	IO	Pad								
			MSS_CPTS0_TS_SYNC			3	O	Pad								
			MSS_MIBSPIB_CLK			5	IO	Pad								
U17	N12	RCSS_MIBSPIB_CS0	RCSS_GPIO_40	PADCW_CFG_REG	0x020C0128	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			RCSS_MIBSPIB_CS0			1	IO	Pad								
			RCSS_I2CB_SCL			2	IO	Pad								
			MSS_CPTS0_TS_COMP			3	O	Pad								
			RCSS_MCASPC_DAT5			4	IO	Pad								
			MSS_MIBSPIB_CS0			5	IO	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
W18	P12	RCSS_MIBSPIB_HOSTIRQ	RCSS_GPIO_41	PADCX_CFG_REG	0x020C012C	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_MIBSPIB_CS1			1	IO	Pad								
			MSS_CPTS0_TS_GENF			3	O	Pad								
			RCSS_MCASPC_DAT4			4	IO	Pad								
			MSS_MIBSPIB_CS1			5	IO	Pad								
			MSS_GPIO_3			6	IO	Pad								
			MSS_GPIO_9			7	IO	Pad								
			RCSS_GPIO_35			10	IO	Pad								
V18	R13	RCSS_MIBSPIB_MISO	RCSS_GPIO_38	PADCU_CFG_REG	0x020C0120	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			RCSS_MIBSPIB_MISO			1	IO	Pad								
			RCSS_I2CA_SCL			2	IO	Pad								
			MSS_CPTS0_HW2TSPUSH			3	I	Pad								
			MSS_MIBSPIB_MISO			5	IO	Pad								
U19	P13	RCSS_MIBSPIB_MOSI	RCSS_GPIO_37	PADCT_CFG_REG	0x020C011C	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			RCSS_MIBSPIB_MOSI			1	IO	Pad								
			RCSS_I2CA_SDA			2	IO	Pad								
			MSS_CPTS0_HW1TSPUSH			3	I	Pad								
			MSS_MIBSPIB_MOSI			5	IO	Pad								
B16	C11	RCSS_UARTA_RX	MSS_GPIO_15	PADDT_CFG_REG	0x020C0184	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			RCSS_UARTA_RX			2	I	Pad								
			RCSS_I2CB_SCL			3	IO	Pad								
			RCSS_MCASPA_DAT9			7	IO	Pad								
			RCSS_MCASPA_DAT1			8	IO	Pad								
			RCSS_GPIO_47			12	IO	Pad								
A17	B11	RCSS_UARTA_TX	MSS_GPIO_14	PADDS_CFG_REG	0x020C0180	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			RCSS_UARTA_TX			2	O	Pad								
			RCSS_I2CB_SDA			3	IO	Pad								
			RCSS_MCASPA_DAT8			7	IO	Pad								
			RCSS_MCASPA_DAT0			8	IO	Pad								
			RCSS_GPIO_46			12	IO	Pad								
P4	L3	Reserved1	Reserved1			0	Reserved									
N3	K3	Reserved2	Reserved2			0	Reserved									
C3	D4	TCK	MSS_GPIO_17	PADAU_CFG_REG	0x020C0050	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			TCK			1	I	Pad								
			MSS_UARTB_TX			2	IO	Pad								
			MSS_MCANA_TX			8	O	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
C5	C5	TDI	MSS_GPIO_23	PADAW_CFG_REG	0x020C0058	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			TDI			1	I	Pad								
			MSS_UARTA_RX			2	IO	Pad								
			DSS_UARTA_RX			7	IO	Pad								
D6	C6	TDO	MSS_GPIO_24	PADAX_CFG_REG	0x020C005C	0	IO	Pad	Off / Off / Off	Off / NA / Off	1	1.8V/3.3V	VIOIN	Yes	Pull Disabled	LVCMOS
			TDO			1	O	Pad								
			MSS_UARTA_TX			2	IO	Pad								
			MSS_UARTB_TX			6	IO	Pad								
			NDMM_EN			9	O	Pad								
D4	C4	TMS	MSS_GPIO_18	PADAV_CFG_REG	0x020C0054	0	IO	Pad	Off / Off / Off	Off / Off / Up	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PU)	LVCMOS
			TMS			1	IO	Pad								
			MSS_MCANA_RX			6	I	Pad								
W12	N6	TRACE_CLK	TRACE_CLK	PADBV_CFG_REG	0x020C00BC	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_47			1	IO	Pad								
			DMM_CLK			2	I	Pad								
			RCSS_MCASPB_DAT5			7	IO	Pad								
			DSS_UARTA_RX			10	IO	Pad								
			RCSS_I2CA_SCL			11	IO	Pad								
V12	R7	TRACE_CTL	TRACE_CTL	PADBW_CFG_REG	0x020C00C0	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_48			1	IO	Pad								
			DMM_SYNC			2	I	Pad								
			RCSS_MCASPB_AHCLKX			7	IO	Pad								
			DSS_UARTA_TX			10	IO	Pad								
V16	P11	TRACE_DATA_0	TRACE_DATA_0	PADBF_CFG_REG	0x020C007C	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			MSS_GPIO_31			1	IO	Pad								
			DMM0			2	I	Pad								
			MSS_UARTA_TX			4	IO	Pad								
			RCSS_MCASPC_DAT1			7	IO	Pad								
			MSS_I2CA_SDA			10	IO	Pad								
U15	R11	TRACE_DATA_1	TRACE_DATA_1	PADBG_CFG_REG	0x020C0080	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_32			1	IO	Pad								
			DMM1			2	I	Pad								
			MSS_EPWMC_SYNCI			3	I	Pad								
			MSS_UARTA_RX			4	IO	Pad								
			RCSS_MCASPC_DAT0			7	IO	Pad								
			MSS_I2CA_SCL			10	IO	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
W16	P10	TRACE_DATA_2	TRACE_DATA_2	PADBH_CFG_REG	0x020C0084	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_33			1	IO	Pad								
			DMM2			2	I	Pad								
			MSS_EPWMB_SYNCI			3	I	Pad								
			RCSS_MCASPC_FSR			7	IO	Pad								
V15	R10	TRACE_DATA_3	TRACE_DATA_3	PADBI_CFG_REG	0x020C0088	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_34			1	IO	Pad								
			DMM3			2	I	Pad								
			MSS_EPWMC_SYNCO			4	O	Pad								
			RCSS_MCASPC_ACLKR			7	IO	Pad								
W15	N9	TRACE_DATA_4	TRACE_DATA_4	PADBJ_CFG_REG	0x020C008C	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_35			1	IO	Pad								
			DMM4			2	I	Pad								
			MSS_EPWMB_SYNCO			4	O	Pad								
			RCSS_MCASPC_FSX			7	IO	Pad								
V14	R9	TRACE_DATA_5	TRACE_DATA_5	PADBK_CFG_REG	0x020C0090	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_36			1	IO	Pad								
			DMM5			2	I	Pad								
			MSS_EPWM_TZ2			4	I	Pad								
			MSS_UARTB_TX			5	IO	Pad								
			RCSS_MCASPC_ACLKX			7	IO	Pad								
U13	P9	TRACE_DATA_6	TRACE_DATA_6	PADBL_CFG_REG	0x020C0094	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_37			1	IO	Pad								
			DMM6			2	I	Pad								
			MSS_EPWM_TZ1			4	I	Pad								
			RCSS_MCASPC_AHCLKX			7	IO	Pad								
W14	R8	TRACE_DATA_7	TRACE_DATA_7	PADBM_CFG_REG	0x020C0098	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_38			1	IO	Pad								
			DMM7			2	I	Pad								
			MSS_EPWM_TZ0			4	I	Pad								
			DSS_UARTA_TX			5	IO	Pad								
			RCSS_MCASPB_ACLKX			7	IO	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
V13	P8	TRACE_DATA_8	TRACE_DATA_8	PADBN_CFG_REG	0x020C009C	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_39			1	IO	Pad								
			DMM8			2	I	Pad								
			MSS_MCANA_TX			4	O	Pad								
			MSS_EPWMA_SYNCI			5	I	Pad								
			RCSS_MCASPB_FSX			7	IO	Pad								
W13	P7	TRACE_DATA_9	TRACE_DATA_9	PADBO_CFG_REG	0x020C00A0	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_40			1	IO	Pad								
			DMM9			2	I	Pad								
			MSS_MCANA_RX			4	I	Pad								
			MSS_EPWMA_SYNCO			5	O	Pad								
			RCSS_MCASPB_ACLKR			7	IO	Pad								
U11	P6	TRACE_DATA_10	TRACE_DATA_10	PADBP_CFG_REG	0x020C00A4	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_41			1	IO	Pad								
			DMM10			2	I	Pad								
			MSS_EPWMC0			4	O	Pad								
			RCSS_MCASPB_FSR			7	IO	Pad								
V11	R6	TRACE_DATA_11	TRACE_DATA_11	PADBQ_CFG_REG	0x020C00A8	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_42			1	IO	Pad								
			DMM11			2	I	Pad								
			MSS_EPWMC1			4	O	Pad								
			RCSS_MCASPB_DAT0			7	IO	Pad								
W11	N5	TRACE_DATA_12	TRACE_DATA_12	PADBR_CFG_REG	0x020C00AC	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_43			1	IO	Pad								
			DMM12			2	I	Pad								
			MSS_EPWMA0			4	O	Pad								
			MSS_MCANB_TX			5	O	Pad								
			RCSS_MCASPB_DAT1			7	IO	Pad								
V10	P5	TRACE_DATA_13	TRACE_DATA_13	PADBS_CFG_REG	0x020C00B0	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_44			1	IO	Pad								
			DMM13			2	I	Pad								
			MSS_EPWMA1			4	O	Pad								
			MSS_MCANB_RX			5	I	Pad								
			RCSS_MCASPB_DAT2			7	IO	Pad								

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
W10	R5	TRACE_DATA_14	TRACE_DATA_14	PADBT_CFG_REG	0x020C00B4	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_45			1	IO	Pad								
			DMM14			2	I	Pad								
			MSS_EPWMB0			4	O	Pad								
			RCSS_MCASPB_DAT3			7	IO	Pad								
T10	N4	TRACE_DATA_15	TRACE_DATA_15	PADBU_CFG_REG	0x020C00B8	0	O	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			RCSS_GPIO_46			1	IO	Pad								
			DMM15			2	I	Pad								
			MSS_EPWMB1			4	O	Pad								
			RCSS_MCASPB_DAT4			7	IO	Pad								
			RCSS_I2CA_SDA			11	IO	Pad								
T1	M1	VBGAP	VBGAP				PWR									
E11, E9, F11, F9, G14, G15, G5, G6, J14, J15, J5, J6, L14, L15, L5, L6, N14, N15, N5, N6, P11, P9, R11, R9	D7, D9, E11, E12, E4, E5, H11, H12, H4, H5, L11, L12, L4, L5, M7, M9	VDD	VDD				PWR					1.2V				
N17	K14	VDD_SRAM1	VDD_SRAM1				PWR					1.2V				
J3	G3	VDD_SRAM2	VDD_SRAM2				PWR					1.2V				
T8	M6	VDD_SRAM3	VDD_SRAM3				PWR					1.2V				
D14, F4, H16, K4, P16, R5, T12	C10, F13, F4, K13, N10	VIOIN	VIOIN				PWR					1.8V/3.3V				
E15, H4, M16, M4, T14	C8, J12, J4, N8	VIOIN_18	VIOIN_18				PWR					1.8V				
R3	M2	VIOIN_18ADC	VIOIN_18ADC				PWR					1.8V				
U2	N2	VIOIN_18CLK	VIOIN_18CLK				PWR					1.8V				
C11, C9		VIOIN_18CSI	VIOIN_18CSI				PWR					1.8V				
U5, U7		VIOIN_18LVDS	VIOIN_18LVDS				PWR					1.8V				
N18	L13	VNWA	VNWA				PWR					1.2V				
U9	N7	VPP	VPP				PWR					1.7V				

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Table 5-1. Pin Attributes (ZCE, NZN Packages) (continued)

ZCE Ball Number	NZN Ball Number	Ball Name	Signal Name	Pin Control Register	Pin Control Address	MUX Mode	Signal Type	DSIS	Ball State During Reset	Ball State After Reset	Mux Mode After Reset	I/O Voltage	Power Domain	Hysteresis	Pull Type	Buffer Type
A1, A14, A19, A3, C7, D10, D12, D16, D8, E12, E13, E5, E7, E8, F12, F13, F14, F6, F7, F8, G10, G11, G12, G13, G7, G8, G9, H10, H11, H12, H13, H7, H8, H9, J10, J11, J12, J13, J7, J8, J9, K10, K11, K12, K13, K7, K8, K9, L10, L11, L12, L13, L7, L8, L9, M10, M11, M12, M13, M7, M8, M9, N10, N11, N12, N13, N7, N8, N9, P12, P13, P14, P6, P7, P8, R12, R13, R15, R7, R8, T16, T6, V2, W1, W19, W9	A1, A15, D10, D11, D12, D5, D6, D8, E10, E6, E7, E8, E9, F10, F11, F12, F5, F6, F7, F8, F9, G10, G11, G12, G4, G5, G6, G7, G8, G9, H10, H6, H7, H8, H9, J10, J11, J5, J6, J7, J8, J9, K10, K11, K12, K4, K5, K6, K7, K8, K9, L10, L6, L7, L8, L9, M10, M11, M12, M4, M5, M8, P2, R1, R15	VSS	VSS				GND					VSS				
K1	H3	WARM_RESET	WARM_RESET	PADAS_CFG_REG	0x020C0048	0	IO	Pad	Off / Off / Off	Off / NA / Off	0	1.8V/3.3V	VIOIN	Yes	Pull Disabled	LVCMOS
J1	G1	XREF_CLK0	MSS_GPIO_1	PADDF_CFG_REG	0x020C014C	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			XREF_CLK0			1	IO	Pad								
			MCU_CLKOUT			6	O	Pad								
			RCSS_GPIO_33			12	IO	Pad								
K2	G2	XREF_CLK1	MSS_GPIO_2	PADDG_CFG_REG	0x020C0150	0	IO	Pad	Off / Off / Off	Off / Off / Down	1	1.8V/3.3V	VIOIN	Yes	PU/PD (PD)	LVCMOS
			XREF_CLK1			1	IO	Pad								
			RCSS_ECAPA_CAPIN_PWMO			3	IO	Pad								
			PMIC_CLKOUT			7	O	Pad								
			RCSS_GPIO_34			12	IO	Pad								

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5.3 Signal Descriptions

Note

All digital IO pins of the device (except NERROR IN, NERROR_OUT, and WARM_RESET) are non-failsafe; hence, care needs to be taken that they are not driven externally without the VIO supply being present to the device

Note

The GPIO state during the power supply ramp is not ensured. In case the GPIO is used in the application where the state of the GPIO is critical, even when NRESET is low, a tri-state buffer should be used to isolate the GPIO output from any attached device. An additional pull resister should be used to define the required state in the application. The NRESET signal could be used to control the output enable (OE) of the tri-state buffer.

Signal Description Header List

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **Signal Name:** The name of the signal passing through the pin.

   Note

   Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function implemented at the pin and selected via PADCONFIG registers. Some device subsystems provide an additional layer of multiplexing for signal functions that are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **Signal Type:** Signal type and direction:
   - I = Input
   - O = Output
   - IO = Input, Output, or simultaneously Input and Output
   - OD = Output, with open-drain output function
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - CAP = LDO capacitor
   - PWR = Power
   - GND = Ground
3. **Description:** Description of the signal
4. **Ball #:** Ball number associated with signal

For more information on the I/O cell configurations, see the *Pad Configuration Registers* section within the *Device Configuration* chapter of the device TRM.

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5.3.1 ADC Signal Descriptions

Table 5-2. ADC Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
ADC1	I	ADC Input Channel 1	R2	L1
ADC2	I	ADC Input Channel 2	P2	P3
ADC3	I	ADC Input Channel 3	R1	K2
ADC4	I	ADC Input Channel 4	P1	K1
ADC5	I	ADC Input Channel 5	M2	J1
ADC6	I	ADC Input Channel 6	T2	L2
ADC7	I	ADC Input Channel 7	N2	N3
ADC8	I	ADC Input Channel 8	N1	J2
ADC9	I	ADC Input Channel 9	M1	M3

5.3.2 CPTS Signal Descriptions

Table 5-3. CPTS Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_CPTS0_TS_COMP	O	Master sub-system Common Platform Time Sync Module 0 Timestamp Comparison Output	B17, G18, G19, U17, W17	A11, E14, E15, N11, N12
MSS_CPTS0_TS_GENF	O	Master sub-system Common Platform Time Sync Module 0 Timestamp Function Generation Output	A18, F19, G17, V17, W18	B12, D15, E13, P12, R12
MSS_CPTS0_TS_SYNC	O	Master sub-system Common Platform Time Sync Module 0 Timestamp Sync Output	B3, U3, V19	B4, R14, R3
MSS_CPTS0_HW1TSPUSH	I	Master sub-system Common Platform Time Sync Module 0 Asynchronous Hardware Timestamp 1 push input	B18, J19, U19	A12, G14, P13
MSS_CPTS0_HW2TSPUSH	I	Master sub-system Common Platform Time Sync Module 0 Asynchronous Hardware Timestamp 2 push input	B19, V18, W2	A13, R13, R4

5.3.3 CSI 2.0 Signal Descriptions

Table 5-4. CSI 2.0 Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
CSI2_RX0CLKM	I	CSI2.0 Receiver 0, Clock Input Negative Polarity	B6	
CSI2_RX0CLKP	I	CSI2.0 Receiver 0, Clock Input Positive Polarity	A6	
CSI2_RX0M0	I	CSI2.0 Receiver 0, Lane 0 Negative Polarity	A8	
CSI2_RX0M1	I	CSI2.0 Receiver 0, Lane 1 Negative Polarity	A7	
CSI2_RX0M2	I	CSI2.0 Receiver 0, Lane 2 Negative Polarity	B5	
CSI2_RX0M3	I	CSI2.0 Receiver 0, Lane 3 Negative Polarity	B4	
CSI2_RX0P0	I	CSI2.0 Receiver 0, Lane 0 Positive Polarity	B8	
CSI2_RX0P1	I	CSI2.0 Receiver 0, Lane 1 Positive Polarity	B7	
CSI2_RX0P2	I	CSI2.0 Receiver 0, Lane 2 Positive Polarity	A5	
CSI2_RX0P3	I	CSI2.0 Receiver 0, Lane 3 Positive Polarity	A4	
CSI2_RX1CLKM	I	CSI2.0 Receiver 1, Clock Input Negative Polarity	A11	
CSI2_RX1CLKP	I	CSI2.0 Receiver 1, Clock Input Positive Polarity	B11	
CSI2_RX1M0	I	CSI2.0 Receiver 1, Lane 0 Negative Polarity	A13	
CSI2_RX1M1	I	CSI2.0 Receiver 1, Lane 1 Negative Polarity	B12	

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Table 5-4. CSI 2.0 Signal Descriptions (continued)

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
CSI2_RX1M2	I	CSI2.0 Receiver 1, Lane 2 Negative Polarity	A10	
CSI2_RX1M3	I	CSI2.0 Receiver 1, Lane 3 Negative Polarity	A9	
CSI2_RX1P0	I	CSI2.0 Receiver 1, Lane 0 Positive Polarity	B13	
CSI2_RX1P1	I	CSI2.0 Receiver 1, Lane 1 Positive Polarity	A12	
CSI2_RX1P2	I	CSI2.0 Receiver 1, Lane 2 Positive Polarity	B10	
CSI2_RX1P3	I	CSI2.0 Receiver 1, Lane 3 Positive Polarity	B9	

5.3.4 DMM Signal Descriptions

Table 5-5. DMM Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
DMM0	I	DMM data input	V16	P11
DMM1	I	DMM data input	U15	R11
DMM2	I	DMM data input	W16	P10
DMM3	I	DMM data input	V15	R10
DMM4	I	DMM data input	W15	N9
DMM5	I	DMM data input	V14	R9
DMM6	I	DMM data input	U13	P9
DMM7	I	DMM data input	W14	R8
DMM8	I	DMM data input	V13	P8
DMM9	I	DMM data input	W13	P7
DMM10	I	DMM data input	U11	P6
DMM11	I	DMM data input	V11	R6
DMM12	I	DMM data input	W11	N5
DMM13	I	DMM data input	V10	P5
DMM14	I	DMM data input	W10	R5
DMM15	I	DMM data input	T10	N4
DMM_CLK	I	DMM clock	W12	N6
DMM_MUX_IN	I	DMM MUX input	E17, G3, J2	C14, E2, F2
DMM_SYNC	I	DMM sync input	V12	R7
NDMM_EN	O	DMM enable input	D6, G1	C6, E3

5.3.5 ECAP Signal Descriptions

Table 5-6. ECAP Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
RCSS_ECAPA_CAPIN_PWMO	IO	Enhanced Capture Module A, Enhanced Capture input or PWM out	A18, C13, G19, K2	A5, A9, B12, B9, E14, G2
RCSS_ECAPA_SYNCIN	I	Enhanced Capture Module A, Sync In	G18	B10, C9, E15
RCSS_ECAPA_SYNCOUT	O	Enhanced Capture Module A, Sync Out	B3	A10, B4, B9

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5.3.6 EPWM Signal Descriptions

Table 5-7. EPWMA Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_EPWMA0	O	Master sub-system, PWM A, Channel 0	C18, E3, F19, G1, J18, W11	B13, D15, D2, E3, G15, N5
MSS_EPWMA1	O	Master sub-system, PWM A, Channel 1	B19, E19, F1, G1, H1, H18, V10	A13, C13, D3, E3, F15, F3, P5
MSS_EPWMA_SYNCI	I	Master sub-system, PWM A, Sync Input	F19, J2, V13	D15, F2, P8
MSS_EPWMA_SYNCO	O	Master sub-system, PWM A, Sync Output	B3, G18, W13	B4, E15, P7

Table 5-8. EPWMB Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_EPWMB0	O	Master sub-system, PWM B, Channel 0	C19, E17, F1, G1, G17, G18, G2, H1, J17, W10	A14, C14, D3, E1, E13, E15, E3, F3, G13, R5
MSS_EPWMB1	O	Master sub-system, PWM B, Channel 1	B18, E17, F16, G17, G19, G2, T10	A12, C14, D14, E1, E13, E14, N4
MSS_EPWMB_SYNCI	I	Master sub-system, PWM B, Sync Input	B3, V9, W16	B4, P10, P4
MSS_EPWMB_SYNCO	O	Master sub-system, PWM B, Sync Output	B19, W15	A13, N9

Table 5-9. EPWMC Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_EPWMC0	O	Master sub-system, PWM C, Channel 0	B3, D18, G2, K18, U11	B14, B4, E1, H14, P6
MSS_EPWMC1	O	Master sub-system, PWM C, Channel 1	C17, F18, G18, V11	C12, D13, E15, R6
MSS_EPWMC_SYNCI	I	Master sub-system, PWM C, Sync Input	B18, U15	A12, R11
MSS_EPWMC_SYNCO	O	Master sub-system, PWM C, Sync Output	C17, V15	C12, R10

Table 5-10. EPWM Trip Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_EPWM_TZ0	I	Master sub-system, PWM Trip Signal 0	H2, W14	F1, R8
MSS_EPWM_TZ1	I	Master sub-system, PWM Trip Signal 1	J2, U13	F2, P9
MSS_EPWM_TZ2	I	Master sub-system, PWM Trip Signal 2	H1, V14	F3, R9

5.3.7 GPIO Signal Descriptions

Table 5-11. MSS GPIO Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_GPIO_0	IO	Master sub-system GPIO	H1, V9	B10, F3, P4
MSS_GPIO_1	IO	Master sub-system GPIO	J1, J2	A10, F2, G1
MSS_GPIO_2	IO	Master sub-system GPIO	H2, K2, U18	A9, F1, G2, N13
MSS_GPIO_3	IO	Master sub-system GPIO	B2, H18, W18	B3, C9, F15, P12
MSS_GPIO_4	IO	Master sub-system GPIO	D19, G17	B15, B9, E13
MSS_GPIO_5	IO	Master sub-system GPIO	D18, G19	B14, E14
MSS_GPIO_6	IO	Master sub-system GPIO	F19, F2	C1, D15

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Table 5-11. MSS GPIO Signal Descriptions (continued)

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_GPIO_7	IO	Master sub-system GPIO	E1, G18	D1, E15
MSS_GPIO_8	IO	Master sub-system GPIO	B3, C2, U18	B2, B4, N13
MSS_GPIO_9	IO	Master sub-system GPIO	B19, D2, W18	A13, A2, A8, P12
MSS_GPIO_10	IO	Master sub-system GPIO	B18, D1	A12, B8, C2
MSS_GPIO_11	IO	Master sub-system GPIO	C17, E2	A7, B1, C12
MSS_GPIO_12	IO	Master sub-system GPIO	A18, E18	B12, C15
MSS_GPIO_13	IO	Master sub-system GPIO	B17, H1	A11, F3
MSS_GPIO_14	IO	Master sub-system GPIO	A17, G1	B11, E3
MSS_GPIO_15	IO	Master sub-system GPIO	B16, G2	C11, E1
MSS_GPIO_16	IO	Master sub-system GPIO	C15, J2	B7, F2
MSS_GPIO_17	IO	Master sub-system GPIO	A16, C3	C7, D4
MSS_GPIO_18	IO	Master sub-system GPIO	B15, D4	B6, C4
MSS_GPIO_19	IO	Master sub-system GPIO	A15, C1	A3, A6
MSS_GPIO_20	IO	Master sub-system GPIO	B1, B14	A4, B5
MSS_GPIO_21	IO	Master sub-system GPIO	C13, C18	A5, B13
MSS_GPIO_22	IO	Master sub-system GPIO	C19	A14, B10
MSS_GPIO_23	IO	Master sub-system GPIO	C5	A10, C5
MSS_GPIO_24	IO	Master sub-system GPIO	D6	A9, C6
MSS_GPIO_25	IO	Master sub-system GPIO	E3	C9, D2
MSS_GPIO_26	IO	Master sub-system GPIO	H2	B9, F1
MSS_GPIO_27	IO	Master sub-system GPIO	F1	A8, D3
MSS_GPIO_28	IO	Master sub-system GPIO	G3	B8, E2
MSS_GPIO_29	IO	Master sub-system GPIO	E17	A7, C14
MSS_GPIO_30	IO	Master sub-system GPIO	A2, P19	C3, M14
MSS_GPIO_31	IO	Master sub-system GPIO	R19, V16	M15, P11

Table 5-12. RCSS GPIO Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
RCSS_GPIO_32	IO	Radar control sub-system GPIO	R18, U15, V9	N15, P4, R11
RCSS_GPIO_33	IO	Radar control sub-system GPIO	J1, R17, W16	G1, N14, P10
RCSS_GPIO_34	IO	Radar control sub-system GPIO	H2, K2, T18, U18, V15	F1, G2, N13, P15, R10
RCSS_GPIO_35	IO	Radar control sub-system GPIO	H18, T19, W15, W18	F15, N9, P12, P14
RCSS_GPIO_36	IO	Radar control sub-system GPIO	G17, U18, V14	E13, N13, R9
RCSS_GPIO_37	IO	Radar control sub-system GPIO	G19, U13, U19	E14, P13, P9
RCSS_GPIO_38	IO	Radar control sub-system GPIO	F19, V18, W14	D15, R13, R8
RCSS_GPIO_39	IO	Radar control sub-system GPIO	G18, V13, V19	E15, P8, R14
RCSS_GPIO_40	IO	Radar control sub-system GPIO	B3, U17, U18, W13	B4, N12, N13, P7
RCSS_GPIO_41	IO	Radar control sub-system GPIO	B19, U11, W18	A13, P12, P6
RCSS_GPIO_42	IO	Radar control sub-system GPIO	B18, V11, V17	A12, R12, R6
RCSS_GPIO_43	IO	Radar control sub-system GPIO	C17, W11, W17	C12, N11, N5
RCSS_GPIO_44	IO	Radar control sub-system GPIO	A18, U3, V10	B12, P5, R3
RCSS_GPIO_45	IO	Radar control sub-system GPIO	B17, W10, W2	A11, R4, R5

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Table 5-12. RCSS GPIO Signal Descriptions (continued)

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
RCSS_GPIO_46	IO	Radar control sub-system GPIO	A17, J19, T10	B11, G14, N4
RCSS_GPIO_47	IO	Radar control sub-system GPIO	B16, H19, W12	C11, F14, N6
RCSS_GPIO_48	IO	Radar control sub-system GPIO	C15, V12	B7, R7
RCSS_GPIO_49	IO	Radar control sub-system GPIO	A16, E19	C13, C7
RCSS_GPIO_50	IO	Radar control sub-system GPIO	B15, F16	B6, D14
RCSS_GPIO_51	IO	Radar control sub-system GPIO	A15, F18	A6, D13
RCSS_GPIO_52	IO	Radar control sub-system GPIO	B14, J18	B5, G15
RCSS_GPIO_53	IO	Radar control sub-system GPIO	C13, J17	A5, G13
RCSS_GPIO_54	IO	Radar control sub-system GPIO	K18	B10, H14
RCSS_GPIO_55	IO	Radar control sub-system GPIO	K16	A10, H13
RCSS_GPIO_56	IO	Radar control sub-system GPIO	L17	A9, J15
RCSS_GPIO_57	IO	Radar control sub-system GPIO	L18	C9, J14
RCSS_GPIO_58	IO	Radar control sub-system GPIO	K19	B9, H15
RCSS_GPIO_59	IO	Radar control sub-system GPIO	M19	A8, K15
RCSS_GPIO_60	IO	Radar control sub-system GPIO	L19	B8, J13
RCSS_GPIO_61	IO	Radar control sub-system GPIO	M18	A7, L14
RCSS_GPIO_62	IO	Radar control sub-system GPIO	N19	L15
RCSS_GPIO_63	IO	Radar control sub-system GPIO	P18	M13

5.3.8 I2C Signal Descriptions

Table 5-13. I2CA Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_I2CA_SCL	IO	Master sub-system, I2C A, serial clock	A18, C1, C19, F18, G2, U15	A14, A3, A7, B12, D13, E1, R11
MSS_I2CA_SDA	IO	Master sub-system, I2C A, serial data	B1, B17, C17, C18, F16, G1, V16	A11, A4, B13, B8, C12, D14, E3, P11

Table 5-14. RCSS I2CB Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
RCSS_I2CB_SCL	IO	Radar control sub-system I2C B, serial clock	B16, B3, G17, M18, T19, U17	B4, C11, C9, E13, L14, N12, P14
RCSS_I2CB_SDA	IO	Radar control sub-system I2C B, serial data	A17, G18, H18, K19, L19, T18, V19	A9, B11, E15, F15, H15, J13, P15, R14

Table 5-15. RCSS I2CA Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
RCSS_I2CA_SCL	IO	Radar control sub-system I2C A, serial clock	B14, F19, M19, R17, V18, W12	A10, B5, D15, K15, N14, N6, R13
RCSS_I2CA_SDA	IO	Radar control sub-system I2C A, serial data	A15, G19, R18, T10, U19	A6, B10, E14, N15, N4, P13

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5.3.9 Clock Signal Descriptions

Table 5-16. Input Clock Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
CLKM	I	Primary crystal or oscillator reference clock input, negative input	U1	N1
CLKP	I	Primary crystal or oscillator reference clock input, positive input	V1	P1
XREF_CLK0	IO	External reference clock input 0	J1	G1
XREF_CLK1	IO	External reference clock input 1	K2	G2

Table 5-17. Output Clock Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MCU_CLKOUT	O	MCU output reference clock	E3, J1	D2, G1
OBS_CLKOUT	O	Observation clock output	E3, F1, G17, H18	D2, D3, E13, F15
OSCCLKOUT	O	Reference clock ouput	T4	R2
PMIC_CLKOUT	O	PMIC synchronization clock output	F1, H1, H2, K2	D3, F1, F3, G2
RCOSC_CLK	O	Internal RCOSC clock output	A2, B2, E17	B3, C14, C3
RCSS_ATL_CLK0	IO	Audio Tracking Logic Clock 0	B19, H18	A13, F15
RCSS_ATL_CLK1	IO	Audio Tracking Logic Clock 1	G17	E13

5.3.10 JTAG Signal Descriptions

Table 5-18. JTAG Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
TCK	I	JTAG test clock	C3	D4
TDI	I	JTAG test data input	C5	C5
TDO	O	JTAG test data output	D6	C6
TMS	IO	JTAG test mode select	D4	C4

5.3.11 LVDS Signal Descriptions

Table 5-19. LVDS Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
LVDS_CLKM	O	LVDS/Aurora Transmitter, Clock, Negative Polarity	W7	
LVDS_CLKP	O	LVDS/Aurora Transmitter, Clock, Positive Polarity	V7	
LVDS_FRCLKM	O	LVDS/Aurora Transmitter, Frame Clock, Negative Polarity	W8	
LVDS_FRCLKP	O	LVDS/Aurora Transmitter, Frame Clock, Positive Polarity	V8	
LVDS_TXM0	O	LVDS/Aurora Transmitter, Data Output, Negative Polarity, Lane 0	V6	
LVDS_TXM1	O	LVDS/Aurora Transmitter, Data Output, Negative Polarity, Lane 1	V5	
LVDS_TXM2	O	LVDS/Aurora Transmitter, Data Output, Negative Polarity, Lane 2	V4	
LVDS_TXM3	O	LVDS/Aurora Transmitter, Data Output, Negative Polarity, Lane 3	V3	

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Table 5-19. LVDS Signal Descriptions (continued)

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
LVDS_TXP0	O	LVDS/Aurora Transmitter, Data Output, Positive Polarity, Lane 0	W6	
LVDS_TXP1	O	LVDS/Aurora Transmitter, Data Output, Positive Polarity, Lane 1	W5	
LVDS_TXP2	O	LVDS/Aurora Transmitter, Data Output, Positive Polarity, Lane 2	W4	
LVDS_TXP3	O	LVDS/Aurora Transmitter, Data Output, Positive Polarity, Lane 3	W3	

5.3.12 MCAN Signal Descriptions

Table 5-20. MCANA Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_MCANA_RX	I	Master sub-system, CAN-FD A, receiver	B2, C1, D18, D4, E2, G2, W13	A3, B1, B14, B3, C4, E1, P7
MSS_MCANA_TX	O	Master sub-system, CAN-FD A, transmitter	A2, B1, C3, D1, D19, G1, V13	A4, B15, C2, C3, D4, E3, P8

Table 5-21. MCANB Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_MCANB_RX	I	Master sub-system, CAN-FD B, receiver	B2, C1, C18, V10	A3, B13, B3, P5
MSS_MCANB_TX	O	Master sub-system, CAN-FD B, transmitter	A2, B1, C19, W11	A14, A4, C3, N5

5.3.13 MCASP Signal Descriptions

Table 5-22. MCASPA Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
RCSS_MCASPA_ACLKR	IO	Multichannel Audio Serial Port A Bit Clk, receiver	A18, K18	B12, H14
RCSS_MCASPA_ACLKX	IO	Multichannel Audio Serial Port A Bit Clk, transmitter	B18, L17	A12, J15
RCSS_MCASPA_AHCLKX	IO	Multichannel Audio Serial Port A High Frequency Clk, transmitter	B19, L18	A13, J14
RCSS_MCASPA_DAT0	IO	Multichannel Audio Serial Port A Data	A17, J18	B11, G15
RCSS_MCASPA_DAT1	IO	Multichannel Audio Serial Port A Data	B16, F18	C11, D13
RCSS_MCASPA_DAT2	IO	Multichannel Audio Serial Port A Data	C15, F16	B7, D14
RCSS_MCASPA_DAT3	IO	Multichannel Audio Serial Port A Data	A16, E19	C13, C7
RCSS_MCASPA_DAT4	IO	Multichannel Audio Serial Port A Data	B15	B6
RCSS_MCASPA_DAT5	IO	Multichannel Audio Serial Port A Data	A15	A6
RCSS_MCASPA_DAT6	IO	Multichannel Audio Serial Port A Data	B14	B5
RCSS_MCASPA_DAT7	IO	Multichannel Audio Serial Port A Data	C13	A5
RCSS_MCASPA_DAT8	IO	Multichannel Audio Serial Port A Data	A17	B10, B11
RCSS_MCASPA_DAT9	IO	Multichannel Audio Serial Port A Data	B16	A10, C11
RCSS_MCASPA_DAT10	IO	Multichannel Audio Serial Port A Data	C15	A9, B7
RCSS_MCASPA_DAT11	IO	Multichannel Audio Serial Port A Data	A16	C7, C9
RCSS_MCASPA_DAT12	IO	Multichannel Audio Serial Port A Data	B15	B6, B9
RCSS_MCASPA_DAT13	IO	Multichannel Audio Serial Port A Data	A15	A6, A8
RCSS_MCASPA_DAT14	IO	Multichannel Audio Serial Port A Data	B14	B5, B8

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Table 5-22. MCASPA Signal Descriptions (continued)

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
RCSS_MCASPA_DAT15	IO	Multichannel Audio Serial Port A Data	C13	A5, A7
RCSS_MCASPA_FSR	IO	Multichannel Audio Serial Port A Frame Sync Clk, receiver	B17, J17	A11, G13
RCSS_MCASPA_FSX	IO	Multichannel Audio Serial Port A Frame Sync Clk, transmitter	C17, K16	C12, H13

Table 5-23. MCASPB Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
RCSS_MCASPB_ACLKR	IO	Multichannel Audio Serial Port B Bit Clk, receiver	N19, W13	L15, P7
RCSS_MCASPB_ACLKX	IO	Multichannel Audio Serial Port B Bit Clk, transmitter	K19, L19, W14	H15, J13, R8
RCSS_MCASPB_AHCLKR	IO	Multichannel Audio Serial Port B High Frequency Clk, receiver	G3, M19	E2, K15
RCSS_MCASPB_AHCLKX	IO	Multichannel Audio Serial Port B High Frequency Clk, transmitter	V12	R7
RCSS_MCASPB_DAT0	IO	Multichannel Audio Serial Port B Data	P19, V11	M14, R6
RCSS_MCASPB_DAT1	IO	Multichannel Audio Serial Port B Data	R19, W11	M15, N5
RCSS_MCASPB_DAT2	IO	Multichannel Audio Serial Port B Data	V10	P5
RCSS_MCASPB_DAT3	IO	Multichannel Audio Serial Port B Data	W10	R5
RCSS_MCASPB_DAT4	IO	Multichannel Audio Serial Port B Data	T10	N4
RCSS_MCASPB_DAT5	IO	Multichannel Audio Serial Port B Data	W12	N6
RCSS_MCASPB_FSR	IO	Multichannel Audio Serial Port B Frame Sync Clk, receiver	P18, U11	M13, P6
RCSS_MCASPB_FSX	IO	Multichannel Audio Serial Port B Frame Sync Clk, transmitter	M18, V13	L14, P8

Table 5-24. MCASPC Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
RCSS_MCASPC_ACLKR	IO	Multichannel Audio Serial Port C Bit Clk, receiver	V15	R10
RCSS_MCASPC_ACLKX	IO	Multichannel Audio Serial Port C Bit Clk, transmitter	V14	R9
RCSS_MCASPC_AHCLKX	IO	Multichannel Audio Serial Port C High Frequency Clk, transmitter	U13	P9
RCSS_MCASPC_DAT0	IO	Multichannel Audio Serial Port C Data	U15	R11
RCSS_MCASPC_DAT1	IO	Multichannel Audio Serial Port C Data	V16	P11
RCSS_MCASPC_DAT2	IO	Multichannel Audio Serial Port C Data	W17	N11
RCSS_MCASPC_DAT3	IO	Multichannel Audio Serial Port C Data	V17	R12
RCSS_MCASPC_DAT4	IO	Multichannel Audio Serial Port C Data	W18	P12
RCSS_MCASPC_DAT5	IO	Multichannel Audio Serial Port C Data	U17	N12
RCSS_MCASPC_FSR	IO	Multichannel Audio Serial Port C Frame Sync Clk, receiver	W16	P10
RCSS_MCASPC_FSX	IO	Multichannel Audio Serial Port C Frame Sync Clk, transmitter	W15	N9

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5.3.14 Ethernet Signal Descriptions

Table 5-25. MDIO Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_MDIO_CLK	O	Master sub-system, Ethernet MDIO clock	R19	M15
MSS_MDIO_DATA	IO	Master sub-system, Ethernet MDIO data	P19	M14

Table 5-26. MII Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_MII_COL	I	Master sub-system, Ethernet MII, collision detect	E19	C13
MSS_MII_CRS	I	Master sub-system, Ethernet MII, carrier sense	F16	D14
MSS_MII_RXCLK	I	Master sub-system, Ethernet MII, receive clock	M19	K15
MSS_MII_RXD0	I	Master sub-system, Ethernet MII, receive data 0	P18	M13
MSS_MII_RXD1	I	Master sub-system, Ethernet MII, receive data 1	N19	L15
MSS_MII_RXD2	I	Master sub-system, Ethernet MII, receive data 2	M18	L14
MSS_MII_RXD3	I	Master sub-system, Ethernet MII, receive data 3	K19, L19	H15, J13
MSS_MII_RXDV	I	Master sub-system, Ethernet MII, receive data valid	J17	G13
MSS_MII_RXER	I	Master sub-system, Ethernet MII, receive error	F18	D13
MSS_MII_TXD0	O	Master sub-system, Ethernet MII, transmit data 0	L18	J14
MSS_MII_TXD1	O	Master sub-system, Ethernet MII, transmit data 1	L17	J15
MSS_MII_TXD2	O	Master sub-system, Ethernet MII, transmit data 2	K16	H13
MSS_MII_TXD3	O	Master sub-system, Ethernet MII, transmit data 3	K18	H14
MSS_MII_TXEN	O	Master sub-system, Ethernet MII, transmit enable	J18	G15

Table 5-27. RMII Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_RMII_CRS_DV	I	Master sub-system, Ethernet RMII, carrier sense/receive data valid	F16	D14
MSS_RMII_REFCLK	IO	Master sub-system, Ethernet RMII, reference clock	E19	C13
MSS_RMII_RXD0	I	Master sub-system, Ethernet RMII, receive data 0	P18	M13
MSS_RMII_RXD1	I	Master sub-system, Ethernet RMII, receive data 1	N19	L15
MSS_RMII_RXER	I	Master sub-system, Ethernet RMII, receive error	F18	D13
MSS_RMII_TXD0	O	Master sub-system, Ethernet RMII, transmit data 0	L18	J14
MSS_RMII_TXD1	O	Master sub-system, Ethernet RMII, transmit data 1	L17	J15
MSS_RMII_TXEN	O	Master sub-system, Ethernet RMII, transmit enable	J18	G15

Table 5-28. RGMII Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_RGMII_RCLK	I	Master sub-system, Ethernet RGMII, receive clock	M19	K15

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Table 5-28. RGMII Signal Descriptions (continued)

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_RGMII_RCTL	I	Master sub-system, Ethernet RGMII, receive control	J17	G13
MSS_RGMII_RD0	I	Master sub-system, Ethernet RGMII, receiver 0	P18	M13
MSS_RGMII_RD1	I	Master sub-system, Ethernet RGMII, receiver 1	N19	L15
MSS_RGMII_RD2	I	Master sub-system, Ethernet RGMII, receiver 2	M18	L14
MSS_RGMII_RD3	I	Master sub-system, Ethernet RGMII, receiver 3	K19, L19	H15, J13
MSS_RGMII_TCTL	O	Master sub-system, Ethernet RGMII, transmit control	J18	G15
MSS_RGMII_TD0	O	Master sub-system, Ethernet RGMII, transmitter 0	L18	J14
MSS_RGMII_TD1	O	Master sub-system, Ethernet RGMII, transmitter 1	L17	J15
MSS_RGMII_TD2	O	Master sub-system, Ethernet RGMII, transmitter 2	K16	H13
MSS_RGMII_TD3	O	Master sub-system, Ethernet RGMII, transmitter 3	K18	H14

5.3.15 GPIO Signal Descriptions

Table 5-29. MSS GPIO Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_GPIO_0	IO	Master sub-system GPIO	H1, V9	B10, F3, P4
MSS_GPIO_1	IO	Master sub-system GPIO	J1, J2	A10, F2, G1
MSS_GPIO_2	IO	Master sub-system GPIO	H2, K2, U18	A9, F1, G2, N13
MSS_GPIO_3	IO	Master sub-system GPIO	B2, H18, W18	B3, C9, F15, P12
MSS_GPIO_4	IO	Master sub-system GPIO	D19, G17	B15, B9, E13
MSS_GPIO_5	IO	Master sub-system GPIO	D18, G19	B14, E14
MSS_GPIO_6	IO	Master sub-system GPIO	F19, F2	C1, D15
MSS_GPIO_7	IO	Master sub-system GPIO	E1, G18	D1, E15
MSS_GPIO_8	IO	Master sub-system GPIO	B3, C2, U18	B2, B4, N13
MSS_GPIO_9	IO	Master sub-system GPIO	B19, D2, W18	A13, A2, A8, P12
MSS_GPIO_10	IO	Master sub-system GPIO	B18, D1	A12, B8, C2
MSS_GPIO_11	IO	Master sub-system GPIO	C17, E2	A7, B1, C12
MSS_GPIO_12	IO	Master sub-system GPIO	A18, E18	B12, C15
MSS_GPIO_13	IO	Master sub-system GPIO	B17, H1	A11, F3
MSS_GPIO_14	IO	Master sub-system GPIO	A17, G1	B11, E3
MSS_GPIO_15	IO	Master sub-system GPIO	B16, G2	C11, E1
MSS_GPIO_16	IO	Master sub-system GPIO	C15, J2	B7, F2
MSS_GPIO_17	IO	Master sub-system GPIO	A16, C3	C7, D4
MSS_GPIO_18	IO	Master sub-system GPIO	B15, D4	B6, C4
MSS_GPIO_19	IO	Master sub-system GPIO	A15, C1	A3, A6
MSS_GPIO_20	IO	Master sub-system GPIO	B1, B14	A4, B5
MSS_GPIO_21	IO	Master sub-system GPIO	C13, C18	A5, B13
MSS_GPIO_22	IO	Master sub-system GPIO	C19	A14, B10
MSS_GPIO_23	IO	Master sub-system GPIO	C5	A10, C5
MSS_GPIO_24	IO	Master sub-system GPIO	D6	A9, C6
MSS_GPIO_25	IO	Master sub-system GPIO	E3	C9, D2

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Table 5-29. MSS GPIO Signal Descriptions (continued)

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_GPIO_26	IO	Master sub-system GPIO	H2	B9, F1
MSS_GPIO_27	IO	Master sub-system GPIO	F1	A8, D3
MSS_GPIO_28	IO	Master sub-system GPIO	G3	B8, E2
MSS_GPIO_29	IO	Master sub-system GPIO	E17	A7, C14
MSS_GPIO_30	IO	Master sub-system GPIO	A2, P19	C3, M14
MSS_GPIO_31	IO	Master sub-system GPIO	R19, V16	M15, P11

Table 5-30. RCSS GPIO Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
RCSS_GPIO_32	IO	Radar control sub-system GPIO	R18, U15, V9	N15, P4, R11
RCSS_GPIO_33	IO	Radar control sub-system GPIO	J1, R17, W16	G1, N14, P10
RCSS_GPIO_34	IO	Radar control sub-system GPIO	H2, K2, T18, U18, V15	F1, G2, N13, P15, R10
RCSS_GPIO_35	IO	Radar control sub-system GPIO	H18, T19, W15, W18	F15, N9, P12, P14
RCSS_GPIO_36	IO	Radar control sub-system GPIO	G17, U18, V14	E13, N13, R9
RCSS_GPIO_37	IO	Radar control sub-system GPIO	G19, U13, U19	E14, P13, P9
RCSS_GPIO_38	IO	Radar control sub-system GPIO	F19, V18, W14	D15, R13, R8
RCSS_GPIO_39	IO	Radar control sub-system GPIO	G18, V13, V19	E15, P8, R14
RCSS_GPIO_40	IO	Radar control sub-system GPIO	B3, U17, U18, W13	B4, N12, N13, P7
RCSS_GPIO_41	IO	Radar control sub-system GPIO	B19, U11, W18	A13, P12, P6
RCSS_GPIO_42	IO	Radar control sub-system GPIO	B18, V11, V17	A12, R12, R6
RCSS_GPIO_43	IO	Radar control sub-system GPIO	C17, W11, W17	C12, N11, N5
RCSS_GPIO_44	IO	Radar control sub-system GPIO	A18, U3, V10	B12, P5, R3
RCSS_GPIO_45	IO	Radar control sub-system GPIO	B17, W10, W2	A11, R4, R5
RCSS_GPIO_46	IO	Radar control sub-system GPIO	A17, J19, T10	B11, G14, N4
RCSS_GPIO_47	IO	Radar control sub-system GPIO	B16, H19, W12	C11, F14, N6
RCSS_GPIO_48	IO	Radar control sub-system GPIO	C15, V12	B7, R7
RCSS_GPIO_49	IO	Radar control sub-system GPIO	A16, E19	C13, C7
RCSS_GPIO_50	IO	Radar control sub-system GPIO	B15, F16	B6, D14
RCSS_GPIO_51	IO	Radar control sub-system GPIO	A15, F18	A6, D13
RCSS_GPIO_52	IO	Radar control sub-system GPIO	B14, J18	B5, G15
RCSS_GPIO_53	IO	Radar control sub-system GPIO	C13, J17	A5, G13
RCSS_GPIO_54	IO	Radar control sub-system GPIO	K18	B10, H14
RCSS_GPIO_55	IO	Radar control sub-system GPIO	K16	A10, H13
RCSS_GPIO_56	IO	Radar control sub-system GPIO	L17	A9, J15
RCSS_GPIO_57	IO	Radar control sub-system GPIO	L18	C9, J14
RCSS_GPIO_58	IO	Radar control sub-system GPIO	K19	B9, H15
RCSS_GPIO_59	IO	Radar control sub-system GPIO	M19	A8, K15
RCSS_GPIO_60	IO	Radar control sub-system GPIO	L19	B8, J13
RCSS_GPIO_61	IO	Radar control sub-system GPIO	M18	A7, L14
RCSS_GPIO_62	IO	Radar control sub-system GPIO	N19	L15
RCSS_GPIO_63	IO	Radar control sub-system GPIO	P18	M13

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5.3.16 Power Supply Signal Descriptions

Table 5-31. Power Supply Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
VBGAP	PWR	Bandgap Output	T1	M1
VDD	PWR	1.2V Core Digital Power	E11, E9, F11, F9, G14, G15, G5, G6, J14, J15, J5, J6, L14, L15, L5, L6, N14, N15, N5, N6, P11, P9, R11, R9	D7, D9, E11, E12, E4, E5, H11, H12, H4, H5, L11, L12, L4, L5, M7, M9
VDD_SRAM1	PWR	1.2V SRAM Digital Power	N17	K14
VDD_SRAM2	PWR	1.2V SRAM Digital Power	J3	G3
VDD_SRAM3	PWR	1.2V SRAM Digital Power	T8	M6
VIOIN	PWR	1.8V/3.3V Digital I/O Power	D14, F4, H16, K4, P16, R5, T12	C10, F13, F4, K13, N10
VIOIN_18	PWR	1.8V Digital I/O Power	E15, H4, M16, M4, T14	C8, J12, J4, N8
VIOIN_18ADC	PWR	1.8V ADC Power	R3	M2
VIOIN_18CLK	PWR	1.8V Clock Power	U2	N2
VIOIN_18CSI	PWR	1.8V CSI Power	C11, C9	
VIOIN_18LVDS	PWR	1.8V LVDS Power	U5, U7	
VNWA	PWR	1.2V N-well bias	N18	L13
VPP	PWR	E-fuse Programming Voltage	U9	N7
VSS	GND	Ground Return	A1, A14, A19, A3, C7, D10, D12, D16, D8, E12, E13, E5, E7, E8, F12, F13, F14, F6, F7, F8, G10, G11, G12, G13, G7, G8, G9, H10, H11, H12, H13, H7, H8, H9, J10, J11, J12, J13, J7, J8, J9, K10, K11, K12, K13, K7, K8, K9, L10, L11, L12, L13, L7, L8, L9, M10, M11, M12, M13, M7, M8, M9, N10, N11, N12, N13, N7, N8, N9, P12, P13, P14, P6, P7, P8, R12, R13, R15, R7, R8, T16, T6, V2, W1, W19, W9	A1, A15, D10, D11, D12, D5, D6, D8, E10, E6, E7, E8, E9, F10, F11, F12, F5, F6, F7, F8, F9, G10, G11, G12, G4, G5, G6, G7, G8, G9, H10, H6, H7, H8, H9, J10, J11, J5, J6, J7, J8, J9, K10, K11, K12, K4, K5, K6, K7, K8, K9, L10, L6, L7, L8, L9, M10, M11, M12, M4, M5, M8, P2, R1, R15

5.3.17 QSPI Signal Descriptions

Table 5-32. QSPI Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_QSPI_CLK	IO	Master sub-system, QSPI clock	E1	D1
MSS_QSPI_CS	O	Master sub-system, QSPI chip-select	F2	C1
MSS_QSPI_D0	IO	Master sub-system, QSPI input/output 0	C2	B2

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Table 5-32. QSPI Signal Descriptions (continued)

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_QSPI_D1	I	Master sub-system, QSPI input/output 1	D2	A2
MSS_QSPI_D2	I	Master sub-system, QSPI input/output 2	D1	C2
MSS_QSPI_D3	I	Master sub-system, QSPI input/output 3	E2	B1

5.3.18 Reserverd Signal Descriptions

Table 5-33. Reserved Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
Reserved1	Reserved	Reserved. VSS short to PCB	P4	L3
Reserved2	Reserved	Reserved. VSS short to PCB	N3	K3

5.3.19 UART Signal Descriptions

Table 5-34. RS232 Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_RS232_RX	IO	Master sub-system, debug RS232 (UART) receiver	A18, G2	B12, E1
MSS_RS232_TX	IO	Master sub-system, debug RS232 (UART) transmitter	B17, G1	A11, E3

Table 5-35. RCSS UARTA Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
RCSS_UARTA_CTS	I	Radar control sub-system, UART A, UART A, Clear to Send	A18, G17	A8, B12, E13
RCSS_UARTA_RTS	IO	Radar control sub-system, UART A, Request to Send	C17, H18	B9, C12, F15
RCSS_UARTA_RX	I	Radar control sub-system, UART A, UART A, receiver	B16, B18, J19	A12, A7, C11, G14
RCSS_UARTA_TX	O	Radar control sub-system UART A, transmitter	A17, B17, B19, H19	A11, A13, B11, B8, F14

5.3.20 SPI Signal Descriptions

Table 5-36. SPIA Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_MIBSPIA_CLK	IO	Master sub-system, SPI A, clock	B2, G19, T18	B3, E14, P15
MSS_MIBSPIA_CS0	IO	Master sub-system, SPI A, chip-select 0	A2, F19, T19	C3, D15, P14
MSS_MIBSPIA_HOSTIRQ	O	Master sub-system, SPI A, host interrupt input	E18, G18, U18	C15, E15, N13
MSS_MIBSPIA_MISO	IO	Master sub-system, SPI A, master input, slave output	B1, G17, R17	A4, E13, N14
MSS_MIBSPIA_MOSI	IO	Master sub-system, SPI A, master output, slave input	C1, H18, R18	A3, F15, N15

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Table 5-37. SPIB Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
MSS_MIBSPIB_CLK	IO	Master sub-system, SPI B, clock	D18, E1, V19	B14, D1, R14
MSS_MIBSPIB_CS0	IO	Master sub-system, SPI B, chip-select 0	D19, F2, U17	B15, C1, N12
MSS_MIBSPIB_CS1	IO	Master sub-system, SPI B, chip-select 1	E17, E18, J2, W18	C14, C15, F2, P12
MSS_MIBSPIB_CS2	IO	Master sub-system, SPI B, chip-select 2	D2, E17, J2, U18	A2, C14, F2, N13
MSS_MIBSPIB_MISO	IO	Master sub-system, SPI B, master input, slave output	C19, C2, V18	A14, B2, R13
MSS_MIBSPIB_MOSI	IO	Master sub-system, SPI B, master output, slave input	C18, D2, U19	A2, B13, P13

Table 5-38. RCSS SPIA Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
RCSS_MIBSPIA_CLK	IO	Radar control sub-system SPI A, clock	T18	P15
RCSS_MIBSPIA_CS0	IO	Radar control sub-system SPI A, chip-select 0	T19	P14
RCSS_MIBSPIA_CS1	IO	Radar control sub-system SPI B, chip-select 1	U18	N13
RCSS_MIBSPIA_MISO	IO	Radar control sub-system SPI A, master input, slave output	R17	N14
RCSS_MIBSPIA_MOSI	IO	Radar control sub-system SPI A, master output, slave input	R18	N15

Table 5-39. RCSS SPIB Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
RCSS_MIBSPIB_CLK	IO	Radar control sub-system SPI B, clock	V19	R14
RCSS_MIBSPIB_CS0	IO	Radar control sub-system SPI B, chip-select 0	U17	N12
RCSS_MIBSPIB_CS1	IO	Radar control sub-system SPI B, chip-select 1	W18	P12
RCSS_MIBSPIB_MISO	IO	Radar control sub-system SPI B, master input, slave output	V18	R13
RCSS_MIBSPIB_MOSI	IO	Radar control sub-system SPI B, master output, slave input	U19	P13

5.3.21 System Signal Descriptions

Table 5-40. System Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
SYNC_IN	I	Low frequency Synchronization signal input	G3	E2

5.3.22 Trace Signal Descriptions

Table 5-41. Trace Signal Descriptions

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
TRACE_CLK	O	Trace clock	W12	N6
TRACE_CTL	O	Trace control	V12	R7
TRACE_DATA_0	O	Trace data	V16	P11
TRACE_DATA_1	O	Trace data	U15	R11
TRACE_DATA_2	O	Trace data	W16	P10
TRACE_DATA_3	O	Trace data	V15	R10
TRACE_DATA_4	O	Trace data	W15	N9

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Table 5-41. Trace Signal Descriptions (continued)

Signal Name	Signal Type	Description	ZCE PIN	NZN PIN
TRACE_DATA_5	O	Trace data	V14	R9
TRACE_DATA_6	O	Trace data	U13	P9
TRACE_DATA_7	O	Trace data	W14	R8
TRACE_DATA_8	O	Trace data	V13	P8
TRACE_DATA_9	O	Trace data	W13	P7
TRACE_DATA_10	O	Trace data	U11	P6
TRACE_DATA_11	O	Trace data	V11	R6
TRACE_DATA_12	O	Trace data	W11	N5
TRACE_DATA_13	O	Trace data	V10	P5
TRACE_DATA_14	O	Trace data	W10	R5
TRACE_DATA_15	O	Trace data	T10	N4

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5.4 Pin Connectivity Requirements

This section describes connectivity requirements for package balls that have specific connectivity requirements and unused package balls.

Note

All power balls must be supplied with the voltages specified in the *Recommended Operating Conditions* section, unless otherwise specified.

Note

For additional clarification, "leave unconnected" or "no connect" (NC) means **no** signal traces can be connected to these device ball numbers.

Note

See associated AM273x Hardware Design Guide for further details and design context.

Table 5-42. Connectivity Requirements - AM273x ZCE Package

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
V1	CLKP	Crystal oscillator excitation output. Can be attached to external crystal terminal or driven with 1.8 V oscillator output.
U1	CLKM	Crystal oscillator excitation input. Can be attached to external crystal terminal. If an external 1.8 V oscillator is used to drive the CLKP pin, this CLKM pin should be attached to VSS. Recommend attaching through pull-down resistor.
T1	VBGAP	Should be attached to external 0.047 uF capacitor for proper bandgap voltage operation.
N18, N17, J3, T8	VNWA, VDD_SRAM_1, VDD_SRAM_2, VDD_SRAM_3	All of these power pins must be shorted to common VDD 1.2 V core supply net and provided separate decoupling capacitance on the PCB.
U9	VPP	Should be connected to valid e-fuse programming voltage source, or routed to connector. If unused, this should be completely disconnected on the PCB.
K1, L1, L3	WARM_RESET, NERROR_OUT and NERROR_IN	WARM_RESET, NERROR_OUT and NERROR_IN are implemented as fail-safe, open-drain I/O. These pins require separate, external pull-up resistor to VIOIN to function correctly.
P4, N3	RESERVED1, RESERVED2	Reserved signals. Should be shorted to VSS.

Table 5-43. Connectivity Requirements - AM273x NZN Package

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
P1	CLKP	Crystal oscillator excitation output. Can be attached to external crystal terminal or driven with 1.8 V oscillator output.
N1	CLKM	Crystal oscillator excitation input. Can be attached to external crystal terminal. If an external 1.8 V oscillator is used to drive the CLKP pin, this CLKM pin should be attached to VSS. Recommend attaching through pull-down resistor.
M1	VBGAP	Should be attached to external 0.047 uF capacitor for proper bandgap voltage operation.
L13, K14, G3, M6	VNWA, VDD_SRAM_1, VDD_SRAM_2, VDD_SRAM_3	All of these power pins must be shorted to common VDD 1.2 V core supply net and provided separate decoupling capacitance on the PCB.
N7	VPP	Should be connected to valid e-fuse programming voltage source, or routed to connector. If unused, this should be completely disconnected on the PCB.

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Table 5-43. Connectivity Requirements - AM273x NZN Package (continued)

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
H3, H1, H2	WARM_RESET, NERROR_OUT and NERROR_IN	WARM_RESET, NERROR_OUT and NERROR_IN are implemented as fail-safe, open-drain I/O. These pins require separate, external pull-up resistor to VIOIN to function correctly.
L3, K3	RESERVED1, RESERVED2	Reserved signals. Should be shorted to VSS.

Note

Internal pull resistors are weak and may not source enough current to maintain a valid logic level for some operating conditions. This can be the case when connected to components with leakage to the opposite logic level, or when external noise sources couple to signal traces attached to balls which are only pulled to a valid logic level by the internal resistor. Therefore, external pull resistors are recommended to hold a valid logic level on balls with external connections.

Many of the device IOs are turned off by default and external pull resistors may be required to hold inputs of any attached device in a valid logic state until software initializes the respective IOs. The state of configurable device IOs are defined in the BALL STATE DURING RESET RX/TX/PULL and BALL STATE AFTER RESET RX/TX/PULL columns of the *Pin Attributes* table. Any IO with its input buffer (RX) turned off is allowed to float without damaging the device. However, any IO with its input buffer (RX) turned on shall never be allowed to float to any potential between V_{ILSS} and V_{IHSS}. The input buffer can enter a high-current state which could damage the IO cell if allowed to float between these levels.

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6 Specifications

6.1 Absolute Maximum Ratings

PARAMETER/PIN(1) (2)	DESCRIPTION		MIN	MAX	UNIT
VDD	1.2V digital power supply		-0.5	1.4	V
VIN_SRAM	1.2V power rail for internal SRAM		-0.5	1.4	V
VNWA	1.2V power rail for SRAM array back bias		-0.5	1.4	V
VIOIN	I/O Supply (3.3V or 1.8V): All LVCMOS1833 I/O would operate on this supply		-0.5	3.8	V
VIOIN_18	1.8V supply for CMOS I/O		-0.5	2	V
VIN_18CLK	1.8V supply for clock module		-0.5	2	V
VIOIN_18DIFF	1.8V supply for CSI2 and LVDS ports		-0.5	2	V
Input Voltage	Dual-voltage LVCMOS inputs, operated at 3.3V or 1.8V (Steady State)		-0.3V to VIOIN +0.3V		V
	Dual-voltage LVCMOS inputs, operated at 3.3V/1.8V (Transient Overshoot/Undershoot)		VIOIN +20% up to 20% of Signal Period		V
	CLKP/CLKN		-0.5	2	V
Clamp Current	Limit clamp current(3)		-20	20	mA
T_J	Operating junction temperature range	Extended Automotive	-40	140	°C
		Extended Industrial	-40	105	
T_{stg}	Storage temperature range after soldered onto PC Board		-55	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) Specifies clamp current that will flow through the internal diode protection cells of the I/O in an overvoltage or undervoltage condition.

6.2 ESD Ratings - Automotive

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ESD stress voltage HBM, per AEC Q100-002(1)	All pins	±2000	V
		ESD stress voltage CDM, per AEC Q100-011	All pins	±500	
			Corner Pins (A1, A19, W1, W19)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Power-On Hours (POH)

PARAMETER(1)	EXTENDED INDUSTRIAL	EXTENDED AUTOMOTIVE
Operating Junction Temperature (T_j)	–40°C to 105°C	–40°C to 140°C
POH at Temperature Profile	See the Extended Industrial Temperature Profile	See the Extended Automotive Temperature Profile

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

6.3.1 Automotive Temperature Profile

Table 6-1. Extended Automotive Temperature Profile

T_J (°C)	HOURS	DAYS	YEARS	PERCENT OF TIME
–40	1200	~50	~0.14	6%
75	4000	~167	~0.46	20%
95	13000	~541	~1.48	65%
130	1600	~67	~0.18	8%
140	200	~8.5	~0.023	1%

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Table 6-1. Extended Automotive Temperature Profile (continued)

T_J (°C)	HOURS	DAYS	YEARS	PERCENT OF TIME
Total	20000	~833	~2.28	100%

6.3.2 Industrial Temperature Profile

Table 6-2. Extended Industrial Temperature Profile

T_J (°C)	TOTAL HOURS	TOTAL DAYS	TOTAL YEARS
95	100000	~4166	~11.41
105(1)	70000	~2916	~7.99

(1) Based on operating at CSI2.0 interface at 50% utilization

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION	MIN	NOM	MAX	UNIT
Power Supply Conditions					
VDD	1.2-V digital power supply	1.14	1.2	1.32	V
VIN-SRAM	1.2-V power rail for internal SRAM	1.14	1.2	1.32	V
VNWA	1.2-V power rail for SRAM array back bias	1.14	1.2	1.32	V
VIOIN	I/O Supply (3.3-V mode): ALL LVCMOS1833 I/O would operate on this supply	3.135	3.3	3.465	V
VIOIN	I/O Supply (1.8-V mode): ALL LVCMOS1833 I/O would operate on this supply	1.71	1.8	1.89	V
VIOIN_18	1.8V supply for LVCMOS1833 I/O	1.71	1.8	1.9	V
VIN_18CLK	1.8V supply for clock module	1.71	1.8	1.9	V
VIN_18ADC	1.8V supply for ADC module	1.71	1.8	1.9	V
VIN_18CSI	1.8V supply for CSI-2 D-PHY buffers	1.71	1.8	1.9	V
VIOIN_18LVDS	1.8V supply for LVDS buffers	1.71	1.8	1.9	V
VPP	1.7V supply for e-Fuse array	1.65	1.7	1.75	V
I/O Conditions					
LVCMOS V_{IH}	LVCMOS18/33 (1.8V mode) Voltage Input High	1.71			V
	LVCMOS18/33 (3.3V mode) Voltage Input High	2.25			V
LVCMOS V_{IL}	LVCMOS18/33 (1.8V mode) Voltage Input Low			0.3 × VIOIN	V
	LVCMOS18/33 (3.3V mode) Voltage Input Low			0.3 × VIOIN	V
LVCMOS V_{OH}	LVCMOS18/33 (1.8 and 3.3V mode) Voltage Output High (I_{OH} = 6 ma)	VIOIN - 0.450			V
LVCMOS V_{OL}	LVCMOS18/33 (1.8V and 3.3V mode) Voltage Output Low(I_{OL} = 6 ma)			0.45	V
NRESET, SOP[4:0] V_{IH}	NRESET, SOP[4:0], (1.8V mode) Voltage Input High	0.96			V
	NRESET, SOP[4:0], (3.3V mode) Voltage Input High	1.57			V
NRESET, SOP[4:0] V_{IL}	NRESET, SOP[4:0], (1.8V mode) Voltage Input Low			0.2	V
	NRESET, SOP[4:0], (3.3V mode) Voltage Input Low			0.3	V
LVDS TX V_{OH}	Voltage Output High			1.5	V
LVDS TX V_{OL}	Voltage Output Low	0.9			V
CSI2 RX V_{IH}(1)	Voltage Input High - LP Mode	0.74			V
CSI2 RX V_{IL}(1)	Voltage Input Low - LP Mode			0.55	V
CSI2 RX V_{IH}(1)	Voltage Input High - HS Mode			0.46	V

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6.4 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION	MIN	NOM	MAX	UNIT
CSI2 RX V_{IL} (1)	Voltage Input Low - HS Mode	-0.04			V
OSC_CLKOUT	Voltage Output High		1.4		V
	Voltage Output Low		VSS		V

(1) CSI2 receivers compatible with MIPI D-PHY standard version 2.1.

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6.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each Operating Performance Point (OPP) for processor clocks and device core clocks.

Note

The OPP voltage and frequency values may change following the silicon characterization result.

Table 6-3 describes the maximum supported frequency per speed grade for the device.

Table 6-3. Device Speed and Memory Grade

DEVICE	GRADE	RAM (MB)	DSP (MHz)	R5FSS (MHz)
AM2731, AM2731-Q1	A	1.5	450	400
AM2732, AM2732-Q1	D	3.5625	450	400
AM2731, AM2731-Q1	L	2	550	400
AM2732, AM2732-Q1	M	3.5625	550	400
AM2731, AM2731-Q1	N	1.5	300	200

6.6 Power Supply Specifications

Table 6-4 describes the four power rails provided from an external power supply and how they map to major sub-systems and power nets of the AM273x device.

Table 6-4. Power Supply Rails Characteristics

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT INPUT POWER NETS ON THE DEVICE
1.8 V	APLL, crystal oscillator, ADC, CSI2, LVDS	Input: VIN18CLK, VIN_18ADC, VIOIN_18DIFF, VIOIN_18LVDS, VIOIN_18CSI
3.3 V (or 1.8 V for 1.8 V I/O mode)	Digital I/O	Input: VIOIN
1.2 V	Core Digital and SRAMs	Input: VDD, VIN_SRAM1, VIN_SRAM2, VIN_SRAM3, VNWA

6.7 I/O Buffer Type and Voltage Rail Dependency

Table 6-5. Buffer Type

BUFFER TYPE (STANDARD)	DESCRIPTION	VOLTAGE RAIL	PERIPHERALS
LVCMOS	Dual voltage 1.8V/3.3V LVCMOS I/O buffer	**VIOIN, VIOIN_18**	**Resets, QSPI, UART, SPI, I^2C, CAN-FD, GPIO, RGMII, MDIO, ePWM, eCAP, JTAG, Trace, SOP, Safety, DMM**
GPADC	General Purpose ADC Input	**VIN_18ADC**	**GPADC**
Clock Subsystem	Clock subsystem crystal or 1.8V single-ended input buffer	**VIN_18CLK**	**CLKP/CLKM**
Clock Subsystem Output	Analog, low-jitter output from clock subsystem	**VIN_18CLK**	**OSC_CLKOUT**
LVDS TX	LVDS high-speed data, differential output buffer	**VIOIN_18DIFF**	**Aurora LVDS**
CSI2.0 RX	MIPI D-PHY CSI2.0 high-speed data, differential input buffer	**VIOIN_18DIFF**	**CSI2**

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6.8 CPU Specifications

Table 6-6. CPU and Hardware Accelerator Specifications

	PARAMETER	MIN	NOM	MAX	UNIT
Main Subsystem (MSS)	**Dual-Core Cortex-R5F, ARMv7** (2)				
	L1 Program Memory (I-Cache) with 64-bit ECC			32	KB
	L1 Data Memory (D-Cache) with 32-bit ECC			32	KB
	L1 Tightly Coupled Memory(3) (TCM) with 32-bit ECC	32		64	KB
	L2 Memory			960	KB
DSP Subsystem (DSS)	**Single Core C66x DSP**				
	Clock Speed			450	MHz
	L1 Program Memory			32	KB
	L1 Data Memory			32	KB
	L2 Memory(1)			384	KB
Shared Memory	Shared L3 Memory 4	1.5		3.5625	MB

(1) C66x L2 memory includes up to 256 KB configuration as RAM or cache
(2) R5F dual-cores configurable as a single, redundant, lock-step device, or two independent cores
(3) R5F maximum 64KB TCM with 32-bit ECC
- In single-core, lock-step mode, the full 64KB L1 TCM is available as 32KB TCMA and 32KB TCMB
- In dual-core, split-mode, each core has 32KB L1 TCM available as 16KB TCMA and 16KB TCMB

(4) Shared L3 memory available to R5F and C66x subsystems

6.9 Thermal Resistance Characteristics for nFBGA Package [ZCE285A]

THERMAL METRICS(1)		°C/W(2) (3)
$R\Theta_{JC}$	Junction-to-case	6.2
$R\Theta_{JB}$	Junction-to-board	5.7
$R\Theta_{JA}$	Junction-to-free air	17.3
Psi_{JT}	Junction-to-package top	1.0
Psi_{JB}	Junction-to-board	5.6

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.10 Thermal Resistance Characteristics for nFBGA Package [NZN225A]

THERMAL METRICS(1)		°C/W(2) (3)
$R\Theta_{JC}$	Junction-to-case	6.1
$R\Theta_{JB}$	Junction-to-board	5.9
$R\Theta_{JA}$	Junction-to-free air	18.2
Psi_{JT}	Junction-to-package top	0.7
Psi_{JB}	Junction-to-board	5.8

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6.11 Power Consumption Summary

Table Table 6-7 summarizes average power consumption of the AM273x device for a set of typical application utilization and thermal parameters. Table Table 6-8 shows hypothetical peak current for the device. Both of these tables can be used to scale power regulator and PCB design. However, specific power utilization of the device is dependent on the software utilization of device cores, accelerators and peripherals and operating temperature. To facilitate accurate power planning, TI provides a power estimation tool (PET) spreadsheet which can be used for estimating device power utilization across a wide number of scenarios. Please see sprad10 for more information.

Table 6-7. Average Power and Current

PARAMETER	SUPPLY NAME	SUPPLY DESCRIPTION	AVERAGE POWER (mW)	AVERAGE CURRENT (mA)
Average Power and Current Consumption for Typical Control and Processing Use-Case: • C66x DSP: 450 MHz, 50% Utilization • R5F Dual Core: 400 MHz, 70% Utilization • CSI2-A/B: 4-Lane, 600 Mbps Operation • SPI: 10% Utilization • Ethernet: 100Mbps Operation, 70% Utilization • CAN: 8Mbps Operation, 10% Utilization • SPI: 25 Mbps Operation, 10% Utilization • T_J= 25 C	VDD	1.2V Core Digital Power	692	576
	VDD_SRAM	1.2V SRAM Power	3	3
	VIOIN	1.8V or 3.3V Digital I/O Power	12	4
	VIOIN_18	1.8V Digital I/O Power	0	0
	VIOIN_18CLK	1.8V Clocking Power	32	18
	VIOIN_18ADC	1.8V ADC Power	3	2
	VIOIN_18CSI	1.8V CSI Power	40	22
	VIOIN_18LVDS	1.8V LVDS Power	125	69
Total Power			907	

Table 6-8. Peak Current

SUPPLY NAME	SUPPLY DESCRIPTION	PEAK CURRENT (mA)
VDD	1.2V Core Digital Power	2315
VDD_SRAM	1.2V SRAM Power	75
VIOIN	1.8V or 3.3V Digital I/O Power	74
VIOIN_18	1.8V Digital I/O Power	1
VIOIN_18CLK	1.8V Clocking Power	18
VIOIN_18ADC	1.8V ADC Power	2
VIOIN_18CSI	1.8V CSI Power	23
VIOIN_18LVDS	1.8V LVDS Power	70

6.12 Timing and Switching Characteristics

6.12.1 Power Supply Sequencing and Reset Timing

The AM273x device expects all external voltage rails and SOP boot mode select lines to be stable before NRESET is de-asserted (brought from VSS level to VIOIN level). Likewise external voltage rails should only be powered down after NRESET is asserted (brought from VIOIN level to VSS level).Figure 6-1 describes the device wake-up and power-down sequence.

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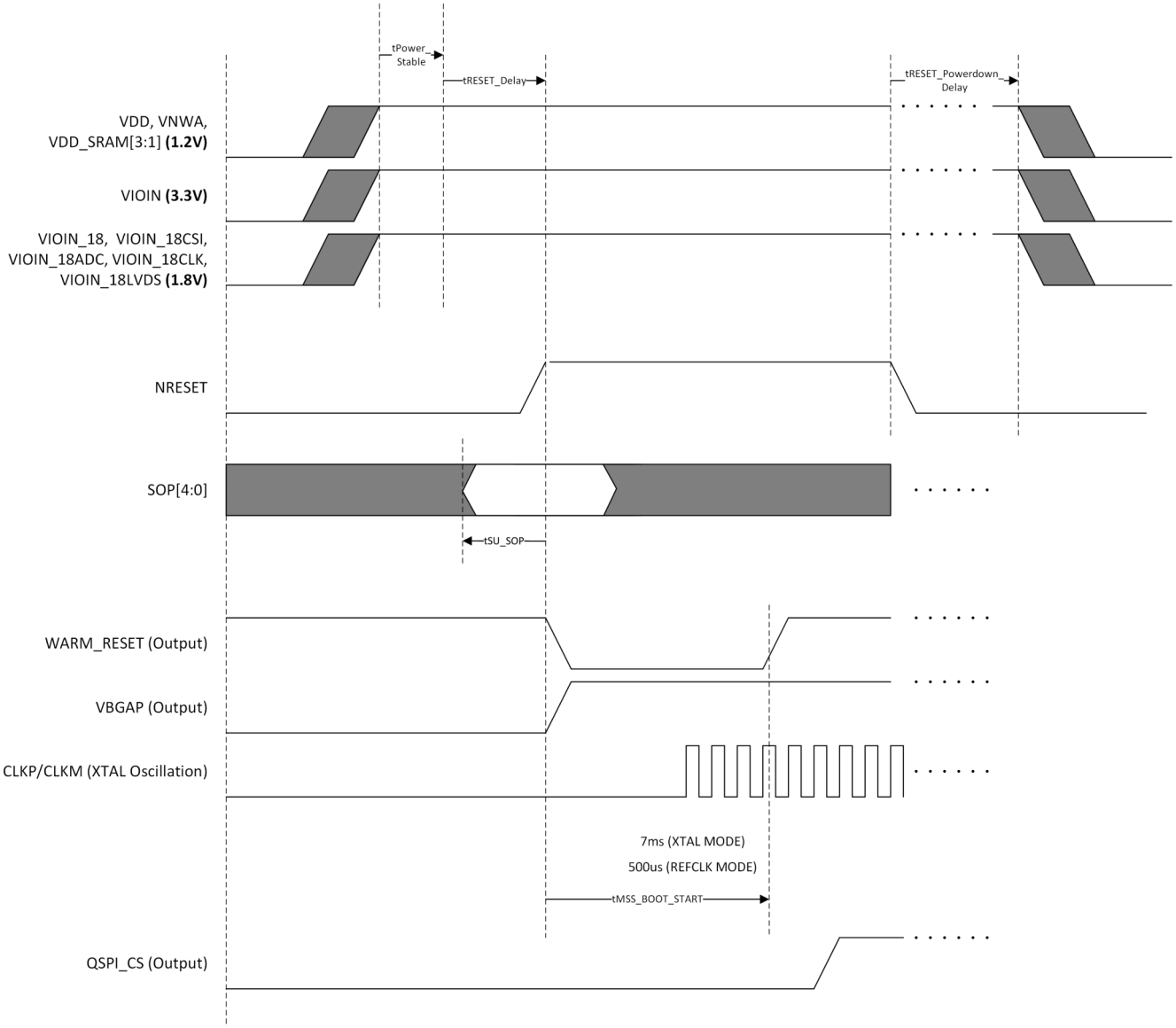


Figure 6-1. Device Wake-up and Power-Down Sequence

Table 6-9 lists the timing values shown in Figure 6-1.

Table 6-9. Device Wake-Up Sequence Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{POWER_STABLE}	Settling time after initial power supply turn-on after which device power nets are at valid, recommended operating conditions. NRESET should not be de-asserted (brought from GND to VIOIN level) before all power pins are at recommended operating point. See Recommended Operating Conditions for recommended operating conditions of all device power pins.	0			ms
t_{RESET_DELAY}	Delay after device power nets are at valid, nominal values, when NRESET can be brought from VSS to VIOIN level. NRESET can be brought from VSS to VIOIN level anytime after power supplies are at recommended operating conditions.	0			ms

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Table 6-9. Device Wake-Up Sequence Timing (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{SU_SOP}	Setup time for SOP signals to be sampled by the rising edge of NRESET. Device is ready to sample SOP pin states anytime after power supplies are at recommended operating conditions.	0			ms
$t_{MSS_BOOT_START}$	Typical delay after NRESET rising edge before boot ROM to begins MSS code execution. Value depends on whether device is operating directly from a crystal source or oscillator (REFCLK) source. Faster startup possible with the oscillator mode.	0.5		7.0	ms
$t_{RESET_POWER_DELAY}$	During power off events, delay after NRESET is brought from VIOIN to VSS level to when power pins can be powered off. Device power pins can be powered off anytime after NRESET is brought to VSS level.	0			ms

6.12.2 Clock Specifications

An external crystal is connected to the device pins. Figure 6-2 shows the crystal implementation.

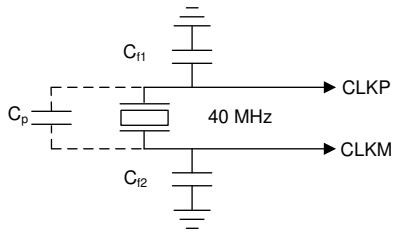


Figure 6-2. Crystal Implementation

Note

The load capacitors, C_{f1} and C_{f2} in Figure 6-2, should be chosen such that Equation 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins. Note that Cf1 and Cf2 include the parasitic capacitances due to PCB routing.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

Table 6-10 lists the electrical characteristics of the clock crystal.

Table 6-10. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_P	Parallel resonance crystal frequency		40		MHz
C_L	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	–40		150	°C
Frequency tolerance	Crystal frequency tolerance(1) (2) (3)	–200		200	ppm
Drive level			50	200	µW

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
(3) Crystal tolerance affects sensor accuracy if AM273x used as clock source for attached sensors.

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A non-crystal oscillator can also be used as the clock reference source. In this case the signal is fed to the CLKP pin only and CLKM is grounded. Table 6-11 lists the electrical, AC timing, and phase noise requirements of the external oscillator input signal.

Table 6-11. External Clock Mode Input Requirements

PARAMETER		SPECIFICATION			UNIT
		MIN	TYP	MAX	
Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referrenced to 40 MHz	Frequency		40		MHz
	AC-Amplitude	700		1200	mV (pp)
	DC-V_{IL}	0.00		0.02	V
	DC-V_{IH}	1.40		1.95	V
	DC-$t_{rise/fall}$			10	ns
	Phase Noise at 1 kHz			–132	dBc/Hz
	Phase Noise at 10 kHz			–143	dBc/Hz
	Phase Noise at 100 kHz			–152	dBc/Hz
	Phase Noise at 1 MHz			–153	dBc/Hz
	Duty Cycle	35		65	%
	Freq Tolerance	–50		50	ppm

6.12.3 Peripheral *Information*

Initial peripheral descriptions and features are provided in the following sections. Additional peripheral details and interface timing information shall be provided in a later product preview or datasheet release.

6.12.3.1 QSPI Flash Memory Peripheral

AM273x includes a Quad-Serial Peripheral Interface for external flash memory access. Flash memory can be be utilized for many purposes including: Secondary boot-loader memory, application program memory, security keys storage, and long-term data logs for security and error conditions.

- ROM bootloader auto identification of supported flash through flash device ID (DEVID) register
- Loopback skew cancellation for clock signal to supported faster flash interface clock rates
- Two chip-select signals to connect two external flash devices
- Memory mapped 'direct' mode and software triggered 'indirect' mode of operation for performing flash data transfers
- 67 MHz operating clock supported

6.12.3.1.1 QSPI Timing Conditions

SPECIFICATION NUMBER	PARAMETER		MIN	TYP	MAX	UNIT
	Input Conditions					
1	t_R	Input rise time	1		3	ns
2	t_F	Input fall time	1		3	ns
	Output Conditions					
3	C_{LOAD}	Output load capacitance	2		15	pF

6.12.3.1.2 QSPI Timing Requirements

SPECIFICATION NUMBER	PARAMETER[1], [2], [3]		MIN	TYP	MAX	UNIT
Q12	$t_{su(D-SCLK)}$	Setup time, D[3:0] valid before falling SCLK edge	5			ns
Q13	$t_{h(SCLK-D)}$	Hold time, D[3:0] valid after falling SCLK edge	0			ns

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SPECIFICATION NUMBER	PARAMETER[1], [2], [3]		MIN	TYP	MAX	UNIT
Q14	$t_{su(D-SCLK)}$	Setup time, final D[3:0] bit valid before final falling SCLK edge	5-P			ns
Q15	$t_{h(SCLK-D)}$	Hold time, final D[3:0] bit valid after final falling SCLK edge	0+P			ns

(1) Clock Mode 0 (clock polarity = 0 ; clockk phase = 0) is the mode of operation.
(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although nonstandard, The falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.
(3) P = SCLK period in ns.

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6.12.3.1.3 QSPI Switching Characteristics

SPECIFICATION NUMBER	PARAMETER[1], [2]		MIN	TYP	MAX	UNIT
Q1	$t_{c(SCLK)}$	Cycle time, sclk	14.9			ns
Q2	$t_{w(SCLKL)}$	Pulse duration, sclk low	0.5*P – 1.5			ns
Q3	$t_{w(SCLKH)}$	Pulse duration, sclk high	0.5*P – 1.5			ns
Q4	$t_{d(CS-SCLK)}$	Delay time, sclk falling edge to cs active edge	–M*P – 1		–M*P + 2.5	ns
Q5	$t_{d(SCLK-CS)}$	Delay time, sclk falling edge to cs inactive edge	N*P – 1		N*P + 2.5	ns
Q6	$t_{d(SCLK-D0)}$	Delay time, sclk falling edge to d[0] transition	–3		5.2	ns
Q7	$t_{ena(CS-D0LZ)}$	Enable time, cs active edge to d[0] driven (lo-z)	–P – 4		–P +3.5	ns
Q8	$t_{dis(CS-D0Z)}$	Disable time, cs active edge to d[0] tri-stated (hi-z)	–P – 4		–P +3.5	ns
Q9	$t_{d(SCLK-D0)}$	Delay time, sclk first falling edge to first d[0] transition (for PHA = 0 only)	–3– P		3.5 – P	ns

(1) P = SCLK period in ns.
(2) M = QSPI_SPI_DC_REG.DDx + 1, N = 2

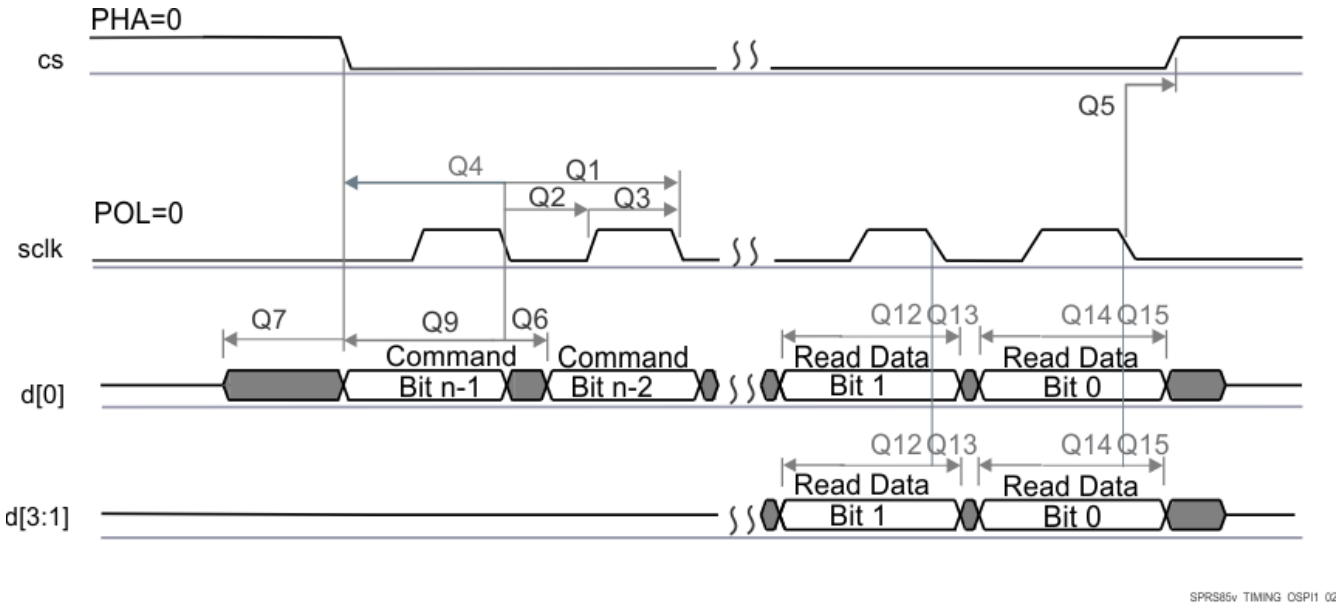


Figure 6-3. QSPI Read (Clock Mode 0)

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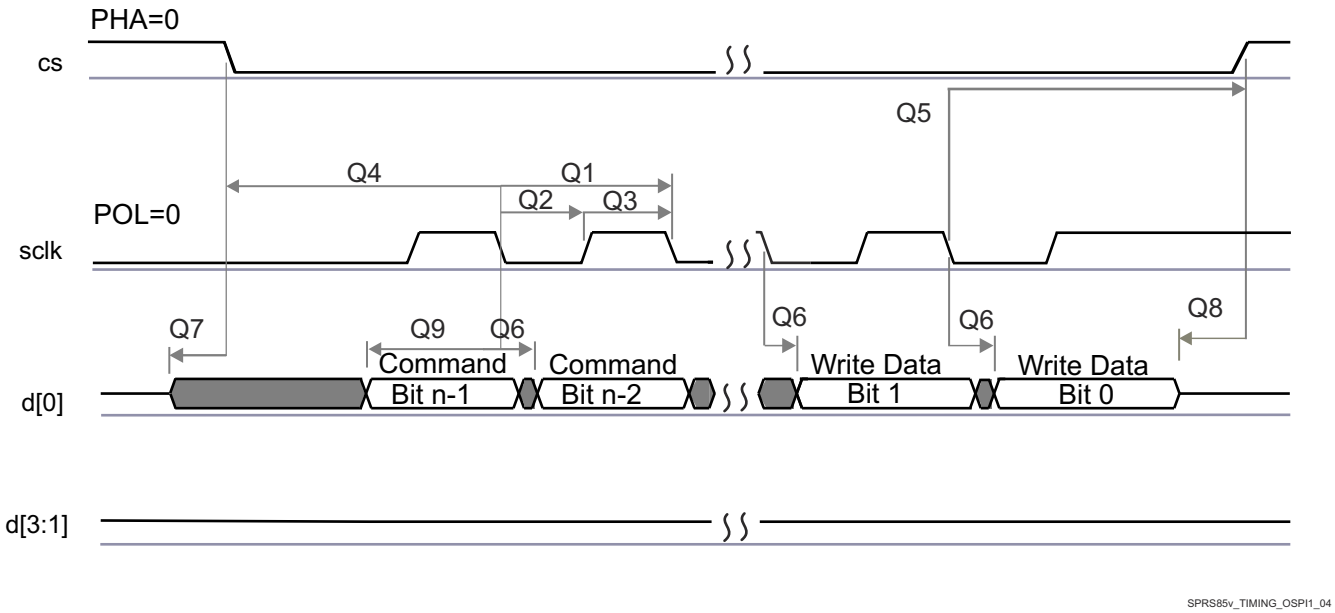


Figure 6-4. QSPI Write (Clock Mode 0)

6.12.3.2 MIBSPI Peripheral

AM273x includes four, Multi-Buffered Serial Peripheral Interface (MIBSPI) master interfaces. Two of these interfaces are intended for external MCU, PMIC, EEPROM, Watchdog, and other system-level communication and are labeled as MSS_MIBSPI. The other two interfaces are intended for independently mastering SPI device sensors and are labeled as RCSS_MIBSPI.

- The maximum clock rate supported over each MIBSPI module is 25 MHz.

Additionally, both the MSS and RCSS MIBSPI have a device-level implemented host interrupt request input signal path. These signals are intended to allow an attached SPI device to signal the AM273x MCU host device of any required action on the attached device. These signals are labeled as HOST_IRQ. See below Table 6-12 highlighting these MIBSPI host IRQ signals. See the AM273x Technical Reference Manual for more information on all features of the MIBSPI peripheral.

Table 6-12. MIBSPI Host Interrupt (IRQ) Signals

Signal Name	Signal Description
MSS_MIBSPIA_HOSTIRQ	MSS MIBSPIA host interrupt request
RCSS_MIBSPIA_HOSTIQ	RCSS MIBSPIA host interrupt request
RCSS_MIBSPIB_HOSTIRQ	RCSS MIBSPIB host interrupt request

6.12.3.2.1 SPI Timing Conditions

NO.	PARAMETER		MIN	TYP	MAX	UNIT
Input Conditions						
1	t_R	Input rise time	1		3	ns
2	t_F	Input fall time	1		3	ns
Output Conditions						
3	C_{LOAD}	Output load capacitance	2		15	pF

6.12.3.2.2 SPI Master Mode Timing and Switching Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)

The following tables and figures present timing requirements and switching characteristics for SPI – Master Mode.

Table 6-13. SPI Master Mode Switching Characteristics (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)[1][3]

see Figure 6-5 and Figure 6-6

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK[2]	40		$256t_{c(VCLK)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
4	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)	$0.5t_{c(SPC)M} - 13$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)	$0.5t_{c(SPC)M} - 13$			
5	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)	$0.5t_{c(SPC)M} - 10.5$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)	$0.5t_{c(SPC)M} - 10.5$			

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Table 6-13. SPI Master Mode Switching Characteristics (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)[1][3] (continued)

see Figure 6-5 and Figure 6-6

NO.	PARAMETER			MIN	TYP	MAX	UNIT
6	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)[5]	CSHOLD = 0	(C2TDELAY+2)* $t_{c(VCLK)}$ – 7.5		(C2TDELAY+2) * $t_{c(VCLK)}$ + 7	ns
			CSHOLD = 1	(C2TDELAY +3) * $t_{c(VCLK)}$ – 7.5		(C2TDELAY+3) * $t_{c(VCLK)}$ + 7	
		Setup time CS active until SPICLK low (clock polarity = 1)[5]	CSHOLD = 0	(C2TDELAY+2)* $t_{c(VCLK)}$ – 7.5		(C2TDELAY+2) * $t_{c(VCLK)}$ + 7	
			CSHOLD = 1	(C2TDELAY +3) * $t_{c(VCLK)}$ – 7.5		(C2TDELAY+3) * $t_{c(VCLK)}$ + 7	
7	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)[5]		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) *$t_{c(VCLK)}$ – 7		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)}$ + 7.5	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)[5]		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) *$t_{c(VCLK)}$ – 7		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)}$ + 7.5	

Table 6-14. SPI Master Mode Timing Requirements (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)[1][3]

see Figure 6-5

NO.	PARAMETER		MIN	TYP	MAX	UNIT
8	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)[4]	5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)[4]	5			
9	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)[4]	3			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)[4]	3			

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared (where x= 0 or 1).
(2) $t_{c(MSS_VCLK)}$ = main subsystem clock time = 1 / $f_{(MSS_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS+1)t_{c(MSS_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS_VCLK)} \geq 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register.

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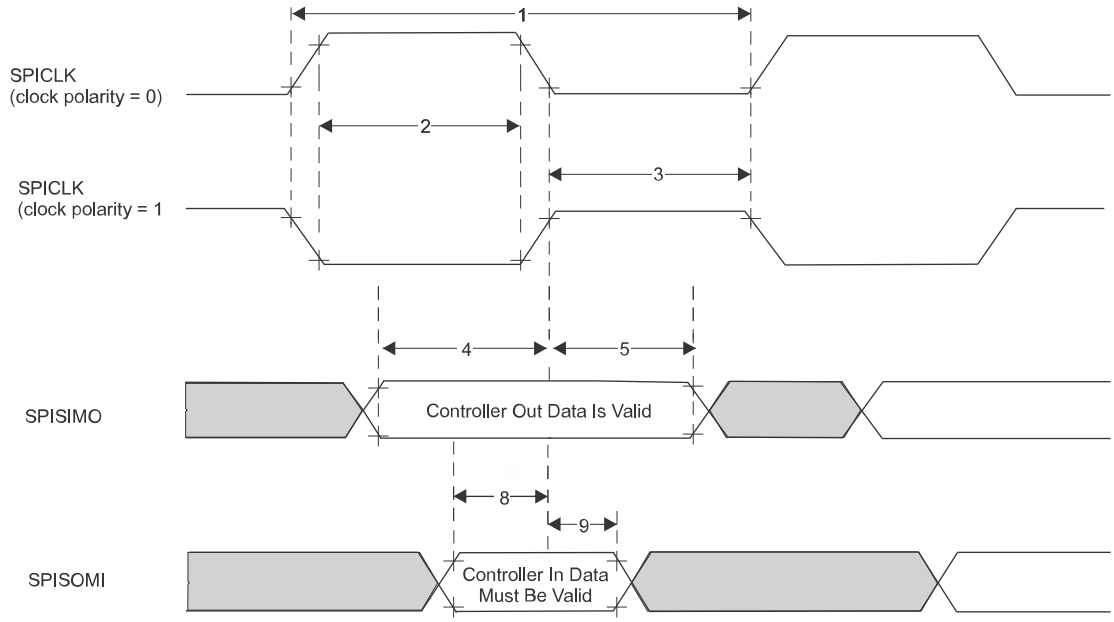


Figure 6-5. SPI Master Mode External Timing (CLOCK PHASE = 0)

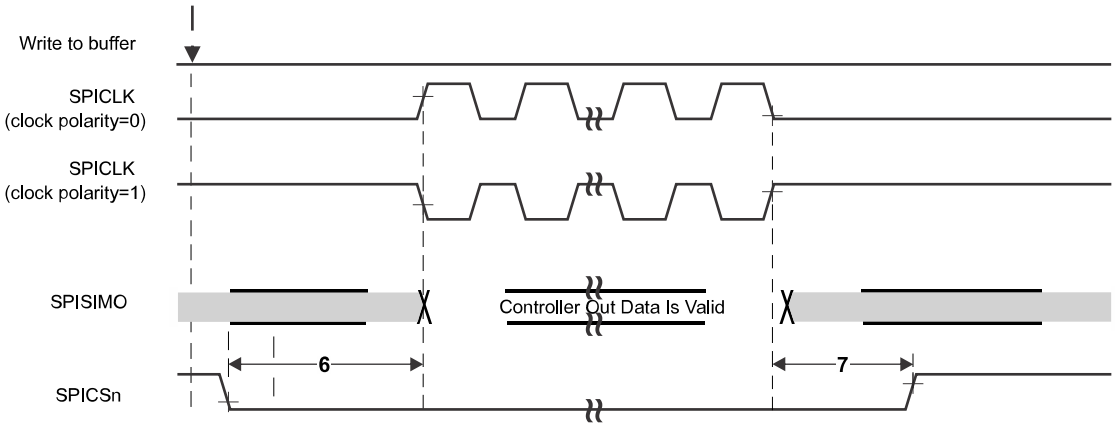


Figure 6-6. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)

6.12.3.2.3 SPI Master Mode Timing and Switching Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)

Table 6-15. SPI Master Mode Switching Characteristics (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)[(1)(3)]

see Figure 6-5 and Figure 6-8

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK[(2)]	40		$256t_{c(VCLK)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
4	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)	$0.5t_{c(SPC)M} - 13$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)	$0.5t_{c(SPC)M} - 13$			

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Table 6-15. SPI Master Mode Switching Characteristics (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)[1][3] (continued)

see Figure 6-5 and Figure 6-8

NO.	PARAMETER			MIN	TYP	MAX	UNIT
5	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 10.5$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 10.5$			
6	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)[5]	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7.5$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7.5$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7$	
		Setup time CS active until SPICLK low (clock polarity = 1)[5]	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2)*t_{c(VCLK)} - 7.5$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7$	
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3)*t_{c(VCLK)} - 7.5$		$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} + 7$	
7	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)[5]		$(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)[5]		$(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	

Table 6-16. SPI Master Mode Timing Requirements (CLOCK PHASE = , SPICLK = output, SPISIMO = output, and SPISOMI = input)[1][3]

see Figure 6-5 and Figure 6-8

NO.	PARAMETER		MIN	TYP	MAX	UNIT
8	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)[4]	5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)[4]	5			
9	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)[4]	3			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)[4]	3			

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set (where x = 0 or 1).
(2) $t_{c(MSS_VCLK)}$ = main subsystem clock time = 1 / $f_{(MSS_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS +1)t_{c(MSS_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS_VCLK)} \geq 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

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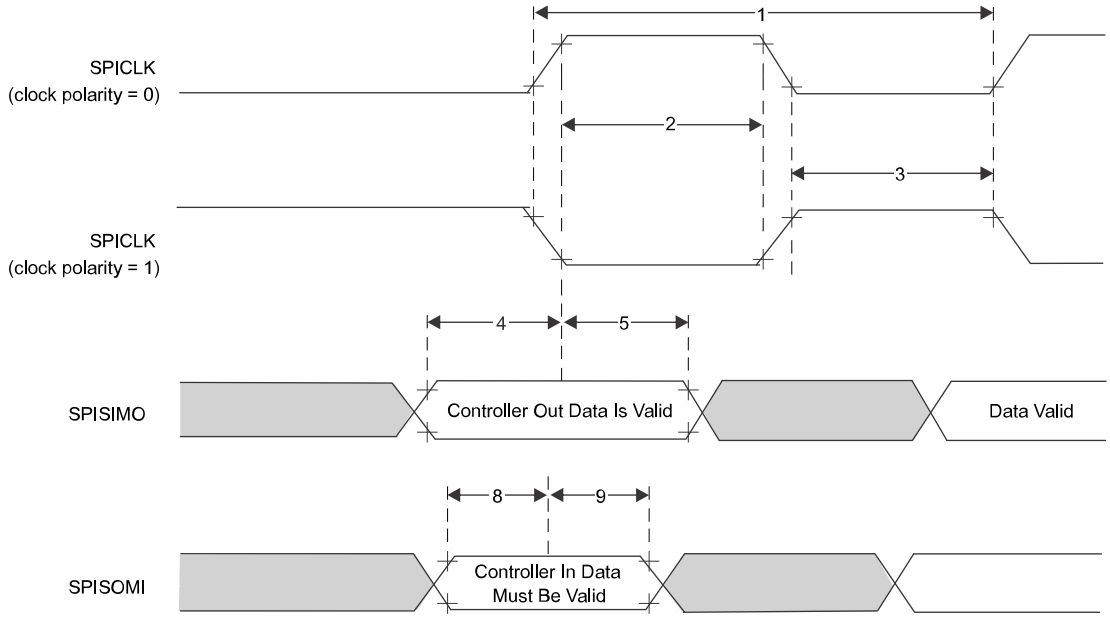


Figure 6-7. SPI Master Mode External Timing (CLOCK PHASE = 1)

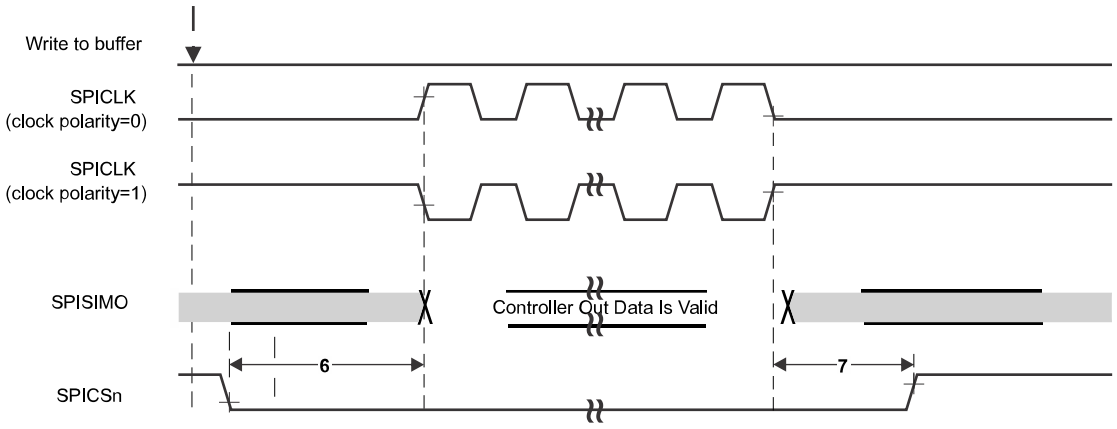


Figure 6-8. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)

6.12.3.2.4 SPI Slave Mode Timing and Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)

Table 6-17. SPI Slave Mode Timing Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)[1][2]

see Figure 6-9 and Figure 6-10

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK [2]	25			ns
2	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	10			ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	10			
3	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	10			ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	10			

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Table 6-17. SPI Slave Mode Timing Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)[1][2] (continued)

see Figure 6-9 and Figure 6-10

NO.	PARAMETER		MIN	TYP	MAX	UNIT
4	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)[3]			11	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)[3]			11	
5	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)[3]	2			ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)[3]	2			

Table 6-18. SPI Slave Mode Switching Characteristics (SPICLK = input, SPISIMO = input, and SPISOMI = output)[1][2]

see Figure 6-9 and Figure 6-10

NO.	PARAMETER		MIN	TYP	MAX	UNIT
6	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)[4]	4.5			ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)[4]	4.5			
7	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)[4]	1			ns
	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)[4]	1			

(1) The MASTER bit (SPIGCRx.0) is cleared (where x = 0 or 1).
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(MSS_VCLK)}$, where PS = prescale value set in SPIFMTx.[15:8].
(3) When the SPI is in Slave mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(MSS_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.For PS values of 0: $t_{c(SPC)S} = 2t_{c(MSS_VCLK)} \geq 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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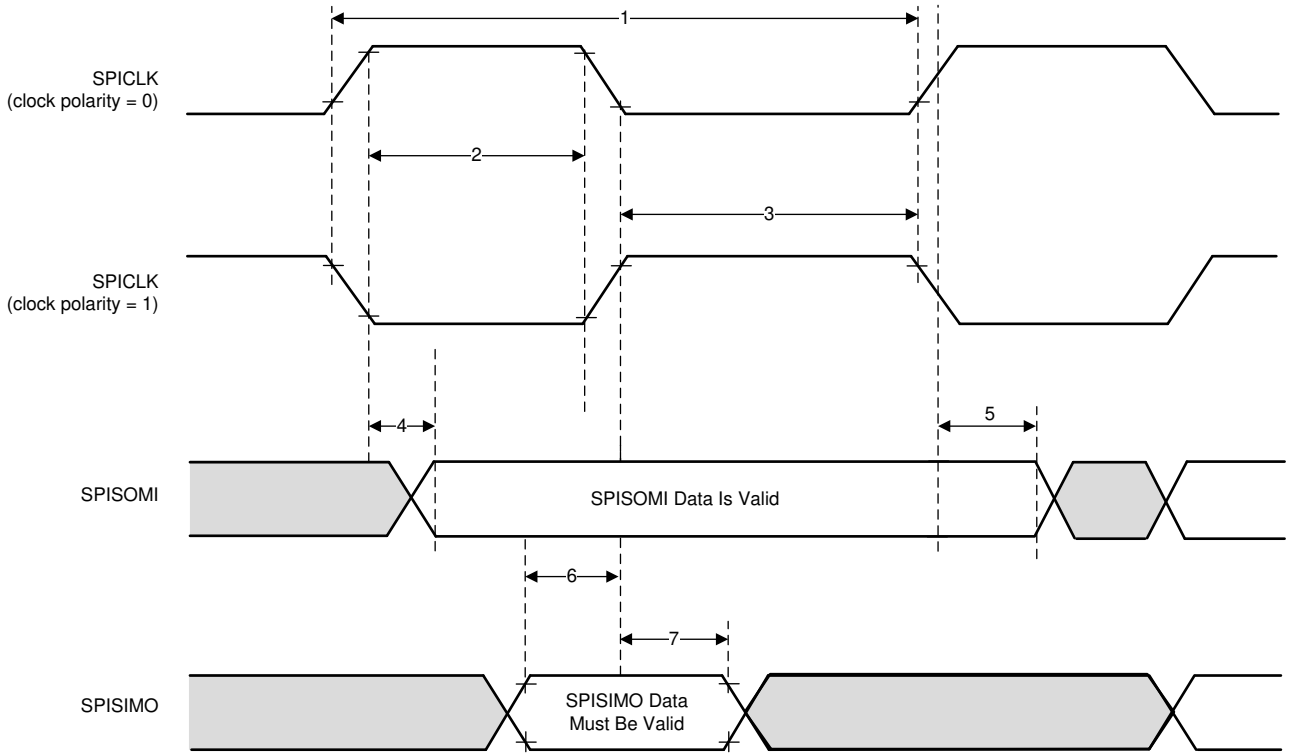


Figure 6-9. SPI Slave Mode External Timing (CLOCK PHASE = 0)

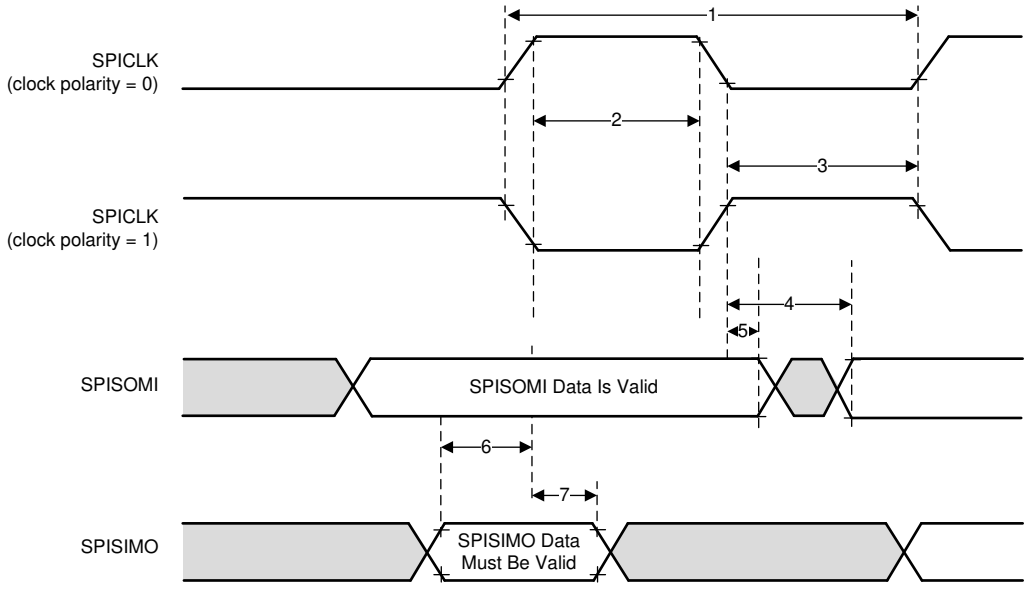


Figure 6-10. SPI Slave Mode External Timing (CLOCK PHASE = 1)

6.12.3.3 Ethernet Switch (RGMII/RMII/MII) Peripheral

AM273x integrates a two port Ethernet switch with one external RGMII/RMII/MII port and another port servicing the Master Sub-System (MSS). This interface is intended to operate primarily as a 100Mbps ECU interface. It can also be used as an instrumentation interface.

- Full Duplex 10/100Mbps wire rate interface to Ethernet PHY over RGMII, RMII, or MII parallel interface
- MDIO Clause 22 and 45 PHY management interface
- IEEE 1588 Synchronous Ethernet support

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- Synchronous trigger output allowing Ethernet to trigger CSI data frames

6.12.3.3.1 RGMII/GMII/MII Timing Conditions

SPECIFICATION NUMBER	PARAMETER		MIN	TYP	MAX	UNIT
	Input Conditions					
1	t_R	Input rise time	1		3	ns
2	t_F	Input fall time	1		3	ns
	Output Conditions					
3	C_{LOAD}	Output load capacitance	2		20	pF

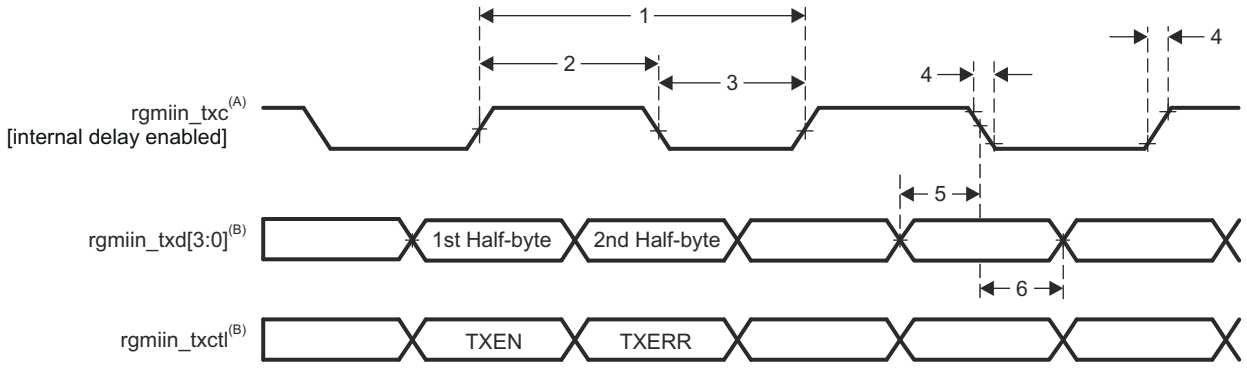
6.12.3.3.2 RGMII Transmit Clock Switching Characteristics

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(TXC)}$	Cycle time, rgmiin_txc	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
2	$t_{w(TXCH)}$	Pulse duration, rgmiin_txc high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
3	$t_{w(TXCL)}$	Pulse duration, rgmiin_txc low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
4	$t_{t(TXC)}$	Transition time, rgmiin_txc	10 Mbps		0.75	ns
			100 Mbps		0.75	ns

6.12.3.3.3 RGMII Transmit Data and Control Switching Characteristics

NO.(1)	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
5	$t_{osu(TXD-TXC)}$	Output Setup time, transmit selected signals valid to MSS_RGMII_TCLK high/low	RGMII, Internal Delay Enabled, 10/100 Mbps	1.2		ns
6	$t_{oh(TXC-TXD)}$	Output Hold time, transmit selected signals valid after MSS_RGMII_TCLK high/low	RGMII, Internal Delay Enabled, 10/100 Mbps	1.2		ns

(1) For RGMII, transmit selected signals include: MSS_RGMII_TXD[3:0] and MSS_RGMII_TCTL.



A. TXC is delayed internally before being driven to the rgmiin_txc pin. This internal delay is always enabled.

B. Data and control information is transmitted using both edges of the clocks. rgmiin_txd[3:0] carries data bits 3-0 on the rising edge of rgmiin_txc and data bits 7-4 on the falling edge of rgmiin_txc. Similarly, rgmiin_txctl carries TXEN on rising edge of rgmiin_txc and TXERR of falling edge of rgmiin_txc.

Figure 6-11. RGMII Transmit Interface Switching Characteristics

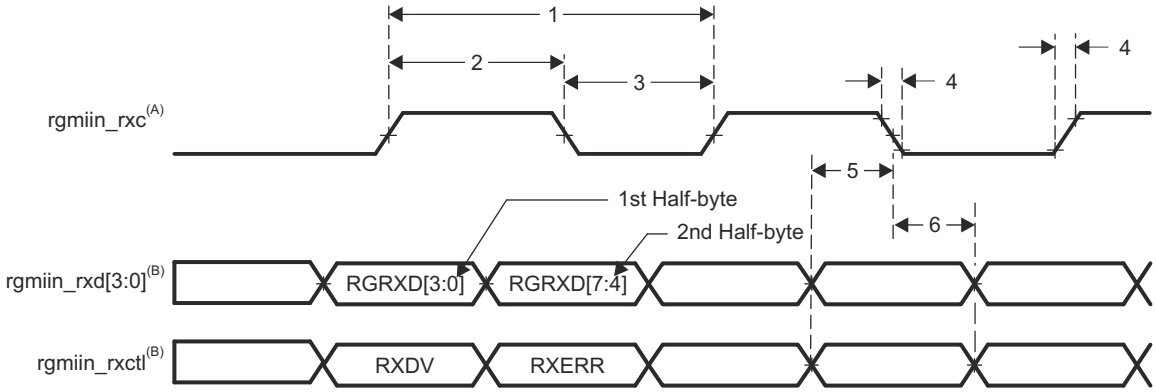
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6.12.3.3.4 RGMII Recieve Clock Timing Requirements

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(RXC)}$	Cycle time, rgmiin_rxc	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
2	$t_{w(RXCH)}$	Pulse duration, rgmiin_rxc high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
3	$t_{w(RXCL)}$	Pulse duration, rgmiin_rxc low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
4	$t_{t(RXC)}$	Transition time, rgmiin_rxc	10 Mbps		0.75	ns
			100 Mbps		0.75	ns

6.12.3.3.5 RGMII Recieve Data and Control Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
5	$t_{su(RXD-RXCH)}$	Setup time, receive selected signals valid before MSS_RGMII_RCLK high/low	2		ns
6	$t_{h(RXCH-RXD)}$	Hold time, receive selected signals valid after MSS_RGMII_RCLK high/low	2		ns



A. rgmiin_rxc must be externally delayed relative to the data and control pins.

B. Data and control information is received using both edges of the clocks. MSS_RGMII_RXD[3:0] carries data bits 3-0 on the rising edge of rgmiin_rxc and data bits 7-4 on the falling edge ofrgmiin_rxc. Similarly, rgmiin_rxctl carries RXDV on rising edge of rgmiin_rxc and RXERR on falling edge of rgmiin_rxc.

Figure 6-12. GMAC Receive Interface Timing, RGMIIn operation

6.12.3.3.6 RMII Transmit Clock Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII7	$t_{c(REF_CLK)}$	Cycle time, REF_CLK	20		ns
RMII8	$t_{w(REF_CLKH)}$	Pulse duration, REF_CLK high	7	13	ns
RMII9	$t_{w(REF_CLKL)}$	Pulse duration, REF_CLK low	7	13	ns
RMII10	$t_{t(REF_CLK)}$	Transistion time, REF_CLK		3	ns

6.12.3.3.7 RMII Transmit Data and Control Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII11	$t_{d(REF_CLK-TXD)}$	Delay time, REF_CLK high to selected transmit signals valid	2	14.2	ns
	$t_{dd(REF_CLK-TXEN)}$				

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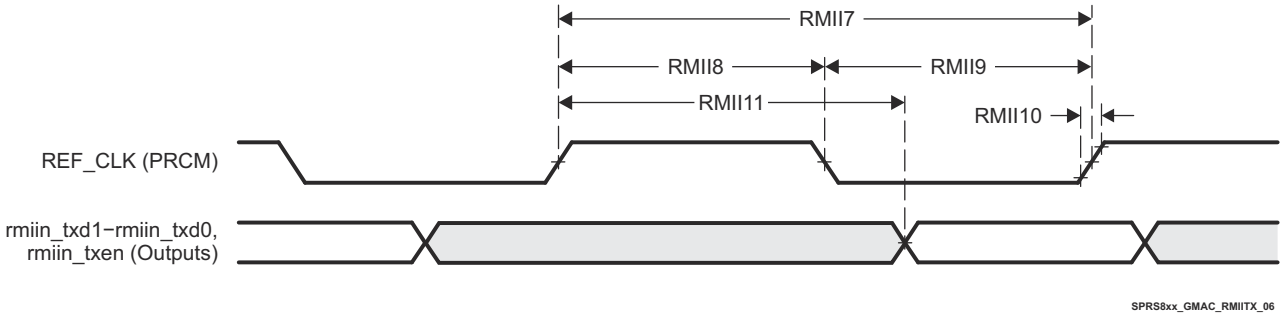


Figure 6-13. GMAC Transmit Interface Timing RMIIn Operation

6.12.3.3.8 RMII Receive Clock Timing Requirements

NO.			MIN	MAX	UNIT
RMII1	$t_{c(REF_CLK)}$	Cycle time, REF_CLK	20		ns
RMII2	$t_{w(REF_CLKH)}$	Pulse duration, REF_CLK high	7	13	ns
RMII3	$t_{w(REF_CLKL)}$	Pulse duration, REF_CLK low	7	13	ns
RMII4	$t_{tt(REF_CLK)}$	Transistion time, REF_CLK		3	ns

6.12.3.3.9 RMII Receive Data and Control Timing Requirements

NO.			MIN	MAX	UNIT
RMII5	$t_{su(RXD-REF_CLK)}$	Setup time, receive selected signals valid before REF_CLK	4		ns
	$t_{su(CRS_DV-REF_CLK)}$				
	$t_{su(RX_ER-REF_CLK)}$				
RMII6	$t_{h(REF_CLK-RXD)}$	Hold time, receive selected signals valid after REF_CLK	2		ns
	$t_{h(REF_CLK-CRS_DV)}$				
	$t_{h(REF_CLK-RX_ER)}$				

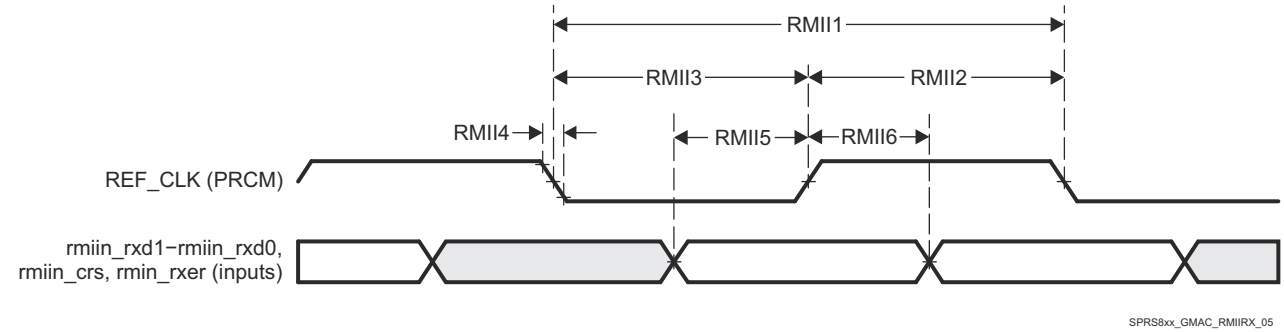


Figure 6-14. GMAC Receive Interface Timing RMIIn operation

6.12.3.3.10 MII Transmit Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{d(TX_CLK-TXD)}$	Delay time, miin_txclk to transmit selected signals valid	0	25	ns
	$t_{d(TX_CLK-TX_EN)}$				
	$t_{d(TX_CLK-TX_ER)}$				

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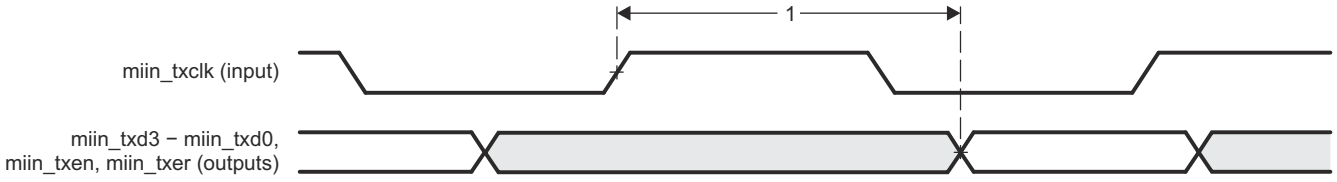


Figure 6-15. GMAC Transmit Interface Timing MIIn operation

6.12.3.3.11 MII Receive Clock Timing Requirements

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(RX_CLK)}$	Cycle time, miin_rxclk	10 Mbps	400		ns
			100 Mbps	40		ns
2	$t_{w(RX_CLKH)}$	Pulse duration, miin_rxclk high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
3	$t_{w(RX_CLKL)}$	Pulse duration, miin_rxclk low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
4	$t_{t(RX_CLK)}$	Transition time, miin_rxclk	10 Mbps		3	ns
			100 Mbps		3	ns

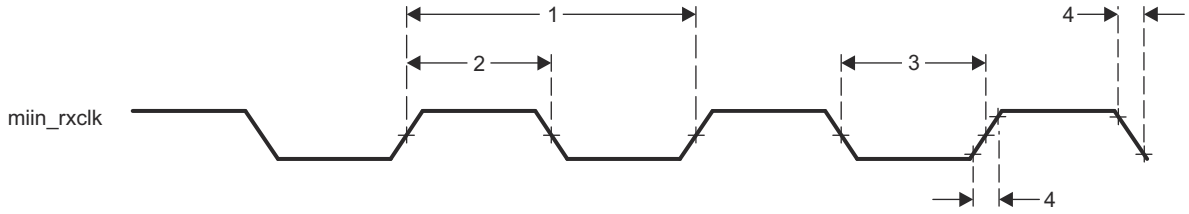


Figure 6-16. Clock Timing (GMAC Receive) - MIIn operation

6.12.3.3.12 MII Receive Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{su(RXD-RX_CLK)}$	Setup time, receive selected signals valid before miin_rxclk	8		ns
	$t_{su(RX_DV-RX_CLK)}$				
	$t_{su(RX_ER-RX_CLK)}$				
2	$t_{h(RX_CLK-RXD)}$	Hold time, receive selected signals valid after miin_rxclk	8		ns
	$t_{h(RX_CLK-RX_DV)}$				
	$t_{h(RX_CLK-RX_ER)}$				

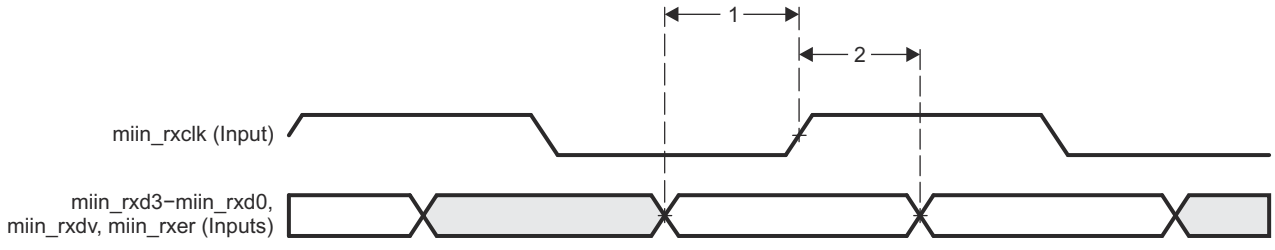


Figure 6-17. GMAC Receive Interface Timing MIIn operation

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6.12.3.3.13 MII Transmit Clock Timing Requirements

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(TX_CLK)}$	Cycle time, miin_txclk	10 Mbps	400		ns
			100 Mbps	40		ns
2	$t_{w(TX_CLKH)}$	Pulse duration, miin_txclk high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
3	$t_{w(TX_CLKL)}$	Pulse duration, miin_txclk low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
4	$t_{t(TX_CLK)}$	Transition time, miin_txclk	10 Mbps		3	ns
			100 Mbps		3	ns

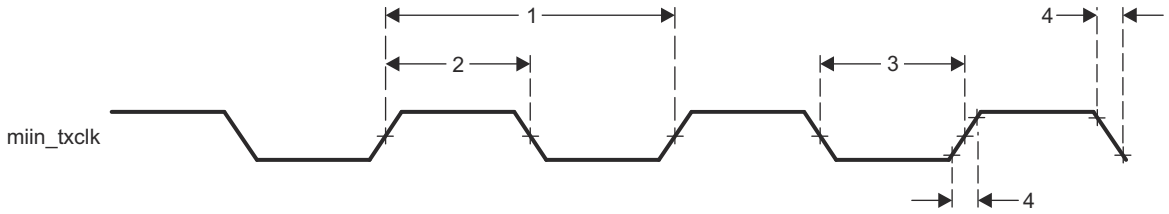


Figure 6-18. Clock Timing (GMAC Transmit) - MIIn operation

6.12.3.3.14 MDIO Interface Timings

CAUTION

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 6-19, Table 6-20 and Figure 6-19 present switching characteristics and timing requirements for the MDIO interface.

Table 6-19. Timing Requirements for MDIO Input

No	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO1	$t_{c(MDC)}$	Cycle time, MDC	400		ns
MDIO2	$t_{w(MDCH)}$	Pulse Duration, MDC High	160		ns
MDIO3	$t_{w(MDCL)}$	Pulse Duration, MDC Low	160		ns
MDIO4	$t_{su(MDIO-MDC)}$	Setup time, MDIO valid before MDC High	90		ns
MDIO5	$t_{h(MDIO_MDC)}$	Hold time, MDIO valid from MDC High	0		ns

Table 6-20. Switching Characteristics Over Recommended Operating Conditions for MDIO Output

NO	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO6	$t_{t(MDC)}$	Transition time, MDC		5	ns
MDIO7	$t_{d(MDC-MDIO)}$	Delay time, MDC low to MDIO valid	10	(P * 0.5) - 10	ns

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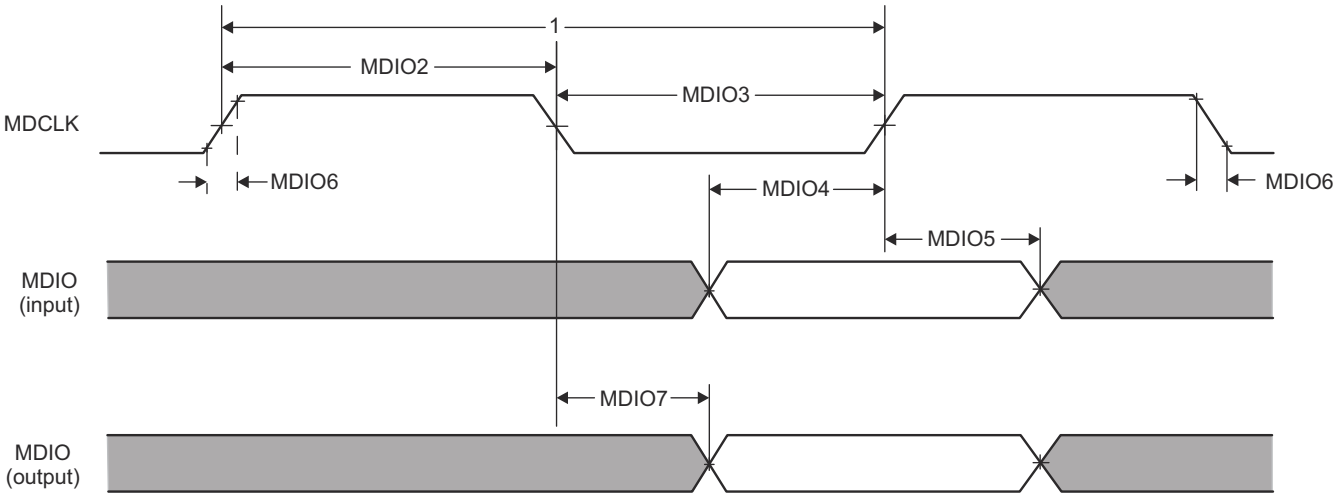


Figure 6-19. GMAC MDIO diagrams

6.12.3.4 LVDS/Aurora Instrumentation and Measurement Peripheral

The AM273x supports a set of LVDS STM-TWP Aurora interface for exporting raw IF ADC sensor data. The LVDS transmitters are shared between the two measurement interface options.

- 4-data lane LVDS interface (two additional lanes for Data Clock and Frame Clock) at 1 Gbps/lane
- 6-lane STM-TWP-Aurora-LVDS interface mode

Please see the AM273x TRM for information regarding programming options for both LVDS interfaces.

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6.12.3.4.1 LVDS Interface Configuration

The supported AM273x LVDS lane configuration is four Data lanes (LVDS_TXP/M), one Bit Clock lane (LVDS_CLKP/M) and one Frame clock lane (LVDS_FRCLKP/M). The LVDS interface supports the following data rates:

- 900 Mbps (450 MHz DDR Clock)
- 600 Mbps (300 MHz DDR Clock)
- 450 Mbps (225 MHz DDR Clock)
- 400 Mbps (200 MHz DDR Clock)
- 300 Mbps (150 MHz DDR Clock)
- 225 Mbps (112.5 MHz DDR Clock)
- 150 Mbps (75 MHz DDR Clock)

Note that the bit clock is in DDR format and hence the numbers of toggles in the clock is equivalent to data.

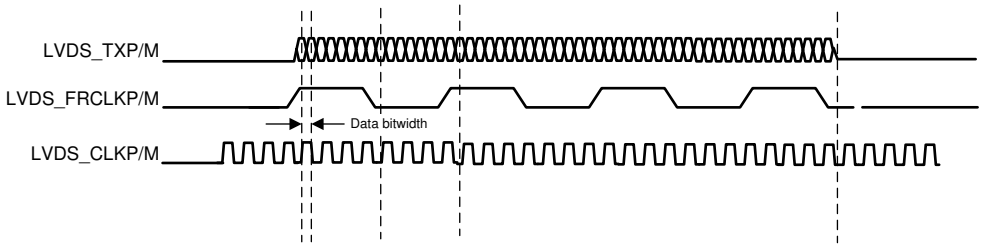


Figure 6-20. LVDS Interface Lane Configuration And Relative Timings

6.12.3.4.2 LVDS Interface Timings

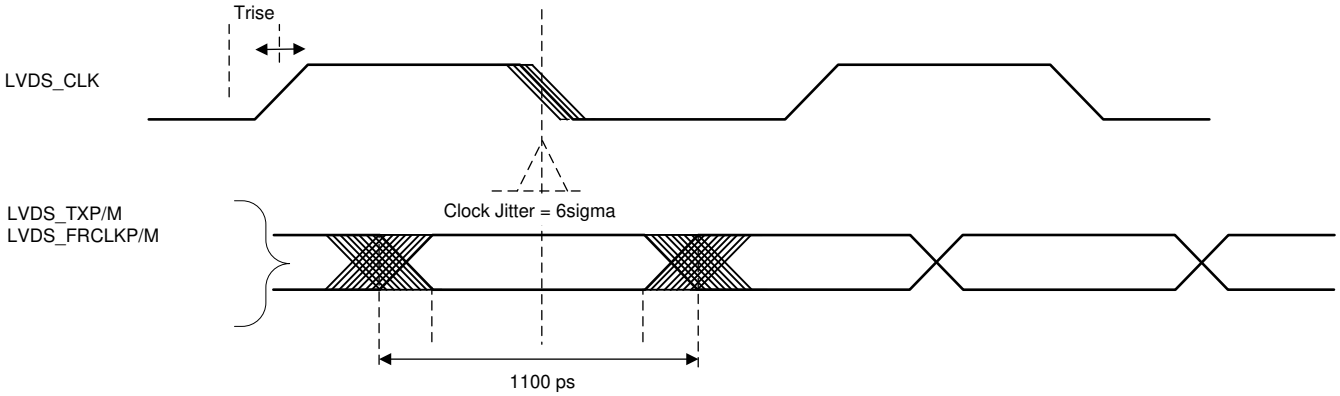


Figure 6-21. Timing Parameters

Table 6-21. LVDS Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty Cycle Requirements	max 1 pF lumped capacitive load on LVDS lanes	48%		52%	
Output Differential Voltage	peak-to-peak single-ended with 100 Ω resistive load between differential pairs	250		450	mV
Output Offset Voltage		1125		1275	mV
Trise and Tfall	20%-80%, 900 Mbps				ps
Jitter (pk-pk)	900 Mbps		80		ps

6.12.3.5 UART Peripheral

AM273x includes four UART interfaces. One UART is intended as a secondary boot loader source, one is intended for use as a register debug interface (with XDS110 class emulator) and two are meant for general UART communication support.

- Maximum baud-rate supported shall be at least 1536Kbaud in all the different clock frequency modes
- UART interfaces multiplexed with other I/O to allow for widest peripheral use flexibility

6.12.3.5.1 UART Timing Requirements

		MIN	TYP	MAX	UNIT
f(baud)	Supported baud rate at 20 pF		921.6		kHz

6.12.3.6 I^2C Protocol Definition

AM273x supports three master or slave Inter-integrated Circuit interfaces (I2C). One I2C interface is intended to be connected to an external PMIC or EEPROM device (alternatively controlled by SPI). The other two I2C are intended as alternative control for sensor devices or other external IC.

- Standard/fast mode I2C interface compliant with Philips I2C specification version 2.1
- Maximum clock rate of 100Kbps in Standard mode and 400Kbps in Fast mode

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6.12.3.6.1 I2C Timing Requirements(1)

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high	250		100		µs
$t_{h(SCLL-SDA)}$(1)	Hold time, SDA valid after SCL low	0	3.45	0	0.9	µs
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
C_b (2) (3)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum th(SDA-SCLL) for I2C bus devices has only to be met if the device does not stretch the low period (tw(SCLL)) of the SCL signal.
(3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

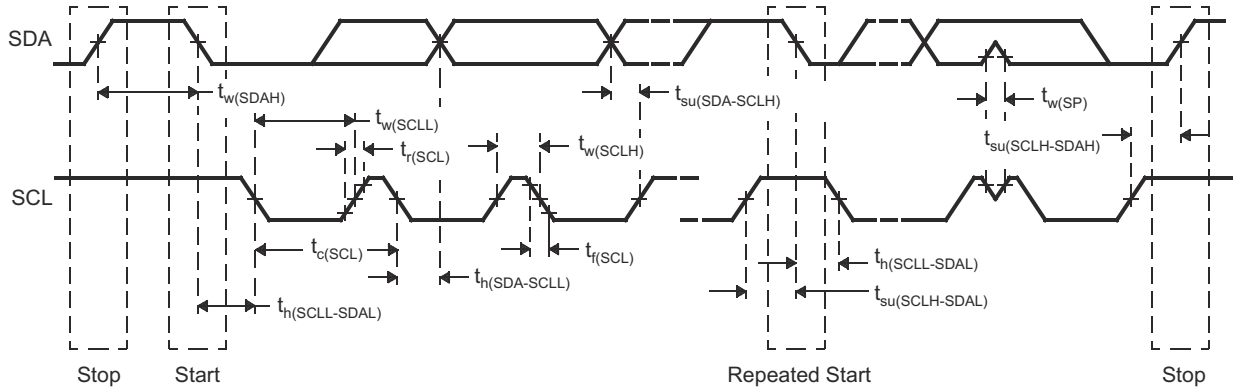


Figure 6-22. I2C Timing Diagram

Note

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum th(SDA-SCLL) has only to be met if the device does not stretch the LOW period (tw(SCLL)) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.

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6.12.3.7 Controller Area Network - Flexible Data-Rate (CAN-FD)

The AM273x integrates two CAN-FD interfaces, MSS_MCANA and MSS_MCANB. This enables support of a typical use case where one CAN-FD interface is used as ECU network interface while the other interface is used as a local network interface, providing communication with the neighboring sensors.

- Support CAN-FD according to ISO 11898-7 protocol with data rate up to 8Mbps
- Multiplexed GPIO can be used for CAN-FD external driver control
- Synchronous trigger output allows CAN-FD to trigger CSI2 data frames

6.12.3.7.1 Dynamic Characteristics for the CAN-FD TX and RX Pins

PARAMETER[1]		MIN	TYP	MAX	UNIT
$t_{d(MSS_CANA_TX)}$	Delay time, transmit shift register to MSS_CANA_TX pin			15	ns
$t_{d(MSS_CANB_TX)}$	Delay time, transmit shift register to MSS_CANB_TX pin			15	ns
$t_{d(MSS_MCANA_RX)}$	Delay time, MSS_MCANA_RX pin to receive shift register			10	ns
$t_{d(MSS_MCANB_RX)}$	Delay time, MSS_MCANB_RX pin to receive shift register			10	ns

(1) These values do not include rise/fall times of the output buffer.

6.12.3.8 CSI-2 Peripheral

AM273x integrates two, 4-lane MIPI CSI-2, D-PHY receiver peripherals: CSI2 receiver 0 (CSI2_RX0) and CSI2 receiver 1 (CSI2_RX1). Each peripheral can be used for capturing sensor data samples. The CSI2 interface is also capable of operating as a hardware-in-the-loop (HIL) interface, allowing for the playback of recorded data for development or diagnostic purposes.

- Interface is compliant with the MIPI CSI-2 D-PHY standard revision 1.2
- 2, 4-lane CSI2 receiver interfaces, working simultaneously at 600 Mbps/lane
- 4-lane, 3-lane, 2-lane, or 1-lane CSI2 configurations
- Support for virtual channels (minimum 4) and data types (minimum 4)
- Support for 8/10/12/14/16-bit RAW data mode with capability of sign extension or zero padding to align with 16-bit memory addressing for RAW 10/12/14 modes
- Support for user defined data types

Please reference the MIPI CSI-2 D-PHY standard revision 1.2 for full receiver timing requirements. Please reference the AM273x TRM for a complete description of all programmable options.

6.12.3.9 General Purpose ADC (GPADC)

AM273x device implements a GPADC module for safety monitoring device and system analog signals such as temperature sensor and voltage regulators.

- Up to 9 external or internal channels supported
- 7.5 ENOB, 625Ksps ADC
- Full-scale range of GPADC input between VSS and 1.8V
- Single or continuous conversion modes
- Data RAM to store the conversion results (1Kbyte results)

6.12.3.10 Enhanced Pulse-Width Modulator (ePWM)

AM273x includes three Enhanced Pulse-Width Modulation (ePWM) modules. These modules can be used to generate duty-cycled controlled waveforms for a power regulator, or a power management systems, or more complex waveforms for motor control applications.

- Dedicated 16-bit time-base counter with period and frequency control for each PWM module
- Each module contains two PWM outputs (EPWMxA and EPWMxB) that shall be usable in the following configurations:

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- Two independent PWM outputs with single-edge operation
- Two independent PWM outputs with dual-edge symmetric operation
- One independent PWM output with dual-edge asymmetric operation

6.12.3.11 Enhanced Capture (eCAP)

AM273x device includes one enhanced capture (eCAP) module. The eCAP module is used to capture external timing events. It is a general-purpose module which has a complementary function to ePWM. Uses include speed measurements of rotating machinery (e.g., toothed sprockets sensed via Hall sensors)

- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derviced from duty cycle encoded current/voltage sensor
- eCAP shall be working on operating clock of minimum 100mHz
- 4-event time-stamp registers (each 32 bits)

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6.12.3.12 General-Purpose Input/Output

Section 6.12.3.12.1 lists the switching characteristics of output timing relative to load capacitance.

6.12.3.12.1 Switching Characteristics for Output Timing versus Load Capacitance (C_L)(1) (2)

PARAMETER		TEST CONDITIONS		VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t_r	Max rise time	Slew control = 0	C_L = 20 pF	2.8	3.0	ns
			C_L = 50 pF	6.4	6.9	
			C_L = 75 pF	9.4	10.2	
t_f	Max fall time		C_L = 20 pF	2.8	2.8	ns
			C_L = 50 pF	6.4	6.6	
			C_L = 75 pF	9.4	9.8	
t_r	Max rise time	Slew control = 1	C_L = 20 pF	3.3	3.3	ns
			C_L = 50 pF	6.7	7.2	
			C_L = 75 pF	9.6	10.5	
t_f	Max fall time		C_L = 20 pF	3.1	3.1	ns
			C_L = 50 pF	6.6	6.6	
			C_L = 75 pF	9.6	9.6	

(1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

6.12.4 Emulation and Debug

6.12.4.1 Emulation and Debug Description

6.12.4.2 JTAG Interface

The JTAG interface implements the IEEE1149.1 standard interface for processor debug and boundary scan testing.

Section 6.12.4.2.1 and Section 6.12.4.2.2 assume the operating conditions stated in Figure 6-23.

6.12.4.2.1 Timing Requirements for IEEE 1149.1 JTAG

Table 6-22. JTAG Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

Table 6-23. JTAG Timing Requirements

NO.			MIN	TYP	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time TCK	66.66			ns
1a	$t_{w(TCKH)}$	Pulse duration TCK high (40% of tc)	26.67			ns
1b	$t_{w(TCKL)}$	Pulse duration TCK low (40% of tc)	26.67			ns
3	$t_{su(TDI-TCK)}$	Input setup time TDI valid to TCK high	2.5			ns

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Table 6-23. JTAG Timing Requirements (continued)

NO.			MIN	TYP	MAX	UNIT
3	$t_{su(TMS-TCK)}$	Input setup time TMS valid to TCK high	2.5			ns
4	$t_{h(TCK-TDI)}$	Input hold time TDI valid from TCK high	18			ns
4	$t_{h(TCK-TMS)}$	Input hold time TMS valid from TCK high	18			ns

6.12.4.2.2 Switching Characteristics for IEEE 1149.1 JTAG

NO.	PARAMETER		MIN	TYP	MAX	UNIT
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0		25	ns

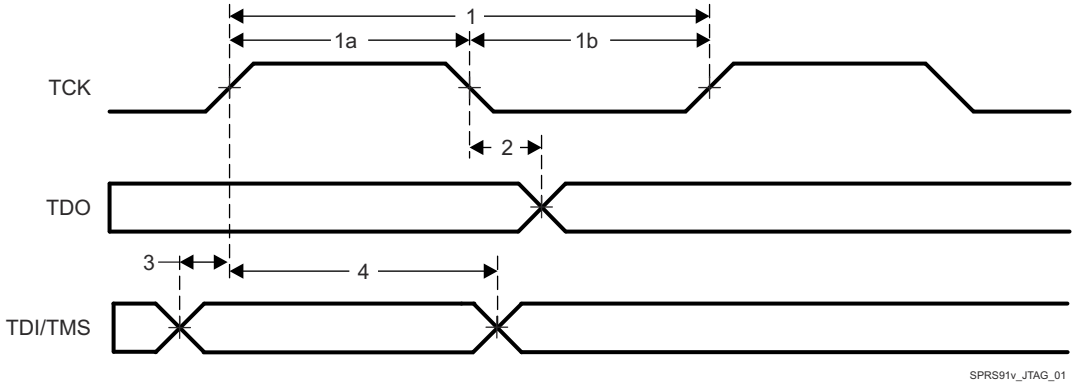


Figure 6-23. JTAG Timing

6.12.4.3 ETM Trace Interface

The ETM Trace interface provides a means of exporting real time processor debug information to a host PC through a compatible emulator toolset.

Section 6.12.4.3.1 and Section 6.12.4.3.2 describe the operating conditions shown in Figure 6-24 and Figure 6-25.

6.12.4.3.1 ETM TRACE Timing Requirements

		MIN	TYP	MAX	UNIT
Output Conditions					
C_{LOAD}	Output load capacitance	2		20	pF

6.12.4.3.2 ETM TRACE Switching Characteristics

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{cyc(ETM)}$	Cycle time, TRACECLK period	16			ns
2	$t_{h(ETM)}$	Pulse Duration, TRACECLK High	7			ns
3	$t_{l(ETM)}$	Pulse Duration, TRACECLK Low	7			ns
4	$t_{r(ETM)}$	Clock and data rise time			3.3	ns
5	$t_{f(ETM)}$	Clock and data fall time			3.3	ns
6	$t_{d(ETMTRACECLKH-ETMDATAV)}$	Delay time, ETM trace clock high to ETM data valid	1		7	ns
7	$t_{d(ETMTRACECLKl-ETMDATAV)}$	Delay time, ETM trace clock low to ETM data valid	1		7	ns

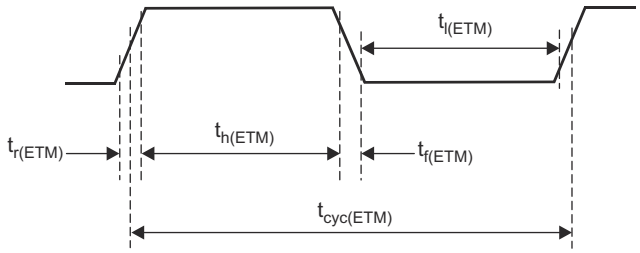


Figure 6-24. ETMTRACECLKOUT Timing

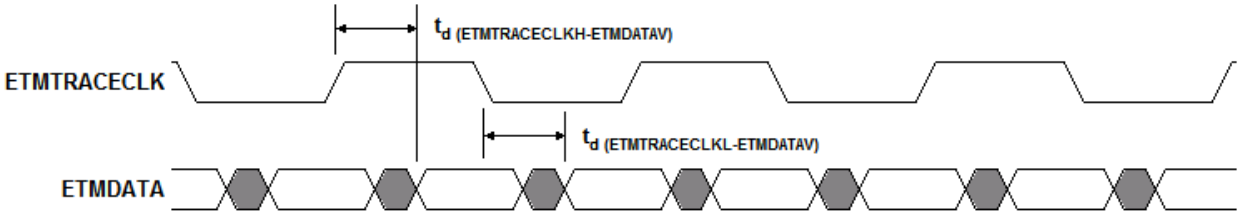


Figure 6-25. ETMDATA Timing

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7 Detailed Description

7.1 Overview

The AM273x is a high performance microcontroller with an integrated C66x DSP and is ideally suited for applications needing requiring conditioning and processing functions. Two R5F cores (with optional lockstep capability) running at 400 MHz with 5MB of internal memory coupled along with a broad range of automotive and industrial connectivity peripherals and an easy to use SDK enables our customers to address a wide range of use cases in automotive and industrial markets. Functional safety and security (HSM) features are integrated to address emerging market trends.

One representative use case is for the AM273x to operate as the MCU host in an automotive radar system. In this role AM273x provides data aggregation, FFT, CFAR, range, velocity and angle estimation and tracking processing. The AM273x can operate as a host in single or dual (cascaded) front-end radar application.

As seen in Figure 3-1 the AM273x is divided into a few high level functional subsystems. Each subsystem contains specific control, signal processing, and digital communication peripherals.

- Main Subsystem (MSS): MCU Core, Cryptographic Core, Mailbox, EDMA, RTI, QSPI, SPI, CAN-FD, I2C, UART, Ethernet and GPIO
- DSP Subsystem (DSS): C66x Core, HWA2.0 Accelerator, Mailbox, EDMA, RTI
- Radar Controller Subsystem (RCSS): EDMA, CSI2A/B, SPIA/B, I2C and GPIO

Each primary subsystem is then interconnected through an ECC enabled, switch interconnect bus, allowing for EDMA transfer of data between peripherals and processing cores.

7.2 Main Subsystem

The main subsystem (MSS) is the primary controller of the device and controls all the other device subsystem cores and peripherals. The MSS contains the Cortex-R5F (MSS R5F) processor and associated peripherals and associated EDMA and Mailbox IPC functions. The MSS also controls wider system connectivity and network peripherals such as the I2C, UART, SPI, CAN-FD, EPWM, and Ethernet. The MSS is connected to the primary interconnect through the Main Subsystem (MSS) Interconnect which is ECC enabled.

The MSS contrains its own dedicated functional safety block consisting of DCC, ESM, LBIST/PBIST, CRC Watchdog Timer and GPADC for safety monitoring of critical system signals such as power supply and temperature monitors.

7.3 DSP Subsystem

The DSP subsystem (DSS) contains the TI high performance C66x DSP, HWA 2.0, and a high-bandwidth interconnect for high performance (128-bit, 150MHz), and associated data transfer peripherals: 6x EDMA for data transfer, 2x RTI and Mailbox IPC. The Aurora/LVDS measurement data output interface is also mastered by the C66x DSP. L3 shared memory is available on the DSS interconnect which is also ECC enabled.

For more information on DSP functionality, see the

7.4 Radar Control Subsystem

The radar control subsystem (RCSS) integrates a high-bandwidth interconnect with a pair of 4-lane, CSI 2.0 receivers (CSI2_RX0 and CSI2_RX1), two SPI controllers (RCSS_SPIA and RCSS_SPIB), I2C controllers and a set of GPIO. The SPI, I2C and GPIO peripherals can be utilized for controlling and configuring the attached sensor devices. The CSI 2.0 receivers allow for receiveing high-speed sensor data samples such as samples.

Within the device pinlist there are also a number of pins which have been named in support of a radar front-end connection use-case. All of these signals resolve to various MSS/RCSS GPIO functionality in the device pinmux and therefore do not exist in the list of pinmux signal. See the below description of these signals.

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Table 7-1. Radar Front-End (FE) Control Signals

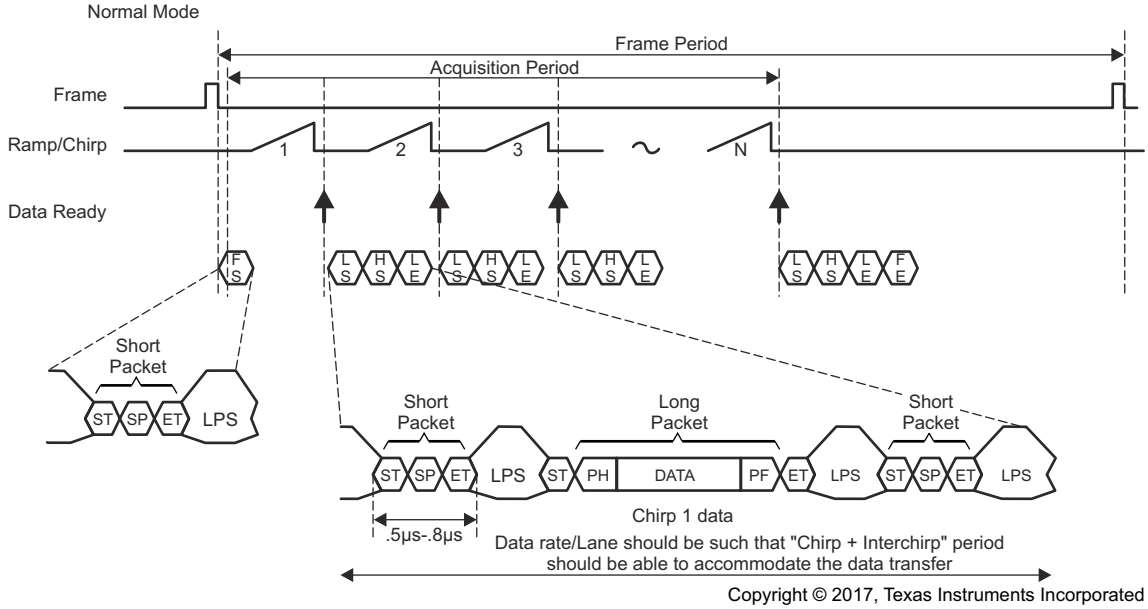
Signal Name	Description and Intended Function
FE1_REFCLK	Radar front-end refrence clock detection input. Could be attached to output clock available from radar front-end device.
FE2_REFCLK	
HW_SYNC_FE1	Radar front-end frame synchronization output trigger input/output. Could be used to drive the attached radar front-end frame trigger, or used to detect the frame trigger source.
HW_SYNC_FE2	
NERRORIN_FE1	Radar front-end error status input. Could be used to deted error output status of attached radar front-end.
NERRORIN_FE2	
NRESET_FE1	Radar front-end reset output. Could be used to drive reset of attached radar front-end.
NRESET_FE2	
NWARMRESET_IN_FE1	Radar front-end warm reset input/output. Could be used to drive warm reset of attached radar front-end, or detect reset status.
NWARMRESET_IN_FE2	

7.5 Other Subsystems

7.5.1 Radar A2D Data Format Over CSI2 Interface

The AM273x device uses MIPI D-PHY / CSI2-based format to receive the raw A2D samples from an external radar transceiver. This is shown in Figure 7-1.

- Supports four data lanes
- CSI-2 data rate scalable from 150 Mbps to 600 Mbps per lane
- Virtual channel based
- CRC generation



Frame **S**tart – CSI2 VSYNC Start Short Packet**L**ine **S**tart – CSI2 HSYNC Start Short Packet**L**ine **E**nd – CSI2 HSYNC End Short Packet**F**rame **E**nd – CSi2 VSYNC End Short Packet

Figure 7-1. CSI-2 Transmission Format

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The data payload is constructed with the following three types of information:

- Chirp profile information
- The actual chirp number
- A2D data corresponding to chirps of all four channels
  - Interleaved fashion
- Chirp quality data (configurable)

The payload is then split across the four physical data lanes and transmitted to the receiving D-PHY. The data packet packing format is shown in Figure 7-2.

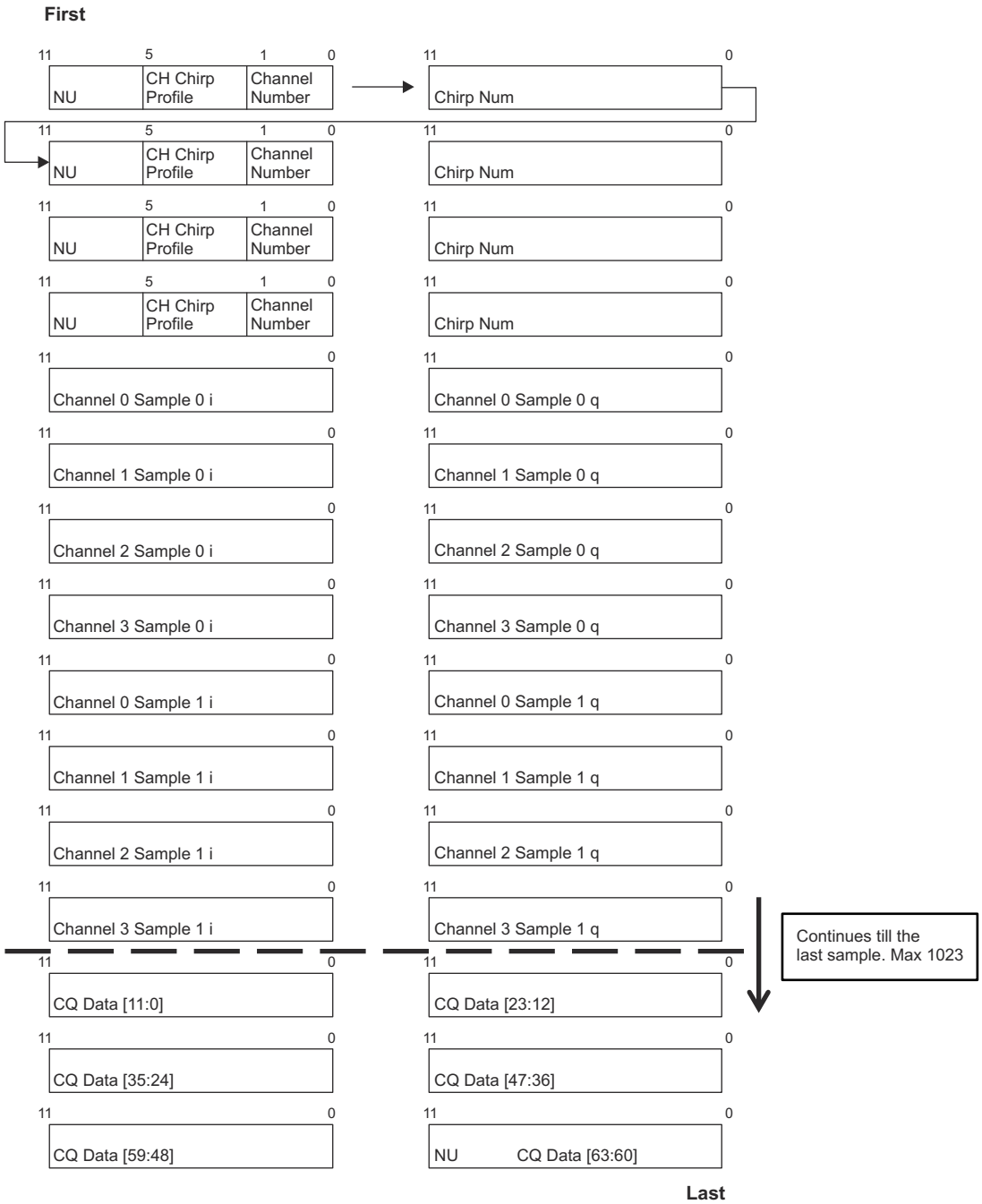


Figure 7-2. Data Packet Packing Format for 12-Bit Complex Configuration

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7.5.2 ADC Channels (Service) for User Application

The AM273x device includes provision for an ADC service for user application, where the GPADC engine present inside the device can be used to measure up to nine external and internal voltages. The ADC1, ADC2, ADC3, ADC4, ADC5, ADC6, ADC7, ADC8 and ADC9 pins are used for this purpose.

Note

GPADC structures are used for measuring the output of internal temperature sensors.

GPADC Specifications:

- 625Ksps SAR ADC
- 0 to 1.8-V input range
- 10-bit resolution

Table 7-2. GPADC Parameters

PARAMETER	TYP	UNIT
ADC supply	1.8	V
ADC unbuffered input voltage range	0 – 1.8	V
ADC buffered input voltage range(1)	0.4 – 1.3	V
ADC resolution	10	bits
ADC offset error	±5	LSB
ADC gain error	±5	LSB
ADC DNL	–1/+2.5	LSB
ADC INL	±2.5	LSB
ADC sample rate	625	Ksps
ADC sampling time	400	ns
ADC internal cap	10	pF
ADC buffer input capacitance	2	pF
ADC input leakage current	3	uA

(1) Outside of given range, the buffer output will become nonlinear.

7.6 Boot Modes

AM273x bootloader functionality is controlled by a set of start on power (SOP) pins. These pins states are latched on de-assertion of the NRESET pin after power on of the device. The SOP pins are multiplexed with functional mode signals before and during NRESET de-assertion. After bootloader execution the functional mode operation is then restored. See the power on reset timing sequence for more details. The following tables describe the SOP pin operation.

Host hardware should provide a means for driving these SOP pins to their required states during NRESET de-assertion, but also allow for their functional mode operation if required by the intended application.

Table 7-3. SOP Pins

Pin	SOP Mode Signal Name	Pinlist Signal Name
D6	SOP[0]	TDO
E17	SOP[1]	MSS_MIBSPIB_CS2
F1	SOP[2]	PMIC_CLKOUT
V9	SOP[3]	MSS_UARTB_TX
W2	SOP[4]	MSS_UARTA_TX

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Table 7-4. SOP Pin Modes

Boot Options	SOP Mode
Bootmode SOP Modes	• SOP[2:0] = 0b011 selects SOP_MODE2 • SOP[2:0] = 0b001 selects SOP_MODE4 • SOP[2:0] = 0b101 selects SOP_MODE5 • All other states reserved and should not be selected.
Crystal Detect SOP Modes	• SOP[4:3] = 0b00 selects 40 MHz Crystal Mode • SOP[4:3] = 0b01 selects 45.1584 MHz Crystal Mode • SOP[4:3] = 0b10 selects 49.152 MHz Crystal Mode • SOP[4:3] = 0b11 selects 50 MHz Crystal Mode

Table 7-5. Bootmode SOP Descriptions

Bootmode SOP Modes	Function	Description
SOP_MODE2	Development Mode	Development boot mode. The AM273x ROM bootloader will setup the device to wait for a JTAG debugger connection.
SOP_MODE4	Functional Mode	Functional boot mode of the AM273x device. In this mode, the ROM bootloader will attempt to load a valid secondary bootloader image from primarily the QSPI interface and secondarily the SPI host interface.
SOP_MODE5	Device Management Mode	QSPI flash programming boot mode of the AM273x device. In this mode the ROM bootloader will attempt to receive a valid QSPI secondary bootloader image over MSS_UARTA_TX/RX (pins W2, U3) and attempt to flash an attached QSPI memory with this image.

Table 7-6. Crystal Detect SOP Mode Description

Crystal Detect SOP Modes	
40 MHz Crystal Crystal Mode	ROM bootloader image expects a 40 MHz nominal crystal clock source.
45.1584 MHz Crystal Mode	ROM bootloader image expects a 45.1584 MHz nominal crystal clock source.
49.152 MHz Crystal Mode	ROM bootloader image expects a 49.152 MHz nominal crystal clock source.
50 MHz Crystal Mode	ROM bootloader image expects a 50 MHz nominal crystal clock source.

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8 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Typical Application

8.1.1 Schematic

The below AM273x Example Schematic shows an exerpt the AM273x EVM schematic. The exerpt focuses only on the AM273x device schematic symbols to show the device pin usage.

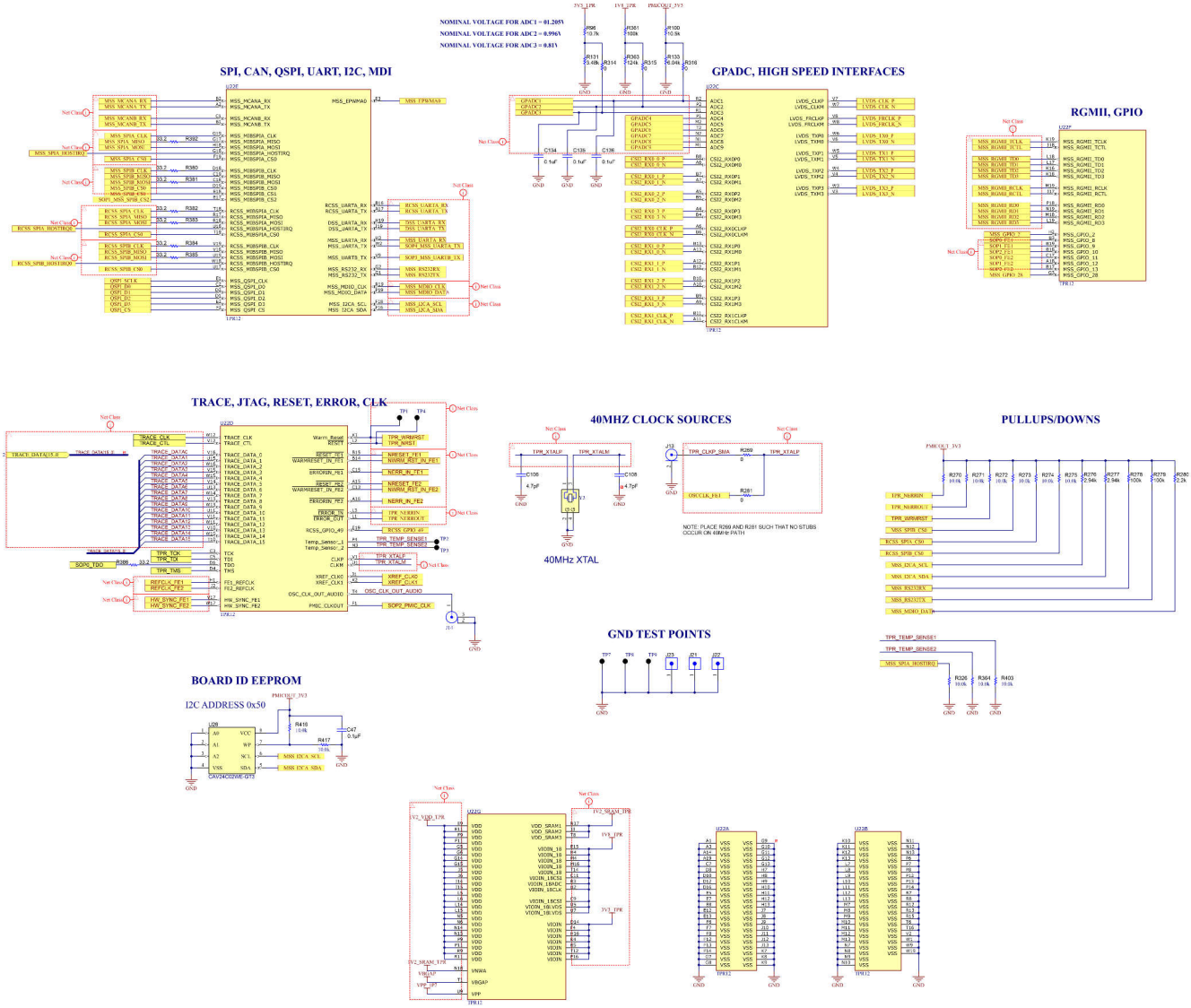


Figure 8-1. AM273x Example Schematic

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8.1.2 Layout

8.1.2.1 Layout Example

The following figures are exerpts from the AM273x EVM PCB layout, assembly and layer stack-up.

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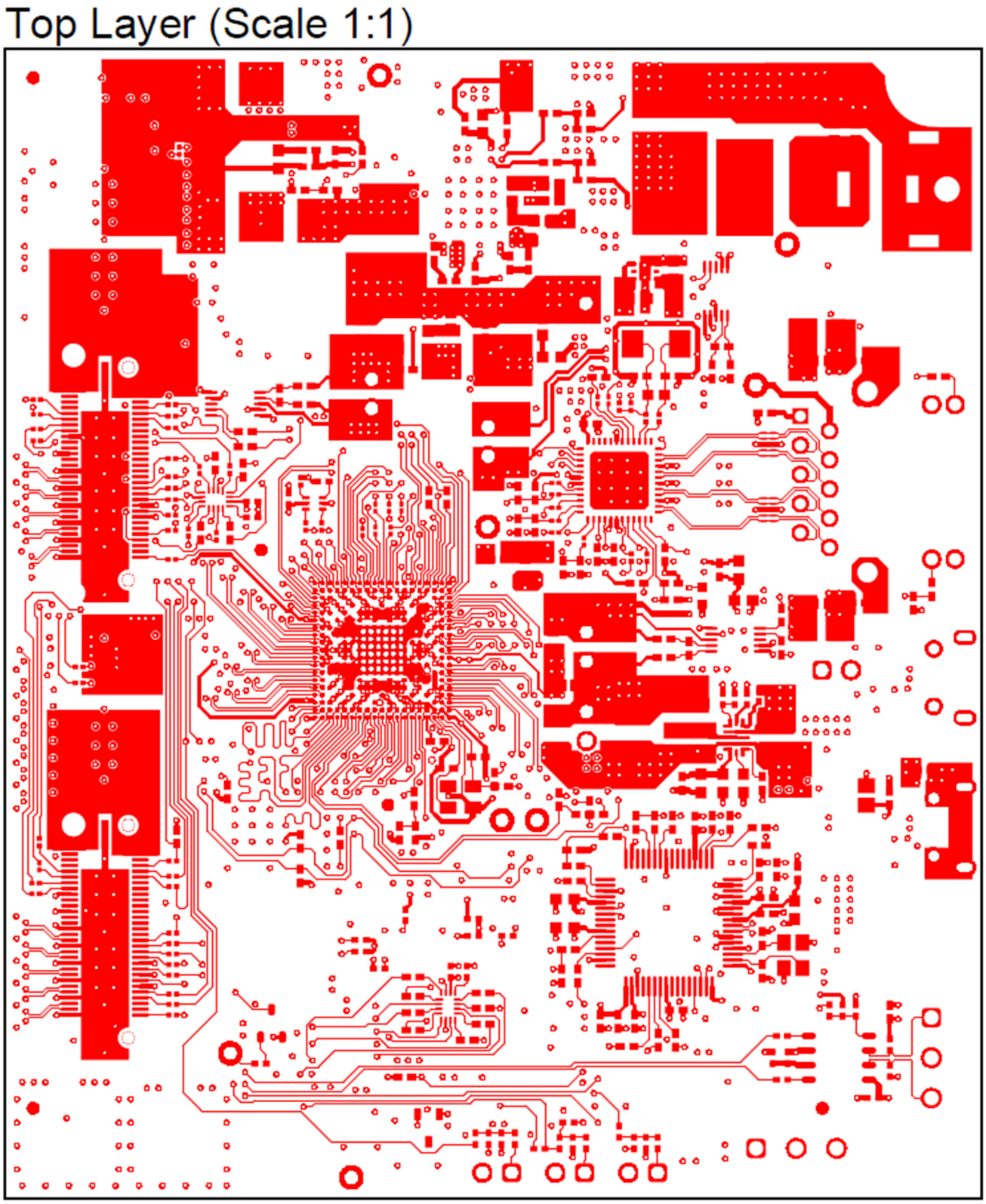


Figure 8-2. AM273x EVM - Layer 1 (Top)

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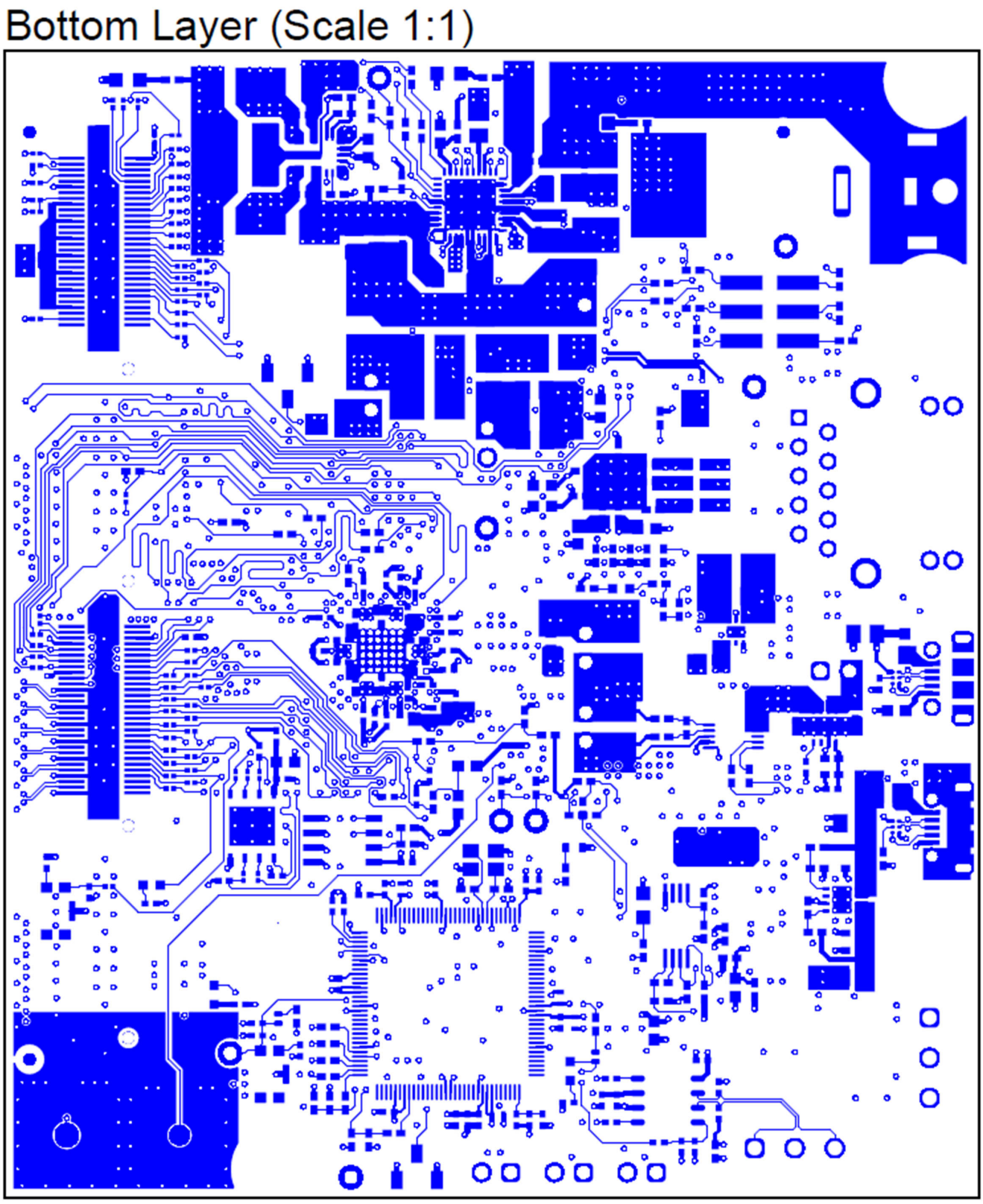


Figure 8-3. AM273x EVM - Layer 10 (Bottom)

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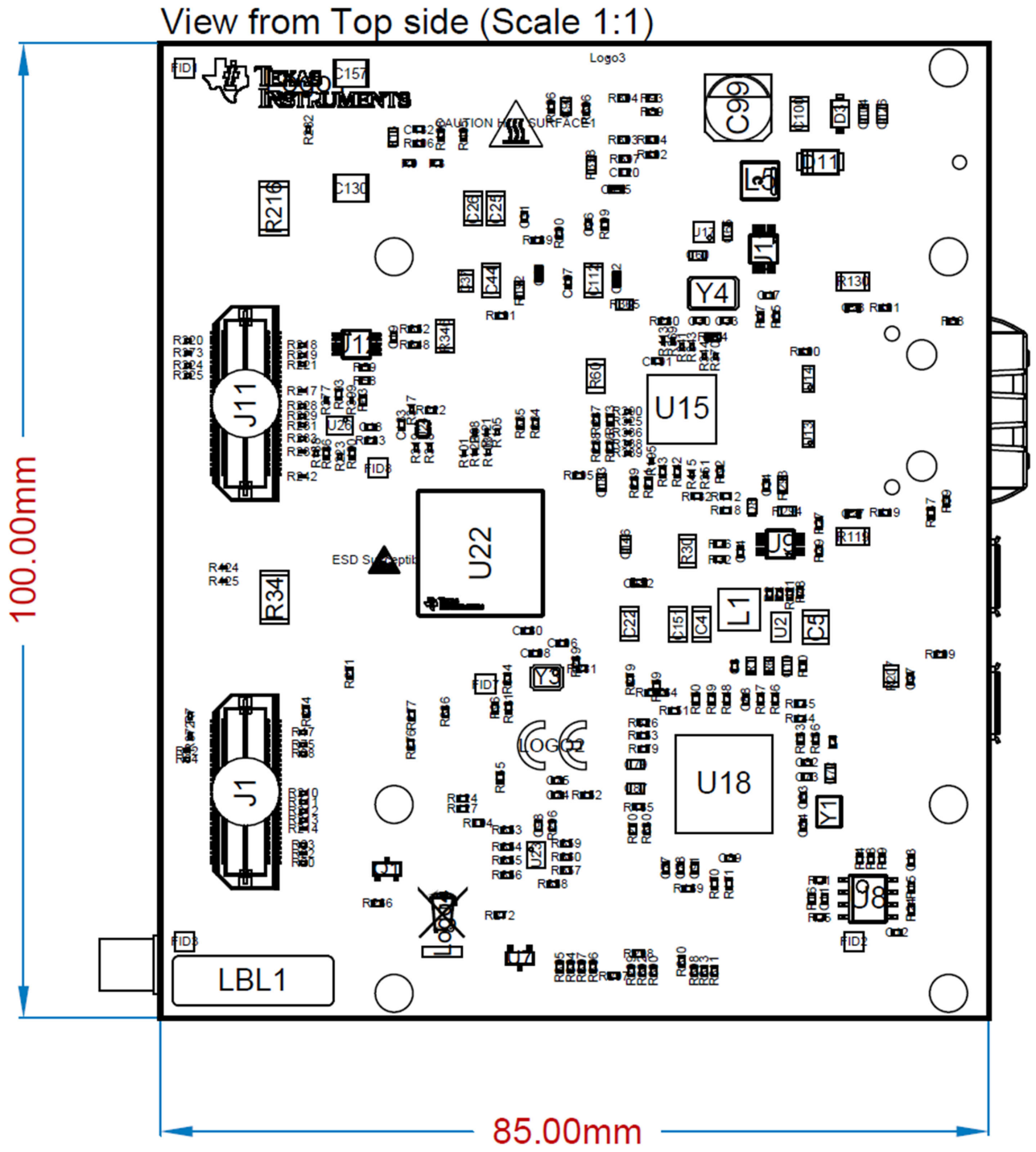


Figure 8-4. AM273x EVM - Top Assembly

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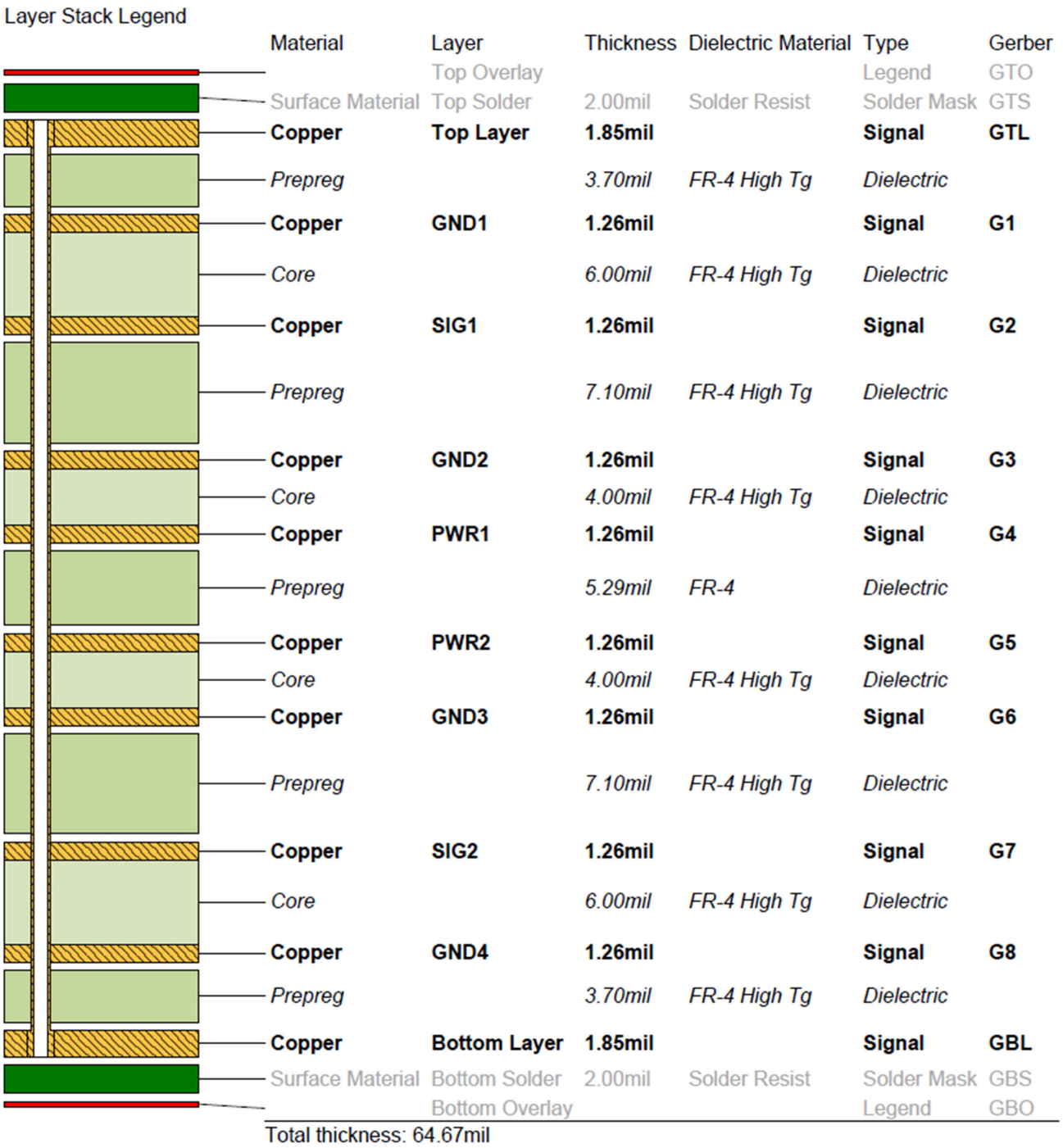


Figure 8-5. AM273x EVM - Layer Stackup

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microcontrollers (MCU) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *AM273x*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, *AM273x*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX and TMDX) through fully qualified production devices and tools (TMS and TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

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TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *ZCE*), the temperature range (for example, blank is the default commercial temperature range), and the device speed range, in megahertz (for example, *400 MHz*). Table 9-1 and Figure 9-1 provides a legend for reading the complete device name for any *AM273x* device.

For orderable part numbers of *AM273x* devices in the *AM273x* package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the Silicon Errata .

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9.1.1 Standard Package Symbolization

Note

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

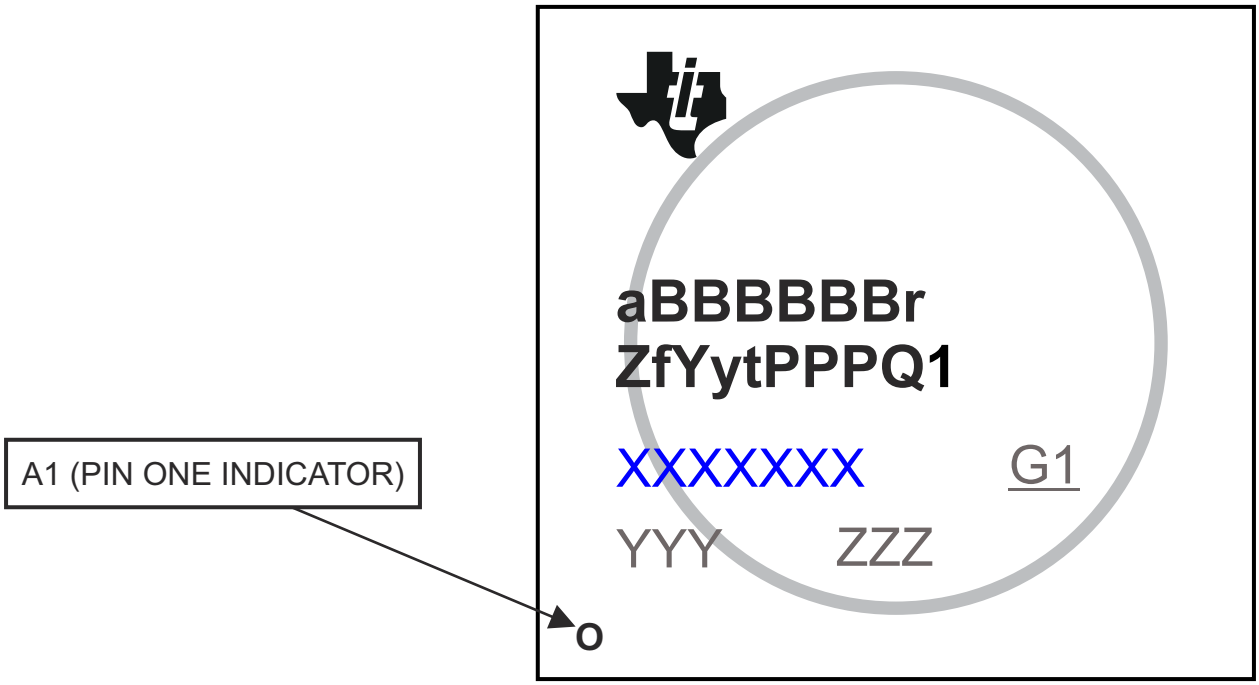


Figure 9-1. Printed Device Reference

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9.1.2 Device Naming Convention

Table 9-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
a(1)	Device evolution stage	X	Prototype
		P	Preproduction (production test flow, no reliability data)
		BLANK	Production
BBBBBB	Base production part number	AM2731	See Table 4-1, *Device Comparison*
		AM2732	
r	Device revision	A	SR 1.0(Non-secure)
		B	SR 1.1(Secure)
		C	SR 1.2(Secure)
Z	Device Speed and Memory Grades	A	See Table 6-3, *Speed and Memory Grade*
		D	
		L	
		M	
		N	
f	Features(see Table 4-1, *Device Comparison*)	R	ZCE Package Device
		S	NZN Package Device
Y	Functional Safety	G	Non-Functional Safety Device
		F	Functional Safety Quality Managed Device
y	Security	G	Non-Secure
		H	Production Key HS Device
t(2)	Temperature (see ,*Absolute Maximum Ratings*)	A	–40°C to 105°C - Extended Industrial
		I	–40°C to 125°C - Automotive
		Q	–40°C to 140°C - Extended Automotive
PPP	Package Designator	ZCE	ZCE NFBGA-N285 (13 mm × 13 mm) 0.65 mm Pitch Package
		NZN	NZN NFBGA-N225 (13 mm × 13 mm) 0.80 mm Pitch Package
Q1	Automotive Designator	Q1	Auto Qualified (AEC-Q100)
		EP	Enhanced Product
XXXXXXX			Lot Trace Code (LTC)
YYY			Production Code; For TI use only
ZZZ			Production Code; For TI use only
O			Pin one designator
G1			ECAT—Green package designator

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.
Prototype devices are shipped against the following disclaimer:
"This product is still in development and is intended for internal evaluation purposes."
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

(2) Applies to device max junction temperature.

Note

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

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9.2 Tools and Software

The following products support development for AM273x platforms:

Development Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

SYSCONFIG The SYSCONFIG Pin MUX Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs. Results are output as C header/code files that can be imported into software development kits (SDKs) or used to configure customer's custom software.

AM273x Power Estimation Tool (PET) AM273x Power Estimation Tool (PET) provides users the ability to gain insight in to the power consumption of select TI processors. The tool includes the ability for the user to choose multiple application scenarios and understand the power consumption as well as how advanced power saving techniques can be applied to further reduce overall power consumption.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

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9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral is listed below.

The following documents describe the AM273x family of devices.

Technical Reference Manual

AM273x Microntrollers Technical Reference Manual Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM273x family of devices.

Errata

AM273x Microntrollers Silicon Errata Describes the known exceptions to the functional specifications for the device.

Hardware Design Guide

AM273x Hardware Design Guide Describes the known exceptions to the functional specifications for the device.

Tip: Search TI.com using literature numbers.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from February 28, 2022 to December 30, 2023 (from Revision A (February 2022) to Revision B (December 2023)) **Page**

- Added NZN package information to feature list. Made changes to Functional Safety section. Aligned package summary to other AM2x devices. Updated recommend PMIC in power features..... 1
- Correcting core memory details. Added additional peripheral and package information for new NZN devices. 5
- Updated companion PMIC part number and links..... 6
- Adding new signal descriptions section format to align with to AM2x standard datasheet formatting.....34

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- Adding new device grades..... 55
- Correcting R5F L1 TCB allocation detail notes. Correcting total L3 shared memory..... 56
- Adding Thermal Resistance Characteristics for nFBGA Package (NZN225A)..... 56
- (Power Supply Sequencing and Reset Timing): Added further detail to the power-on/off sequence diagram. Added power-on/off sequence timing table for further clarification.....57
- Added some additional clarification on the MSS vs. RCSS MIBSPI peripherals and the HOSTIRQ functions..... 64
- Adding more context to the radar front-end (FE) signals in the device pinlist..... 85
- Updates to support NZN package, AM2731 and SR1.2 revision devices..... 99
- Adding hardware design guide links.....101

Changes from December 17, 2021 to February 28, 2022 (from Revision * (December 2021) to Revision A (February 2022)) **Page**

- (Device Comparison): Added Q1, automotive device product links..... 5
- (ESD Ratings - Automotive): Updating HBM tolerance to +/-2kV..... 52
- (Power-On Hours (POH): Added extended industrial POH data. Modified automotive/industrial table formatting. 52
- (Power-On Hours (POH)): Added automotive temperature profile table..... 52
- (Power-On Hours (POH)): Added industrial temperature profile table..... 53
- (Operating Performance Points): Changing order of device grades.....55
- (Power Supply Sequencing and Reset Timing): Added further detail to the power-on/off sequence diagram. Added power-on/off sequence timing table for further clarification.....57

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

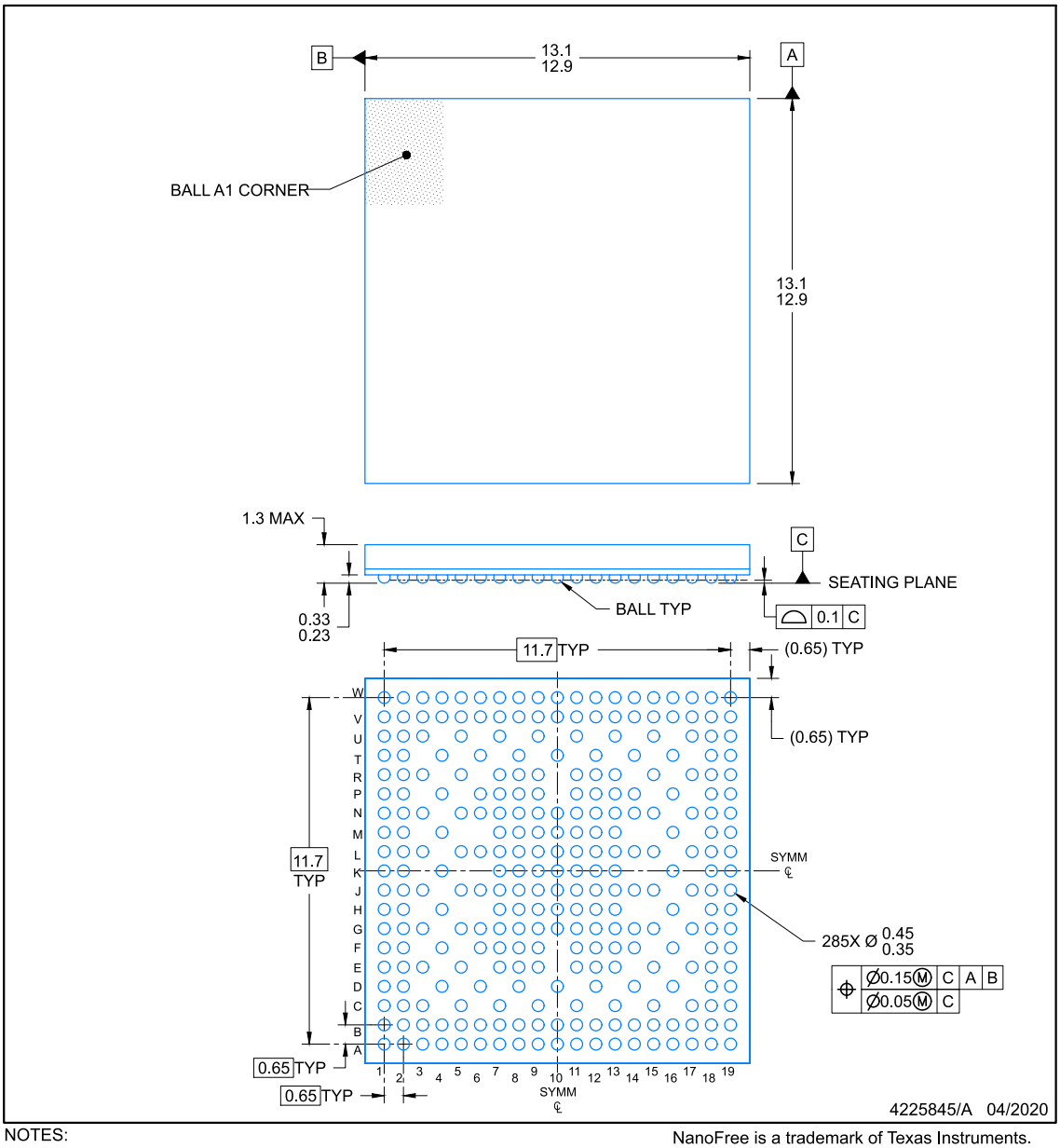
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PACKAGE OUTLINE

ZCE0285A-C01

NFBGA - 1.3 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

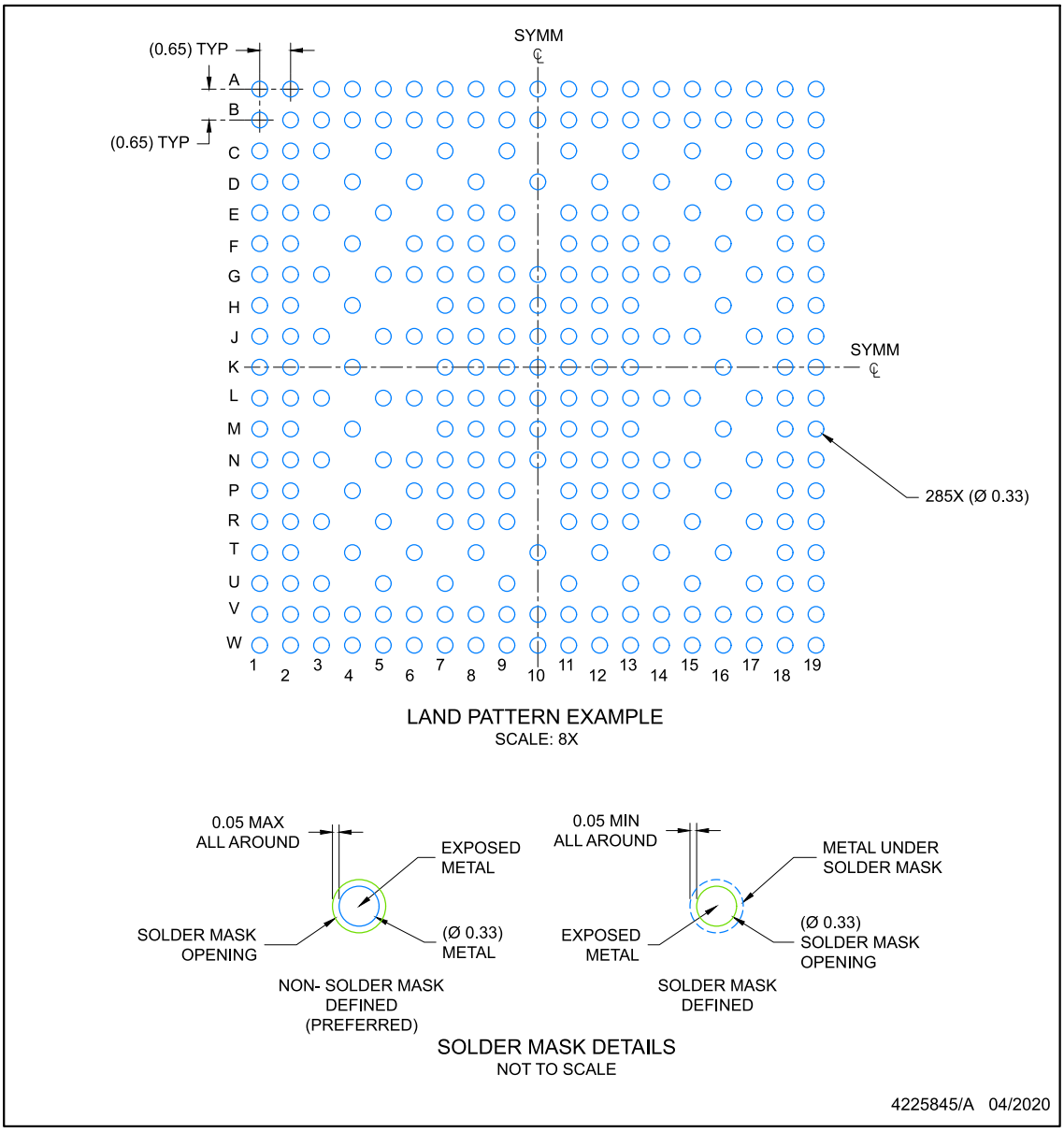
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EXAMPLE BOARD LAYOUT

ZCE0285A-C01

NFBGA - 1.3 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

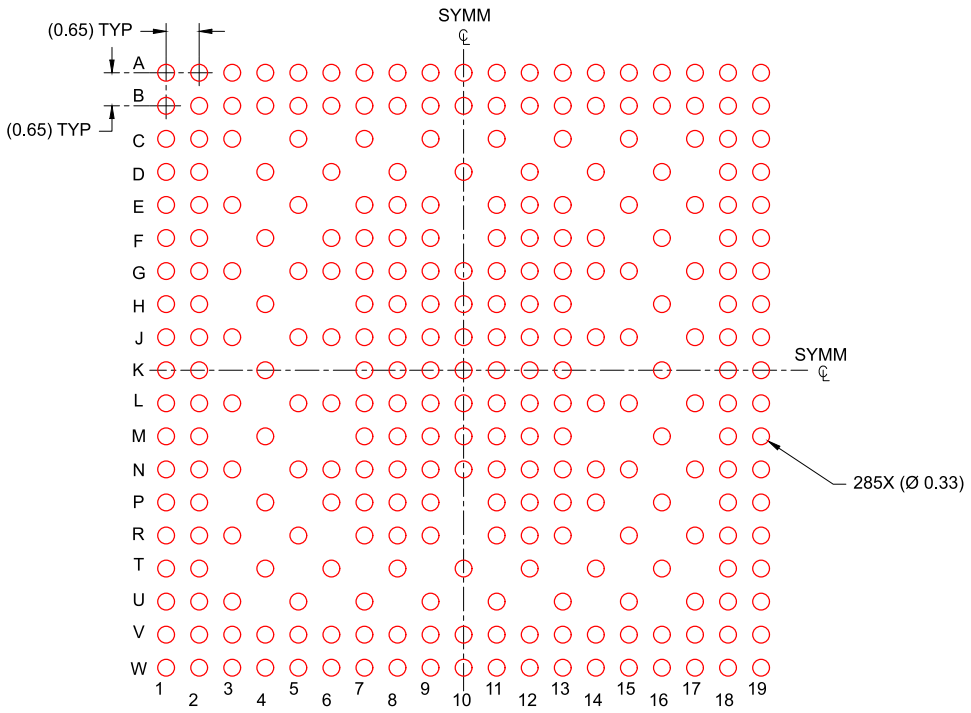
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

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EXAMPLE STENCIL DESIGN

ZCE0285A-C01 — **NFBGA - 1.3 mm max height**

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4225845/A 04/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM2731CLSFHQNZNRQ1	ACTIVE	NFBGA	NZN	225	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 140	AM2731C LSFHQNZN 711	Samples
AM2732ADRFGAZCER	ACTIVE	NFBGA	ZCE	285	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	AM2732A DRFGAZCE 711	Samples
AM2732ADRFGQZCERQ1	ACTIVE	NFBGA	ZCE	285	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 140	AM2732A DRFGQZCEQ1 711	Samples
AM2732CDRFHAZCER	ACTIVE	NFBGA	ZCE	285	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	AM2732C DRFHAZCE 711	Samples
AM2732CDRFHQZCERQ1	ACTIVE	NFBGA	ZCE	285	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 140	AM2732C DRFHQZCEQ1 711	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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OTHER QUALIFIED VERSIONS OF AM2732, AM2732-Q1 :

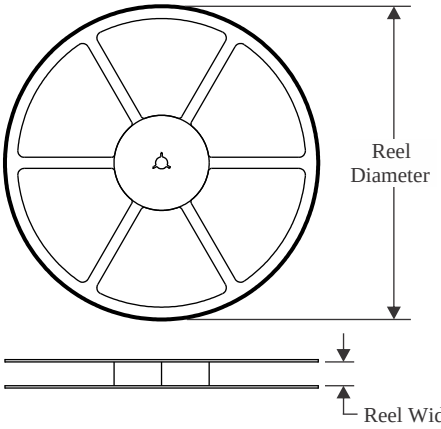
- Catalog : AM2732
- Automotive : AM2732-Q1

NOTE: Qualified Version Definitions:

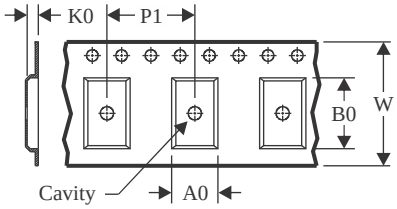
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

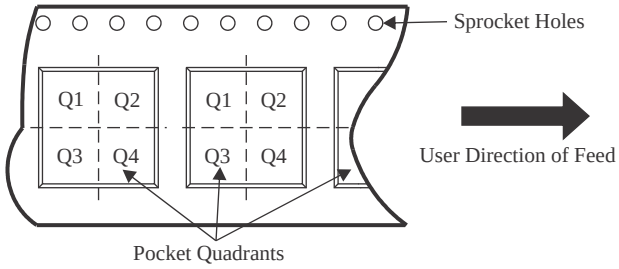


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

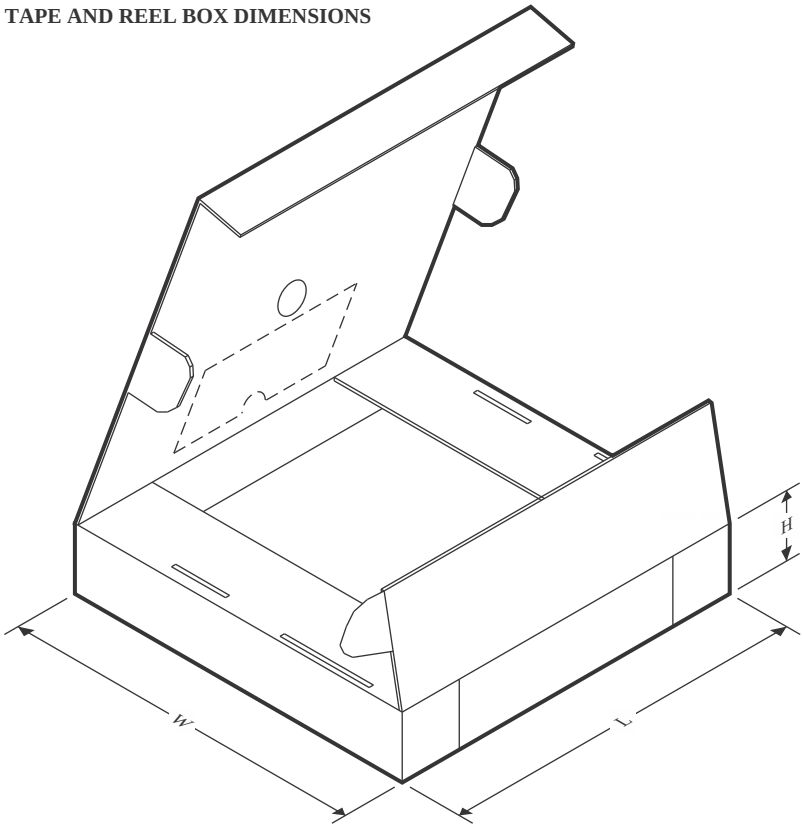
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM2731CLSFHQNZNRQ1	NFBGA	NZN	225	1000	330.0	24.4	13.3	13.3	2.35	16.0	24.0	Q1
AM2732ADRFGAZCER	NFBGA	ZCE	285	1000	330.0	24.4	13.3	13.3	2.35	16.0	24.0	Q1
AM2732ADRFGQZCERQ1	NFBGA	ZCE	285	1000	330.0	24.4	13.3	13.3	2.35	16.0	24.0	Q1
AM2732CDRFHAZCER	NFBGA	ZCE	285	1000	330.0	24.4	13.3	13.3	2.35	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

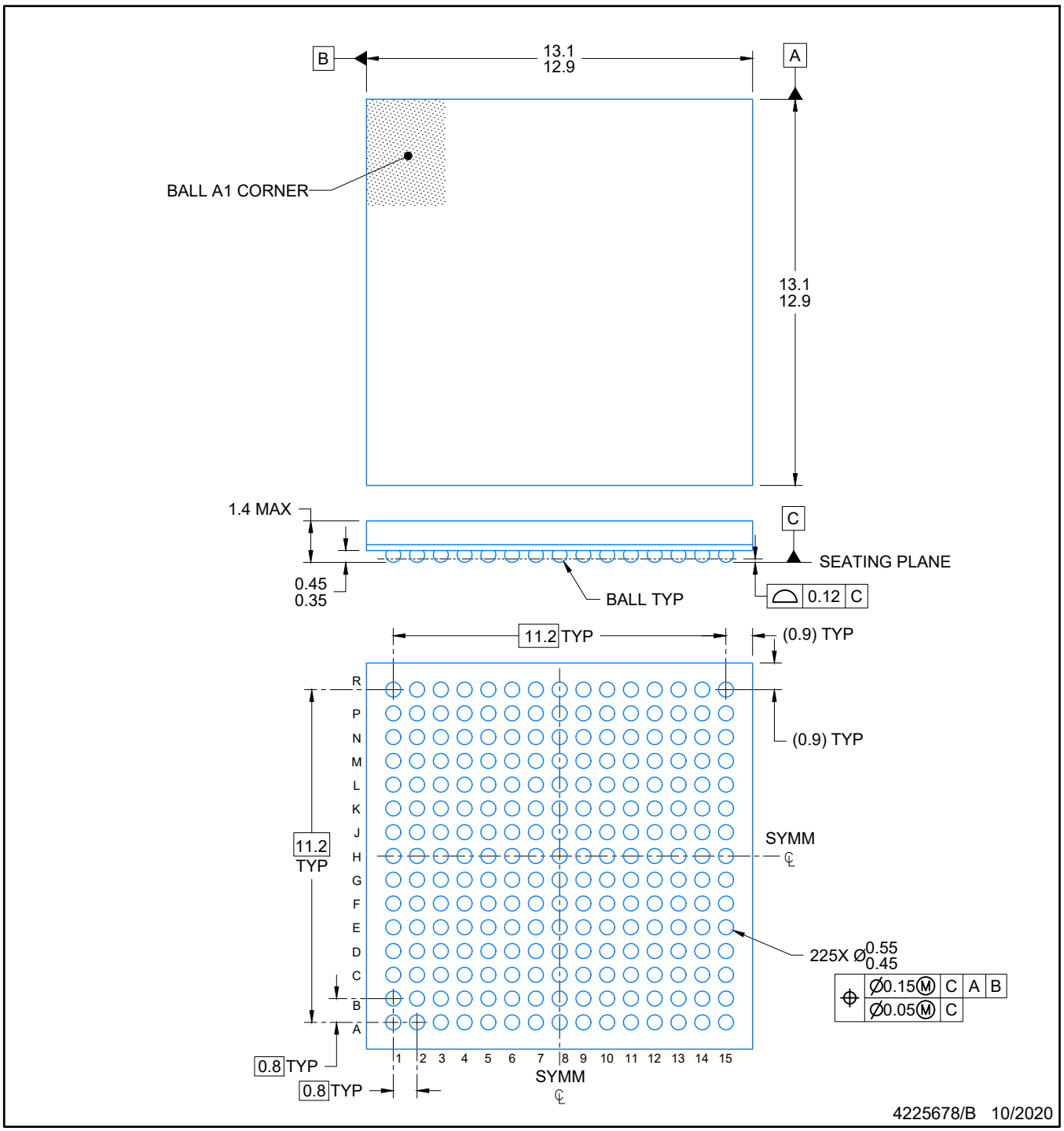
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM2731CLSFHQNZNRQ1	NFBGA	NZN	225	1000	336.6	336.6	41.3
AM2732ADRFGAZCER	NFBGA	ZCE	285	1000	336.6	336.6	41.3
AM2732ADRFGQZCERQ1	NFBGA	ZCE	285	1000	336.6	336.6	41.3
AM2732CDRFHAZCER	NFBGA	ZCE	285	1000	336.6	336.6	41.3

PACKAGE OUTLINE

NZN0225A

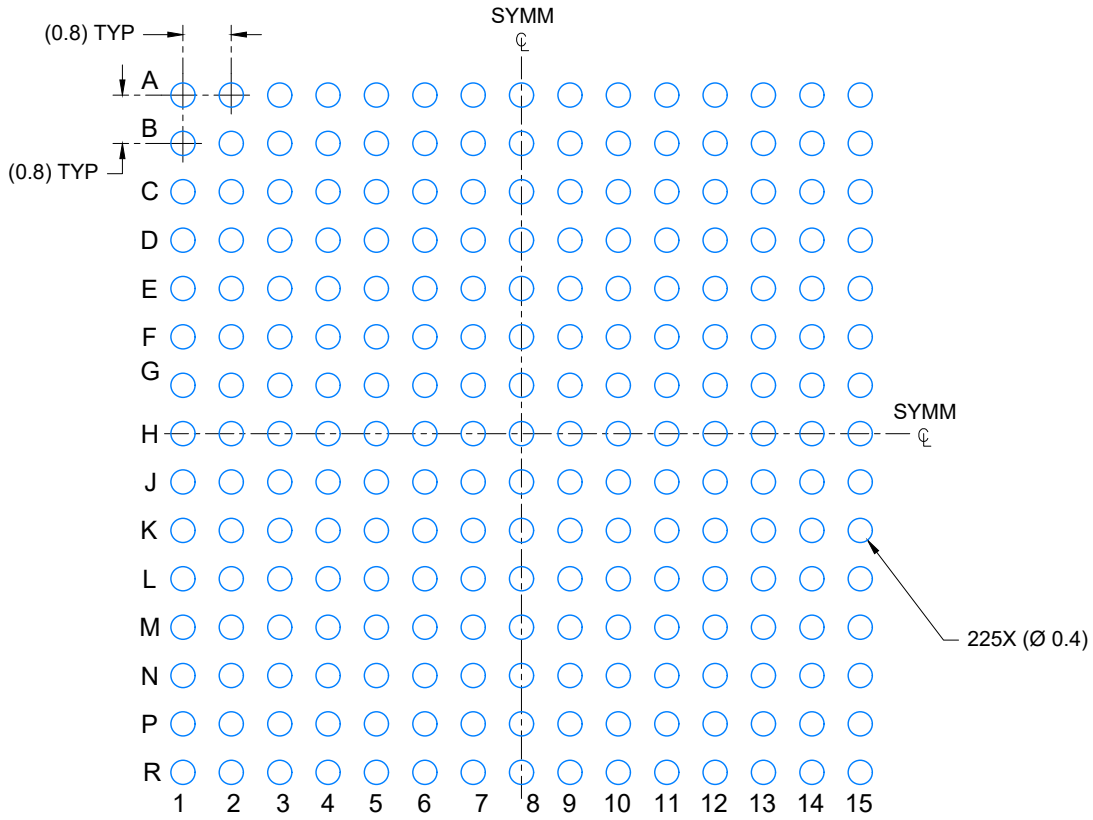
NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY

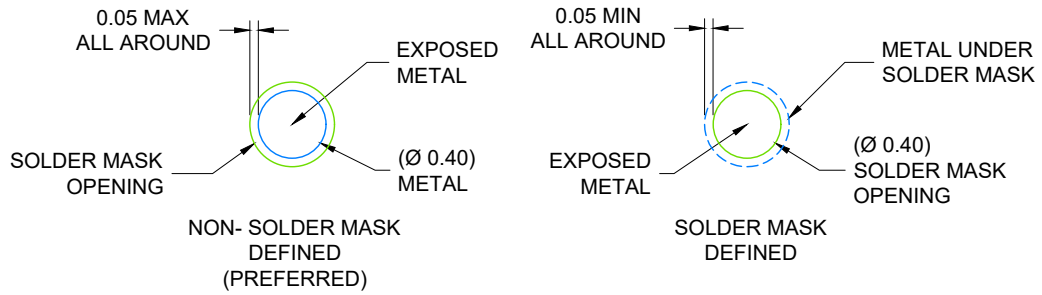


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 8X

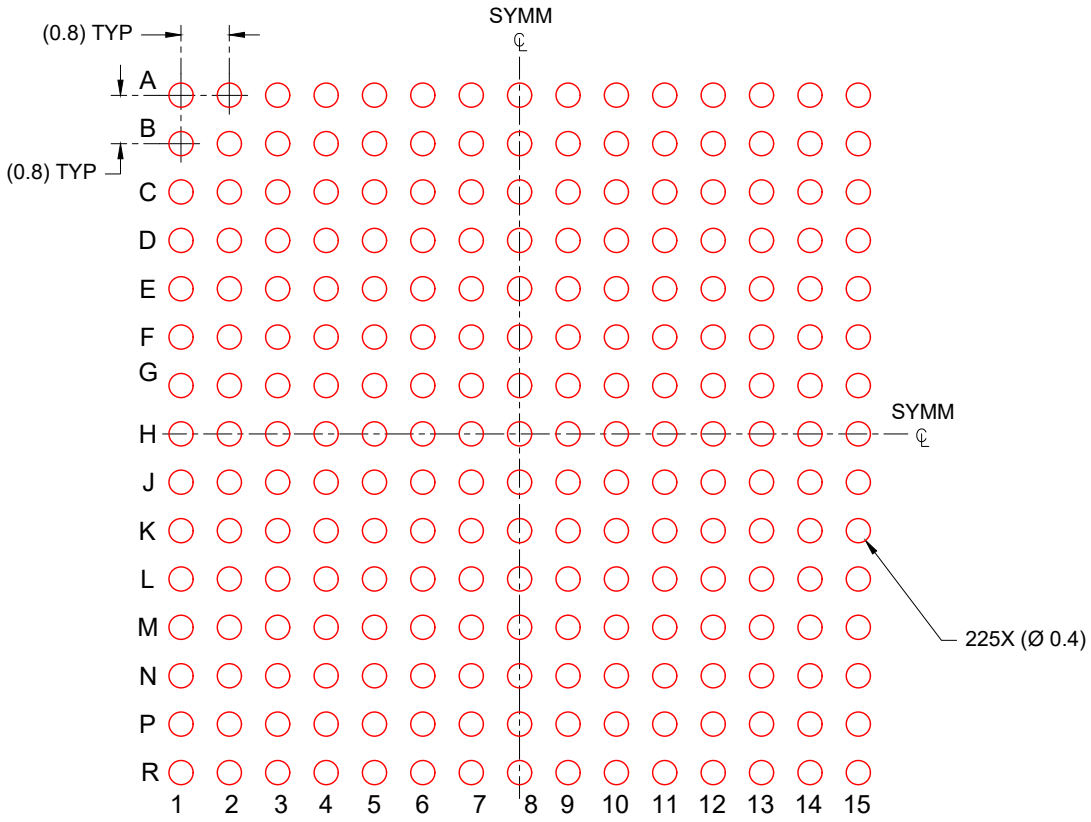


SOLDER MASK DETAILS
NOT TO SCALE

4225678/B 10/2020

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 8X

4225678/B 10/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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