TEXAS INSTRUMENTS

UCC28050, UCC28051, UCC38050, UCC38051

SLUS515G – SEPTEMBER 2002 – REVISED DECEMBER 2015

UCC2805x, UCC3805x Transition Mode PFC Controller

1 Features

- Transition Mode PFC Controller for Low Implementation Cost
- Industry Pin Compatibility With Improved Feature Set
- Improved Transient Response With Slew-Rate Comparator
- Zero Power Detect to Prevent Overvoltage Protection (OVP) During Light Load Conditions
- Accurate Internal VREF for Tight Output Regulation
- Two UVLO Options
- OVP, Open-Feedback Protection, and Enable Circuits
- ±750-mA Peak Gate Drive Current
- Low Start-Up and Operating Currents
- Lead (Pb)-Free Packages

2 Applications

- Single-Stage PFC Flyback Converters for Lighting and Motor Drives
- Switch-Mode Power Supplies for Desktops, Monitors, TVs, and Set Top Boxes (STBs)
- AC Adapter Front-End Power Supplies
- Electronic Ballasts

3 Description

The UCC38050 and UCC38051 are PFC controllers for low-to-medium power applications requiring compliance with IEC 1000-3-2 harmonic reduction standard. The controllers are designed for a boost preregulator operating in transition mode (also referred to as boundary-conduction mode or critical conduction-mode operation). They feature a transconductance voltage amplifier for feedback error processing, a simple multiplier for generating a current command proportional to the input voltage, a current-sense (PWM) comparator, PWM logic, and a totem-pole driver for driving an external FET.

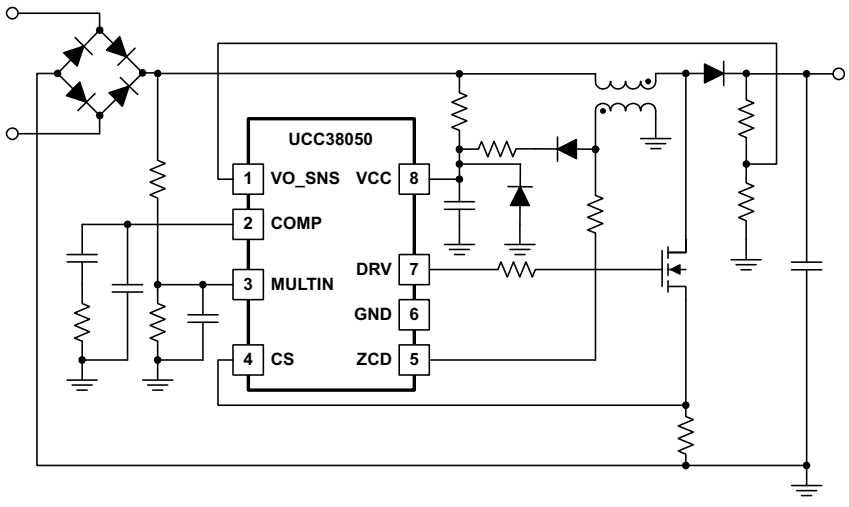
In the transition mode operation, the PWM circuit is self-oscillating, with the turnon being governed by an inductor zero-current detector (ZCD pin), and the turnoff being governed by the current-sense comparator. Additionally, the controller provides features such as peak current limit, default timer, overvoltage protection (OVP) and enable.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28050, UCC28051, UCC38050, UCC38051	SOIC (8)	3.91 mm × 4.90 mm
	PDIP (8)	6.35 mm × 9.81 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision F (March 2009) to Revision G **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

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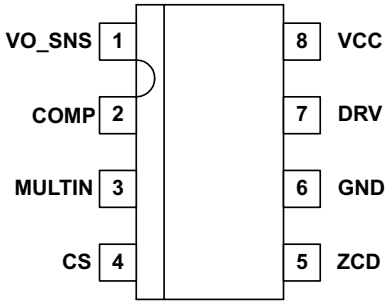
5 Pin Configuration and Functions

D or P Package
8-Pin SOIC or PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	2	O	Output of the transconductance error amplifier. Loop compensation components are connected between this pin and ground. The output current capability of this pin is 10-µA under normal conditions, but increases to approximately 1-mA when the differential input is greater than the specified values in the specifications table. This voltage is one of the inputs to the multiplier, with a dynamic input range of 2.5 V to 3.8 V. During zero power or overvoltage conditions, this pin goes below 2.5 V nominal. When it goes below 2.3 V, the zero power comparator is activated, which prevents the gate drive from switching.
CS	4	I	This pin senses the instantaneous switch current in the boost switch and uses it as the internal ramp for PWM comparator. The internal circuitry filters out switching noise spikes without requiring external components. In addition, an external R-C filter may be required to suppress the noise spikes. An internal clamp on the multiplier output terminates the switching cycle if this pin voltage exceeds 1.7 V. Additional external filtering may be required. CS threshold is approximately equal to: $$L = \frac{\left(V_{AC(min)}\right)^2 \times \left(V_{OUT} - \sqrt{2} \times V_{AC(min)}\right)}{2 \times F_{s(min)} \times V_{OUT} \times P_{IN}} \quad (1)$$ V_{OFFSET} is approximately 75 mV to improve the zero crossing distortion.
DRV	7	O	The gate drive output for an external boost switch. This output is capable of delivering up to 750-mA peak currents during turn-on and turn-off. An external gate drive resistor may be needed to limit the peak current depending on the V_{CC} voltage being used. Below the UVLO threshold, the output is held low.
GND	6	–	The chip reference ground. All bypassing elements are connected to ground pin with shortest loops feasible.
MULTIN	3	I	This pin senses the instantaneous boost regulator input voltage through a voltage divider. The voltage acts as one of the inputs to the internal multiplier. Recommended operating range is 0 V to 2.5 V at high line.
VCC	8	–	The supply voltage for the chip. This pin should be bypassed with a high-frequency capacitor (greater than 0.1-µF) and tied to GND. The UCC38050 has a wide UVLO hysteresis of approximately 6.3 V that allows use of a lower value supply capacitor on this pin for quicker and easier start-up. The UCC38051 has a narrow UVLO hysteresis with of about 2.8 V, and a start-up voltage of about 12.5 V for applications where the operation of the PFC device must be controlled by a downstream PWM controller.
VO_SNS	1	I	This pin senses the boost regulator output voltage through a voltage divider. Internally, this pin is the inverting input to the transconductance amplifier (with a nominal value of 2.5 V) and also is input to the OVP comparator. Additionally, pulling this pin below the ENABLE threshold turns off the output switching, ensuring that the gate drive is held off while the boost output is pre-charging, and also ensuring no runaway if the feedback path is open.
ZCD	5	I	Input for the zero current detect comparator. The boost inductor current is indirectly sensed through the bias winding on the boost inductor. The ZCD pin input goes low when the inductor current reaches zero and that transition is detected. Internal active voltage clamps are provided to prevent this pin from going below ground or too high. If zero current is not detected within 400 µs, a reset timer sets the latch and gate drive.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}	(Internally clamped)		20	V
Input current into V_{CC} clamp	I_{DD}		30	mA
Input current	ZCD		±10	mA
Gate drive current (peak), I_{DRV}	DRV		±750	mA
Input voltage, V_{CC}	VO_SNS, MULTIN, CS		5	V
Maximum negative voltage	VO_SNS, MULTIN, DRV, CS		–0.5	V
Power dissipation at T_A = 50°C	D package		650	mW
	P package		1	W
Operating junction temperature range, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
SOIC PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VCC input voltage from a low-impedance source	VCC_{OFF} + 1 V		18	V
Operating junction temperature, T_J	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC2805x, UCC3805x		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.6	55.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.3	45.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.3	32.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14	23.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	32.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

T_A = 0°C to 70°C for the UCC3805x, –40°C to +105°C for the UCC2805x, $T_A = T_J$, V_{CC} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{CC} operating voltage					18	V
Shunt voltage		I_{VCC} = 25 mA	18	19	20	V
Supply current, off		$V_{CC} = V_{CC}$ turnon threshold –300 mV		75	125	µA
Supply current, disabled		VO_SNS = 0.5 V		2	4	mA
Supply current, on		75 kHz, C_L = 0 nF		4	6	mA
Supply current, dynamic operating		75 kHz, C_L = 1 nF		5	7	mA
UVLO						
V_{CC} turnon threshold	UCCx8050		15.4	15.8	16.4	V
	UCCx8051		12	12.5	13	
V_{CC} turnoff threshold			9.4	9.7	10	V
UVLO hysteresis	UCCx8050		5.8	6.3	6.8	V
	UCCx8051		2.3	2.8	3.3	
VOLTAGE AMPLIFIER (VO_SNS)						
Input voltage (V_{REF})	UCC3805x		2.46	2.5	2.54	V
	UCC2805x		2.45	2.5	2.55	
Input bias current					0.5	µA
V_{COMP} high		VO_SNS = 2.1 V	4.5		5.5	V
V_{COMP} low		VO_SNS = 2.55 V		1.8	2.45	V
gM		T_J = 25 °C, V_{COMP} = 3.5 V	60	90	130	µS
Source current	UCCx8050	VO_SNS = 2.1 V, V_{COMP} = 3.5 V	–0.2	–0.1		mA
	UCCx8051	VO_SNS = 2.1 V, V_{COMP} = 2.5 V	–200	–300	–400	µA
Sink current		VO_SNS = 2.7 V, V_{COMP} = 3.5 V	0.2	1		mA
OVER VOLTAGE PROTECTION / ENABLE						
Overvoltage reference	UCCx8050		VREF + 0.165	VREF + 0.19	VREF + 0.21	V
	UCCx8051		VREF + 0.15	VREF + 0.18	VREF + 0.21	
Hysteresis	UCCx8050		175	200	225	mV
	UCCx8051		150	180	210	
Enable threshold	UCCx8050		0.62	0.67	0.72	V
	UCCx8051		0.18	0.23	0.28	
Enable hysteresis			0.05	0.1	0.2	V
MULTIPLIER						
Multiplier gain constant (k)		V_{MULTIN} = 0.5 V, COMP = 3.5 V	0.43	0.65	0.87	1/V
Dynamic input range, V_{MULTIN} INPUT			0 to 2.5	0 to 3.5		V
Dynamic input range, COMP INPUT			2.5 to 3.8	2.5 to 4		V
Input bias current, MULTIN				0.1	1	µA
ZERO POWER						
Zero power comparator threshold(1)		Measured on V_{COMP}	2.1	2.3	2.5	V

(1) Ensured by design. Not production tested.

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Electrical Characteristics (continued)

T_A = 0°C to 70°C for the UCC3805x, –40°C to +105°C for the UCC2805x, $T_A = T_J$, V_{CC} = 12 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ZERO CURRENT DETECT					
Input threshold (rising edge)(1)		1.5	1.7	2	V
Hysteresis(1)		250	350	450	mV
Input high clamp	I = 3 mA		5	6	V
Input low clamp	I = −3 mA	0.3	0.65	0.9	V
Restart time delay		200	400		µs
CURRENT SENSE COMPARATOR					
Input bias current	CS = 0 V		0.1	1	µA
Input offset voltage(1)		–10		10	mV
Delay to output	CS to DRV		300	450	ns
Maximum current sense threshold voltage		1.55	1.7	1.8	V
PFC GATE DRIVER					
GT1 pull-up resistance	I_{OUT} = –125 mA		5	12	Ω
GT1 pull-down resistance	I_{OUT} = 125 mA		2	10	Ω
GT1 output rise time	C_{LOAD} = 1 nF, R_{LOAD} = 10 Ω		25	75	ns
GT1 output fall time	C_{LOAD} = 1 nF, R_{LOAD} = 10 Ω		10	50	ns

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6.6 Typical Characteristics

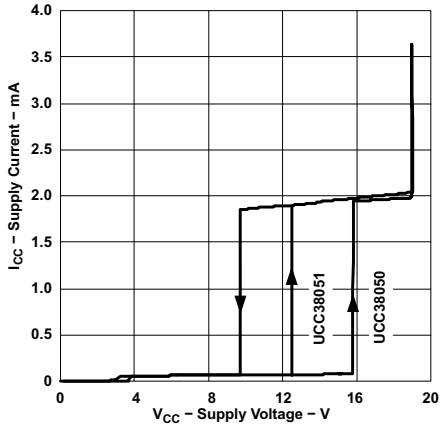

Figure 1. Supply Current vs Supply Voltage

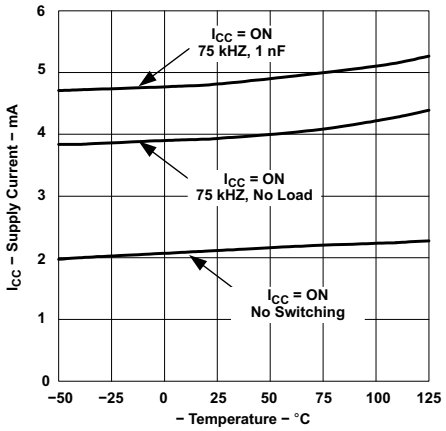

Figure 2. Supply Current vs Temperature

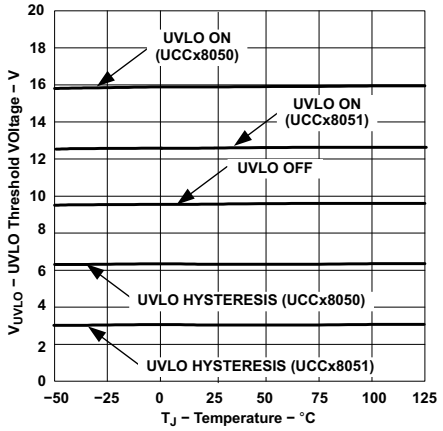

Figure 3. UVLO Thresholds vs Temperature

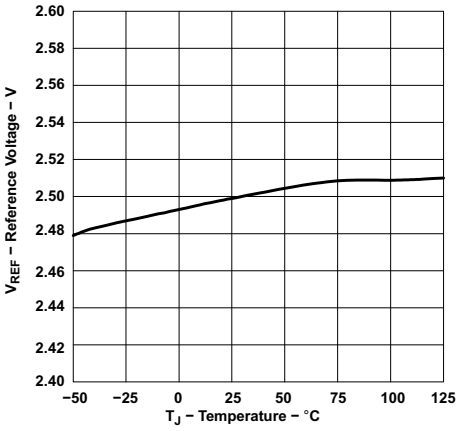

Figure 4. Reference Voltage vs Temperature

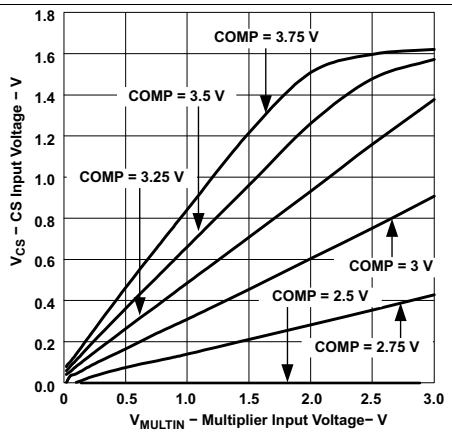

Figure 5. Current Sense Input Threshold vs Multiplier Input Voltage

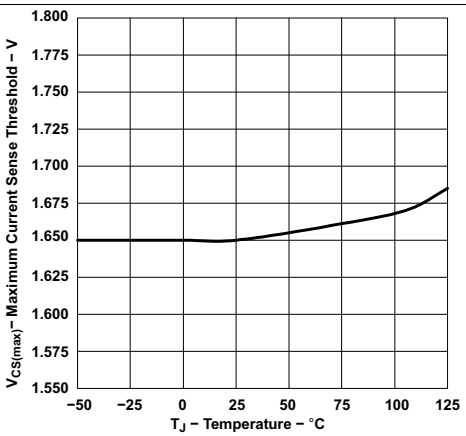

Figure 6. Maximum Current Sense Threshold vs Temperature

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Typical Characteristics (continued)

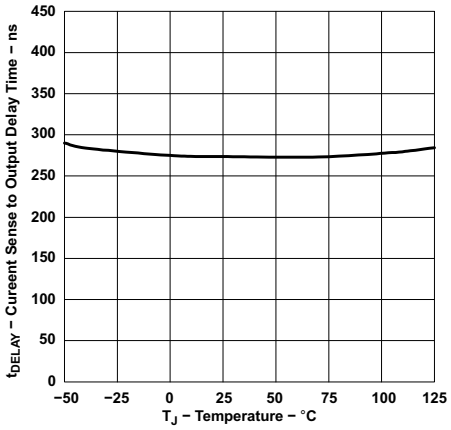

Figure 7. CS To Output Delay Time vs Temperature

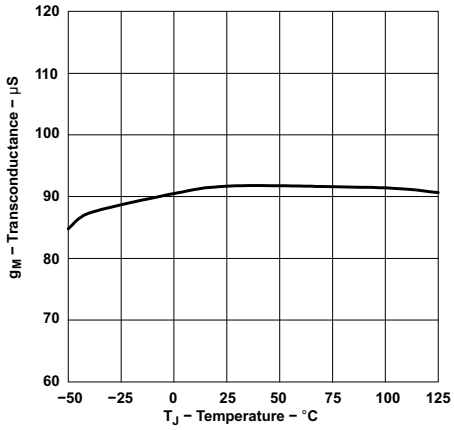

Figure 8. Transconductance vs Temperature

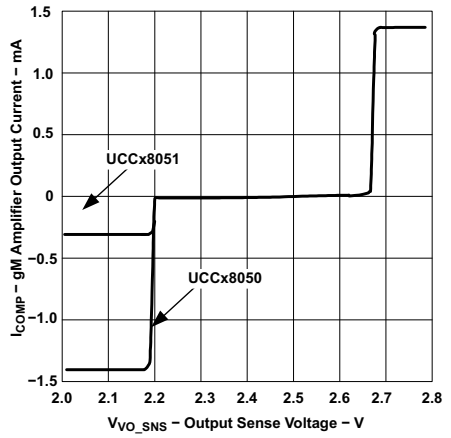

Figure 9. g_M Amplifier Output Current vs Output Sense Voltage

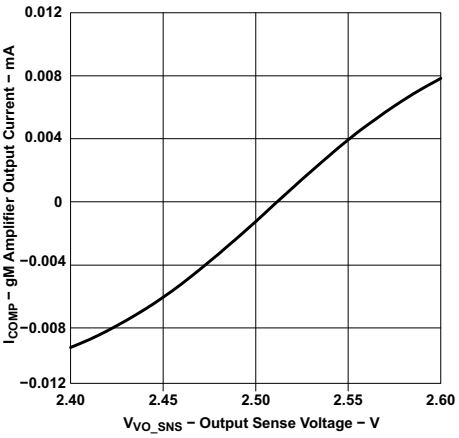

Figure 10. g_M Amplifier Output Current vs Output Sense Voltage (Small Signal View)

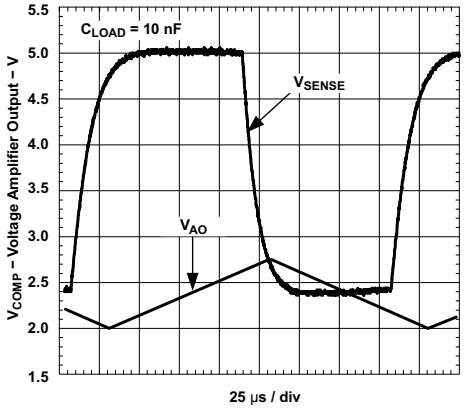

Figure 11. Voltage Amplifier Output vs Time (UCC38050)

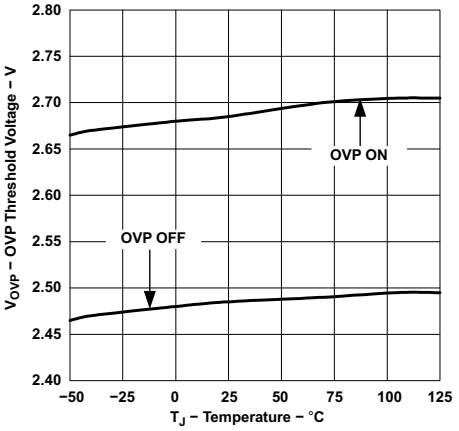

Figure 12. Overvoltage Protection Thresholds vs Temperature

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Typical Characteristics (continued)

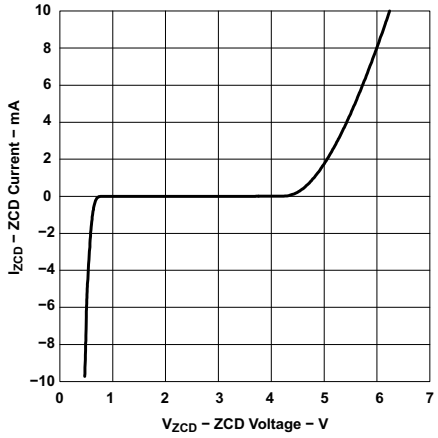

Figure 13. Zero Current Detection Clamp Current vs Voltage

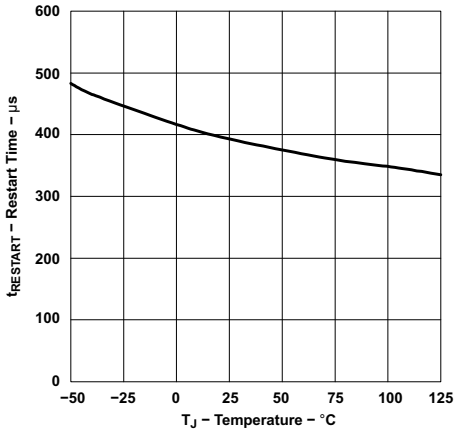

Figure 14. Restart Time vs Temperature

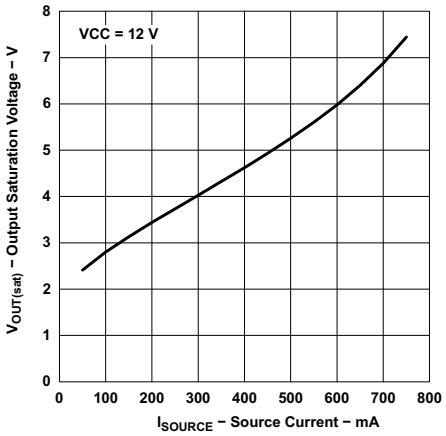

Figure 15. Output Saturation Voltage vs Source Current

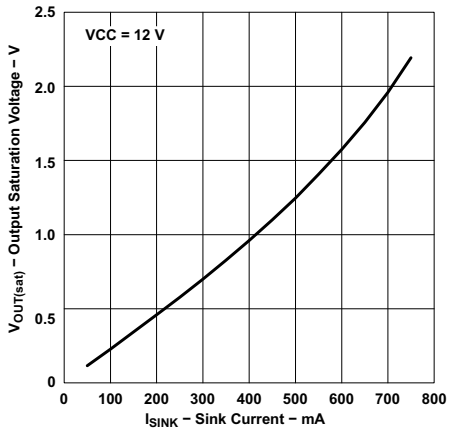

Figure 16. Output Saturation Voltage vs Sink Current

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7 Detailed Description

7.1 Overview

The UCC38050 and UCC38051 are PFC controllers for low-to-medium power applications requiring compliance with IEC 1000-3-2 harmonic reduction. The controller is designed for a boost preregulator operating in transition mode (also referred to as boundary-conduction mode or critical conduction-mode operation). It features a transconductance voltage amplifier for feedback error processing, a simple multiplier for generating a current command proportional to the input voltage, a current-sense (PWM) comparator, PWM logic, and a totem-pole driver for driving an external FET.

The UCC38050 and UCC38051, while being pin-compatible with other industry controllers providing similar functionality, offer many feature enhancements and tighter specifications, leading to an overall reduction in system implementation cost. The system performance is enhanced by incorporation of a zero-power detect function, which allows the controller output to shut down at light load conditions without running into overvoltage. The device also features innovative slew rate enhancement circuits, which improve the large signal transient performance of the voltage error amplifier. The low start-up and operating currents of the device result in low power consumption and ease of start-up. Highly accurate internal bandgap reference leads to tight regulation of output voltage in normal and OVP conditions, resulting in higher system reliability. The enable comparator ensures that the controller is off if the feedback sense path is broken or if the input voltage is very low.

There are two key parameteric differences between UCC38050 and UCC38051. The UVLO turn-on threshold of UCC38050 is 15.8 V, while for UCC38051 it is 12.5 V. Secondly, the gM amplifier source current for UCC38050 is typically 1.3 mA, while for UCC38051 it is 300 µA. The higher UVLO turn-on threshold of the UCC38050 allows quicker and easier start-up with a smaller V_{CC} capacitance, while the lower UVLO turn-on threshold of UCC38051 allows the operation of the PFC chip to be easily controlled by the downsteam PWM controller in two-stage power converters. The UCC38050 gM amplifier also provides a full 1.3-mA typical source current for faster start-up and improved transient response when output is low, either at start-up or during transient conditions. The UCC38051 scales this source current back down to 300-µA typical source current to gradually increase the error voltage, preventing a step increase in line currents at start-up, but still providing good transient response. The UCC38051 is suitable for multiple applications, including AC adapters, where a two-stage power conversion is needed. The UCC38050 is suitable for applications such as electronic ballasts, where there is no down-stream PWM conversion and the advantages of a smaller V_{CC} capacitor and improved transient response can be realized.

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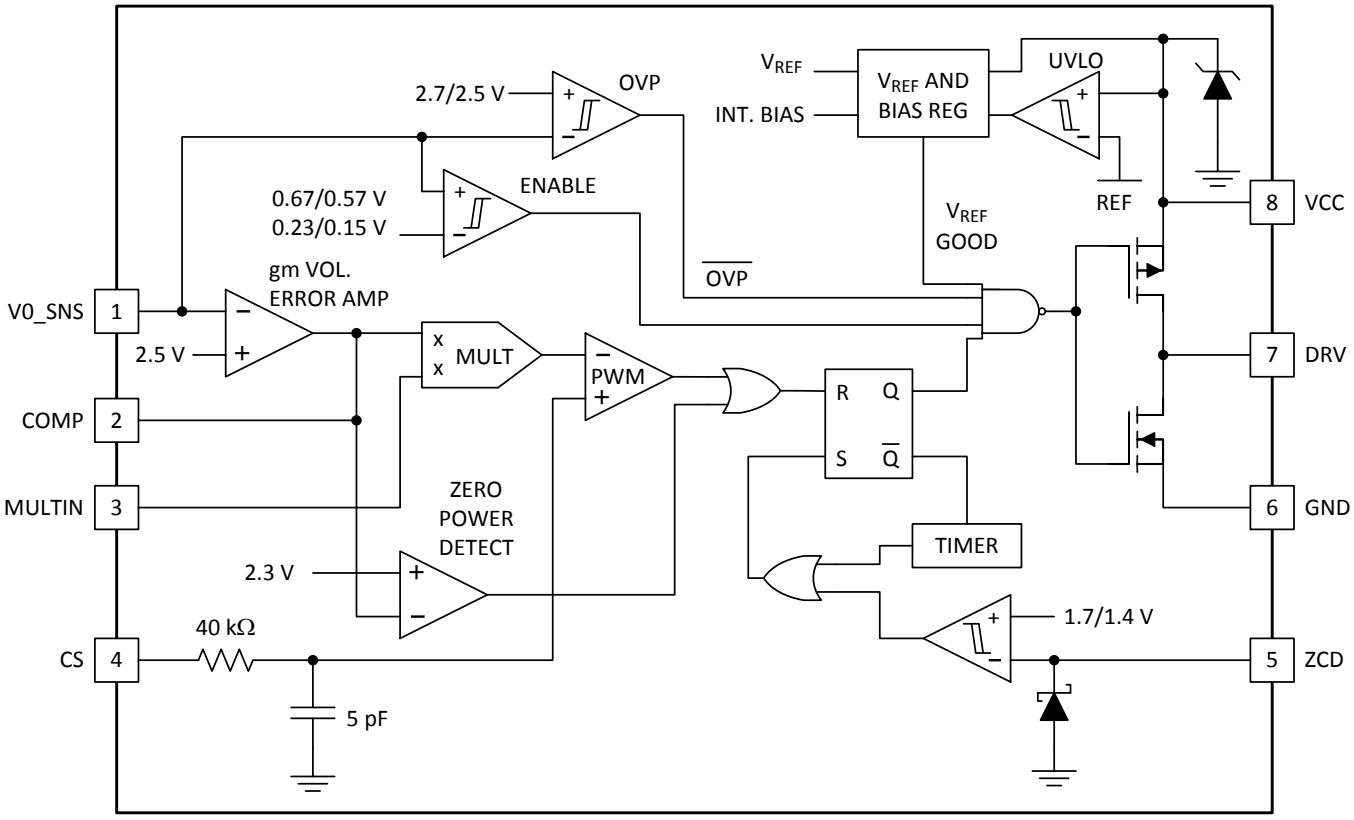
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 UVLO and Reference Block

This block generates a precision reference voltage used to obtain tightly controlled UVLO threshold. In addition to generating a 2.5-V reference for the non-inverting terminal of the gM amplifier, it generates the reference voltages for blocks such as OVP, enable, zero power, and multiplier. An internal rail of 7.5 V is also generated, to drive all the internal blocks.

7.3.2 Error Amplifier

The voltage error amplifier in UCC3805x is a transcoductance amplifier, with a typical transconductance value of 90 µS. A transconductance amplifier is advantageous in that the inverting input of the amplifier is solely determined by the external resistive-divider from the output voltage, and not the transient behavior of the amplifier itself. This allows the VO_SNS pin to be used for sensing overvoltage conditions.

The sink and source capability of the error amplifier is approximately 10 µA during normal operation of the amplifier. However, when the VO_SNS pin voltage is beyond the normal operating conditions (VO_SNS > 1.05 × V_{REF}, VO_SNS < 0.88 × V_{REF}), additional circuitry to enhance the slew-rate of the amplifier is activated. Enhanced slew-rate of the compensation capacitor results in a faster start-up and transient response. This prevents the output voltage from drifting too high or too low, which can happen if the compensation capacitor were to be slewed by the normal slewing current of 10 µA. When VO_SNS rises above the normal range, the enhanced sink current capability is in excess of 1 mA. When VO_SNS falls below the normal range, the UCC38050 can source more than 1 mA, and the UCC38051 sources approximately 300 µA. The limited source current in the UCC38051 helps to gradually increase the error voltage on the COMP pin preventing a step increase in line current. The actual rate of increase of V_{COMP} depends on the compensation network connected to the COMP pin.

7.3.3 Zero Current Detection and Re-Start Timer Blocks

When the boost inductor current becomes zero, the voltage at the power MOSFET drain end falls. This is indirectly sensed with a secondary winding connected to the ZCD pin. The internal active clamp circuitry prevents the voltage from going to a negative or a high positive value. The clamp has the sink and source capability of 10 mA. The resistor value in series with the secondary winding should be chosen to limit the ZCD current to less than 10 mA. The rising edge threshold of the ZCD comparator can be as high as 2 V. The auxiliary winding should be chosen such that the positive voltage (when the power MOSFET is off) at the ZCD pin is in excess of 2 V.

The restart timer attempts to set the gate drive high in case the gate drive remains off for more than 400 µs nominally. The minimum guaranteed time period of the timer is 200 µs. This translates to a minimum switching frequency of 5 kHz. In other words, the boost inductor value should be chosen for switching frequencies greater than 5 kHz.

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Feature Description (continued)

7.3.4 Enable Block

The gate drive signal is held low if the voltage at the VO_SNS pin is less than the ENABLE threshold. This feature can disable the converter by pulling VO_SNS low. If the output feedback path is broken, VO_SNS is pulled to ground, and the output is disabled to protect the power stage.

7.3.5 Zero Power Block

When the output of the g_M amplifier goes below 2.3 V, the zero power comparator latches the gate drive signal low. The slew rate enhancement circuitry of the gM amplifier activated during overvoltage conditions slews the COMP pin to approximately 2.4 V. This ensures that the zero power comparator is not activated during transient behavior, when the slew rate enhancement circuitry is enhanced.

7.3.6 Multiplier Block

The multiplier block has two inputs. One is the error amplifier output voltage (V_{COMP}), and the other is V_{MULTIN}, which is obtained by a resistive divider from the rectified line. The multiplier output is approximately $0.67 \times V_{MULTIN} \times (V_{COMP} - 2.5\ V)$. There is a positive offset of about 75 mV to the V_{MULTIN} signal because this improves the zero-crossing distortion and thus the THD performance of the controller in the application. The dynamic range of the inputs can be found in *Electrical Characteristics*.

7.3.7 Overvoltage Protection (OVP) Block

The OVP feature in the part is not activated under most operating conditions because of the presence of the slew rate enhancement circuitry present in the error amplifier. As soon as the output voltage reaches to approximately 5% to 7% above the nominal value, the slew rate enhancement circuit is activated, and the error amplifier output voltage is pulled below the dynamic range of the multiplier block. This prevents further rise in output voltage.

If the COMP pin is not pulled low fast enough and the voltage rises further, the OVP circuit acts as a second line of protection. When the voltage at the VO_SNS pin is more than 7.5% of the nominal value ($> (V_{REF} + 0.19)$), the OVP feature is activated. It stops the gate drive from switching as long as the voltage at the VO_SNS pin is above the nominal value (V_{REF}). This prevents the output DC voltage from going above 7.5% of the nominal value designed for, and protects the switch and other components of the system such as the boost capacitor.

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7.4 Device Functional Modes

7.4.1 Transition Mode Control

The boost converter, the most common topology used for power factor correction, can operate in two modes: continuous conduction code (CCM) and discontinuous conduction mode (DCM). Transition mode control, also referred to as critical conduction mode (CRM) or boundary conduction mode, maintains the converter at the boundary between CCM and DCM by adjusting the switching frequency.

The CRM converter typically uses a variation of hysteretic control, with the lower boundary equal to zero current. It is a variable frequency control technique that has inherently stable input current control while eliminating reverse recovery rectifier losses. As shown in Figure 17, the switch current is compared to the reference signal (output of the multiplier) directly. This control method has the advantage of simple implementation and good power factor correction.

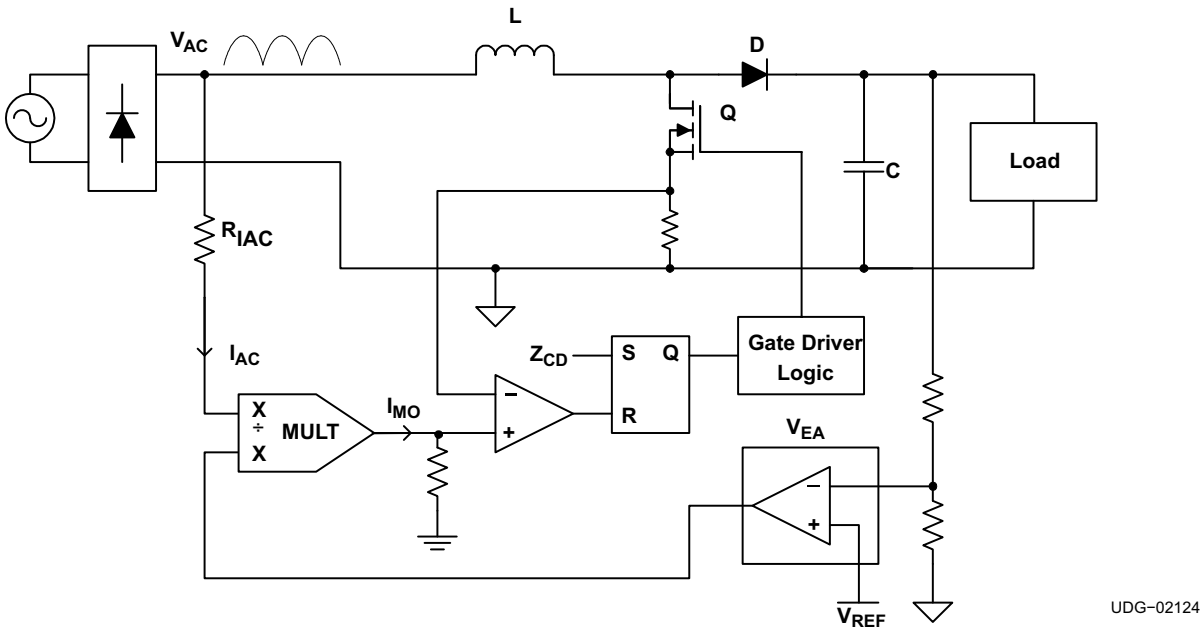

Figure 17. Basic Block Diagram of CRM Boost PFC

The power stage equations and the transfer functions of the CRM are the same as the CCM. However, implementations of the control functions are different. Transition mode forces the inductor current to operate just at the border of CCM and DCM. The current profile is also different, and affects the component power loss and filtering requirements. The peak current in the CRM boost is twice the amplitude of CCM, leading to higher conduction losses. The peak-to-peak ripple is twice the average current, which affects MOSFET switching losses and magnetics ac losses.

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Device Functional Modes (continued)

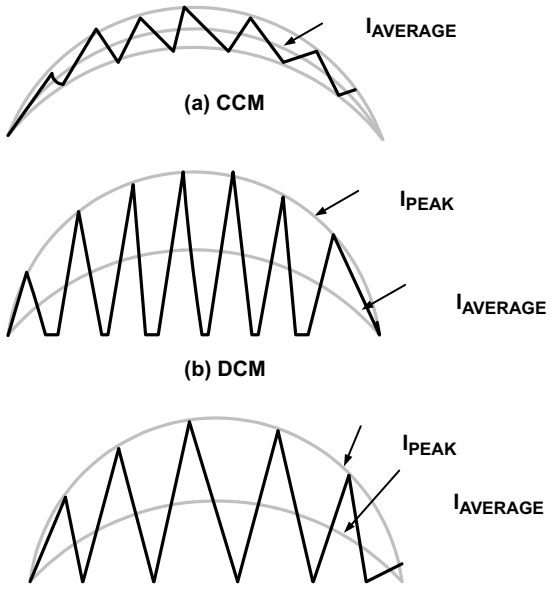

Figure 18. PFC Inductor Current Profiles

For low to medium power applications up to approximately 300 W, the CRM boost has an advantage in losses. The filtering requirement is not severe, and therefore is not a disadvantage. For medium to higher power applications, where the input filter requirements dominate the size of the magnetics, the CCM boost is a good choice due to lower peak currents (which reduces conduction losses) and lower ripple current (which reduces filter requirements). The main tradeoff in using CRM boost is lower losses due to no reverse recovery in the boost diode vs. higher ripple and peak currents.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC38050 and UCC38051 are switch-mode controllers used in boost converters for power factor correction operating in transition mode. In the transition mode operation, the PWM circuit is self-oscillating, with the turnon being governed by an inductor zero-current detector (ZCD pin), and the turnoff being governed by the current-sense comparator. Additionally, the controller provides features such as peak current limit, default timer, OVP, and enable.

There are two key parametric differences between UCC38050 and UCC38051. The UVLO turnon threshold of UCC38050 is 15.8 V, while for UCC38051 it is 12.5 V. Secondly, the gM amplifier source current for UCC38050 is typically 1.3 mA, while for UCC38051 it is 300 µA. The UCC38051 is suitable for multiple applications, including AC adapters, where a two-stage power conversion is needed. The UCC38050 is suitable for applications such as electronic ballasts, where there is no down-stream PWM conversion and the advantages of a smaller VCC capacitor and improved transient response can be realized. Figure 19 is an example of a critical conduction mode power factor correction boost converter utilizing the UCC38050.

8.2 Typical Application

The UCC38050 is used for the off-line power factor corrected pre-regulator with operation over a universal input range of 85 V to 265 V with a 400-V_{DC} regulated output. The schematic is shown in Figure 19, and the board layout for the reference design is shown in Figure 24.

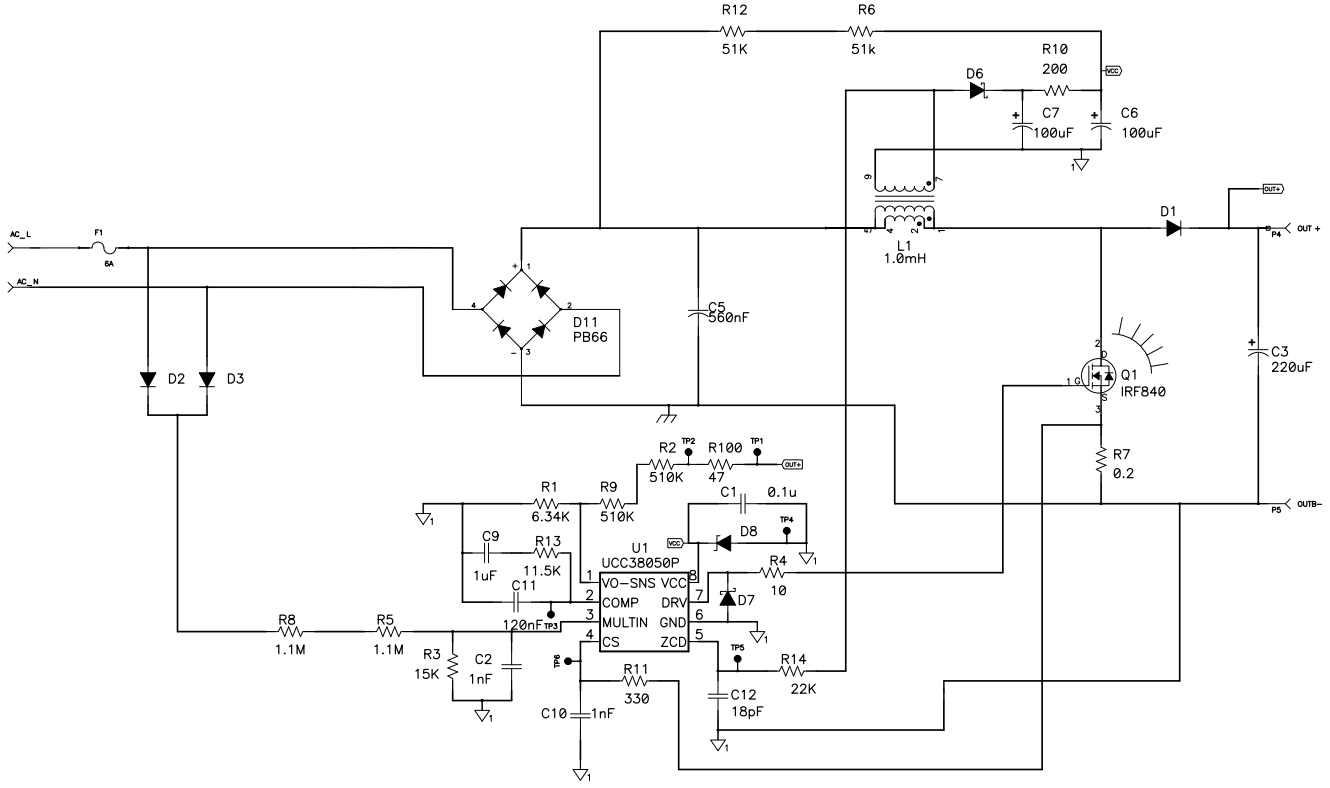

Figure 19. Universal Line Input 100-W Boost Converter

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Typical Application (continued)

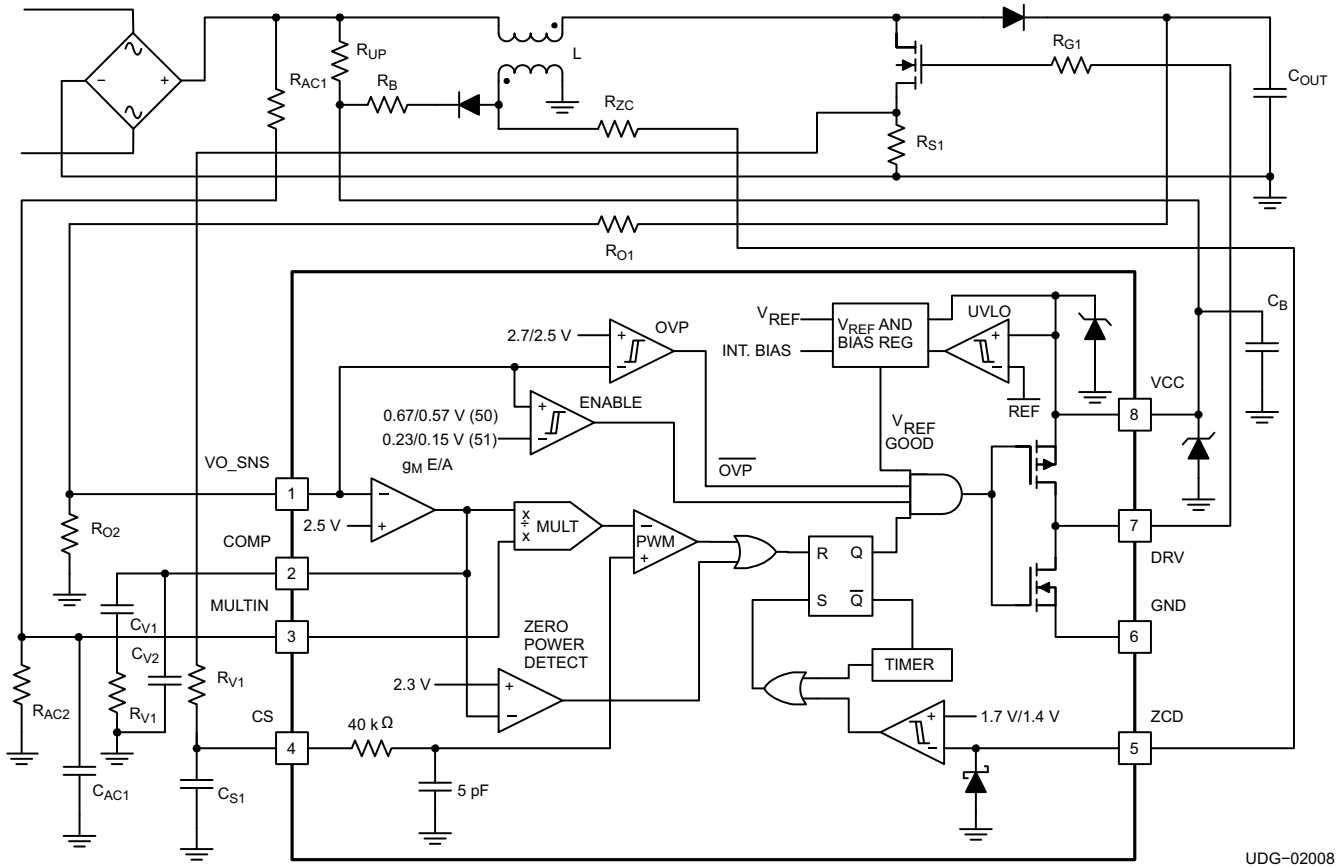

Figure 20. Typical Application Diagram

8.2.1 Design Requirements

Table 1 shows the design requirements for a CCM, PFC boost converter utilizing the UCC38050.

Table 1. UCC38050 Design Requirements

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		85		265	V_{RMS}
	Input frequency			60		Hz
V_{OUT}	Output voltage DC	V_{IN} = 85 V_{RMS}	370	400	425	V
V_{OUT}	Output voltage DC	V_{IN} = 265 V_{RMS}	370	390	410	V
P_{OUT}	Output power		0		100	W
	Output voltage ripple	V_{IN} = 85 V_{RMS}			3%	
	Efficiency	P_{OUT} = 100 W	90%			
	Total harmonic distortion (THD)	V_{IN} = 85 V_{RMS}, P_{OUT} = 100 W		5%		
	Total harmonic distortion (THD)	V_{IN} = 265 V_{RMS}, P_{OUT} = 100 W		15%		
	Hold-up time		16.7			ms

8.2.2 Detailed Design Procedure

For a selected V_{OUT} and minimum switching frequency, the following equations outline the design guidelines for power stage component selection, using a universal input, 100-W PFC converter with an output voltage of 390 V. Refer to Figure 20 for reference designators.

8.2.2.1 Inductor Selection

In the transition mode control, the inductor value must be calculated to start the next switching cycle at zero current. The time it takes to reach zero depends on line voltage and inductance and as shown in Equation 2. L determines the frequency range of the converter.

$$L = \frac{\left(V_{AC(min)}\right)^2 \times \left(V_{OUT} - \sqrt{2} \times V_{AC(min)}\right)}{2 \times F_{s(min)} \times V_{OUT} \times P_{IN}}$$

where

- V_{AC} = RMS line voltage
- $V_{AC(min)}$ = minimum AC line voltage
- P_{IN} = maximum input power averaged over the ac line period

(2)

$$I_{L(peak)} = 2 \times \sqrt{2} \times (P_{IN}/V_{AC(min)}) \quad (3)$$

$$I_{L(rms)} = I_{L(peak)} / \sqrt{6} \quad (4)$$

8.2.2.2 MOSFET Selection

The main switch selection is driven by the amount of power dissipation allowable. Choose a device that minimizes gate charge and capacitance, and minimizes the sum of switching and conduction losses at a given frequency.

$$I_{Q(rms_crm)} = \sqrt{\frac{1}{6} - \left(4 \times \sqrt{2}\right) \times \left(\frac{V_{AC(min)}}{9\pi \times V_{OUT}}\right)} \times IL_{PEAK(crm)} \quad (5)$$

$$V_{Q(max)} = V_{OUT} \quad (6)$$

8.2.2.3 Diode Selection

The effects of the reverse recovery current in the diode can be eliminated with relatively little negative impact to the system. The diode selection is based on reverse voltage, forward current, and switching speed.

$$I_{D(avg)} = I_{OUT(avg)} \quad (7)$$

$$I_{D(rms)} = I_{L(peak)} \sqrt{\frac{\sqrt{2} \times V_{AC}}{\pi \times V_{OUT}}} \quad (8)$$

$$V_{D(peak)} = V_{OUT} \quad (9)$$

8.2.2.4 Capacitor Selection

The hold-up time is the main requirement in determining the output capacitance. ESR and the maximum RMS ripple current rating can also be important, especially at higher power levels.

$$C_{OUT(min)} = (2 \times P_{OUT} \times t_{HOLDUP}) / ((V_{OUT})^2 - (V_{OUT(min)})^2)$$

where

- $V_{OUT(min)}$ = minimum regulator input voltage for operation

(10)

$$I_{C(rms)} = \sqrt{\left(I_{L(peak)}\right)^2 \times \frac{\sqrt{2} \times V_{AC(max)}}{\pi \times V_{OUT}} - \left(\frac{P_{OUT}}{V_{OUT}}\right)^2 + (\text{ac rms load currents})^2} \quad (11)$$

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8.2.2.5 Multiplier Set-Up

Select R_{AC1} and R_{AC2} so that their ratio uses the full dynamic range of the multiplier input at the peak line voltage, and yet with values small enough to negate the effects of the multiplier bias current. To use the maximum range of the multiplier, select the divider ratio so that V_{MULTIN}, evaluated at the peak of the maximum ac line voltage, is the maximum of the minimum dynamic input range of MULTIN, which is 2.5 V. Choose R_{AC1} so that it has at least 100 µA at the peak of the minimum AC operating line voltage.

$$\frac{R_{AC1}}{R_{AC2}} = \left(\frac{\sqrt{2}}{2.5} V_{AC(max)}\right) - 1 \quad (12)$$

In extreme cases, switching transients can contaminate the MULTIN signal, so it can be beneficial to add capacitor C_{AC1}. Select the value of C_{AC1} so that the corner frequency of the resulting filter is greater than the lowest switching frequency. The low corner frequency of this filter may compromise the overall power factor.

8.2.2.6 Sense Resistor Selection

The current sense resistor value must be chosen to limit the output power, and it must also use the full dynamic range of the multiplier during normal steady state operation. The value of R_{S1} is thus selected for maximum power operation at low ac line voltage conditions. To use the full dynamic range, set the V_{SENSE} threshold as a function of the dynamic input range of V_{COMP} and the peak of the minimum MULTIN voltage.

$$R_{S1} = \frac{0.67 \times \left(COMP_{(MAX)} - COMP_{(MIN)}\right) \times \left(MULTIN_{(PEAK)@VAC(min)} - 0.075\right)}{2 \times \sqrt{2} \times \frac{P_{IN(max)}}{V_{AC(min)}}}$$

where

- $COMP_{(MAX)}$ = 3.8 V
- $COMP_{(MIN)}$ = 2.5 V
- $MULTIN_{(PEAK)@VAC(min)} = \sqrt{2} \times V_{AC(min)}(R_{AC2} / (R_{AC2}+R_{AC1}))$ (13)

If the exact value R_{S1} is not available, R_{S2} and R_{S3} can be added for further scaling. The CS pin already has an internal filter for noise due to switching transients. Additional filtering at switching transient frequencies can be achieved by adding CS1.

8.2.2.7 Output Voltage Sense Design

Select the divider ratio of R_{O1} and R_{O2} to set the VO_SNS voltage to 2.5 V at the desired output voltage. The current through the divider should be at least 200 µA.

8.2.2.8 Voltage Loop Design

How well the voltage control loop is designed directly impacts line current distortion. UCC38050 employs a transconductance amplifier (g_M amp) with gain scheduling for improved transient response (refer to Figure 9). Integral type control at low frequencies is preferred, because the loop gain varies considerably with line conditions. The largest gain occurs at maximum line voltage. If the power factor corrector load is dc-to-dc switching converter, the small signal model of the controller and the power factor corrector, from COMP to PFC output voltage is given by:

$$\frac{\hat{V}_{OUT}(s)}{\hat{V}_{COMP}(s)} = \frac{k_1 \times \left(V_{AC}\right)^2}{V_{OUT(avg)} \times R_{S1} \times k_{CRM} \times C_{OUT}} \times \frac{1}{S}$$

where

- $\hat{V}_{OUT}$ = small signal variations in V_{OUT}
- $\hat{V}_{COMP}$ = small signal variations in V_{COMP}
- k_1 = multiplier gain = 0.65
- k_{CRM} = peak to average factor = 2 (14)

A controller that has integral control at low frequencies requires a zero near the crossover frequency to be stable. The resulting gM amplifier configuration is shown in Figure 21.

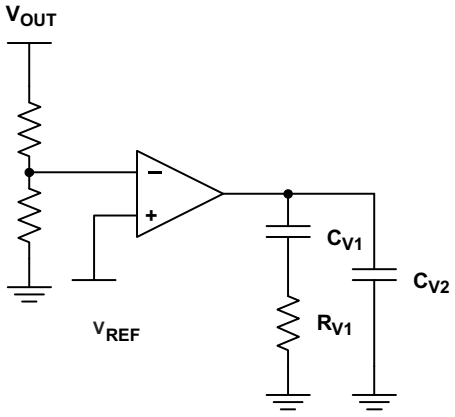

Figure 21. gM Amplifier Configuration

The compensator transfer function is:

$$A_V = \frac{gM}{C_{V1} + C_{V2}} \times \frac{1 + \left(R_{V1} \times C_{V1} \times s\right)}{s\left(1 + \left(R_{V1} \times \frac{\left[C_{V1} \times C_{V2}\right]}{\left[C_{V1} \times C_{V2}\right]}\right) \times s\right)}$$

where

- gM = DC transconductance gain = 100 µs (15)

The limiting factor of the gain is usually the allowable third harmonic distortion, although other harmonics can dominate. The crossover frequency of the control loop will be much lower than twice the AC line voltage. To choose the compensator dynamics, determine the maximum allowable loop gain at twice the line frequency, and solve for capacitor C_{V2}. This also determines the crossover frequency.

$$C_{V2} = \left(\frac{V_{AC(max)}}{4\pi f_{AC}}\right) 2 \times \left(\frac{gM \times k_1}{V_{OUT(avg)} \times R_{S1} \times k_{(crm)} \times C_{OUT(\text{max loop gain at } 2f_{AC})}}\right) \quad (16)$$

$$f_{CO} = \frac{V_{AC}}{\pi} \sqrt{\frac{gM \times k_1}{C_{V2} \times V_{OUT} \times R_{S1} \times k_{(cmr)} \times C_{OUT}}} \quad (17)$$

Select C_{V1} so that the low frequency zero is one-tenth of the crossover frequency.

$$C_{V1} = 9\ C_{V2} \quad (18)$$

Select R_{V1} so that the pole is at the crossover frequency.

$$\approx 1 / 2\pi\ f_{CO}\ C_{V2} \quad (19)$$

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8.2.3 Application Curves

Figure 22 and Figure 23 show the input current and rectified line for the power module.

- Channel 3 = Rectified Line Voltage
- Channel 4 = Power Module Input Current

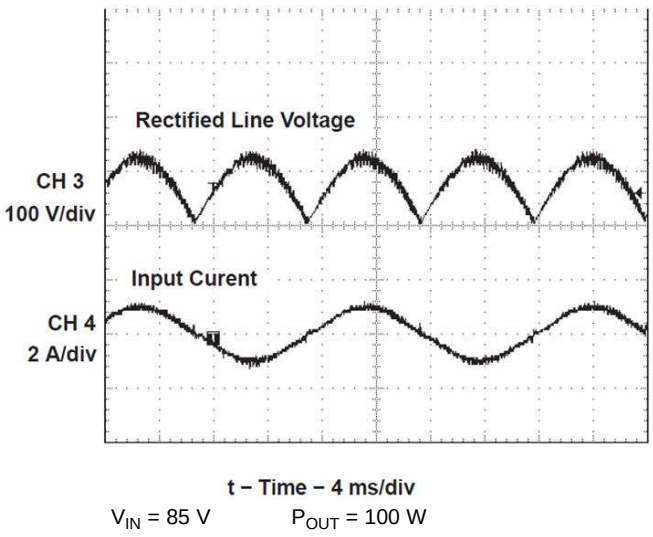

Figure 22. Rectified Line Voltage and Power Module Input Current at 85 V/100 W

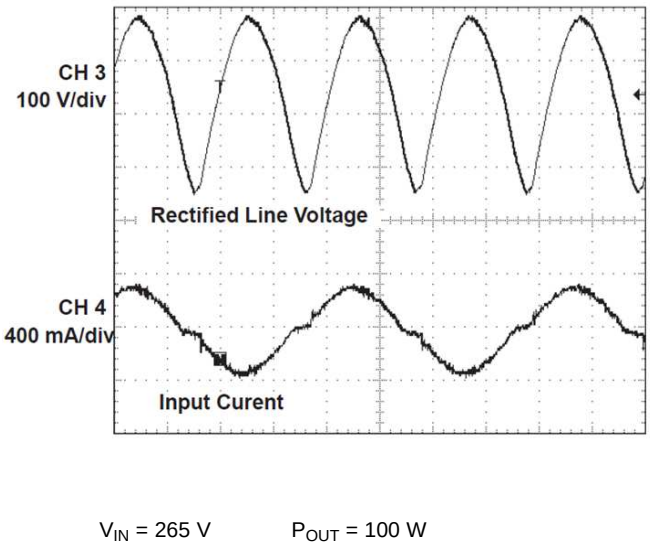

Figure 23. Rectified Line Voltage and Power Module Input Current at 265 V/100 W

9 Power Supply Recommendations

The supply voltage for the device comes from VCC pin. This pin must be bypassed with a high-frequency capacitor (greater than 0.1 µF) and tied to GND. The UCC38050 has a wide UVLO hysteresis of approximately 6.3 V that allows use of a lower value supply capacitor on this pin for quicker and easier start-up. The UCC38051 has a narrow UVLO hysteresis with of about 2.8 V, and a start-up voltage of about 12.5 V for applications where the operation of the PFC device must be controlled by a downstream PWM controller.

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10 Layout

10.1 Layout Guidelines

10.1.1 Bias Current

The bias voltage is supplied by a bias winding on the inductor. Select the turns ratio so that sufficient bias voltage can be achieved at low AC line voltage. The bias capacitor must be large enough to maintain sufficient voltage with AC line variations. Connect a 0.1-µF bypass capacitor between the VCC pin and the GND pin as close to the integrated circuit as possible. For wide line variations, a resistor, R_B, is necessary to permit clamping action. The bias voltage should also be clamped with an external zener diode to a maximum of 18 V.

10.1.2 Zero Current Detection

The zero current detection activates when the ZCD voltage falls below 1.4 V. The bias winding can provide the necessary voltage. This pin has a clamp at approximately 5 V. Add a current limiting resistor, R_{ZC}, to keep the maximum current below 1 mA.

10.2 Layout Example

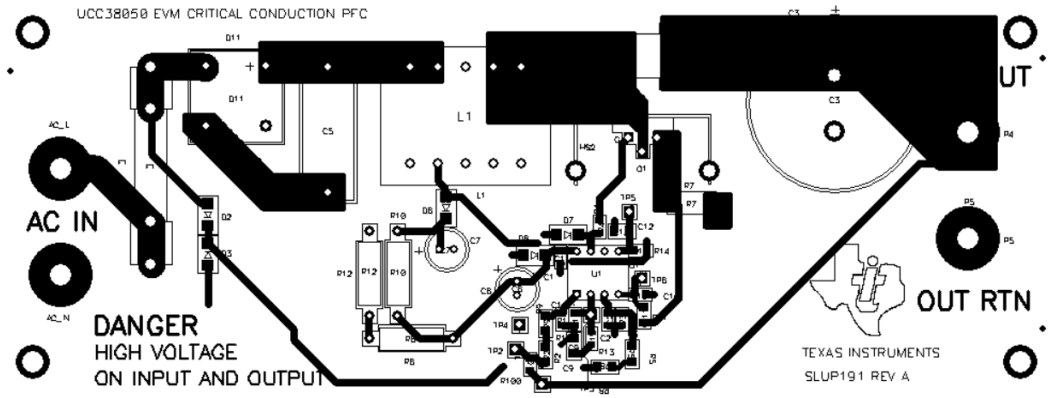

Figure 24. UCC38050 Layout Example

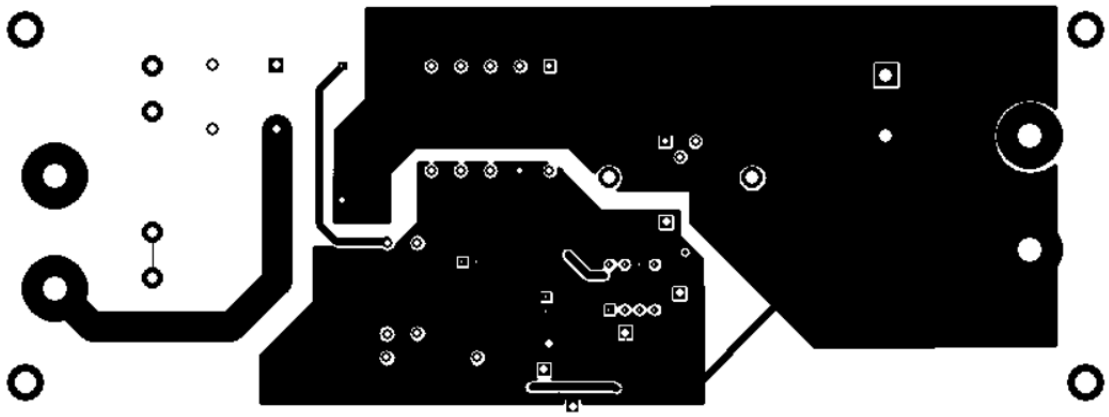

Figure 25. UCC38050 Bottom-Layer Layout Example

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

Reference Design, *100-W Universal Line Input PFC Boost Converter Using the UCC38050* (SLUU134)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC28050	Click here	Click here	Click here	Click here	Click here
UCC28051	Click here	Click here	Click here	Click here	Click here
UCC38050	Click here	Click here	Click here	Click here	Click here
UCC38051	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28050D	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28050
UCC28050D.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28050
UCC28050DR	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28050
UCC28050DR.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28050
UCC28050P	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	28050
UCC28050P.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	28050
UCC28051D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28051
UCC28051D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28051
UCC28051DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28051
UCC28051DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28051
UCC28051DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28051
UCC28051DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	28051
UCC28051P	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	28051
UCC28051P.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	28051
UCC38050D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	38050
UCC38050D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	38050
UCC38050P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	38050
UCC38050P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	38050
UCC38051D	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	38051
UCC38051D.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	38051

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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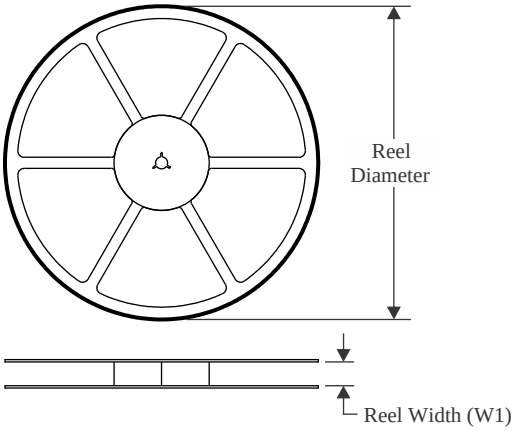
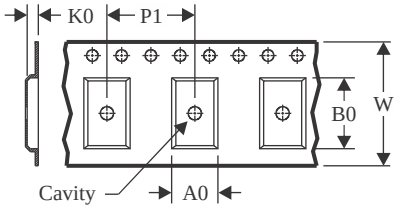
TAPE AND REEL INFORMATION

REEL DIMENSIONS

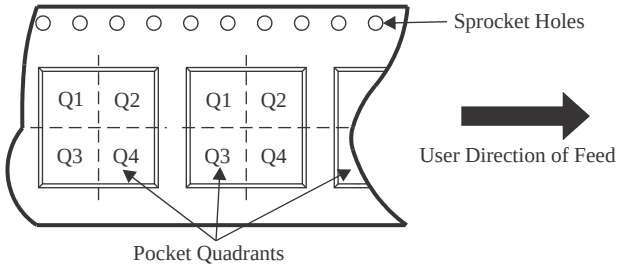


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

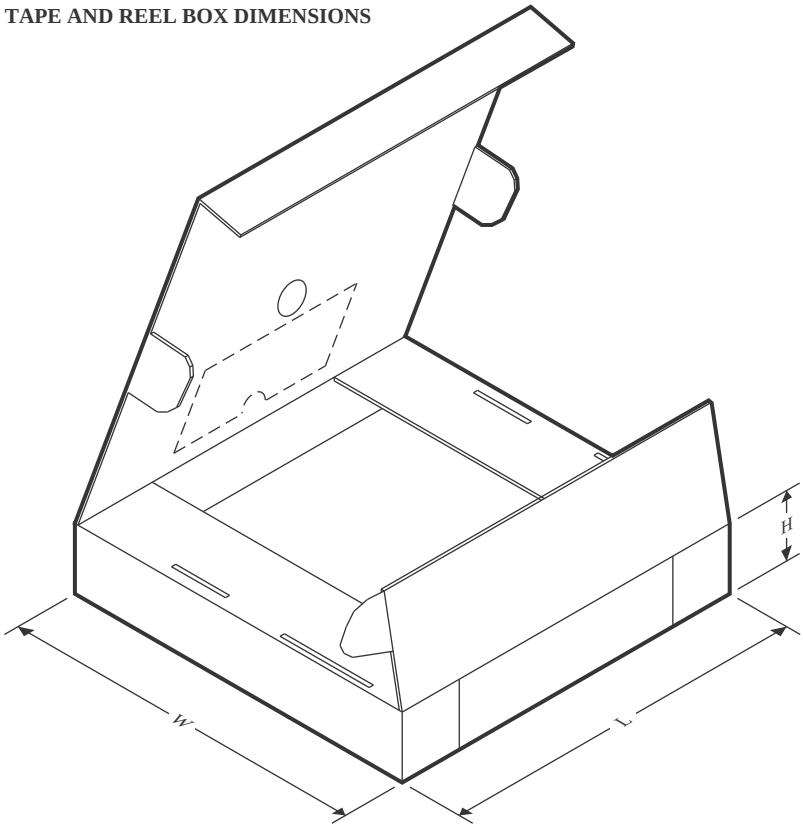
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28050DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28051DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

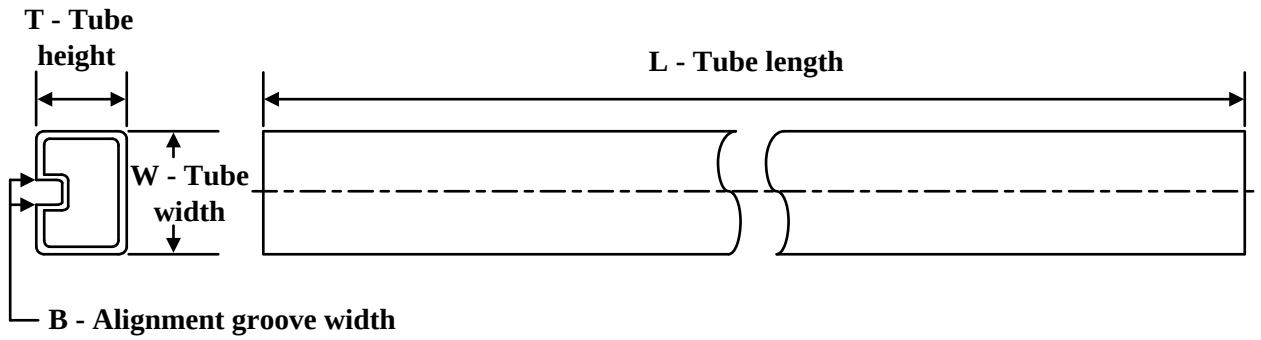
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

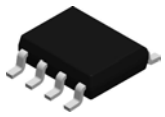
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28050DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28051DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC28050D	D	SOIC	8	75	507	8	3940	4.32
UCC28050D.A	D	SOIC	8	75	507	8	3940	4.32
UCC28050P	P	PDIP	8	50	506	13.97	11230	4.32
UCC28050P.A	P	PDIP	8	50	506	13.97	11230	4.32
UCC28051D	D	SOIC	8	75	507	8	3940	4.32
UCC28051D.A	D	SOIC	8	75	507	8	3940	4.32
UCC28051DG4	D	SOIC	8	75	507	8	3940	4.32
UCC28051P	P	PDIP	8	50	506	13.97	11230	4.32
UCC28051P.A	P	PDIP	8	50	506	13.97	11230	4.32
UCC38050D	D	SOIC	8	75	507	8	3940	4.32
UCC38050D.A	D	SOIC	8	75	507	8	3940	4.32
UCC38050P	P	PDIP	8	50	506	13.97	11230	4.32
UCC38050P.A	P	PDIP	8	50	506	13.97	11230	4.32
UCC38051D	D	SOIC	8	75	507	8	3940	4.32
UCC38051D.A	D	SOIC	8	75	507	8	3940	4.32

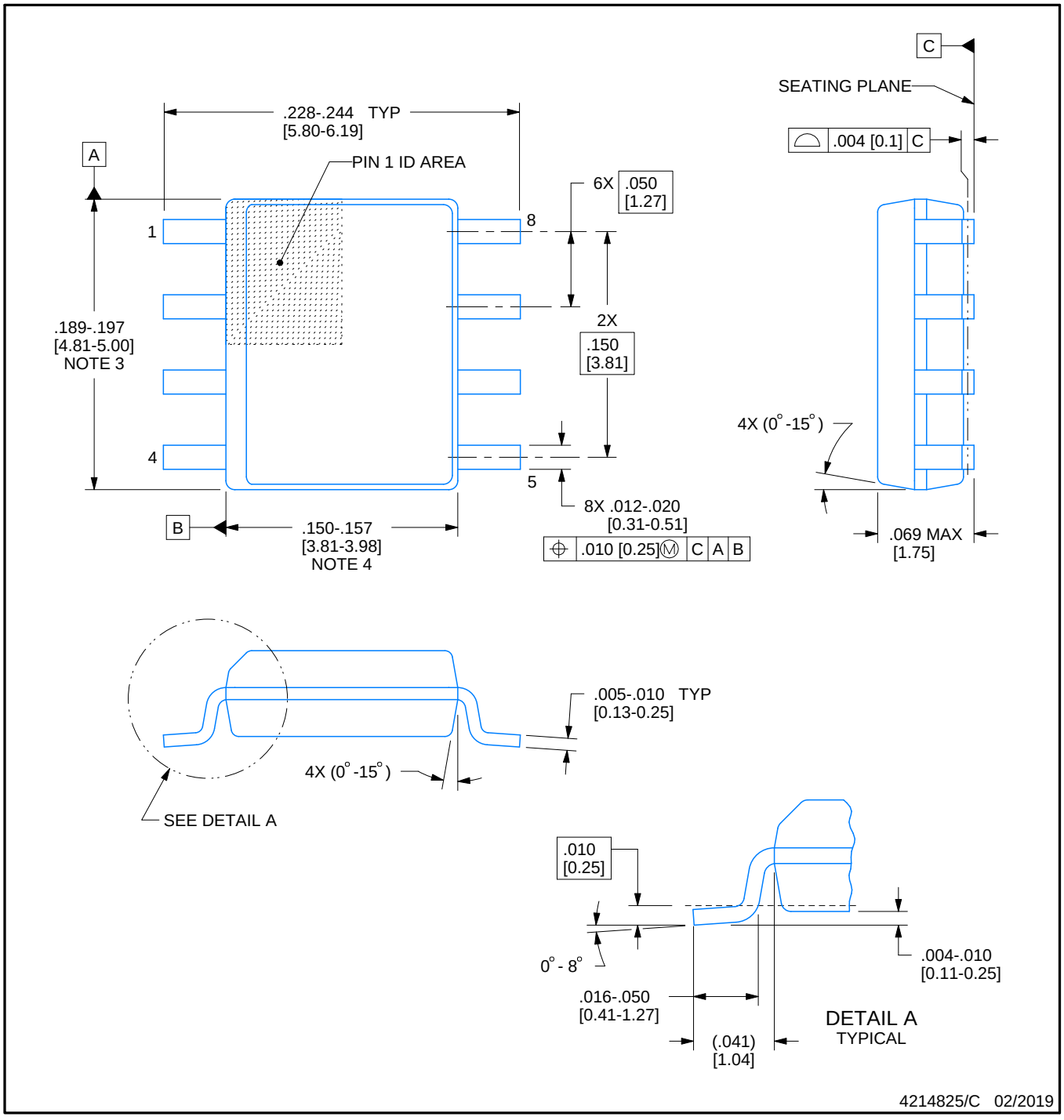


PACKAGE OUTLINE

D0008A

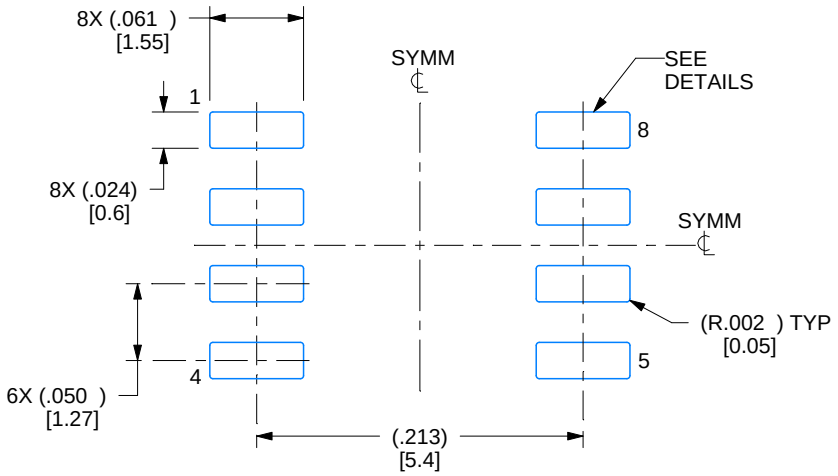
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

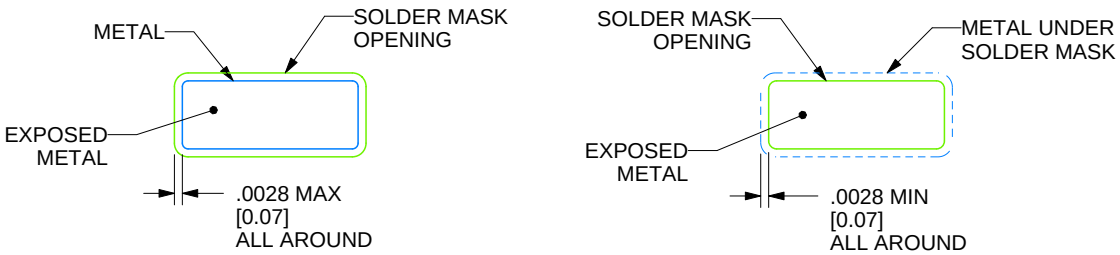


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

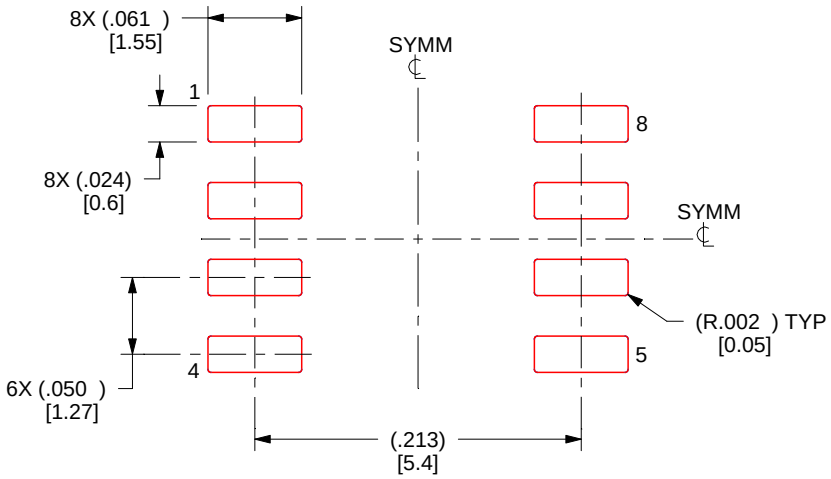
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



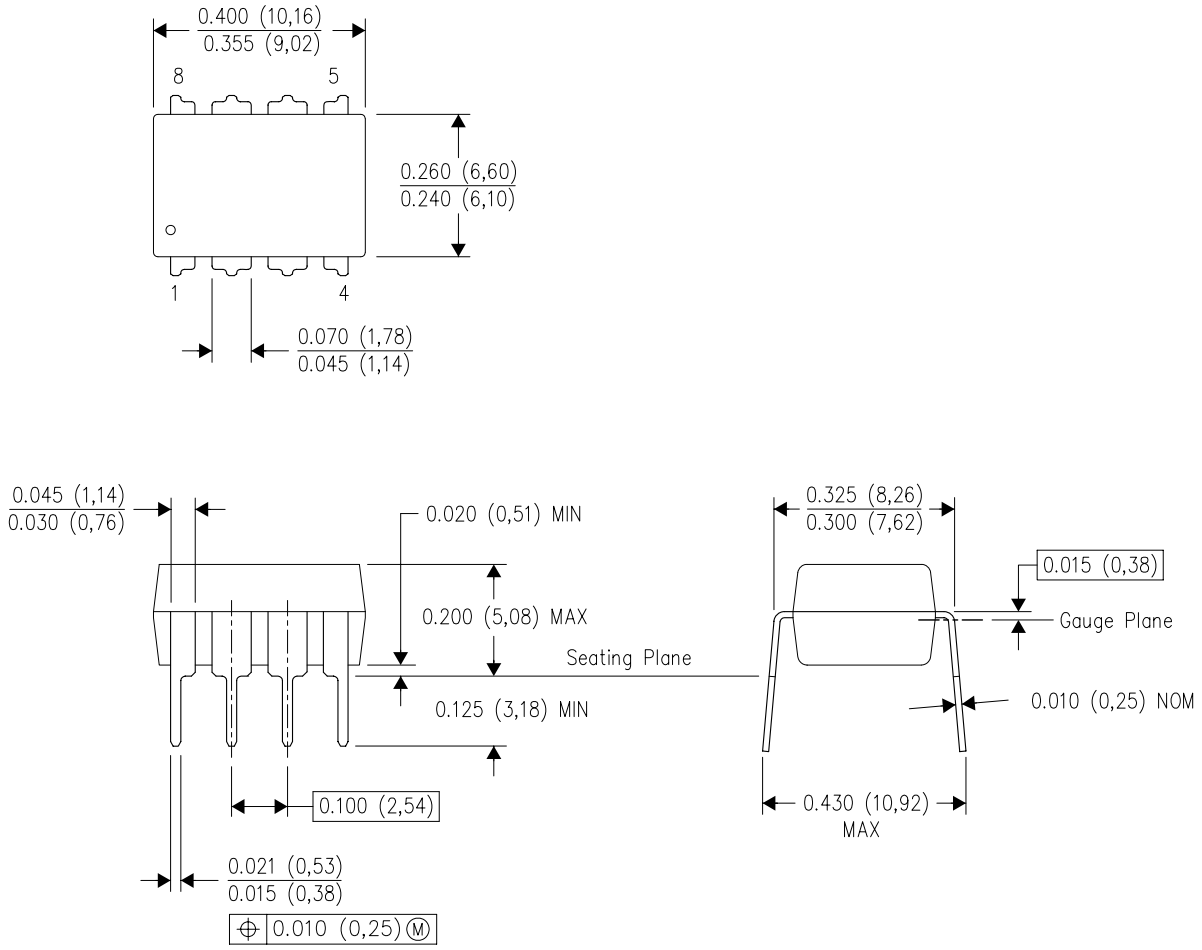
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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