

Programmable, Off-Line, PWM Controller

FEATURES

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-Current Off Line Start Circuit
- Voltage Feed Forward or Current Mode Control
- High Current Totem Pole Output
- 50% Absolute Max Duty Cycle
- PWM Latch for Single Pulse Per Period
- Pulse-by-Pulse Current Limiting plus Shutdown for Over-Current Fault
- No Start-Up or Shutdown Transients
- Slow Turn-On Both Initially and After Fault Shutdown
- Shutdown Upon Over or Under Voltage Sensing
- Latch Off or Continuous Retry After Fault
- 1% Reference Accuracy
- 500kHz Operation
- 18 Pin DIL or 20 Pin PLCC Package

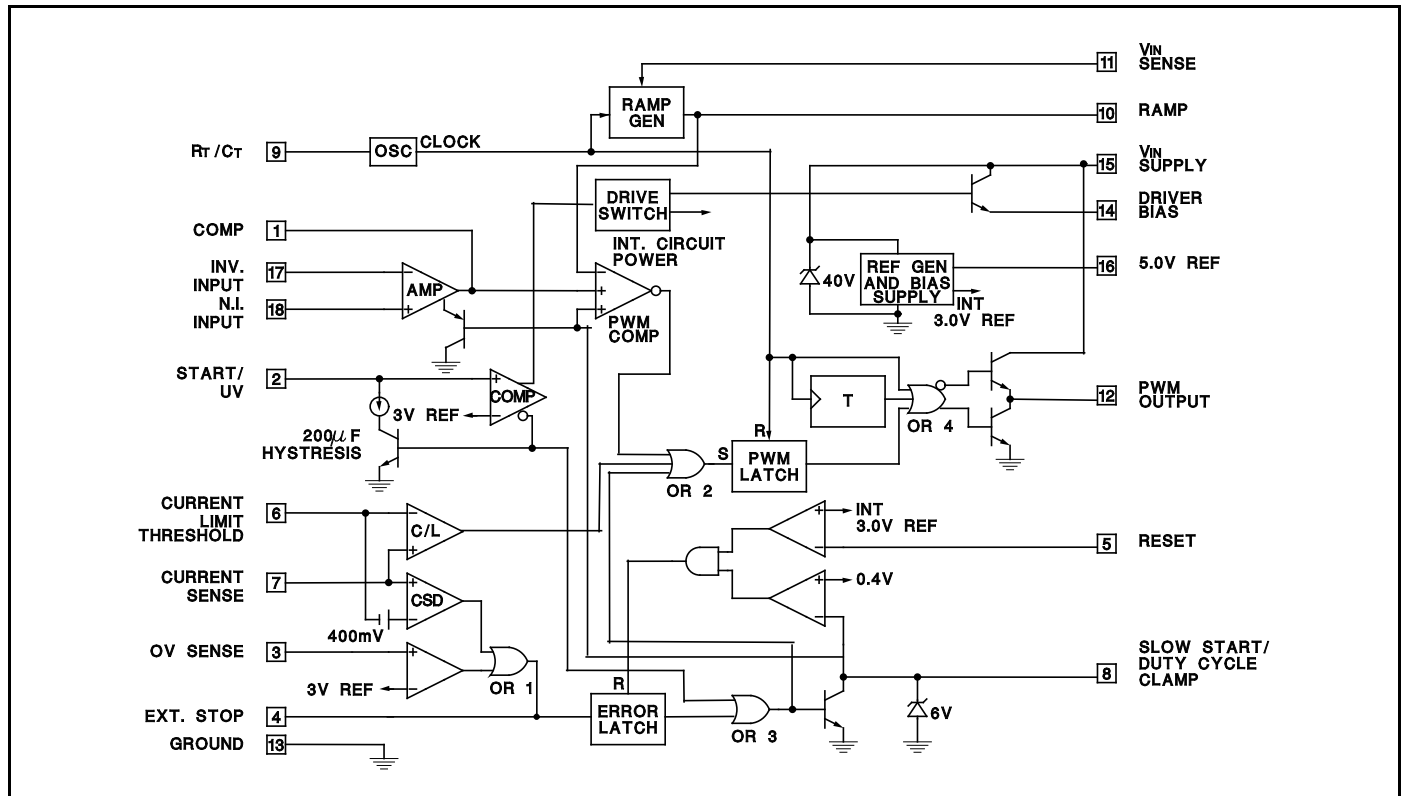
DESCRIPTION

The UC1851 family of PWM controllers are optimized for off-line primary side control. These devices include a high current totem pole output stage and a toggle flip-flop for absolute 50% duty cycle limiting. In all other respects this line of controllers is pin for pin compatible with the UC1841 series. Inclusion of all major housekeeping functions in these high performance controllers makes them ideal for use in cost sensitive applications.

Important features of these controllers include low current start-up, linear feed-forward for constant volt-second operation, and compatibility with both voltage or current mode control. In addition, these devices include a programmable start threshold, as well as programmable over-voltage, under-voltage, and over current fault thresholds. The fault latch on these devices can be configured for automatic restart, or latched off response to a fault.

These devices are packaged in 18-pin plastic or ceramic dual-in-line packages, or for surface mount applications, a 20 Pin PLCC. The UC1851 is characterized for -55°C to +125°C operation while the UC2851 and UC3851 are designed for -40°C to +85°C and 0°C to +70°C, respectively.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, +V_{IN} (Pin 15)

Voltage Driven	+32V
Current Driven, 100mA maximum	Self-limiting
PWM Output Voltage (Pin 12)	40V
PWM Output Current, Steady-State (Pin 12)	400mA
PWM Output Peak Energy Discharge	20μJoules
Driver Bias Current (Pin 14)	-200mA
Reference Output Current (Pin 16)	-50mA
Slow-Start Sink Current (Pin 8)	20mA
V _{IN} Sense Current (Pin 11)	10mA
Current Limit Inputs (Pins 6 & 7)	-0.5 to +5.5V
Stop Input (Pin 4)	-0.3 to +5.5V

Comparator Inputs

(Pins 1–7, 9–11, 16)	Internally clamped at 12V
Power Dissipation at T _A = 25°C (Note 3)	1000mW
Power Dissipation at T _C = 25°C (Note 3)	2000mW
Operating Junction Temperature	-55°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Note 1: All voltages are with respect to ground, Pin 13.

Currents are positive-into, negative-out of the specified terminal

Note 2: All pin numbers are referenced to DIL-18 package.

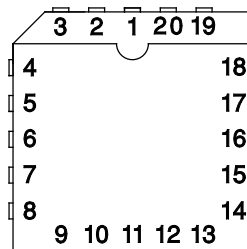
Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW) J or N, DW Package

COMP	1	18	N.I. INPUT
START/UV	2	17	INV. INPUT
OV SENSE	3	16	5.0V REF
STOP	4	15	+V _{IN} SUPPLY
RESET	5	14	DRIVE BIAS
CUR THRESH	6	13	GROUND
CUR SENSE	7	12	PWM OUT
SLOW START	8	11	V _{IN} SENSE
R _T /C _T	9	10	RAMP

PLCC-20, LCC-20 (TOP VIEW) Q, L PACKAGE



PACKAGE PIN FUNCTIONS

FUNCTION	PIN
COMP	1
START/UV	2
OV SENSE	3
STOP	4
RESET	5
CUR THRESH	7
CUR SENSE	8
SLOW START	9
R _T /C _T	10
RAMP	11
V _{IN} SENSE	12
PWM OUT	13
GROUND	14
DRIVE BIAS	15
+V _{IN} SUPPLY	17
5.0V REF	18
INV. INPUT	19
N.I. INPUT	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1851, -40°C to +85°C for the UC2851, and 0°C to 70°C for the UC3851; V_{IN} = 20V, R_T = 20kΩ, C_T = .001 mfd, R_R = 10kΩ, C_R = .001mfd. Current Limit Threshold = 200mV, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1851 / UC2851			UC3851			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Inputs								
Start-Up Current	V _{IN} = 30V, Pin 2 = 2.5V		4.5	6		4.5	6	mA
Operating Current	V _{IN} = 30V, Pin 2 = 3.5V		15	21		15	21	mA
Supply OV Clamp	V _{IN} = 20mA	33	39	45	33	39	45	V
Reference Section								
Reference Voltage	T _J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V _{IN} = 8 to 30V		10	15		10	20	mV
Load Regulation	I _L = 0 to 10mA		10	20		10	30	mV
Total Ref Variation	Over Operating Temperature Range	4.9		5.1	4.85		5.15	V
Short Circuit Current	V _{REF} = 0, T _J = 25°C		-80	-100		-80	-100	mA
Oscillator								
Nominal Frequency	T _J = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	V _{IN} = 8 to 30V		0.5	1		0.5	1	%
Total Ref Variation	Over Operating Temperature Range	45		55	43		57	kHz
Maximum Frequency	R _T = 2kΩ, C _T = 330pF	500			500			kHz

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ for the UC1851, -40°C to $+85^{\circ}\text{C}$ for the UC2851, and 0°C to 70°C for the UC3851; $V_{IN} = 20\text{V}$, $R_T = 20\text{k}\Omega$, $C_T = .001\text{ mfd}$, $R_R = 10\text{k}\Omega$, $C_R = .001\text{ mfd}$. Current Limit Threshold = 200mV , $T_A = T_J$.

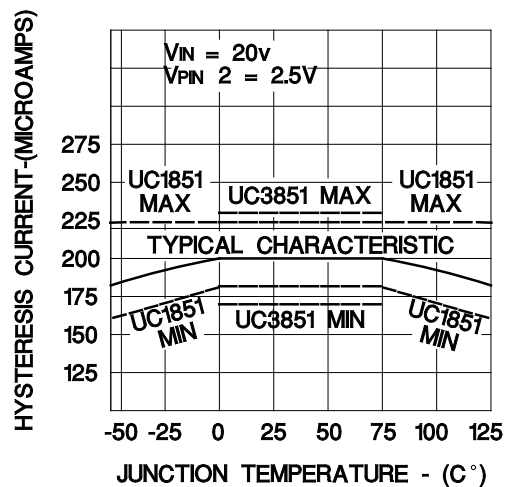
PARAMETER	TEST CONDITIONS	UC1851 / UC2851			UC3851			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Ramp Generator								
Ramp Current, Minimum	ISENSE = -10μA		-11	-14		-11	-14	μA
Ramp Current, Maximum	ISENSE = 1.0mA	-0.9	-95		-0.9	-95		mA
Ramp Valley		0.3	0.4	0.6	0.3	0.4	0.6	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V
Error Amplifier								
Input Offset Voltage	VCM = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	μA
Input Offset Current				0.5			0.5	μA
Open Loop Gain	ΔVo = 1 to 3V	60	66		60	66		dB
Output Swing (Max Output ≤ Ramp Peak - 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	VCM = 1.5 to 5.5V	70	80		70	80		dB
PSRR	VIN = 8 to 30V	70	80		70	80		dB
Short Circuit Current	VCOMP = 0V		-4	-10		-4	-10	mA
Gain Bandwidth (Note 1)	TJ = 25°C, AVOL = 0dB	1	2		1	2		MHz
Slew Rate (Note 1)	TJ = 25°C, AVCL = 0dB		0.8			0.8		V/μs
PWM Section								
Continuous Duty Cycle Range (other than zero) (Note 1)	Minimum Total Continuous Range Ramp Peak < 4.2V	2		46	2		46	%
Output High Level	ISOURCE = 20mA	18	18.5		18	18.5		V
	ISOURCE = 200mA	17	18.5		17	18.5		V
Rise Time (Note 1)	TJ = 25°C, CL = 1nF		50	150		50	150	ns
Fall Time (Note 1)	TJ = 25°C, CL = 1nF		50	150		50	150	ns
Output Saturation	IOUT = 20mA		0.2	0.4		0.2	0.4	V
	IOUT = 200mA		1.7	2.2		1.7	2.2	V
Comparator Delay (Note 1)	Pin 8 to Pin 12, TJ = 25°C, RL = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 5 = 0V		-1.0	-4.0		-1.0	-4.0	μA
Input Leakage	Pins 3, 5 = 10V		0.1	2.0		0.1	2.0	μA
Start/UV Hysteresis Current	Pin 2 = 2.5V	170	200	220	170	200	230	μA
Ext. Stop Threshold	Pin 4	0.8	1.6	2.4	0.8	1.6	2.4	V
Error Latch Activate Current	Pin 4 = 0V, Pin 3 > 3V		-120	-200		-120	-200	μA
Driver Bias Saturation Voltage, VIN-VOH	IB = -50mA		2	3		2	3	V
Driver Bias Leakage	VB = 0V		-0.1	-10		-0.1	-10	μA
Slow-Start Saturation	IS = 10mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	VS = 4.5V		0.1	2.0		0.1	2.0	μA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		-2	-5		-2	-5	μA
Common Mode Range (Note 1)		-0.4		3.0	-0.4		3.0	V
Current Limit Delay (Note 1)	TJ = 25°C, Pin 7 to 12, RL = 1k		200	400		200	400	ns

Note 1: Guaranteed by design. Not 100% tested in production.

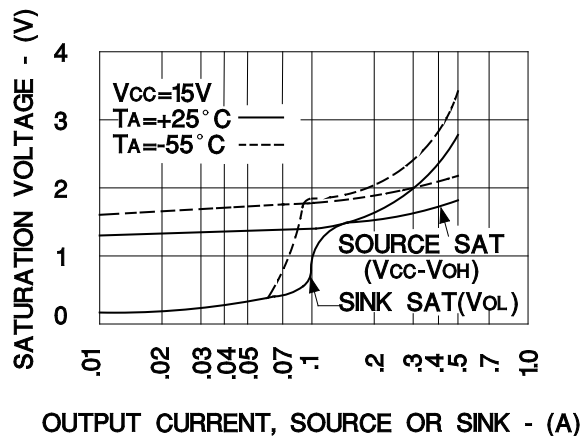
FUNCTIONAL DESCRIPTION

PWM CONTROL	
1. Oscillator	Generates a fixed-frequency internal clock from an external R_T and C_T . Frequency = $\frac{K_C}{R_T C_T}$ where K_C is a first-order correction factor $\approx 0.3 \log (C_T \times 10^{12})$.
2. Ramp Generator:	Develops linear ramp with slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$. C_R is normally selected $\leq C_T$ and its value will have some effect upon valley duty cycle. Limiting the minimum value for I_{SENSE} into pin 11 will establish a maximum duty cycle clamp. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable. The output is held low by the slow start voltage at turn on in order to minimize overshoot.
4. Reference Generator:	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of $\pm 2\%$. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator:	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch:	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch:	Totem pole output stage capable of sourcing and sinking 1 amp peak current. The active "on" state is high.
SEQUENCING FUNCTIONS	
1. Start/UV Sense:	With an increasing voltage, this comparator generates a turn-on signal and releases the slow start clamp at a start threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200 μ A hysteresis current.
2. Drive Switch:	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias:	Supplies drive to external circuitry upon start-up.
4. Slow Start:	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
PROTECTION FUNCTIONS	
1. Error Latch:	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.2V (Typically 3V) b. Stop > 2.4V (Typically 1.6V) c. Current Sense 400mV over threshold. (Typical). Error Latch resets when slow start voltage falls to 0.4V if Reset Pin < 2.8V. With Pin 5 > 3.2V, Error Latch will remain set.
2. Current Limiting:	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV (typical) above threshold, a shutdown signal is sent to Error Latch.
3. External Stop:	A voltage over 2.4 will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a Typical Delay of 13ms/ μ F.

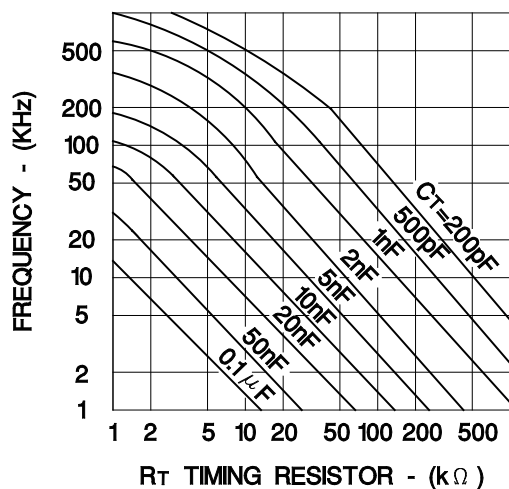
Start/UV Hysteresis Current



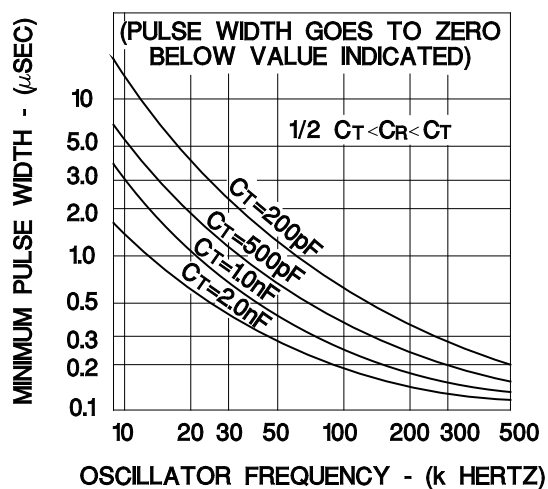
Output Saturation Characteristics



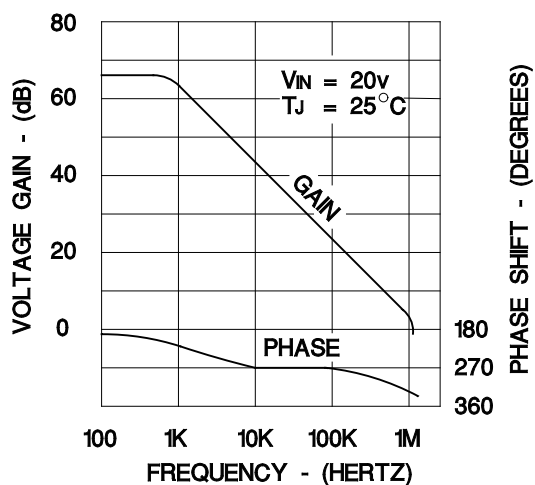
Oscillator Frequency



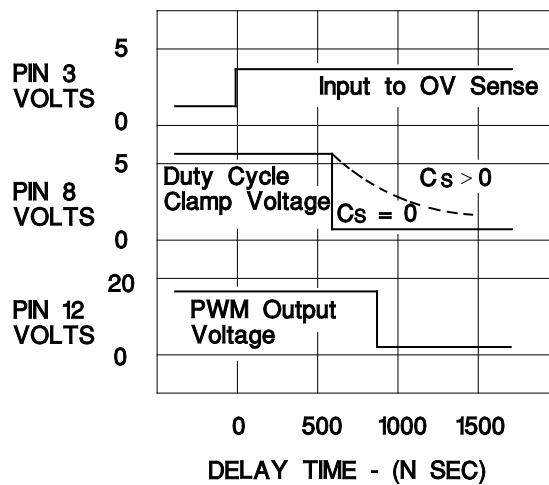
PWM Output Minimum Pulse Width



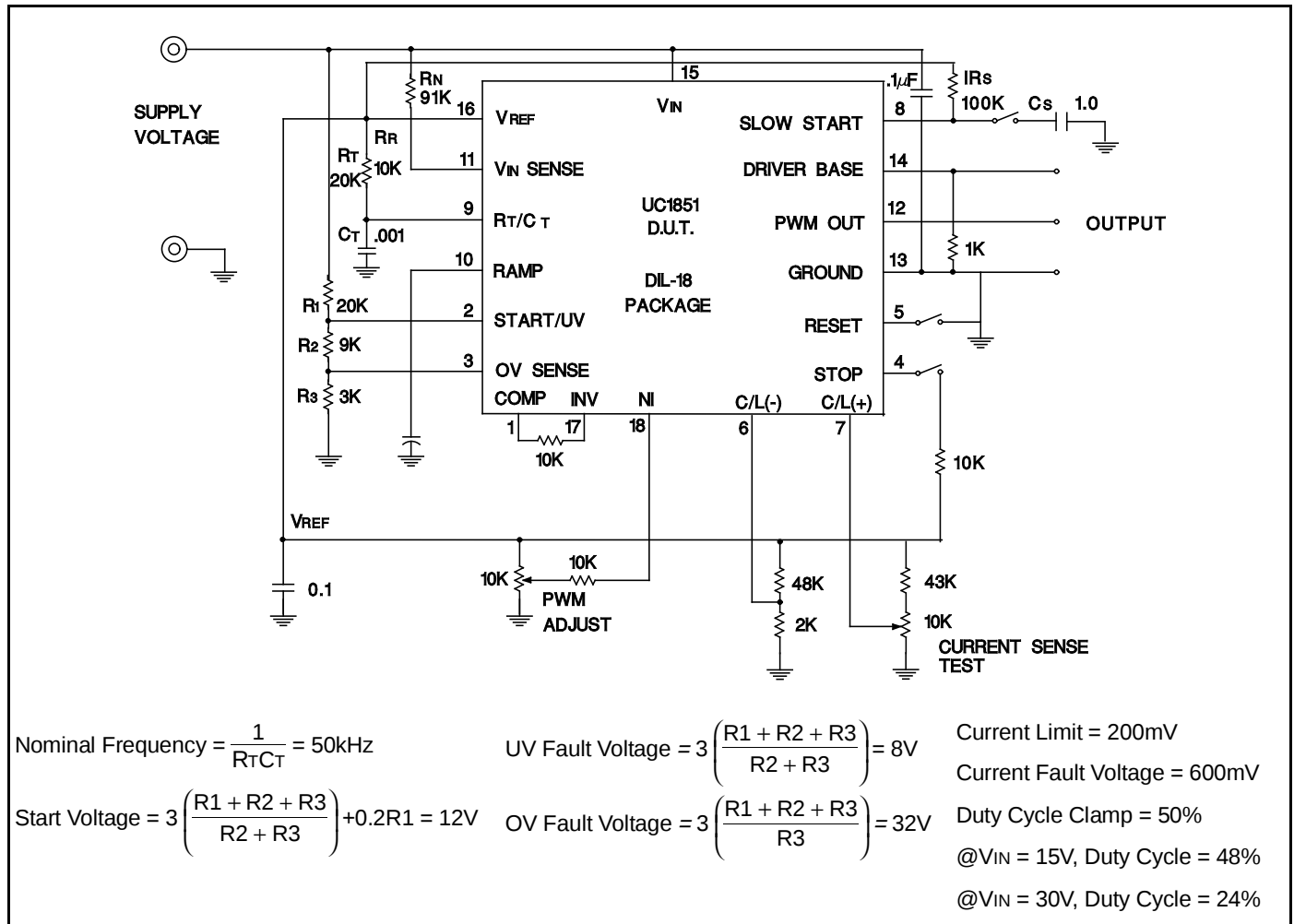
Error Amplifier Open-Loop Gain and Phase



Shutdown Timing

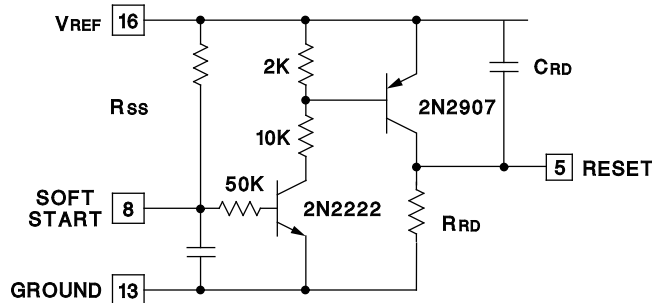


OPEN-LOOP CIRCUIT



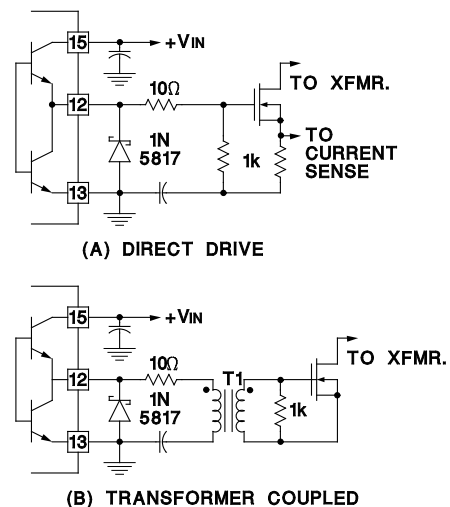
High Peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 13 in a single ground point.

Programmable Soft Start and Restart Delay Circuit



For further application information see UC1840/UC1841 Data Sheets

UC1851 Power MOSFET Drive Interface



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC2851DW	Active	Production	SOIC (DW) 18	40 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2851DW
UC2851DW.A	Active	Production	SOIC (DW) 18	40 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2851DW
UC2851N	NRND	Production	PDIP (N) 18	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2851N
UC2851N.A	NRND	Production	PDIP (N) 18	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2851N
UC3851DW	Obsolete	Production	SOIC (DW) 18	-	-	Call TI	Call TI	0 to 70	UC3851DW
UC3851DWTR	Active	Production	SOIC (DW) 18	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3851DW
UC3851DWTR.A	Active	Production	SOIC (DW) 18	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3851DW
UC3851N	NRND	Production	PDIP (N) 18	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3851N
UC3851N.A	NRND	Production	PDIP (N) 18	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3851N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UC2851DW	DW	SOIC	18	40	507	12.83	5080	6.6
UC2851DW.A	DW	SOIC	18	40	507	12.83	5080	6.6
UC2851N	N	PDIP	18	20	506	13.97	11230	4.32
UC2851N.A	N	PDIP	18	20	506	13.97	11230	4.32
UC3851N	N	PDIP	18	20	506	13.97	11230	4.32
UC3851N.A	N	PDIP	18	20	506	13.97	11230	4.32

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