

## DUAL CHANNEL POWER DRIVER

### FEATURES

- Two Independent Drivers
- 1.5 A Totem Pole Outputs
- Inverting and Non-Inverting Inputs
- 40 ns Rise and Fall Into 1000 pF
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog Shutdown With Optional Latch
- Low Quiescent Current
- 5 V to 40 V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package
- 20-Pin PLCC and CLCC Package

### DESCRIPTION

The UC1707 family of power drivers is made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices—particularly power MOSFETs. These devices contain two independent channels, each of which can be activated by either a high or low input logic level signal. Each output can source or sink up to 1.5 A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, it can be forced low in common through the action either of a digital high signal at the Shutdown terminal or a differential low-level analog signal. The Shutdown command from either source can either be latching or not, depending on the status of the Latch Disable pin.

Supply voltage for both  $V_{IN}$  and  $V_C$  can independently range from 5 V to 40 V.

These devices are available in two-watt plastic "bat-wing" DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for –55°C to +125°C operation. Also available in surface mount DW, Q, L packages.

**TRUTH TABLE**  
**(Each Channel)<sup>(1)</sup>**

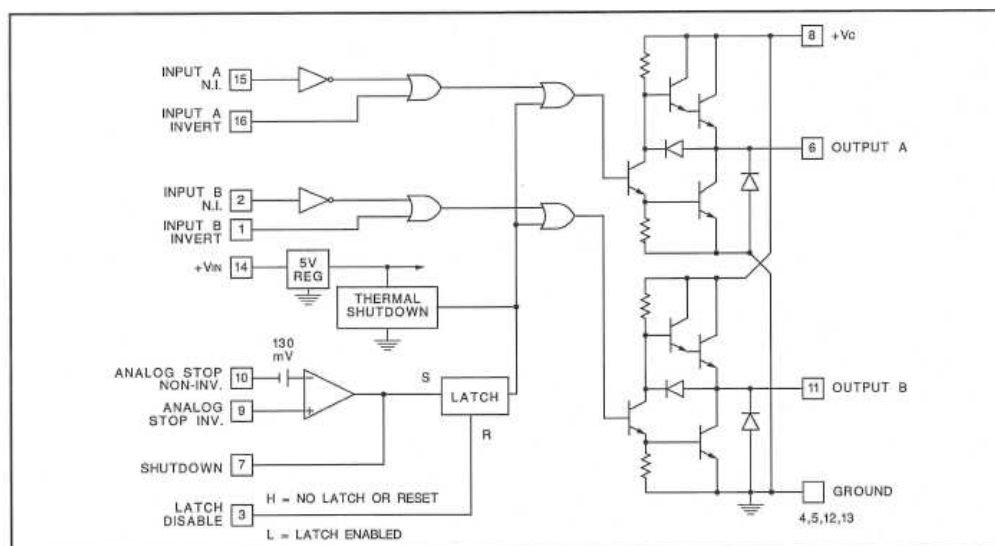
| INV. | N.I. | OUT |
|------|------|-----|
| H    | H    | L   |
| L    | H    | H   |
| H    | L    | L   |
| L    | L    | L   |

(1)  $\overline{OUT} = \overline{INV}$  and N.I.  
 $\overline{OUT} = INV$  or N.I.

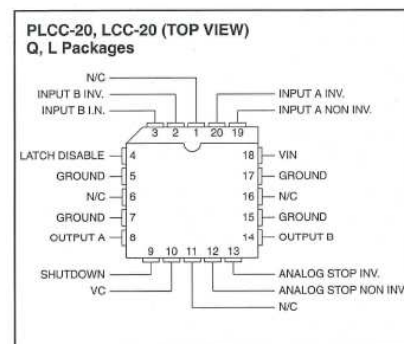
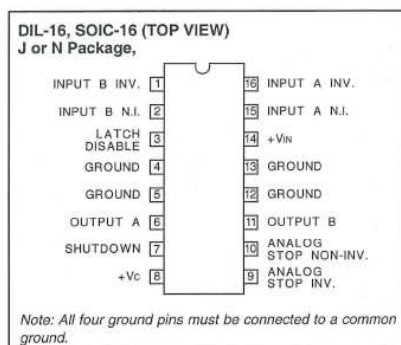


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## BLOCK DIAGRAM



## CONNECTION DIAGRAMS



## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

|          |                                                                           |             | MIN | MAX      | UNIT             |
|----------|---------------------------------------------------------------------------|-------------|-----|----------|------------------|
| $V_{IN}$ | Supply voltage                                                            | N/J package |     | 40       | V                |
| $V_C$    | Collector supply voltage                                                  | N/J package |     | 40       | V                |
|          | Output current (each output, source or sink) steady-state                 | N/J package |     | ±500     | mA               |
|          | Peak transient                                                            | N package   |     | ±1.5     | A                |
|          |                                                                           | J package   |     | ±1.0     |                  |
|          | Capacitive discharge energy                                               | N package   |     | 20       | mJ               |
|          |                                                                           | J package   |     | 15       |                  |
|          | Digital inputs <sup>(1)</sup>                                             | N/J-package |     | 5.5      | V                |
|          | Analog stop inputs                                                        | N/J package |     | $V_{IN}$ |                  |
|          | Power dissipation at $T_A = 25^\circ\text{C}$                             | N package   |     | 2        | W                |
|          |                                                                           | J package   |     | 1        |                  |
|          | Power dissipation at $T$ (leads/case) = $25^\circ\text{C}$ <sup>(1)</sup> | N package   |     | 5        | W                |
|          |                                                                           | J package   |     | 2        |                  |
|          | Operating temperature range                                               |             | –55 | +125     | $^\circ\text{C}$ |
|          | Storage temperature range                                                 |             | –65 | +150     | $^\circ\text{C}$ |
|          | Lead temperature (soldering, 10 seconds)                                  |             |     | 300      | $^\circ\text{C}$ |

- (1) All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal. Digital drive can exceed 5.5 V if input current is limited to 10 mA. Consult packaging section of databook for thermal limitations and considerations of package.

## ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1707,  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2707, and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3707;  $V_{IN} = V_C = 20\text{ V}$ .  $T_A = T_J$ .

| PARAMETER                    | TEST CONDITIONS                              | MIN | TYP   | MAX  | UNIT             |
|------------------------------|----------------------------------------------|-----|-------|------|------------------|
| $V_{IN}$ Supply current      | $V_{IN} = 40\text{ V}$                       |     | 12    | 15   | mA               |
| $V_C$ Supply current         | $V_C = 40\text{ V}$ , outputs low            |     | 5.2   | 7.5  | mA               |
| $V_C$ Leakage current        | $V_{IN} = 0$ , $V_C = 30\text{ V}$ , no load |     | 0.05  | 0.1  | mA               |
| Digital input low level      |                                              |     |       | 0.8  | V                |
| Digital input high level     |                                              | 2.2 |       |      | V                |
| Input current                | $V_I = 0$                                    |     | –0.06 | –1.0 | mA               |
| Input leakage                | $V_I = 5\text{ V}$                           |     | 0.05  | 0.1  | mA               |
| $V_C - V_O$ Output high sat. | $I_O = -50\text{ mA}$                        |     |       | 2.0  | V                |
|                              | $I_O = -500\text{ mA}$                       |     |       | 2.5  |                  |
| $V_O$ Output low sat.        | $I_O = -50\text{ mA}$                        |     |       | 0.4  | V                |
|                              | $I_O = -500\text{ mA}$                       |     |       | 2.5  |                  |
| Analog threshold             | $V_{CM} = 0$ to $15\text{ V}$                | 100 | 130   | 160  | mV               |
| Input bias current           | $V_{CM} = 0$                                 |     | –10   | –20  | $\mu\text{A}$    |
| Thermal shutdown             |                                              |     | 155   |      | $^\circ\text{C}$ |
| Shutdown threshold           | Pin 7 input                                  | 0.4 | 1.0   | 2.2  | V                |
| Latch disable threshold      | Pin 3 input                                  | 0.8 | 1.2   | 2.2  | V                |

**TYPICAL SWITCHING CHARACTERISTICS**

$V_{IN} = V_C = 20\text{ V}$ ,  $T_A = 25^\circ\text{C}$ . Delays measured to 10% output change.

| PARAMETER                                     | TEST CONDITIONS        | OUTPUT CL = |     |     | UNIT |
|-----------------------------------------------|------------------------|-------------|-----|-----|------|
| <b>From Inv. Input to Output</b>              |                        | open        | 1.0 | 2.2 | nF   |
| Rise time delay                               |                        | 40          | 50  | 60  | ns   |
| 10% to 90% rise                               |                        | 25          | 40  | 50  | ns   |
| Fall time delay                               |                        | 30          | 40  | 50  | ns   |
| 90% to 10% fall                               |                        | 25          | 40  | 50  | ns   |
| <b>From N.I. Input to Output</b>              |                        |             |     |     |      |
| Rise time delay                               |                        | 30          | 40  | 50  | ns   |
| 10% to 90% rise                               |                        | 25          | 40  | 50  | ns   |
| Fall time delay                               |                        | 45          | 55  | 65  | ns   |
| 90% to 10% fall                               |                        | 25          | 40  | 50  | ns   |
| $V_C$ cross-conduction current spike duration | Output rise            | 25          |     |     | ns   |
|                                               | Output fall            | 0           |     |     | ns   |
| Analog shutdown delay                         | Stop non-Inv. = 0 V    | 180         |     |     | ns   |
|                                               | Stop Inv. = 0 to 0.5 V | 180         |     |     | ns   |
| Digital shutdown delay                        | 2 V input on Pin 7     | 50          |     |     | ns   |

## SIMPLIFIED INTERNAL CIRCUITRY

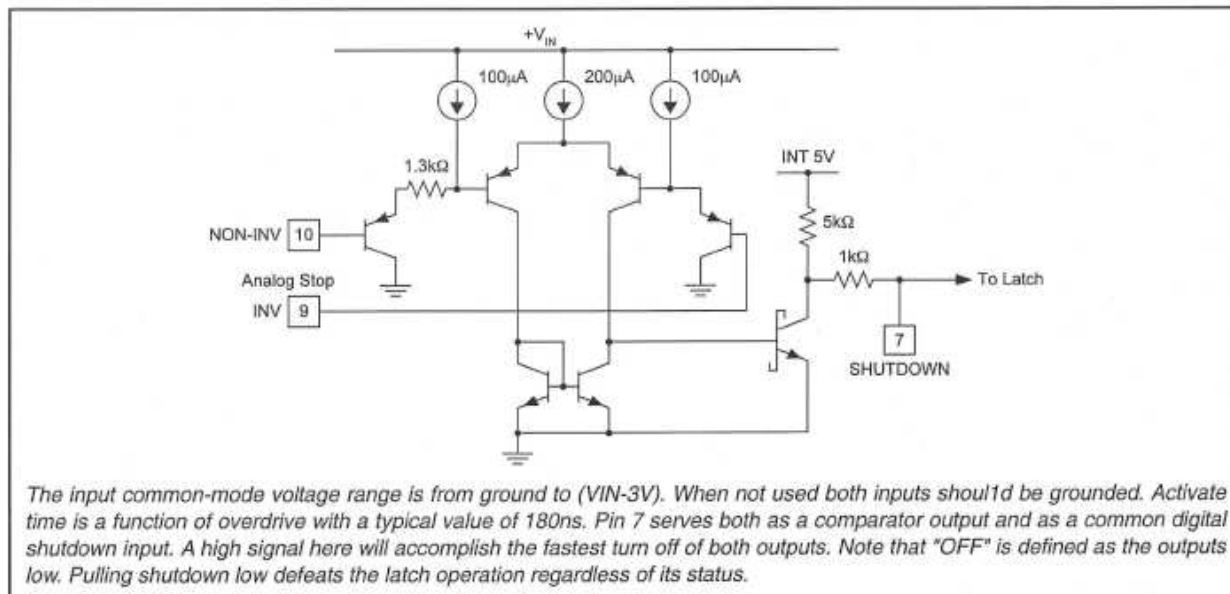


Figure 1. Typical Digital Input Gate

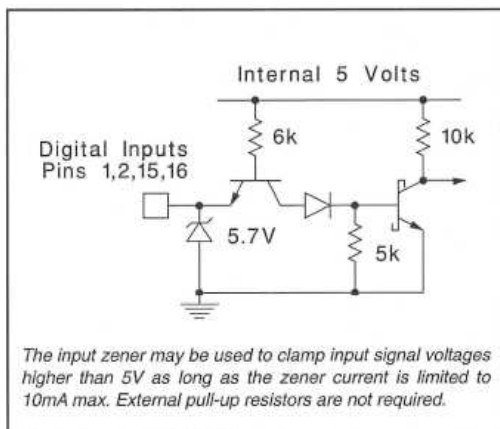


Figure 2. Typical Digital Input Gate

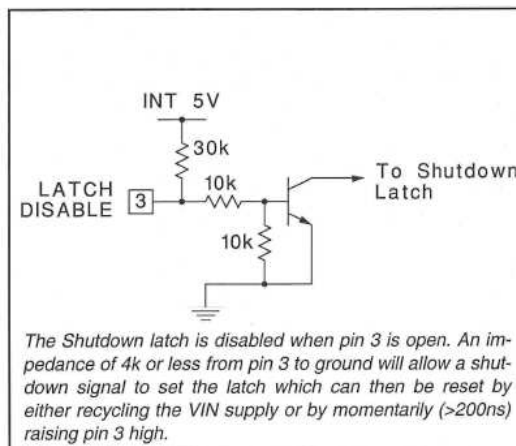
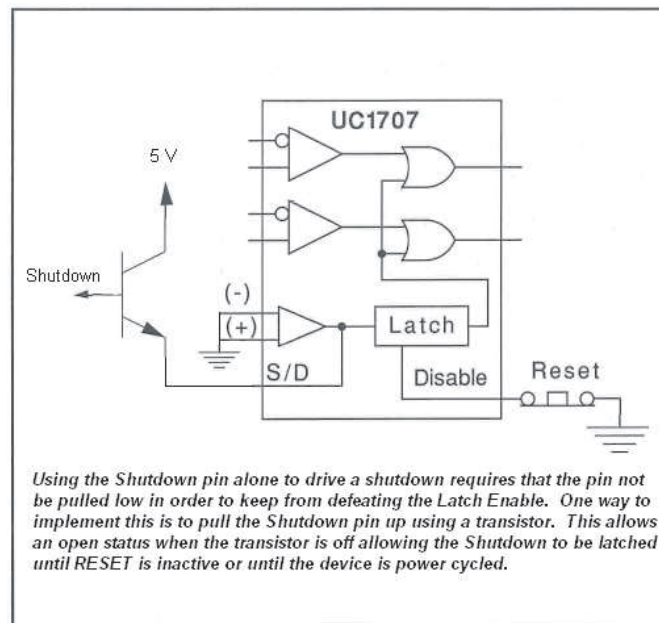


Figure 3. Latch Disable

**SIMPLIFIED INTERNAL CIRCUITRY (continued)****Figure 4. Use of the Shutdown Pin****SHUTDOWN CIRCUIT DESCRIPTION**

The function of the circuitry is to be able to provide a shutdown of the device. This is defined as functionality that will drive both outputs to the low state. There are three different inputs that govern this shutdown capability.

- **Analog Stop Pins** — The differential inputs to this comparator provide a way to execute a shutdown.
- **Latch Disable Pin** — Assuming that the Shutdown pin is left open, a high on this pin disables the latching functionality of the Analog Stop shutdown. A low on this pin enables the latching functionality of the Analog Stop shutdown. If a shutdown occurs through the Analog Stop circuit while Latch Disable is high, then the outputs will go low, but will return to normal operation as soon as the Analog Stop circuit allows it. If a shutdown occurs through the Analog Stop circuit while Latch Disable is low, then the outputs will go low and remain low even if the Analog Stop circuit no longer drives the shutdown. The outputs will remain "latched" low (in shutdown) until the Latch Disable goes high and the Analog Stop circuit allows it to return from shutdown or the VIN voltage is cycled to 0V and then returned above 5V.
- **Shutdown Pin** — This pin serves two purposes.
  1. It can be used as an output of the Analog Stop circuit.
  2. It can be used as an input to force a shutdown or to force the device out of shutdown. This pin can override both the Analog Stop circuit as well as the Latch Disable Pin. When driving hard logic levels into the Shutdown pin, the Latch Disable functionality will be overridden and the Latch Disable will not function as it does when used in conjunction with the Analog Stop circuit. When the Shutdown pin is high, the outputs will be in the low state (shutdown). When the Shutdown pin is low (hard logic low) the outputs will operate normally, regardless of the state of the Latch Disable pin or the Analog Stop pins.

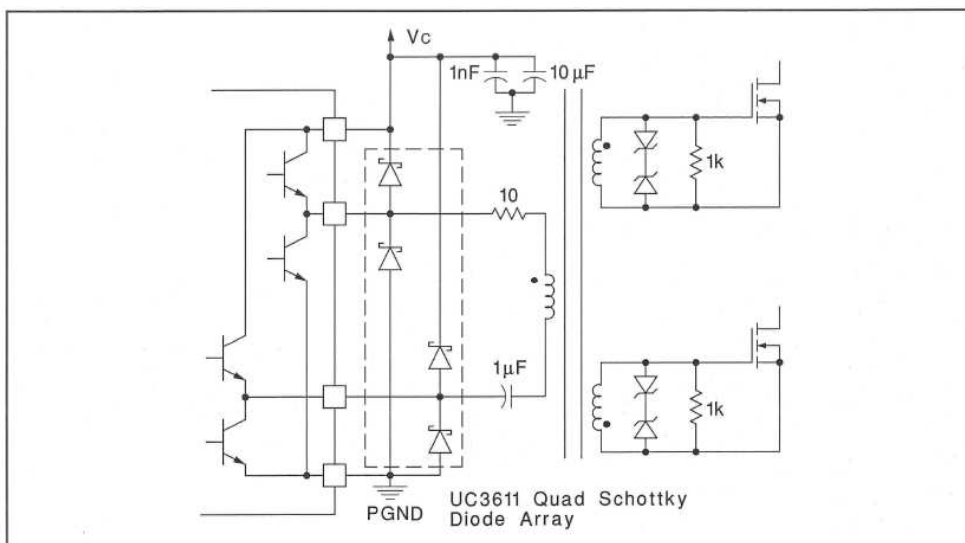
In order to use the Shutdown Pin with the Latch Disable functional it is necessary to use either a diode in series with the Shutdown signal or to use an open collector pull-up so that the Shutdown pin is not pulled low. This configuration will allow the Latch Disable function to work with the Shutdown pin.

# SIMPLIFIED INTERNAL CIRCUITRY (continued)

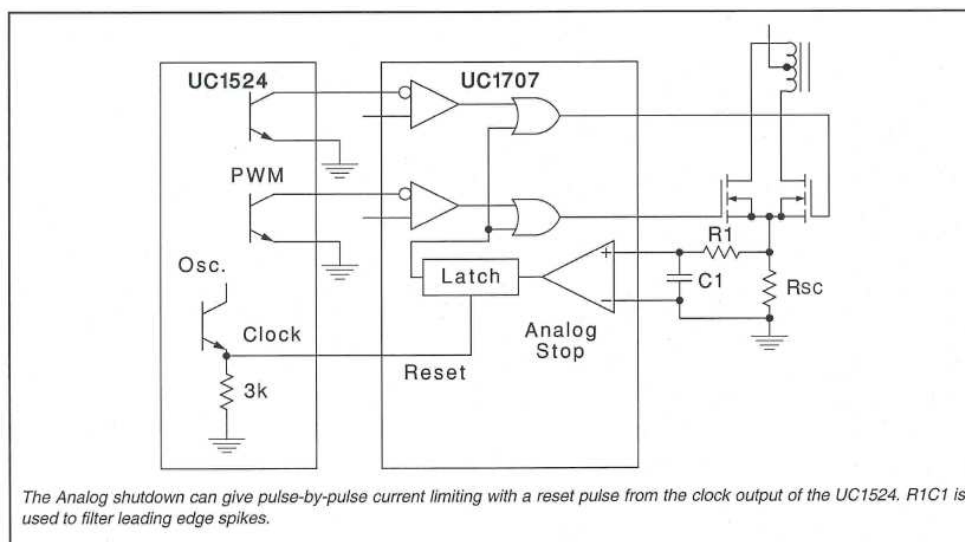
## UG1707 SHUTDOWN TRUTH TABLE

| ANALOG STOP LOGIC | SHUTDOWN | LATCH DISABLE | PREVIOUS STATE OF OUTPUT | OUTPUT                          |
|-------------------|----------|---------------|--------------------------|---------------------------------|
| X                 | 0        | X             | X                        | Follows Input Logic             |
| X                 | 1        | X             | X                        | Low (Shutdown)                  |
| 1                 | Open     | X             | X                        | Low (Shutdown)                  |
| 0                 | Open     | 0             | Shutdown                 | <sup>(1)</sup> Latched Shutdown |
| 0                 | Open     | 0             | Normal                   | Follows Input Logic             |
| 0                 | Open     | 1             | X                        | Follows Input Logic             |

- (1) If the output was previously in Shutdown and Latch Disable was low and stays low, then even if the Analog Stop Logic is changed or the Shutdown pin is open, the outputs will remain in Shutdown.



**Figure 5. Transformer Coupled Push-Pull MOSFET Drive Circuit**



**Figure 6. Current Limiting**

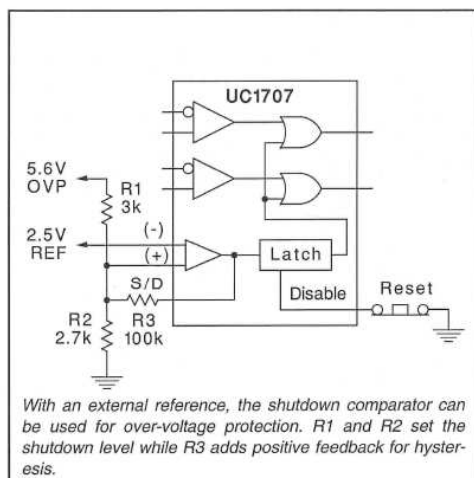


Figure 7. Over-Voltage Protection

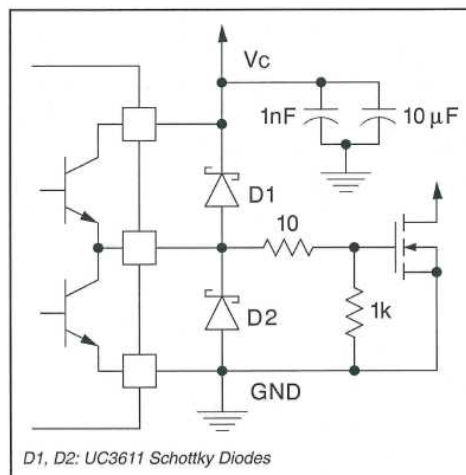


Figure 8. Power MOSFET Drive Circuit

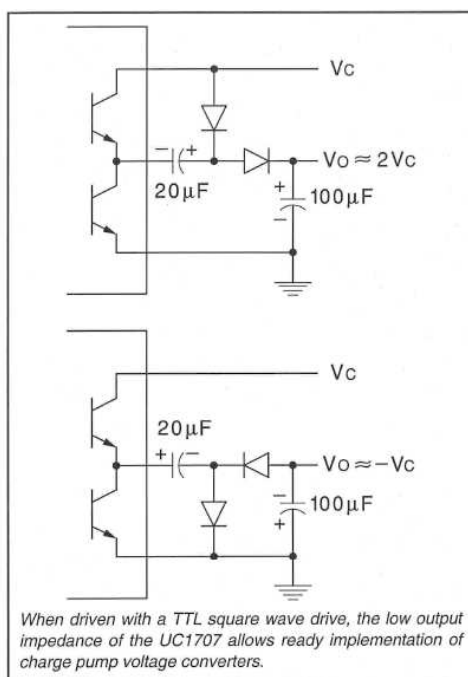
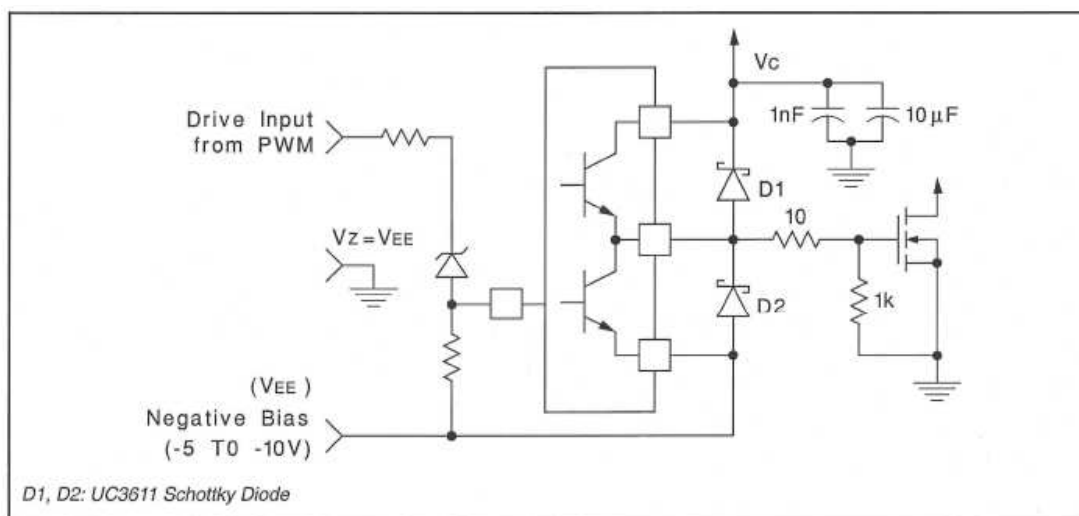


Figure 9. Charge Pump Circuits



### Figure 11. Transformer Coupled MOSFET Drive Circuit



**Figure 12. Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting to Ground Reference PWM**

**PACKAGING INFORMATION**

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                     |
|--------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-----------------------------------------|
| <a href="#">5962-87619012A</a> | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>87619012A<br>UC1707L/<br>81032 |
| 5962-87619012A.A               | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>87619012A<br>UC1707L/<br>81032 |
| <a href="#">5962-8761901EA</a> | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8761901EA<br>UC1707J/80900         |
| 5962-8761901EA.A               | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8761901EA<br>UC1707J/80900         |
| <a href="#">UC1707J</a>        | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1707J                                 |
| UC1707J.A                      | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1707J                                 |
| <a href="#">UC1707J883B</a>    | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1707J/883B                            |
| UC1707J883B.A                  | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1707J/883B                            |
| <a href="#">UC1707L</a>        | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1707L                                 |
| UC1707L.A                      | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1707L                                 |
| <a href="#">UC1707L883B</a>    | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1707L/<br>883B                        |
| UC1707L883B.A                  | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1707L/<br>883B                        |
| <a href="#">UC2707DW</a>       | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2707DW                                |
| UC2707DW.A                     | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2707DW                                |
| <a href="#">UC2707DWTR</a>     | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2707DW                                |
| UC2707DWTR.A                   | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2707DW                                |
| <a href="#">UC2707N</a>        | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | UC2707N                                 |
| UC2707N.A                      | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | UC2707N                                 |
| UC2707NG4                      | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | UC2707N                                 |
| <a href="#">UC3707DW</a>       | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3707DW                                |
| UC3707DW.A                     | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3707DW                                |
| <a href="#">UC3707DWTR</a>     | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3707DW                                |

| Orderable part number   | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| UC3707DWTR.A            | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3707DW            |
| <a href="#">UC3707J</a> | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | 0 to 70      | UC3707J             |
| UC3707J.A               | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | 0 to 70      | UC3707J             |
| <a href="#">UC3707N</a> | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UC3707N             |
| UC3707N.A               | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UC3707N             |
| UC3707NG4               | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UC3707N             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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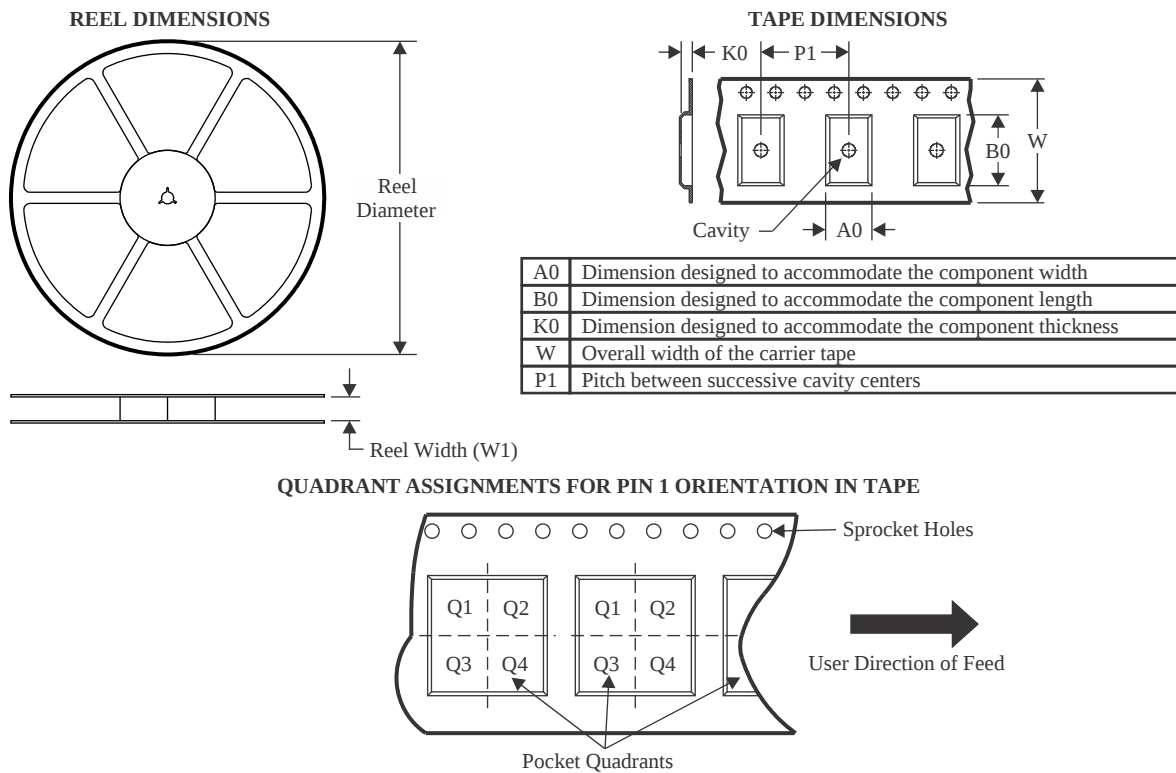
**OTHER QUALIFIED VERSIONS OF UC1707, UC3707, UC3707M :**

- Catalog : [UC3707](#), [UC3707M](#), [UC3707](#)
- Military : [UC1707](#), [UC1707](#)
- Space : [UC1707-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

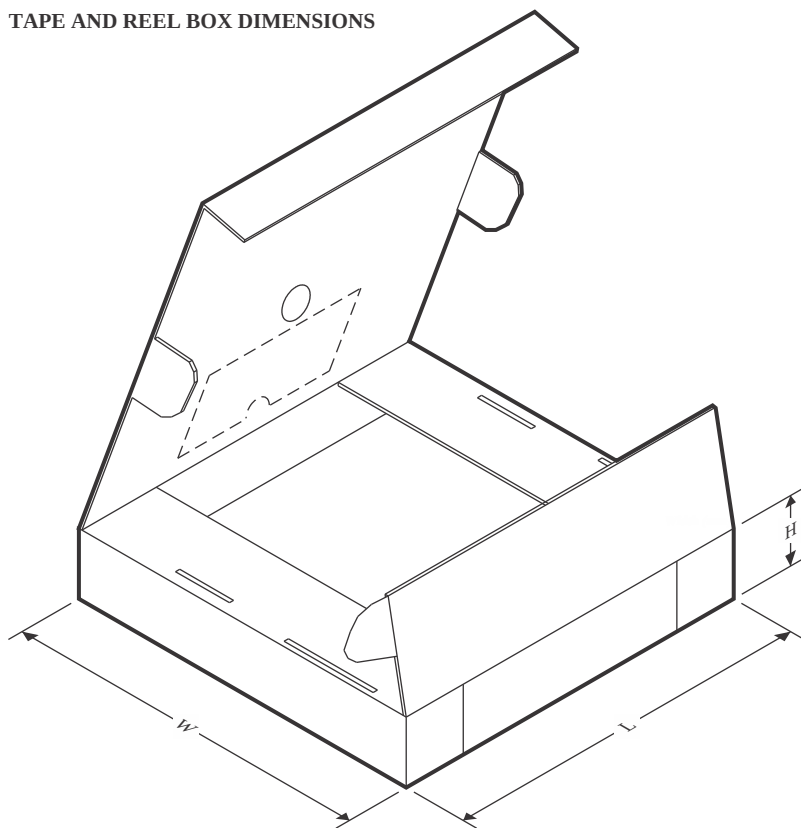
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UC2707DWTR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| UC3707DWTR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| UC2707DWTR | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| UC3707DWTR | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device           | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-87619012A   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| 5962-87619012A.A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1707L          | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1707L.A        | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1707L883B      | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1707L883B.A    | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC2707DW         | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2707DW.A       | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2707N          | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC2707N.A        | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC2707NG4        | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC3707DW         | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3707DW.A       | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3707N          | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC3707N.A        | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC3707NG4        | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |

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