TXB0104W-Q1 Automotive 4-Bit Bidirectional Voltage-Level Translator with Automatic Direction Sensing and ±15kV ESD Protection

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
- 1.1V to 3.6V on A port and 1.65V to 5.5V on B port
- No power supply sequencing required - either VCCA or VCCB can be ramped up first
- VCCA can be >,=,< VCCB
- V_{CC} isolation feature – if either V_{CC} input is at GND, all outputs are in the high-impedance state
- OE input circuit referenced to V_{CCA}
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22
  - A port
    - ±2500V human-body model (A114-B)
    - ±1000V charged-device model (C101)
  - B port
    - ±15000V human-body model (A114-B)
    - ±1000V charged-device model (C101)

2 Applications

- Infotainment and cluster
- Advanced driver assistance system (ADAS)

3 Description

Voltage-level translators address the challenges posed by simultaneous use of different supply-voltage levels on the same circuit board. This 4-bit non-inverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. VCCA accepts any supply voltage from 1.1V to 3.6V. The B port is designed to track V_{CCB}. VCCB accepts any supply voltage from 1.65V to 5.5V. This allows for universal low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state. To establish high-impedance state during power up or power down, OE must be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

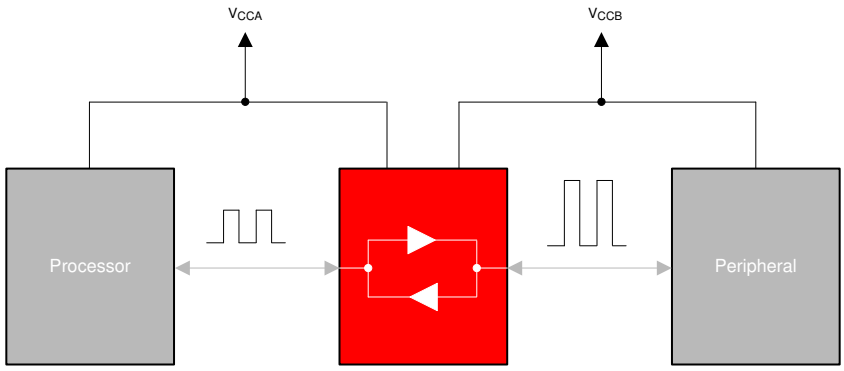
The TXB0104W is designed so that the OE input circuit is supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Package Information

PART NUMBER (1)	PACKAGE	PACKAGE SIZE(2)
TXB0104W-Q1	RUT (UQFN, 12)	2.00mm × 1.70mm
	BQA (WQFN, 14)	3.00mm × 2.5mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Block Diagram for TXB0104W

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4 Pin Configuration and Functions

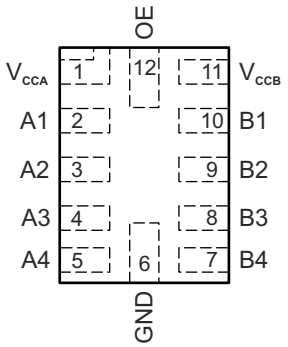


Figure 4-1. RUT Package (Top View)

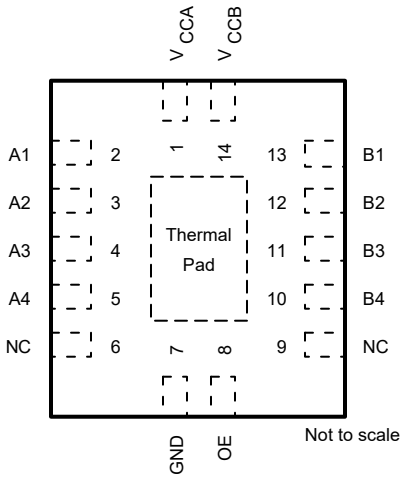


Figure 4-2. BQA Package, 14-Pin WQFN With Exposed Thermal Pad (Top View)

NC − No internal connection

Table 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	BQA	RUT		
VCCA	1	1	I	A-port supply voltage 1.1V ≤ V_{CCA} ≤ 3.6V.
A1	2	2	I/O	Input/output 1. Referenced to V_{CCA}.
A2	3	3	I/O	Input/output 2. Referenced to V_{CCA}.
A3	4	4	I/O	Input/output 3. Referenced to V_{CCA}.
A4	5	5	I/O	Input/output 4. Referenced to V_{CCA}.
NC	6	-	–	No connection. Not internally connected.
GND	7	6	–	Ground
OE	8	12	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
NC	9	-	–	No connection. Not internally connected.
B4	10	7	I/O	Input/output 4. Referenced to V_{CCB}.
B3	11	8	I/O	Input/output 3. Referenced to V_{CCB}.
B2	12	9	I/O	Input/output 2. Referenced to V_{CCB}.
B1	13	10	I/O	Input/output 1. Referenced to V_{CCB}.
VCCB	14	11	I	B-port supply voltage 1.65V ≤ V_{CCB} ≤ 5.5V.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		–0.5	4.6	V
V_{CCB}			–0.5	6.5	
V_I	Input voltage	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V_O	Voltage applied to any output in the high-impedance or power-off state	A port	–0.5	4.6	V
		B port	-0.5	6.5	
V_O	Voltage applied to any output in the high or low state(2)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	A Port	±2500	V
			B Port	±15000	
		Charged-device model (CDM), per AEC Q100-011	A Port	±1000	
			B Port	±1000	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.1	3.6	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs	1.1V to 3.6V	1.65V to 5.5V	V_{CCI} × 0.65(2)	V_{CCI}	V
		OE	1.1V to 3.6V	1.65V to 5.5V	V_{CCA} × 0.65	5.5	
V_{IL}	Low-level input voltage	Data inputs	1.1V to 5.5V	1.65V to 5.5V	0	V_{CCI} × 0.35(2)	V
		OE	1.1V to 3.6V	1.65V to 5.5V	0	V_{CCA} × 0.35	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A-port	1.1V to 3.6V	1.65V to 5.5V	0	3.6	V
		B-port			0	5.5	
Δt/Δv	Input transition Rise or fall rate	A-port inputs	1.1V to 3.6V	1.65V to 5.5V		40	ns/V
		B-port inputs	1.1V to 3.6V	1.65V to 3.6V		40	
				4.5V to 5.5V		30	
T_A	Operating free-air temperature				–40	125	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, that is, both at V_{CCI} or both at GND.
(2) V_{CCI} is the supply voltage associated with the input port.

5.4 Thermal Information

THERMAL METRIC (1)		TXB0104W-Q1		UNIT
		RUT	BQA	
		12 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	146.94	77.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	134.61	80.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	61.51	46.9	
Ψ_{JT}	Junction-to-top characterization parameter	34.24	6.1	
Ψ_{JB}	Junction-to-board characterization parameter	61.52	46.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	23.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{OHA}		I_{OH} = –20µA	1.1V to 3.6V					V_{CCA} – 0.4			V
V_{OLA}		I_{OL} = 20µA	1.1V to 3.6V							0.4	V
V_{OHB}		I_{OH} = –20µA		1.65V to 5.5V				V_{CCB} – 0.4			V
V_{OLB}		I_{OL} = 20µA		1.65V to 5.5V						0.4	V
I_I	OE	V_I = V_{CCI} or GND	1.1V to 3.6V	1.65V to 5.5V			±1			±5	µA
I_{off}	A port	V_I or V_O = 0 to 3.6V	0V	0V to 5.5V			±1			±10	µA
	B port	V_I or V_O = 0 to 5.5V	0V to 3.6V	0V			±1			±10	
I_{OZ}	A or B port	OE = GND	1.1V to 3.6V	1.65V to 5.5V			±1			±10	µA

over recommended operating free-air temperature range (unless otherwise noted) (1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0	1.1V to 3.6V	1.65V to 5.5V						20	µA
			3.6V	0V						15	
			0V	5.5V						–15	
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.1V to 3.6V	1.65V to 5.5V						20	µA
			3.6V	0V						–15	
			0V	5.5V						15	
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.1V to 3.6V	1.65V to 5.5V						40	µA
I_{CCZA}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.1V to 3.6V	1.65V to 5.5V						15	µA
I_{CCZB}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.1V to 3.6V	1.65V to 5.5V						15	µA
C_i	OE		1.1V to 3.6V	1.65V to 5.5V		4					pF
C_{io}	A port		1.1V to 3.6V	1.65V to 5.5V		6					pF
	B port					13					pF

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.

5.6 Timing Requirements: V_{CCA} = 1.2 ± 0.1V

over recommended operating free-air temperature range, V_{CCA} = 1.2V ± 0.1V (unless otherwise noted)

			V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			30		30		30		20	Mbps
t_w	Pulse duration	Data inputs	33.33		33.33		33.33		50		ns

5.7 Timing Requirements: V_{CCA} = 1.5V ± 0.1V

over recommended operating free-air temperature range, V_{CCA} = 1.5V ± 0.1V (unless otherwise noted)

			V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			50		65		70		55	Mbps
t_w	Pulse duration	Data inputs	20		15		14		18		ns

5.8 Timing Requirements: V_{CCA} = 1.8V ± 0.15V

over recommended operating free-air temperature range, V_{CCA} = 1.8V ± 0.15V (unless otherwise noted)

			V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			55		80		80		95	Mbps
t_w	Pulse duration	Data inputs	18		12		12		10.5		ns

5.9 Timing Requirements: V_{CCA} = 2.5V ± 0.2V

over recommended operating free-air temperature range, V_{CCA} = 2.5V ± 0.2V (unless otherwise noted)

			V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			60		100		120		120	Mbps
t_w	Pulse duration	Data inputs	16		10		8		8		ns

5.10 Timing Requirements: V_{CCA} = 3.3V ± 0.3V

over recommended operating free-air temperature range, V_{CCA} = 3.3V ± 0.3V (unless otherwise noted)

			V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			60		100		140		140	Mbps
t_w	Pulse duration	Data inputs	16		10		7		7		ns

5.11 Switching Characteristics: V_{CCA} = 1.2 ± 0.1V

over recommended operating free-air temperature range, V_{CCA} = 1.2V ± 0.1V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		15.3		11.6		10.6		18.2	ns
	B	A		17.1		14.7		14.1		13.6	
t_{en}	OE	A or B		1		1		1		1	µs
t_{dis}	OE	A or B		432		432		432		432	ns
t_{rA}, t_{fA}	A-port rise and fall times			5.7		5.7		5.6		5.6	ns
t_{rB}, t_{fB}	B-port rise and fall times			3.9		2.8		2.3		1.9	ns

5.12 Switching Characteristics: V_{CCA} = 1.5V ± 0.1V

over recommended operating free-air temperature range, V_{CCA} = 1.5V ± 0.1V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		13		9		8		6.6	ns
	B	A		11.7		9.54		9		8.2	
t_{en}	OE	A or B		1		1		1		1	µs
t_{dis}	OE	A or B		394		305		305		305	ns
t_{rA}, t_{fA}	A-port rise and fall times			3.2		3.3		3.3		3.3	ns
t_{rB}, t_{fB}	B-port rise and fall times			4		2.8		2.3		1.9	ns

5.13 Switching Characteristics: V_{CCA} = 1.8V ± 0.15V

over recommended operating free-air temperature range, V_{CCA} = 1.8V ± 0.15V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		12.1		8.3		6.8		5.65	ns
	B	A		10.2		7.91		7.1		6.55	
t_{en}	OE	A or B		1		1		1		1	µs
t_{dis}	OE	A or B		393		256		248		248	ns
t_{rA}, t_{fA}	A-port rise and fall times			2.7		2.7		2.7		2.6	ns
t_{rB}, t_{fB}	B-port rise and fall times			4		2.8		2.3		1.9	ns

5.14 Switching Characteristics: V_{CCA} = 2.5V ± 0.2V

over recommended operating free-air temperature range, V_{CCA} = 2.5V ± 0.2V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		11.8		7.4		5.9		4.8	ns
	B	A		8.5		6.2		5.4		4.8	
t_{en}	OE	A or B		1		1		1		1	µs
t_{dis}	OE	A or B		400		255		185		170	ns
t_{rA}, t_{fA}	A-port rise and fall times			2.1		2		2		2	ns
t_{rB}, t_{fB}	B-port rise and fall times			4		2.8		2.3		1.8	ns

5.15 Switching Characteristics: V_{CCA} = 3.3V ± 0.3V

over recommended operating free-air temperature range, V_{CCA} = 3.3V ± 0.3V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		11.7		7.3		5.6		4.3	ns
	B	A		8.3		5.7		4.8		4	
t_{en}	OE	A or B		1		1		1		1	µs
t_{dis}	OE	A or B		392		255		185		130	ns
t_{rA}, t_{fA}	A-port rise and fall times			1.8		1.8		1.7		1.8	ns
t_{rB}, t_{fB}	B-port rise and fall times			4		2.8		2.3		1.9	ns

5.16 Operating Characteristics

T_A = 25°C (1)

PARAMETER		TEST CONDITIONS	V_{CCA}							UNIT
			1.2V	1.2V	1.5V	1.8V	2.5V	2.5V	3.3V	
			V_{CCB}							
			5V	1.8V	1.8V	1.8V	2.5V	5V	3.3V to 5V	
			TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10MHz, t_r = t_f = 1ns, OE = V_{CCA} (outputs enabled)	7.8	10	9	8	8	8	9	pF
	B-port input, A-port output		12	11	11	11	11	11	11	
C_{pdB}	A-port input, B-port output		38.1	28	28	28	29	29	29	
	B-port input, A-port output		25.4	19	18	18	19	21	22	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10MHz, t_r = t_f = 1ns, OE = GND (outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C_{pdB}	A-port input, B-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.04	

(1) Cpd parameter is the capacitance used to determine the no-load dynamic power dissipation per logic function for CMOS devices as per the formula: $P_D = C_{pd} (V_{CC})^2 + I_{CC}V_{CC}$. For more details about the use of C_{pd} to calculate power dissipation, refer to the *CMOS Power Consumption and C_{pd} Calculation* application note.

5.17 Typical Characteristics

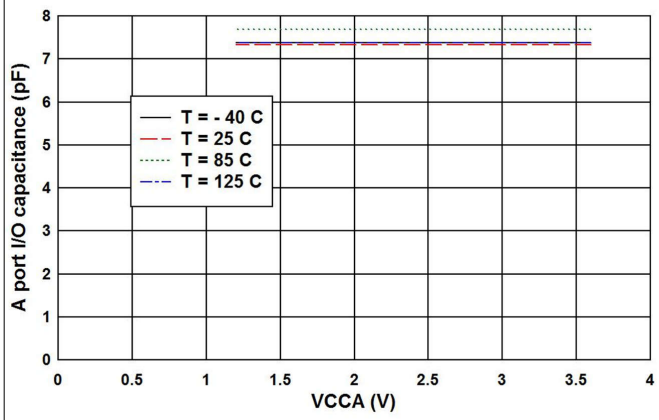


Figure 5-1. Capacitance for A port I/O pins (C_{iO}) vs Power Supply (V_{CCA}) for V_{CCB} = 3.3V

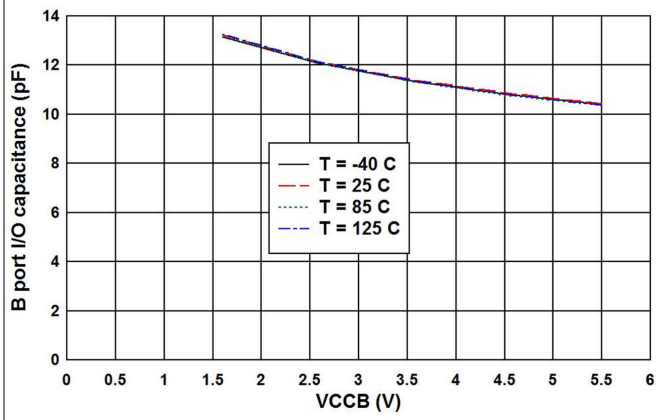
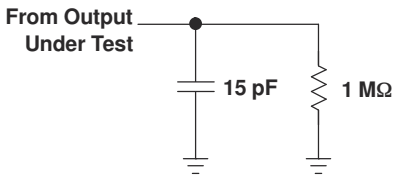
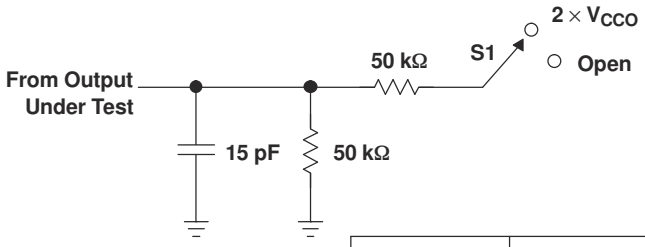


Figure 5-2. Capacitance for B port I/O pins (C_{iO}) vs Power Supply (V_{CCB}) for V_{CCA} = 3.3V

6 Parameter Measurement Information

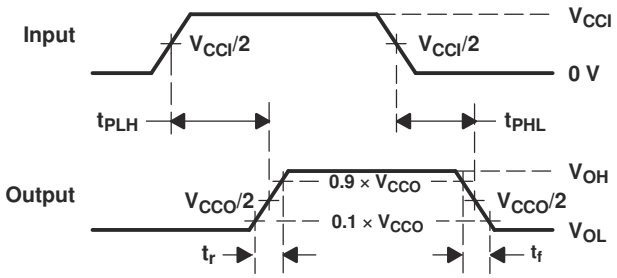


LOAD CIRCUIT FOR MAX DATA RATE, PULSE DURATION PROPAGATION DELAY OUTPUT RISE AND FALL TIME MEASUREMENT

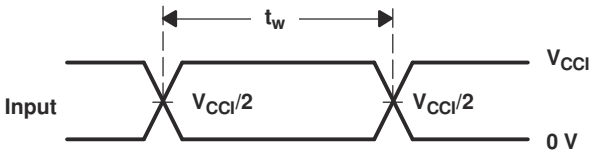


LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT

TEST	S1
t_{PZL}/t_{PLZ} t_{PHZ}/t_{PZH}	$2 \times V_{CCO}$ Open



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATION

A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. V_{CCI} is the V_{CC} associated with the input port.
F. V_{CCO} is the V_{CC} associated with the output port.
G. All parameters and waveforms are not applicable to all devices.

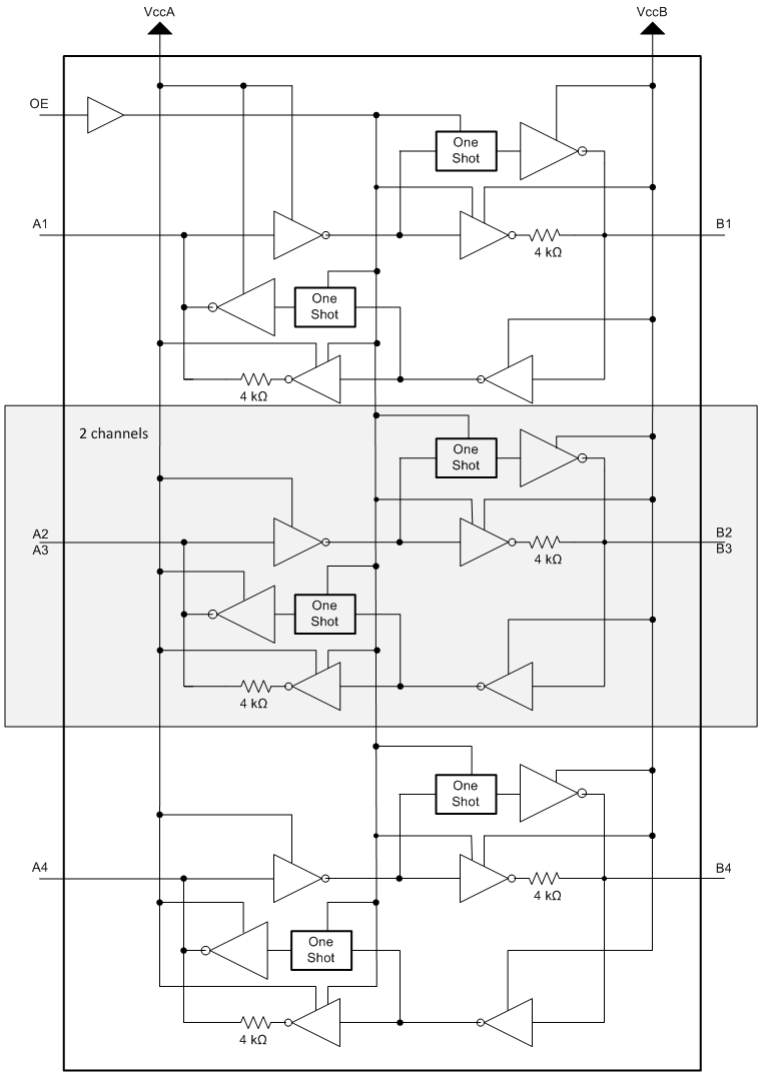
Figure 6-1. Load Circuits and Voltage Waveforms

7 Detailed Description

7.1 Overview

The TXB0104W device is a 4-bit, bi-directional voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.1V to 3.6V, while the B port can accept I/O voltages from 1.65V to 5.5V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI's TXS010X products.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Architecture

The TXB0104W architecture (see *Section 7.2*) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the TXB0104W can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration which speeds up the high-to-low transition. The typical output impedance during output transition is 70Ω at V_{CCO} = 1.2V to 1.8V, 50Ω at V_{CCO} = 1.8V to 3.3V, and 40Ω at V_{CCO} = 3.3V to 5V.

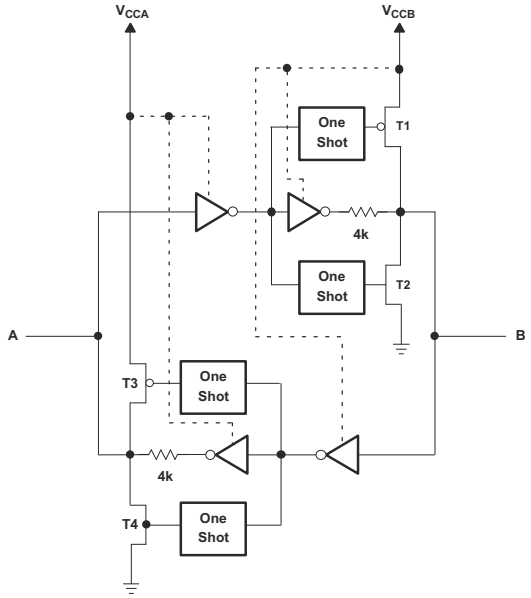


Figure 7-1. Architecture of TXB0104W I/O Cell

7.3.2 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0104W are shown in Figure 7-2. For proper operation, the device driving the data I/Os of the TXB0104 must have drive strength of at least ±2mA.

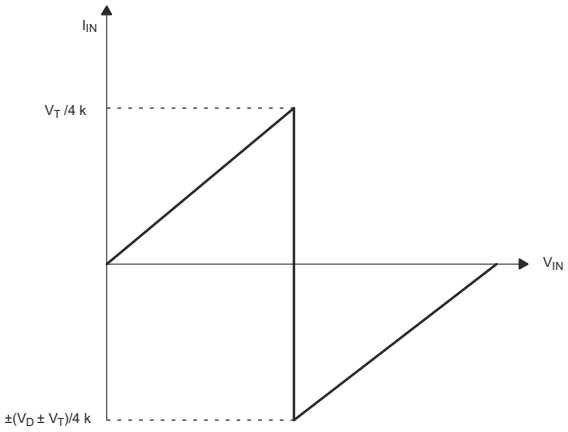


Figure 7-2. Typical I_{IN} vs V_{IN} Curve

7.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to verify that proper one shot (O.S.) triggering takes place. PCB signal trace-lengths must be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXB0104W output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

7.3.4 Enable and Disable

The TXB0104W has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

7.3.5 Pullup or Pulldown Resistors on I/O Lines

The TXB0104W is designed to drive capacitive loads of up to 70pF. The output drivers of the TXB0104W have low DC drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50kΩ to ensure that they do not contend with the output drivers of the TXB0104W.

For the same reason, the TXB0104W must not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

7.4 Device Functional Modes

The TXB0104W device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high impedance state. Setting the OE input to high enables the device.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TXB0104W can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI TXS010X products. Any external pulldown or pullup resistors are recommended larger than 50kΩ.

8.2 Typical Application

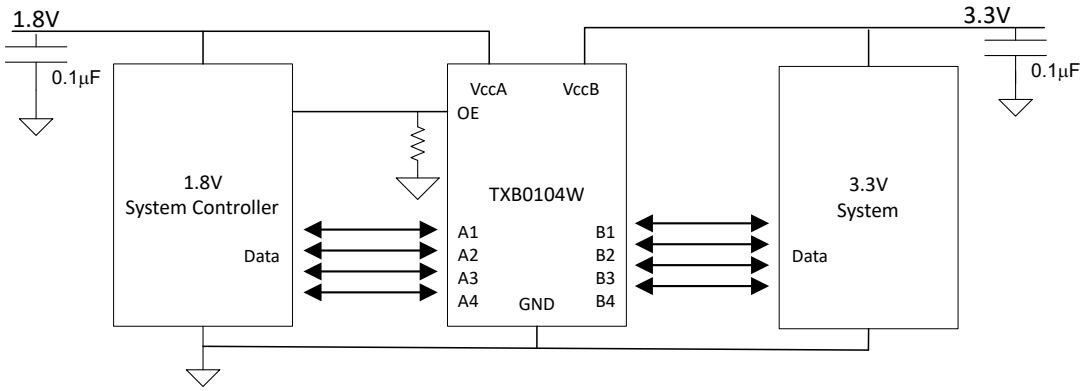


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	1.1V to 3.6V
Output voltage range	1.65V to 5.5V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

Input Voltage Range

Use the supply voltage of the device that is driving the TXB0104W device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.

Output Voltage Range

Use the supply voltage of the device that the TXB0104W device is driving to determine the output voltage range. It is not recommended to have the external pullup or pulldown resistors. If mandatory, it is recommended the value must be larger than 50kΩ.

An external pulldown or pullup resistor decreases the output V_{OH} and V_{OL}. Use the below equations to draft estimate the V_{OH} and V_{OL} as a result of an external pulldown and pullup resistor.

$$V_{OH} = V_{CCx} \times R_{PD} \div (R_{PD} + 4.5k\Omega) \quad (1)$$

$$V_{OL} = V_{CCx} \times 4.5k\Omega \div (R_{PU} + 4.5k\Omega) \quad (2)$$

where

- V_{CCx} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor
- R_{PU} is the value of the external pull up resistor
- 4.5kΩ is the counting the variation of the serial resistor 4kΩ in the I/O line

8.2.3 Application Curve

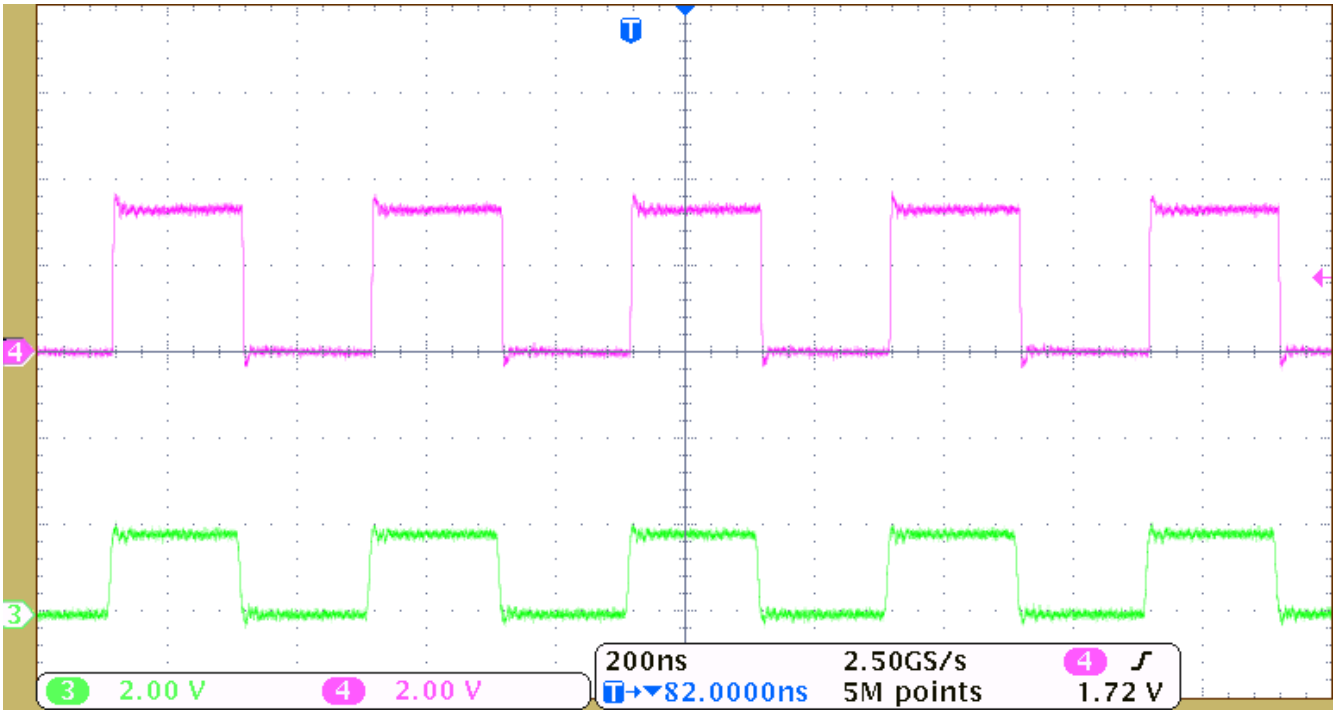


Figure 8-2. Example of Level Translation of a 2.5MHz 1.8V Signal (Green) to a 3.3V Signal (Pink)

8.3 Power Supply Recommendations

The TXB0104W has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B}$ = 0V). The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

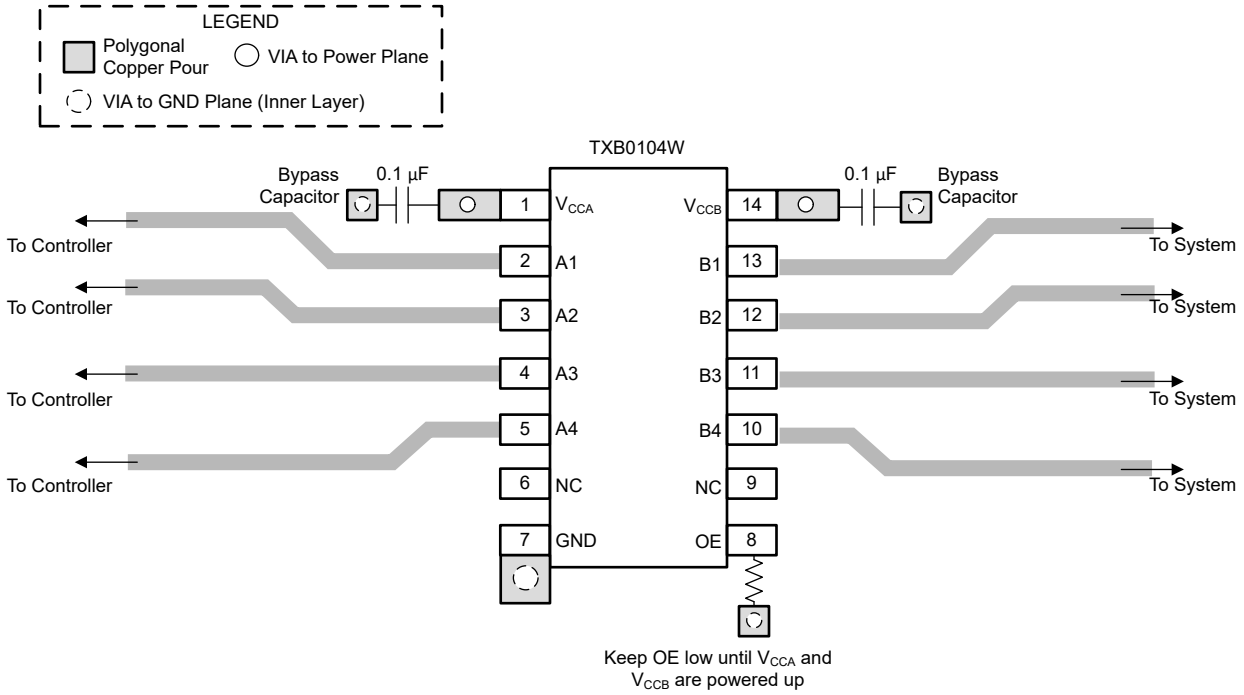
8.4 Layout

8.4.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on power supplies. Place the bypass capacitors as close as possible to the VCCA, VCCB pin, and GND pin
- Use short trace-lengths to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 10ns, to verify that any reflection encounters low impedance at the source driver

8.4.2 Layout Example



9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXB0104WQRUTRQ1	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1UW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

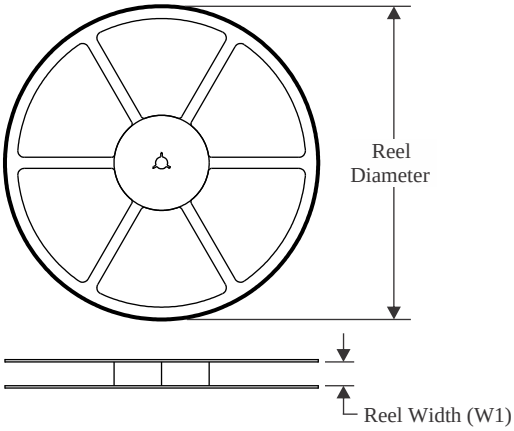
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

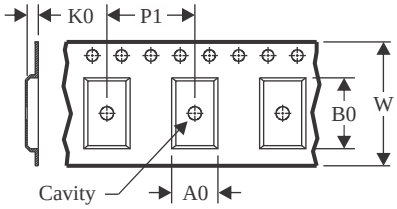
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

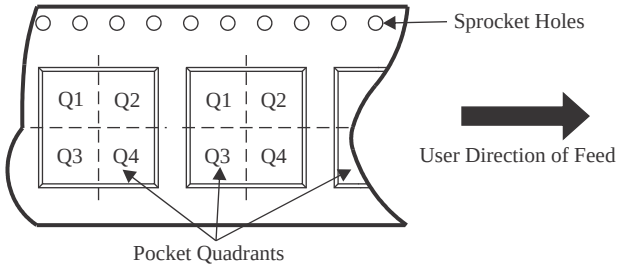


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

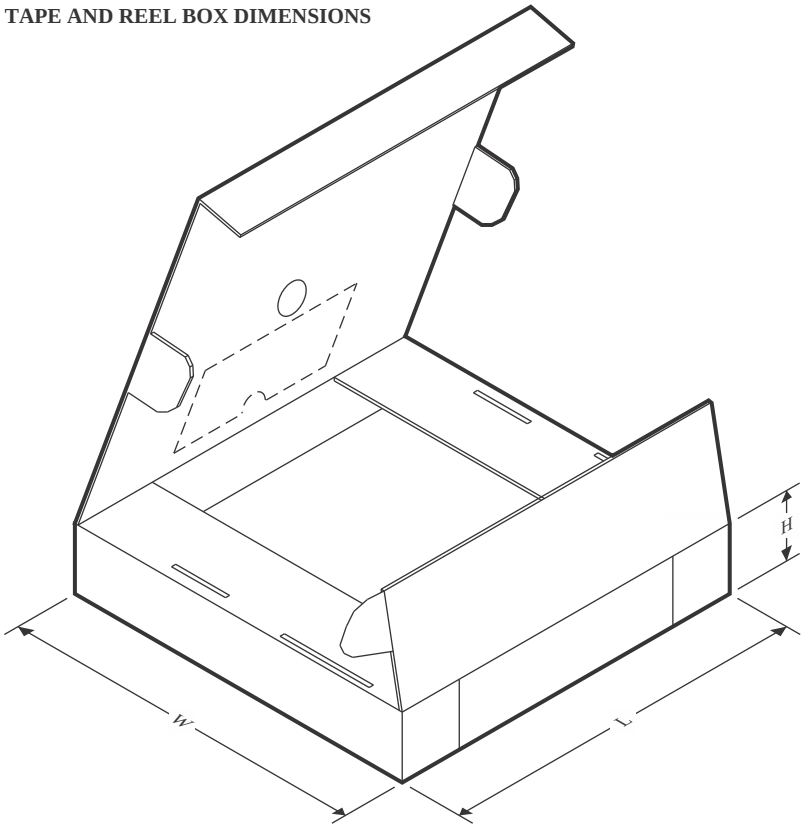
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0104WQRUTRQ1	UQFN	RUT	12	3000	180.0	8.4	2.0	2.3	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

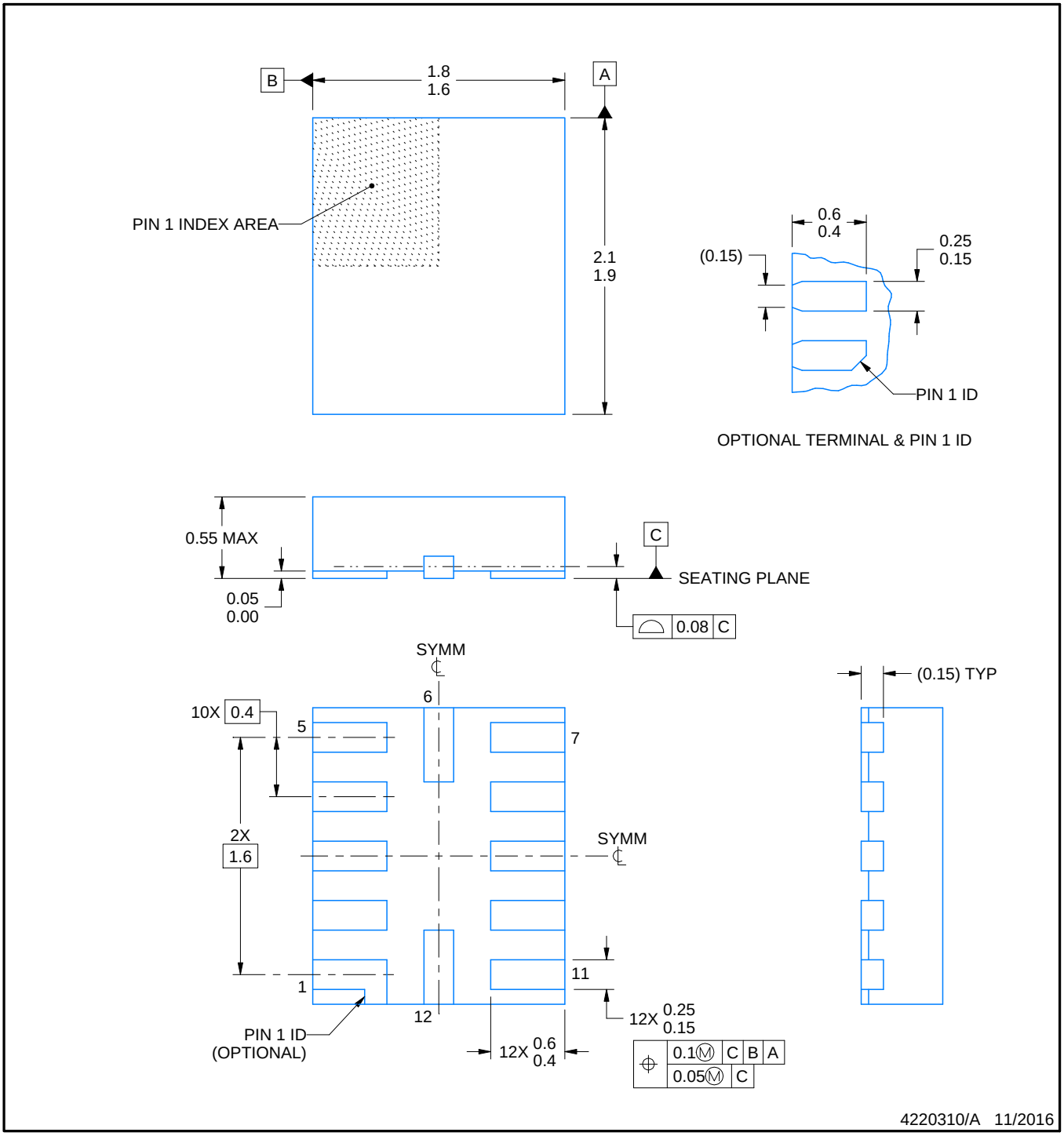
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0104WQRUTRQ1	UQFN	RUT	12	3000	210.0	185.0	35.0

RUT0012A

PACKAGE OUTLINE

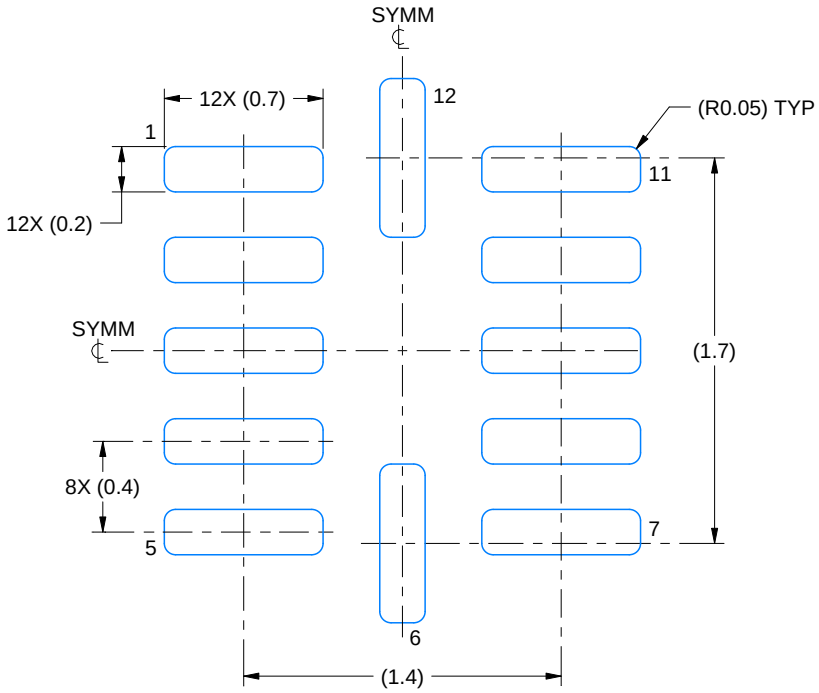
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

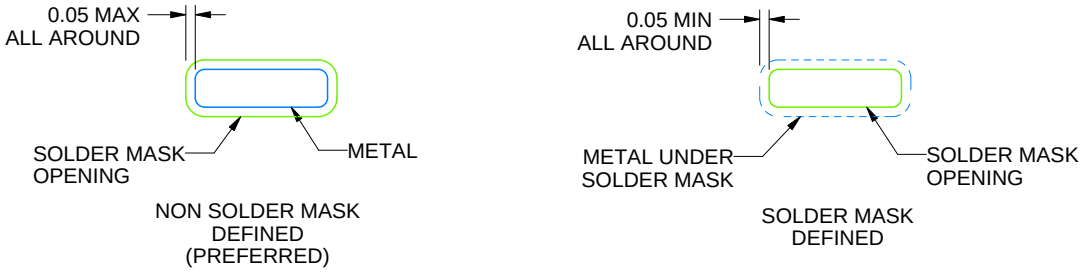


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

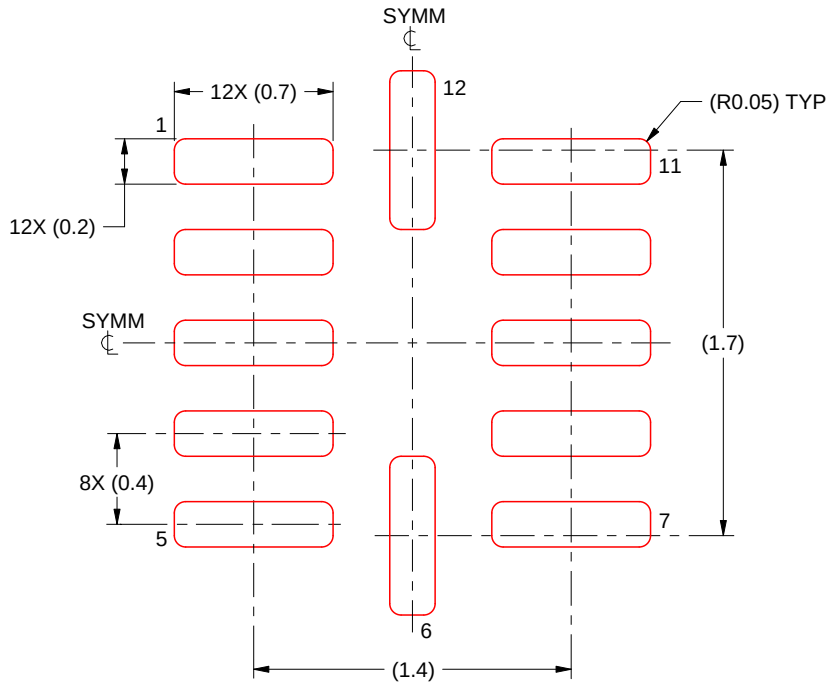


SOLDER MASK DETAILS

4220310/A 11/2016

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025