

TUSB2514B Four-Port Hi-Speed USB Hub

1 Features

- Compliant to USB Specification Rev. 2.0
- Single 3.3V power supply
- Hi-Speed USB 2.0 hub with 4 downstream ports
 - Multi Transaction Translator (MTT)
 - Full power management with per-port or ganged power switching and overcurrent detection
 - Supports USB Battery Charging specification Rev. 1.2
 - Integrated USB termination and pull-up/pull-down resistors
- I²C EEPROM or SMBus target interface for device configuration:
 - Vendor ID and Product ID
 - USB polarity swap
 - Downstream port configuration
- Secure for enterprise operations
 - Hardware-based state machine eliminates firmware injection risks via MCU-free operation
- 24MHz crystal or oscillator clock input
- Extended 105°C maximum ambient temperature range for datacenter applications

2 Applications

- Data center compute
- Data center networking
- Docking station
- Flat-panel monitor
- Multifunction printer
- Desktop PC/motherboard

3 Description

The TUSB2514B is a 4-port Hi-Speed USB hub that supports USB Hi-Speed (480Mbps) and Full-

Speed (12Mbps) connections on the upstream port. The device also provides USB Hi-Speed, Full-Speed, or Low-Speed (1.5Mbps) connections on the four downstream ports. The TUSB2514B hardware-based state machine eliminates firmware injection risks, enabling secure deployment in enterprise and datacenter applications without an external microcontroller.

All four downstream ports comply with the USB Battery Charging Specification Rev. 1.2. Charging Downstream Port (CDP) mode is supported when the upstream port is connected; DCP mode is the final fallback when the upstream port is not connected and other charging modes are disabled or unsupported. Each port supports individual overcurrent detection and per-port or ganged power switching.

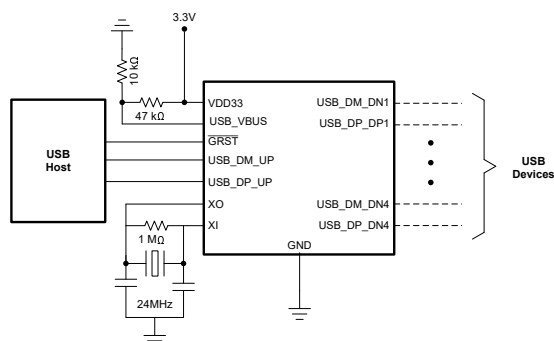
The TUSB2514B operates without an external EEPROM using pin-strap configuration. Pin-strap selectable features include per-port battery charging, port enable/disable, and activity indicators.

For advanced customization, the TUSB2514B supports an I²C EEPROM or SMBus target interface to configure the Vendor ID (VID), Product ID (PID), USB channel polarity, and additional downstream port behavior.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TUSB2514B	RHH (VQFN, 36)	6mm × 6mm

- (1) For all available packages, see [Section 11](#).
 (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application



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4 Pin Configuration and Functions

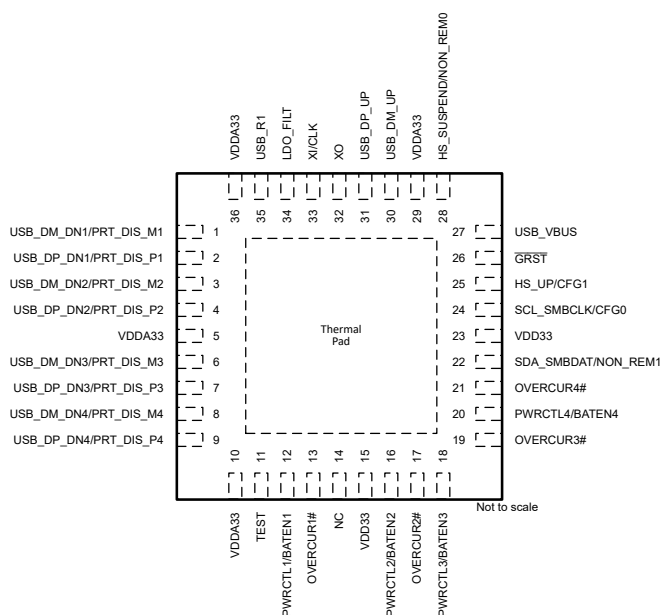


Figure 4-1. RHH Package, 36-pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		I/O ⁽¹⁾	TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.			
USB_DM_DN1/ PRT_DIS_N1	1	I/O	—	USB high-speed differential transceiver (negative) This pin is sampled at GRST# to determine if the port is disabled. To disable a port, pull both positive and negative pins to 3.3V with 10kΩ pullup resistor for the corresponding port number.
USB_DM_DN2/ PRT_DIS_N2	3			
USB_DM_DN3/ PRT_DIS_N3	6			
USB_DM_DN4/ PRT_DIS_N4	8			
USB_DP_DN1/ PRT_DIS_P1	2	I/O	—	USB high-speed differential transceiver (positive) This pin is sampled at GRST# to determine if the port is disabled. To disable a port, pull both positive and negative pins to 3.3V with 10kΩ pullup resistor for the corresponding port number.
USB_DP_DN2/ PRT_DIS_P2	4			
USB_DP_DN3/ PRT_DIS_P3	7			
USB_DP_DN4/ PRT_DIS_P4	9			
V _{DDA33}	5, 10	—	PWR	3.3V analog power rail
V _{DD33}	15,23,29 ,36	—	PWR	3.3V power rail
TEST	11	I	PD	This pin is reserved for factory test. Leave unconnected; an internal pulldown resistor holds this pin low.
PWRCTL1/BATEN1	12	I/O	PD	USB port 1 power-on control for downstream power and battery charging enable. The pin is used as an input to the downstream power switch for port 1. The value of the pin is sampled at the deassertion of GRST# to determine the value of the battery charging support for Port 1 indicated in the Battery Charging Support register. 0 = Battery charging not supported 1 = Battery charging supported

Table 4-1. Pin Functions (continued)

PIN		I/O ⁽¹⁾	TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.			
OVERCUR1#	13	I	PU	USB port 1 overcurrent detection. This pin is used to connect the overcurrent output of the downstream port power switch for port 1. 0 = An overcurrent event occurred. 1 = An overcurrent event has not occurred. If power management is not implemented, leave this pin unconnected.
NC	14	I	—	This pin can be left unconnected or tied to GND through a capacitor.
PWRCTL2/BATEN2	16	I/O	PD	USB port 2 power-on control for downstream power and battery charging enable. The pin is used as an input to the downstream power switch for port 2. The value of the pin is sampled at the deassertion of GRST# to determine the value of the battery charging support for Port 2 indicated in the Battery Charging Support register. 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR2#	17	I	PU	USB port 2 overcurrent detection. This pin is used to connect the overcurrent output of the downstream port power switch for port 2. 0 = An overcurrent event occurred. 1 = An overcurrent event has not occurred. If power management is not implemented, leave this pin unconnected.
PWRCTL3/BATEN3	18	I/O	PD	USB port 3 power-on control for downstream power and battery charging enable. The pin is used as an input to the downstream power switch for port 3. The value of the pin is sampled at the deassertion of GRST# to determine the value of the battery charging support for Port 3 indicated in the Battery Charging Support register. 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR3#	19	I	PU	USB port 3 overcurrent detection. This pin is used to connect the overcurrent output of the downstream port power switch for port 3. 0 = An overcurrent event occurred. 1 = An overcurrent event has not occurred. If power management is not implemented, leave this pin unconnected.
PWRCTL4/BATEN4	20	I/O	PD	USB port 4 power-on control for downstream power and battery charging enable. The pin is used as an input to the downstream power switch for port 4. The value of the pin is sampled at the deassertion of GRST# to determine the value of the battery charging support for Port 4 indicated in the Battery Charging Support register. 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR4#	21	I	PU	USB port 4 overcurrent detection. This pin is used to connect the overcurrent output of the downstream port power switch for port 4. 0 = An overcurrent event occurred. 1 = An overcurrent event has not occurred. If power management is not implemented, leave this pin unconnected.
SDA_SMBDAT/ NON_REM1	22	I/O	PD	I²C data or SMBus data. When configured for pin-strap mode, this pin, along with NON_REM0, determines which downstream ports are marked non-removable as described in Table 6-4.
SCL_SMBCLK/CFG0	24	I/O	PD	I²C clock or SMBus clock. At the rising edge of GRST#, this pin is sampled along with CFG1 to determine I²C, SMBus, or pin-strap operation as described in Table 6-2.

Table 4-1. Pin Functions (continued)

PIN		I/O ⁽¹⁾	TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.			
HS_UP/ CFG1	25	I/O	PD	After reset, this signal indicates the high-speed USB connection status of the upstream port as described in Table 6-4 . At the rising edge of GRST#, this pin is sampled along with CFG0 to determine I ² C, SMBus, or pin-strap operation as described in Table 6-2 .
GRST#	26	I	—	Global power reset. This reset brings all of the TUSB2514B internal registers to the default states. When GRST# is asserted, the device is completely nonfunctional. See Section 6.3.4 for reset timing requirements.
USB_VBUS	27	I	—	USB upstream port power monitor. The VBUS detection requires a voltage divider. In a detachable hub application, USB_VBUS can be connected to VBUS through a 90.9kΩ ±1% resistor and to ground through a 10kΩ ±1% resistor from the signal to ground. In a self-powered application, it can be controlled by the permanently attached host or connected to 3.3V through a 47kΩ ±1% resistor and to ground through a 10kΩ ±1% resistor from the signal to ground.
HS_SUSPEND/ NON_REM0	28	I/O	PD	When configured for pin-strap mode, this pins, along with NON_REM1, determines which downstream ports are marked non-removable as described in Table 6-4 . If SMBus is selected, this pin functions as a HS_SUSPEND (upstream HS suspend indicator) as described in Table 6-4 .
USB_DM_UP	30	I/O	—	USB high-speed differential transceiver (negative)
USB_DP_UP	31	I/O	—	USB high-speed differential transceiver (positive)
XO	32	O	—	24MHz Crystal output. This pin is the crystal output for the internal oscillator. If the XI pin is driven by an external oscillator, this pin can be left unconnected. When using a crystal, a 1MΩ feedback resistor is required between the XI and XO pins.
XI/CLK	33	I	—	24MHz Crystal input. This pin is the crystal input for the internal oscillator. The input can alternately be driven by the output of an external oscillator. When using a crystal, a 1MΩ feedback resistor is required between the XI and XO pins.
LDO_FILT	34	I	—	LDO Filter Capacitor: this pin must have up to a 2.2μF capacitor to VSS.
USB_R1	35	I	—	Precision resistor reference. Connect a 9.53kΩ ±1% resistor between this pin and GND.
Thermal Pad		—	GND	Ground. The thermal pad must be connected to ground.

(1) I = Input, O = Output, I/O = Input/output, PU = Internal pull-up resistor, PD = Internal pull-down resistor, and PWR = Power signal, GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage range	V _{DD} Supply voltage range	−0.3	3.8	V
Voltage range	USB_VBUS terminal	−0.3	1.4	V
	XI terminal	−0.3	2.45	V
	All other terminals	−0.3	3.8	V
Junction temperature	T _{J(max)}	−40	105	°C
Storage temperature	T _{stg}	−65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	3.3V Supply voltage	3.0	3.3	3.6	V
USB_VBUS	Voltage at USB_VBUS terminal.	0		1.155	V
T _A	Ambient temperature	−40		85	°C
T _J	Junction temperature	−40		105	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TUSB2514B	
		RHH	UNIT
		36 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	28.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	17.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	10.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	10.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW POWER MODES						
I _{DD33_SUS} PEND	V _{DD33} current in suspend	V _{DD} = 1.1V; V _{DD33} = 3.3V; T _A = 25°C;	8	16	30	mA
ACTIVE POWER MODES						
I _{DD33_SMB} US	V _{DD33} current during SMBus programming	V _{DD33} = 3.3V; T _A = 25°C;		50		mA
I _{DD33_2H_} OSS_1HS	V _{DD33} current upstream port connected to USB 2.0 Host, downstream port(s) connected to 1 HS device.	V _{DD33} = 3.3V; T _A = 25°C;		100		mA
I _{DD33_2H_} OSS_4HS	V _{DD33} current upstream port connected to USB 2.0 Host, downstream port(s) connected to 4 HS device.	V _{DD33} = 3.3V; T _A = 25°C;	115	140	170	mA
3.3V I/O						
V _{IH}	High-level input voltage ⁽¹⁾		2		3.6	V
V _{IL}	Low-level input voltage ⁽¹⁾		0	0.4	0.8	V
t _t	Input transition time (t _{RISE} and t _{FALL})			10	25	ns
V _{HYS}	Input hysteresis ⁽²⁾				0.468	V
V _{OH, IO}	High-level output voltage	I _{OH} = –4 mA	2.4	3.3		V
V _{OL, IO}	Low-level output voltage	I _{OH} = 4 mA		.05	0.4	V
I _{OZP}	High-impedance output current with internal pullup or pulldown resistor. ⁽³⁾	V _I = 0 to V _{DD33} ;	–350		350	μA

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{I, IO}$	Input current ⁽⁴⁾	$V_I = 0$ to V_{DD33}	–15		15	μA
$R_{PD, IO}$	Internal pulldown resistance		7	11	18	$k\Omega$
$R_{PU, IO}$	Internal pullup resistance		9	14	18	$k\Omega$

- (1) Applies to external inputs and bidirectional buffers
 (2) Applies to GRST#
 (3) Applies to pins with internal pullups/pulldowns.
 (4) Applies to external input buffers

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Power-on timings.					
t_{su_io}	Setup for MISC inputs. ⁽¹⁾ Sampled at the deassertion of GRSTz	0.1			μs
t_{hd_io}	Hold for MISC inputs. ⁽¹⁾ Sampled at the deassertion of GRSTz	0.1			μs
$t_{VDD33_RAM P}$	V_{DD33} supply ramp requirement.	0.2		100	ms

- (1) MISC pins sampled at deassertion of GRST#: BATEN[4:1]

6 Detailed Description

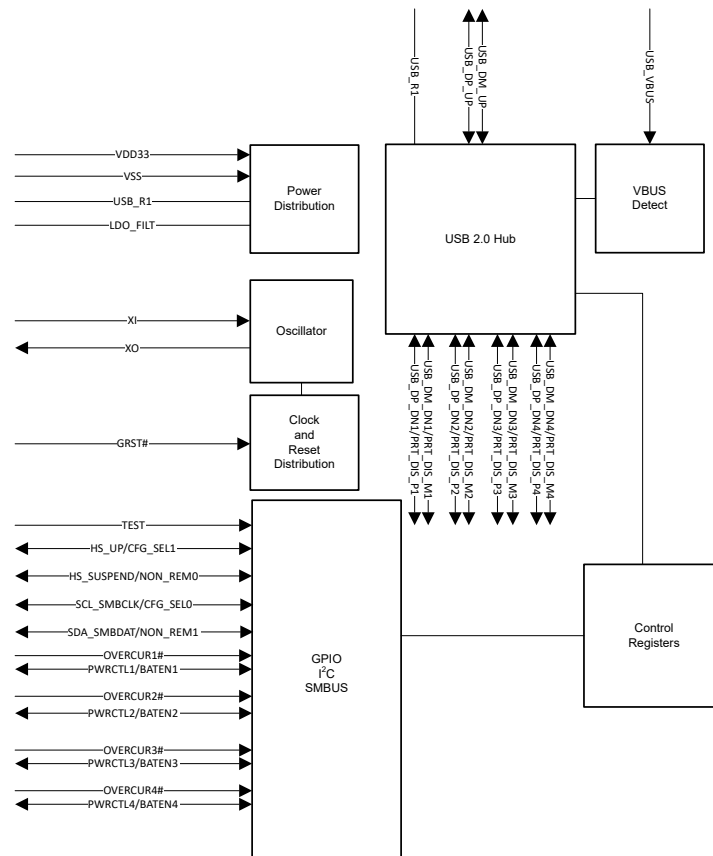
6.1 Overview

The TUSB2514B is a four-port USB 2.0 hub compliant with the USB Specification Rev. 2.0. The upstream port supports Hi-Speed (480Mbps) and Full-Speed (12Mbps) operation. The four downstream ports support Hi-Speed, Full-Speed, and Low-Speed (1.5Mbps) connections. When the upstream port connects at Hi-Speed, all downstream ports operate at full Hi-Speed capability. When the upstream port is limited to Full-Speed or lower, Hi-Speed connectivity on the downstream ports is automatically disabled.

The device includes a Multi Transaction Translator (MTT), allowing each downstream port to manage transactions independently. All four downstream ports comply with the USB Battery Charging Specification Rev. 1.2, supporting both Charging Downstream Port (CDP) and Dedicated Charging Port (DCP) modes.

The TUSB2514B supports four operating modes selected at reset: pin-strap, SMBus target, bus-powered pin-strap, and I²C EEPROM controller. A hardware-based state machine with no external microcontroller eliminates firmware injection risks. For details on each mode, see [Section 6.4](#).

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Battery Charging Features

The TUSB2514B provides support for USB Battery Charging (BC1.2) and custom divider-mode charging. Battery charging support can be enabled on a per port basis through the Battery Charging Support Register or the BATENn pins.

USB Battery charging support includes both Charging Downstream Port (CDP) and Dedicated Charging Port (DCP) modes. The DCP mode is compliant with the Chinese Telecommunications Industry Standard YD/T 1591-2009. CDP is enabled when the upstream port has detected valid VBUS, configured, and host sets port power. When the upstream port is not connected and battery charging support is enabled, the TUSB2514B enables DCP mode once all other battery modes such as ACPx have failed or are disabled.

In addition to USB Battery charging (BC1.2), the TUSB2514B supports custom charging indications: Divider Charging (ACP3, ACP2, ACP1 modes), and Galaxy compatible charging. These custom charging modes are only supported when upstream port is unconnected and Automode is enabled. The divided mode places a fixed DC voltage on the port's DP and DM signals which allows devices to identify the capabilities of the charger. Automode, and other battery charging features, can be enabled or disabled as shown in [Table 6-1](#) with detailed descriptions of each register in [Section 7](#).

Table 6-1. Battery Charging Settings

Enable bits	Default Value	Register	Bit Field(s)
Battery Charging	X (pin-strap)	Battery Charging Support Register	bcSupDsn
Automode	0 (enabled)	Configuration Register 2	autoModeEnz
Full automode	0 (disabled)	Configuration Register 3	FullAutoEn
ACP3 (high current) mode	0 (disabled)	Configuration Register 2	HiCurAcpModeEn
Galaxy mode	0 (enabled)	Configuration Register 3	Galaxy_Enz

Refer to [Figure 6-1](#) to determine the sequence of attempted battery charging modes. When the upstream port is not connected and battery charging support is enabled for a port, the TUSB2514B drives the port power enable active.

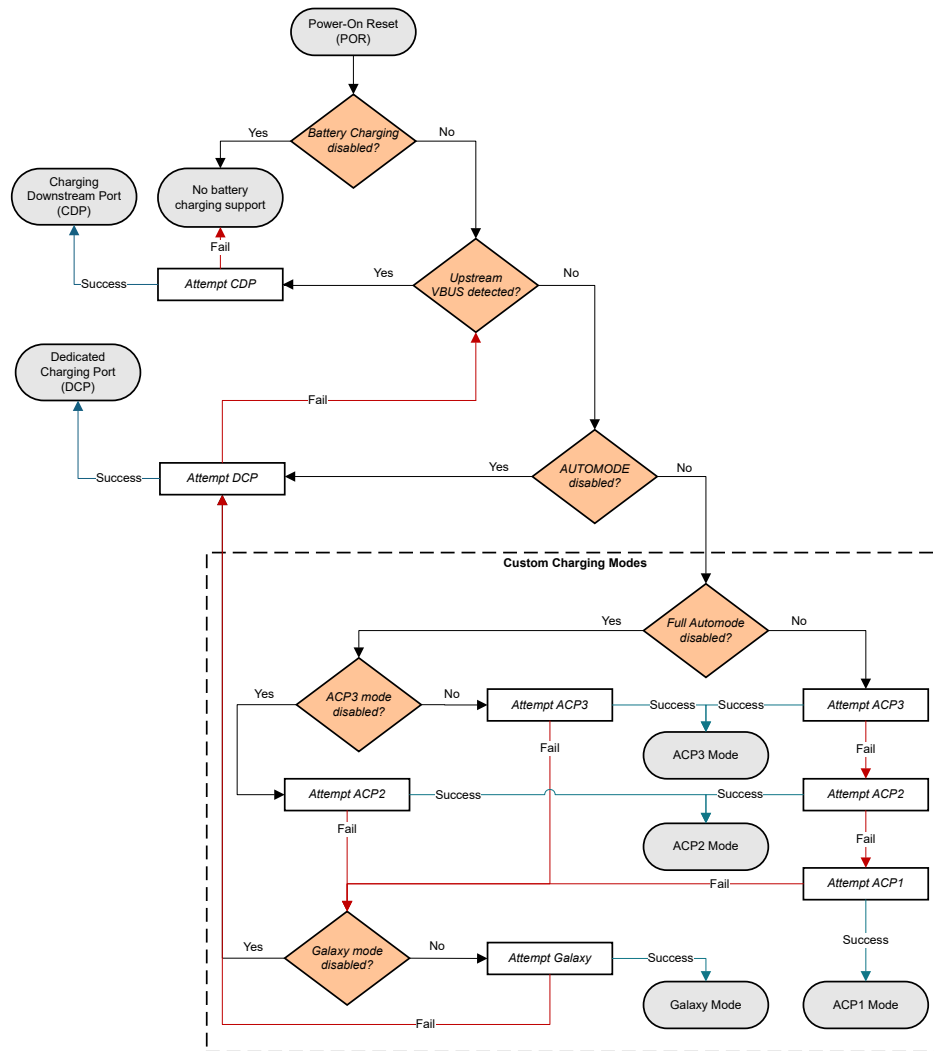


Figure 6-1. Battery Charging Diagram

If AUTOMODE is enabled, then the TUSB2514B remains in highest ACP current mode enabled as long as a pullup is not detected on DP pin. If a pullup is detected on DP pin, then TUSB2514B drives the port power enable inactive and switches to Galaxy mode, if enabled, or to DCP mode if Galaxy mode is disabled. The TUSB2514B again drives the port power enable active. The TUSB2514B remains in Galaxy mode as long as no pullup is detected on DP pin.

If a pullup is detected on the DP pin when in Galaxy mode, then TUSB2514B drives the port power enable inactive and transitions to DCP mode. The TUSB2514B again drives the port power enable active. In DCP mode, the TUSB2514B looks for a pullup detected on DP pin or RxVdat. If a pullup or RxVdat is detected on DP, the TUSB2514B remains in DCP mode. If no pullup or RxVdat is detected on DP pin after 2 seconds, the TUSB2514B drives the port power enable inactive and transitions back to ACPx mode. This sequence repeats until upstream port is connected.

6.3.2 USB Power Management

The TUSB2514B can be configured for power-switched applications using either per-port (full power managed) or ganged power-enable controls and overcurrent status inputs. When battery charging is enabled, the device always operates in full power managed mode.

Power switch support is enabled via Configuration Register 1 (fullPwrMgmtz), and the per-port or ganged mode is selected using Configuration Register 1 (ganged).

The TUSB2514B supports both active-high and active-low power-on controls. The output polarity of the PWRCTL_n pins is configured through Configuration Register 2 (pwrctlPol).

The TUSB2514B also features an overcurrent detection circuit, which protects from device damage due to electrical overstress that can occur from VBUS being shorted to the D+ or D- pins. When power switch support is set to per-port, this turns off VBUS to the individual downstream ports by asserting PWRCTL output to a connected VBUS power switch. The TUSB2514B also updates its internal USB Port Status register to reflect the overcurrent event, which is detected by the USB host. When power switch support is set to ganged mode, VBUS to all downstream ports will be disabled simultaneously. The timing of these events can be modified through the Additional Feature Configuration register (pwrnTime).

6.3.3 Clock Generation

The TUSB2514B accepts a 24MHz crystal input or an external clock source to drive an internal oscillator. If a clock is provided to XI instead of a crystal, XO is left open. Otherwise, if a crystal is used, the connection must follow the guidelines below. The XI and XO are coupled to other leads and supplies on the PCB. Keep the XI and XO as short as possible and away from any switching leads. TI also recommends minimizing the capacitance between XI and XO by shielding CL1 and CL2 with the clean ground lines.

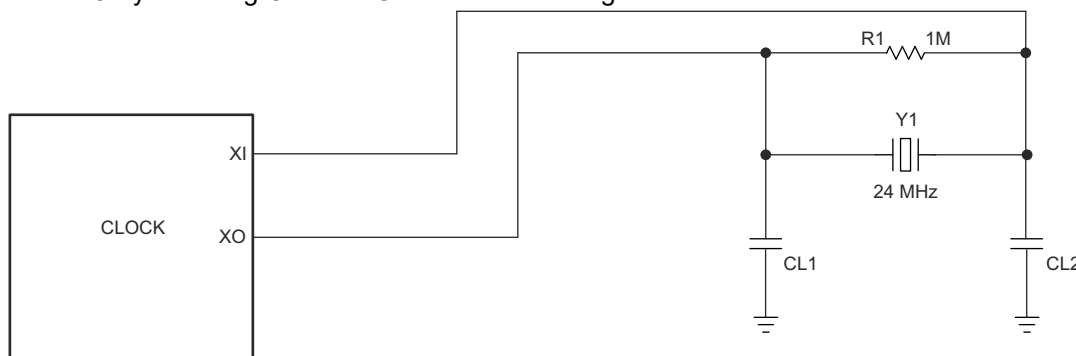


Figure 6-2. TUSB2514B Crystal Oscillator Circuit

6.3.3.1 Crystal Requirements

The crystal must be fundamental mode with a load capacitance of 12pF to 24pF and frequency stability rating of ± 100 PPM or better. To ensure proper start-up oscillation conditions, TI recommends a maximum crystal equivalent series resistance (ESR) of 50 Ω . If a crystal source is used, use a parallel load capacitor. The exact load capacitance value used depends on the crystal vendor. Refer to the [Selection and Specification for Crystals for Texas Instruments USB 2.0 Devices](#) for details on how to determine the load capacitance value.

6.3.3.2 Input Clock Requirements

When using an external clock source such as an oscillator, make sure the reference clock has ± 100 PPM or better frequency stability, less than 50ps absolute peak-to-peak jitter, and less than 25ps peak-to-peak jitter. TI recommends to tie XI to the 1.8V clock source and to leave the XO unconnected.

6.3.4 Power-Up and Reset

The TUSB2514B does not have specific power sequencing requirements as long as GRST# is held in an asserted state while the VDD33 supply ramps.

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered up must be limited to 100 hours over the projected life-time of the device.
- Bus contention while VDD33 is powered down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. The supply bus is powered down when the voltage is below that range, either stable or in transition.

A minimum reset duration of 3ms is required. This is defined as the time when the power supplies are in the recommended operating range to the deassertion of GRST#. This can be generated using programmable-delay supervisory device or using an RC circuit. When a RC circuit is used, the external capacitor size chosen must be large enough to meet the 3ms minimum duration requirement. The R of the RC circuit is the internal R_{PU} .

6.4 Device Functional Modes

The mode of the device is determined by the state of the SCL_SMBCLK/CFG0 and HS_UP/CFG1 pins upon deassertion of GRST# as shown in [Table 6-2](#).

Table 6-2. Operating Mode Selection

HS_UP/CFG1	SCL_SMBCLK/CFG0	Description
0	0	Pin-strap mode - Individual power switching - Individual overcurrent sensing - HS_UP is asserted high when the upstream USB port is connected at high-speed.
0	1	SMBus target mode - Registers are loaded by external SMBus controller - The TUSB2514B uses 7-bit target address 0x44 - HS_UP is asserted high when the upstream USB port is connected at high-speed.
1	0	Bus-powered pin strap mode - Bus-powered through VBUS - Individual power switching - Individual overcurrent sensing - HS_UP is asserted low when the upstream USB port is connected at high-speed.
1	1	I²C controller mode - All registers are configured by reading external I²C EEPROM - External I²C EEPROM 7-bit target address is 0x50 - HS_UP is asserted low when the upstream USB port is connected at high-speed.

6.4.1 I²C EEPROM Operation

The TUSB2514B supports a single-controller, standard mode (100kHz) or fast mode (400kHz) connection to a dedicated I²C EEPROM when the I²C interface mode is enabled. In I²C mode, the TUSB2514B reads the contents of the EEPROM at bus address 50h using 7-bit addressing starting at offset 00h. The TUSB2514B reads the entire EEPROM contents using a single burst read transaction. The burst read transaction ends when the address reaches FFh.

If the value of the EEPROM contents at address byte 00h equals 55h, the TUSB2514B loads the configuration registers according to the EEPROM map. If the first byte is not 55h, the TUSB2514B exits the I²C mode and continues execution with the default values in the configuration registers. The hub does not connect on the upstream port until the configuration is completed.

The internal configuration registers are accessed on byte boundaries. The configuration register values are loaded with defaults, but can be overwritten when the TUSB2514B device is in I²C or SMBus mode. The minimum size I²C EEPROM required is 2Kbit.

Table 6-3. EEPROM Memory Map

BYTE ADDRESS	CONTENTS	EEPROM CONFIGURABLE
00h	ROM Signature Register	No
01h	Vendor ID LSB	Yes
02h	Vendor ID MSB	Yes
03h	Product ID LSB	Yes
04h	Product ID MSB	Yes
05h	Device Configuration Register	Yes
06h	Battery Charging Support Register	Yes
07h	Device Removable Configuration Register	Yes
08h	Port Used Configuration Register	Yes
09h	Reserved	Yes, program to 00h
0Ah	Device Configuration Register 2	Yes
0Bh	USB 2.0 Port Polarity Control Register	Yes
0Ch to 0Fh	Reserved	No
10h to 1Fh	UUID Byte [15:0]	No
20h to 21h	LangID Byte [1:0]	Yes, if customStrings is set
22h	Serial Number String Length	Yes, if customSerNum is set
23h	Manufacturer String Length	Yes, if customStrings is set
24h	Product String Length	Yes, if customStrings is set
25h	Device Configuration Register 3	Yes
26h to 2Fh	Reserved	No
30h to 4Fh	Serial Number String Byte [31:0]	Yes, if customSerNum is set
50h to 8Fh	Manufacturer String Byte [63:0]	Yes, if customStrings is set
90h to CFh	Product String Byte [63:0]	Yes, if customStrings is set
D0 to DFh	Reserved	No
F0h	Additional Feature Configuration Register	Yes
F1 to F7h	Reserved	No
F8h	Device Status and Command Register	No
F9 to FFh	Reserved	No

Note

The bytes located above offset Ah are optional. The requirement for data in those addresses is dependent on the options configured in the Configuration 1 and Configuration 2 registers.

For details on I²C operation refer to the UM10204 I²C-bus Specification and User Manual.

6.4.2 SMBus Target Operation

When the SMBus interface mode is enabled, the TUSB2514B supports read block and write block protocols as a target-only SMBus device. The TUSB2514B 7-bit target address is 44h. The full 8-bit address is 0b1000100x, where the upper 7 bits form the 7-bit address (44h), and the LSB "x" is the read (1) or write (0) bit.

If the TUSB2514B is addressed by a host using an unsupported protocol, the device does not respond. The TUSB2514B waits indefinitely for configuration by the SMBus host and does not connect on the upstream port until the SMBus host indicates configuration is complete by clearing the cfgActive bit in the SMBus Device Status and Command Register shown in [Section 7](#). The order of operations are as follows:

1. Hub enters SMBus mode and sets cfgActive
2. SMBus host writes configuration registers

3. SMBus host clears cfgActive
4. Hub connects on the upstream port

For details on SMBus requirements, refer to the System Management Bus Specification.

6.4.3 Port Configuration

The TUSB2514B port configurations can be selected by registers. The Port Used Configuration Register defines how many ports can be reported by the hub. Ports may be disabled by pulling the DP/PRT_DIS_Pn and DM/PRT_DIS_Mn high and are sampled upon the deassertion of GRST#.

The TUSB2514B downstream ports can also be configured for either removable or non-removable based on the sampled state of the NON_REMn pins. HS_SUSPEND/NON_REM0 pin can be either active low or active high output as detailed in the table below.

Table 6-4. Non-removable Configuration

NON_REM1	NON_REM0	Descriptions
0	0	All downstream ports are removable. HS_SUSPEND is active high.
0	1	Port 1 is non-removable. Remaining ports are removable. HS_SUSPEND is active low.
1	0	Ports 1 and 2 are non-removable. Remaining ports are removable. HS_SUSPEND is active high.
1	1	Ports 1, 2, and 3 are non-removable. Remaining ports are removable. HS_SUSPEND is active low.

The Device Removable Configuration Register defines if the ports that are reported as used have permanently connected devices or not.

7 Register Maps

7.1 TUSB2514 Registers

Table 7-1 lists the memory-mapped registers for the TUSB2514 registers. All register offset addresses not listed in Table 7-1 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. TUSB2514 Registers

Offset	Acronym	Register Name	Section
0h	ROM Signature		Section 7.1.1
1h	Vendor ID		Section 7.1.2
3h	Product ID		Section 7.1.3
5h	Configuration Register 1		Section 7.1.4
6h	Battery Charging Support		Section 7.1.5
7h	Device Removable Configuration		Section 7.1.6
8h	Port Used Configuration		Section 7.1.7
Ah	Configuration Register 2		Section 7.1.8
Bh	USB 2.0 Port Polarity Control		Section 7.1.9
10h	UUID		Section 7.1.10
20h	Language ID		Section 7.1.11
22h	Serial Number String Length		Section 7.1.12
23h	Manufacturer String Length		Section 7.1.13
24h	Product String Length		Section 7.1.14
25h	Configuration Register 3		Section 7.1.15
30h	Serial Number String		Section 7.1.16
50h	Manufacturer String		Section 7.1.17
90h	Product String		Section 7.1.18
F0h	Additional Feature Configuration		Section 7.1.19
F8h	SMBus Device Status and Command		Section 7.1.20

Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. TUSB2514 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R-0	Read Returns 0s
R-1	R-1	Read Returns 1s
RH	RH	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

7.1.1 ROM Signature Register (Offset = 0h) [Reset = 00h]

ROM Signature is shown in [Table 7-3](#).

Return to the [Summary Table](#).

Table 7-3. ROM Signature Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	romSig	R/W	0h	ROM Signature Register. This register is used by the TUSB2514 in I2C mode to validate the attached EEPROM has been programmed. The first byte of the EEPROM is compared to the mask 55h and if not a match, the TUSB2514 aborts the EEPROM load and executes with the register defaults.

7.1.2 Vendor ID Register (Offset = 1h) [Reset = 0451h]

Vendor ID is shown in [Table 7-4](#).

Return to the [Summary Table](#).

Table 7-4. Vendor ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	vid	R/W	451h	Vendor ID. Unique vendor ID assigned by the USB-IF in little-endian byte order. Value used for this field is the non-zero value written by EEPROM/SMBus to both PID and VID. If a zero value is written by EEPROM/ SMBus to both PID and VID, then the default value is used.

7.1.3 Product ID Register (Offset = 3h) [Reset = 6041h]

Product ID is shown in [Table 7-5](#).

Return to the [Summary Table](#).

Table 7-5. Product ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pid	R/W	6041h	Product ID LSB. Unique product ID assigned by the USB-IF in little-endian byte order. Value used for this field is the non-zero value written by EEPROM/SMBus to both PID and VID. If a zero value is written by EEPROM/ SMBus to both PID and VID, then value used for this field is the non-zero value from OTP. If a zero value is written by OTP, then value used for this field is 8442h .

7.1.4 Configuration Register 1 (Offset = 5h) [Reset = 10h]

Configuration Register 1 is shown in [Table 7-6](#).

Return to the [Summary Table](#).

Table 7-6. Configuration Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	customStrings	R/W	0h	Custom strings enable. This bit controls the ability to write to the Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers 0h = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers are read only 1h = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers may be loaded by EEPROM or written by SMBus
6	customSernum	R/W	0h	Custom serial number enable. This bit controls the ability to write to the serial number registers. . 0h = The Serial Number String Length and Serial Number String registers are read only 1h = Serial Number String Length and Serial Number String registers may be loaded by EEPROM or written by SMBus The default value of this bit is 0
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R-1	1h	Reserved
3	ganged	R/W	0h	Ganged. When the TUSB2514 is in I2C mode, the TUSB2514 loads this bit from the contents of the EEPROM. When the TUSB2514 is in SMBUS mode, the value may be over-written by an SMBus host. 0h = Each port is individually power switched and enabled by the PWRCTL/BATEN pins 1h = The power switch control for all ports is ganged and enabled by the PWRCTL/BATEN pin
2	fullPwrMgmtz	R/W	0h	Full Power Management. When the TUSB2514 is in I2C mode, the TUSB2514 loads this bit from the contents of the EEPROM. When the TUSB2514 is in SMBUS mode, the value may be over-written by an SMBus host. 0h = Port power switching status reporting is enabled 1h = Port power switching status reporting is disabled
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R-0	0h	Reserved

7.1.5 Battery Charging Support Register (Offset = 6h) [Reset = 00h]

Battery Charging Support is shown in [Table 7-7](#).

Return to the [Summary Table](#).

Table 7-7. Battery Charging Support Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R-0	0h	Reserved
3	bcSupDs4	R/W	0h	Battery Charger Support for USB downstream port 4. The bits in this field indicate whether the downstream port implements the charging port features. The default value is loaded at the de-assertion of reset with the value of PWRCTL/BATEN4. When in I2C/SMBus mode the bits in this field may be over-written by EEPROM contents or by an SMBus host. 0h = The port is not enabled for battery charging support features 1h = The port is enabled for battery charging support features
2	bcSupDs3	R/W	0h	Battery Charger Support for USB downstream port 3. The bits in this field indicate whether the downstream port implements the charging port features. The default value is loaded at the de-assertion of reset with the value of PWRCTL/BATEN3. When in I2C/SMBus mode the bits in this field may be over-written by EEPROM contents or by an SMBus host. 0h = The port is not enabled for battery charging support features 1h = The port is enabled for battery charging support features
1	bcSupDs2	R/W	0h	Battery Charger Support for USB downstream port 2. The bits in this field indicate whether the downstream port implements the charging port features. The default value is loaded at the de-assertion of reset with the value of PWRCTL/BATEN2. When in I2C/SMBus mode the bits in this field may be over-written by EEPROM contents or by an SMBus host. 0h = The port is not enabled for battery charging support features 1h = The port is enabled for battery charging support features
0	bcSupDs1	R/W	0h	Battery Charger Support for USB downstream port 1. The bits in this field indicate whether the downstream port implements the charging port features. The default value is loaded at the de-assertion of reset with the value of PWRCTL/BATEN1. When in I2C/SMBus mode the bits in this field may be over-written by EEPROM contents or by an SMBus host. 0h = The port is not enabled for battery charging support features 1h = The port is enabled for battery charging support features

7.1.6 Device Removable Configuration Register (Offset = 7h) [Reset = 0Fh]

Device Removable Configuration is shown in [Table 7-8](#).

Return to the [Summary Table](#).

Table 7-8. Device Removable Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	customRmbl	R/W	0h	Custom Removable. This bit controls selection of port removable bits, port used bits, and USB2_ONLY bits. This bit may be written simultaneously with rmb[3:0]. 0h = rmb and used bits are read only and the values are loaded from the OTP ROM 1h = rmb and used bits are read/write and can be loaded by EEPROM or written by SMBus
6-4	RESERVED	R-0	0h	Reserved
3	rmbIDs4	R/W	1h	Removable. The bits in this field indicate whether a device attached to downstream port 4 is removable or permanently attached. This field is read only unless the customRmbl bit is set to 1. Otherwise the value of this field reflects the inverted values of the OTP ROM non_rmb[3:0] field. 0h = The device attached to the port is not removable 1h = The device attached to the port is removable
2	rmbIDs3	R/W	1h	Removable. The bits in this field indicate whether a device attached to downstream port 3 is removable or permanently attached. This field is read only unless the customRmbl bit is set to 1. Otherwise the value of this field reflects the inverted values of the OTP ROM non_rmb[3:0] field. 0h = The device attached to the port is not removable 1h = The device attached to the port is removable
1	rmbIDs2	R/W	1h	Removable. The bits in this field indicate whether a device attached to downstream port 2 is removable or permanently attached. This field is read only unless the customRmbl bit is set to 1. Otherwise the value of this field reflects the inverted values of the OTP ROM non_rmb[3:0] field. 0h = The device attached to the port is not removable 1h = The device attached to the port is removable
0	rmbIDs1	R/W	1h	Removable. The bits in this field indicate whether a device attached to downstream port 1 is removable or permanently attached. This field is read only unless the customRmbl bit is set to 1. Otherwise the value of this field reflects the inverted values of the OTP ROM non_rmb[3:0] field. 0h = The device attached to the port is not removable 1h = The device attached to the port is removable

7.1.7 Port Used Configuration Register (Offset = 8h) [Reset = 0Fh]

Port Used Configuration is shown in [Table 7-9](#).

Return to the [Summary Table](#).

Table 7-9. Port Used Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	Reserved
3	usedDs4	R/W	1h	Used. The bits in this field indicate whether a port is enabled. This field is read only unless the customRmbl bit is set to 1. 0h = The port is not used or disabled 1h = The port is used or enabled
2	usedDs3	R/W	1h	Used. The bits in this field indicate whether a port is enabled. This field is read only unless the customRmbl bit is set to 1. 0h = The port is not used or disabled 1h = The port is used or enabled
1	usedDs2	R/W	1h	Used. The bits in this field indicate whether a port is enabled. This field is read only unless the customRmbl bit is set to 1. 0h = The port is not used or disabled 1h = The port is used or enabled
0	usedDs1	R/W	1h	Used. The bits in this field indicate whether a port is enabled. This field is read only unless the customRmbl bit is set to 1. 0h = The port is not used or disabled 1h = The port is used or enabled

7.1.8 Configuration Register 2 (Offset = Ah) [Reset = 20h]

Configuration Register 2 is shown in [Table 7-10](#).

Return to the [Summary Table](#).

Table 7-10. Configuration Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R-0	0h	Reserved
6	customBCfeatures	R/W	0h	Custom Battery Charging Feature Enable. This bit controls the ability to write to the battery charging feature configuration controls. This bit may be written simultaneously with HiCurAcpModeEn. 0h = The HiCurAcpModeEn is read only and the values are loaded from the OTP ROM. 1h = The HiCurAcpModeEn bit is read/write and can be loaded by EEPROM or written by SMBus.
5	pwrctlPol	R/W	1h	When the TUSB2514 is in I2C mode, the TUSB2514 loads this bit from the contents of the EEPROM. When the TUSB2514 is in SMBUS mode, the value may be over-written by an SMBus host. 0h = PWRCTL polarity is active low 1h = PWRCTL polarity is active high
4	HiCurAcpModeEn	R/W	0h	High-current ACP mode enable. This bit enables the high-current tablet charging mode when the automatic battery charging mode is enabled for downstream ports. This bit is read only unless the customBCfeatures bit is set to 1. If customBCfeatures is 0, the value of this bit reflects the value of the OTP ROM HiCurAcpModeEn bit. 0h = High current divider mode disabled . High current is ACP2(default) 1h = High current divider mode enabled. High current mode is ACP3
3-2	RESERVED	R/W	0h	Reserved
1	autoModeEnz	R/W	0h	Automatic Mode Enable. The automatic mode only applies to downstream ports with battery charging enabled when the upstream port is not connected. 0h = Automatic mode battery charging features are enabled. 1h = Automatic mode is disabled; only Battery Charging DCP and CDP mode is supported.
0	RESERVED	R-0	0h	Reserved

7.1.9 USB 2.0 Port Polarity Control Register (Offset = Bh) [Reset = 00h]

USB 2.0 Port Polarity Control is shown in [Table 7-11](#).

Return to the [Summary Table](#).

Table 7-11. USB 2.0 Port Polarity Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	customPolarity	R/W	0h	Custom USB 2.0 Polarity. This bit controls the ability to write the p[4:0]_usb2pol bits. This bit may be written simultaneously with the p[4:0]_usb2pol bits. 0h = The p[4:0]_usb2pol bits are read only and the values are loaded from the OTP ROM. 1h = The p[4:0]_usb2pol bits are read/write and can be loaded by EEPROM or written by SMBus.
6-5	RESERVED	R-0	0h	Reserved
4	p4_usb2pol	R/W	0h	Downstream Port 4 DM/DP Polarity. This controls the polarity of the port. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p4_usb2pol bit. 0h = USB 2.0 port polarity is as documented by the pin out 1h = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM.
3	p3_usb2pol	R/W	0h	Downstream Port 3 DM/DP Polarity. This controls the polarity of the port. . This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p3_usb2pol bit. 0h = USB 2.0 port polarity is as documented by the pin out 1h = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM.
2	p2_usb2pol	R/W	0h	Downstream Port 2 DM/DP Polarity. This controls the polarity of the port. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p2_usb2pol bit. 0h = USB 2.0 port polarity is as documented by the pin out 1h = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM.
1	p1_usb2pol	R/W	0h	Downstream Port 1 DM/DP Polarity. This controls the polarity of the port. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p1_usb2pol bit. 0h = USB 2.0 port polarity is as documented by the pin out 1h = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM.
0	p0_usb2pol	R/W	0h	Upstream Port DM/DP Polarity. This controls the polarity of the port. This bit is read only unless the customPolarity bit is set to 1. If customPolarity is 0 the value of this bit reflects the value of the OTP ROM p0_usb2pol bit. 0h = USB 2.0 port polarity is as documented by the pin out 1h = USB 2.0 port polarity is swapped from that documented in the pin out, i.e. DM becomes DP, and DP becomes DM.

7.1.10 UUID Register (Offset = 10h) [Reset = 000000000000000000000000000000h]

UUID is shown in [Table 7-12](#).

Return to the [Summary Table](#).

Table 7-12. UUID Register Field Descriptions

Bit	Field	Type	Reset	Description
127-0	uuid	R	0h	UUID byte N. The UUID returned in the Container ID descriptor. The value of this register is provided by the device and is meets the UUID requirements of Internet Engineering Task Force (IETF) RFC 4122 A UUID URN Namespace.

7.1.11 Language ID Register (Offset = 20h) [Reset = 0409h]

Language ID is shown in [Table 7-13](#).

Return to the [Summary Table](#).

Table 7-13. Language ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	langid	R/W	409h	Language ID least significant byte. This register contains the value returned in the LANGID code in string index 0. The TUSB2514 only supports one language ID. The default value of this register is 0409h in little-endian byte order. 0409h represents the LangID indicating English (United States). When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host.

7.1.12 Serial Number String Length Register (Offset = 22h) [Reset = 18h]

Serial Number String Length is shown in [Table 7-14](#).

Return to the [Summary Table](#).

Table 7-14. Serial Number String Length Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R-0	0h	Reserved
6-0	serNumStringLen	R/W	18h	Serial number string length. The string length in bytes for the serial number string. The default value is 18h indicating that a 24 byte serial number string is supported. The maximum string length is 32 bytes. When customSernum is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a serial number string of serNumbStringLen bytes is returned at string index 1 from the data contained in the Serial Number String registers.

7.1.13 Manufacturer String Length Register (Offset = 23h) [Reset = 00h]

Manufacturer String Length is shown in [Table 7-15](#).

Return to the [Summary Table](#).

Table 7-15. Manufacturer String Length Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R-0	0h	Reserved
6-0	mfgStringLen	R/W	0h	Manufacturer string length. The string length in bytes for the manufacturer string. The default value is 0, indicating that a manufacturer string is not provided. The maximum string length is 64 bytes. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a manufacturer string of mfgStringLen bytes is returned at string index 3 from the data contained in the Manufacturer String registers.

7.1.14 Product String Length Register (Offset = 24h) [Reset = 00h]

Product String Length is shown in [Table 7-16](#).

Return to the [Summary Table](#).

Table 7-16. Product String Length Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R-0	0h	Reserved
6-0	prodStringLen	R/W	0h	Product string length. The string length in bytes for the product string. The default value is 0, indicating that a product string is not provided. The maximum string length is 64 bytes. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a product string of prodStringLen bytes is returned at string index 3 from the data contained in the Product String registers.

7.1.15 Configuration Register 3 (Offset = 25h) [Reset = 10h]

Configuration Register 3 is shown in [Table 7-17](#).

Return to the [Summary Table](#).

Table 7-17. Configuration Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R-0	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	1h	Reserved
3	USB2_DFP_UNCONF	R/W	0h	This field when set enables USB 2.0-defined Unconfigured state on DFPs.
2	I2C_100k	R/W	0h	I2C 100kHz. This bit controls the clock rate of the I2C master for both USB to I2C requests. The EEPROM reads occurs at 400K unless eFuse is used to set the rate to 100k. This bit is read/write but the read value returned is the Boolean OR of this bit and the corresponding eFuse bit. If either bit is set, this feature is enabled.
1	Galaxy_Enz	R/W	0h	Disable Galaxy compatible modes. When this field is high, Galaxy charging compatible mode does not included in AUTOMODE charger sequence. This bit is read/write but the read value returned is the Boolean OR of this bit and the corresponding eFuse bit. If either bit is set, this feature is disabled.
0	FullAutoEn	R/W	0h	Enable all divider battery charging modes. When automode is enabled and this bit is set, any DS port enabled for battery charging attempts all divider battery charging modes before DCP, starting with the highest current option. The bit is writable, but the value read back is the Boolean OR of this bit and the corresponding eFuse control. If either bit is set, eFuse or this register, this feature is enabled.

**7.1.16 Serial Number String Register (Offset = 30h) [Reset =
 XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXh]**

Serial Number String is shown in [Table 7-18](#).

Return to the [Summary Table](#).

Table 7-18. Serial Number String Register Field Descriptions

Bit	Field	Type	Reset	Description
255-0	serialNumber	R/W	X	Serial Number. The serial number returned in the Serial Number string descriptor at string index 1. The default value of these registers is assigned by TI. When customSernum is 1, these registers may be over-written by EEPROM contents or by an SMBus host.

7.1.17 Manufacturer String Register (Offset = 50h) [Reset =

[illegible]

Manufacturer String is shown in [Table 7-19](#).

Return to the [Summary Table](#).

Table 7-19. Manufacturer String Register Field Descriptions

Bit	Field	Type	Reset	Description
511-0	mfgString	R/W	0h	Manufacturer. These registers provide the string values returned for string index 3 when mfgStringLen is greater than 0. The number of bytes returned in the string is equal to mfgStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

7.1.18 Product String Register (Offset = 90h) [Reset =

[illegible]

Product String is shown in [Table 7-20](#).

Return to the [Summary Table](#).

Table 7-20. Product String Register Field Descriptions

Bit	Field	Type	Reset	Description
511-0	prodString	R/W	0h	Product string. These registers provide the string values returned for string index 2 when prodStringLen is greater than 0. The number of bytes returned in the string is equal to prodStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

7.1.19 Additional Feature Configuration Register (Offset = F0h) [Reset = 00h]

Additional Feature Configuration is shown in [Table 7-21](#).

Return to the [Summary Table](#).

Table 7-21. Additional Feature Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6-5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3-1	pwrnTime	R/W	0h	Power On Delay Time. When the efuse_pwrnTime field is all 0s, this field sets the delay time from the removal disable of PWRCTL to the enable of PWRCTL when transitioning battery charging modes. For example, when disabling the power on a transition from ACP to DCP Mode. This field may be over-written by EEPROM contents or by an SMBus host. 0h = 0ms 1h = 200ms 2h = 400ms 3h = 600ms 4h = 800ms 5h = 1000ms 6h = 1200ms 7h = 1400ms
0	RESERVED	R/W	0h	Reserved

7.1.20 SMBus Device Status and Command Register (Offset = F8h) [Reset = 00h]

SMBus Device Status and Command is shown in [Table 7-22](#).

Return to the [Summary Table](#).

Table 7-22. SMBus Device Status and Command Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	rsvd15	R/W	0h	Reserved. Read only, returns 0 when read.
1	smbusRst	RH/W1S	0h	SMBus interface reset. This bit loads the registers back to their GRST# values. Note, that since this bit can only be set when in SMBus mode the cfgActive bit is also reset to 1. When software sets this bit it must reconfigure the registers as necessary. This bit is set by writing a 1 and is cleared by hardware on completion of the reset. A write of 0 has no effect.
0	cfgActive	R/W1S	0h	Configuration active. This bit indicates that configuration of the TUSB2514 is currently active. The bit is set by hardware when the device enters the I2C or SMBus mode. The TUSB2514 shall not connect on the upstream port while this bit is 1. When in I2C mode, the bit is cleared by hardware when the TUSB2514 exits the I2C mode. When in the SMBus mode, this bit must be cleared by the SMBus host in order to exit the configuration mode and allow the upstream port to connect. The bit is cleared by a writing 1. A write of 0 has no effect.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TUSB2514B device is a four-port USB 2.0 hub. The TUSB2514B provides USB high-speed and full-speed connections on the upstream port and provides USB high-speed, full-speed, or low-speed connections on the downstream port. The TUSB2514B device can be used in any application that requires additional USB-compliant ports. For example, a notebook may only have two USB ports available for USB devices. By connecting the upstream USB port of the TUSB2514B device, the total number of available downstream USB ports on the notebook can be increased to five.

8.2 Typical Application

A common application for the TUSB2514B device is as a self-powered standalone USB-hub product. The product is powered by an external 3.3V DC power supply. In this application the upstream port of the TUSB2514B device is plugged into a USB host controller. The downstream ports of the TUSB2514B device are exposed to users for connecting USB peripherals, such as hard drives, cameras, flash drives, and so forth.

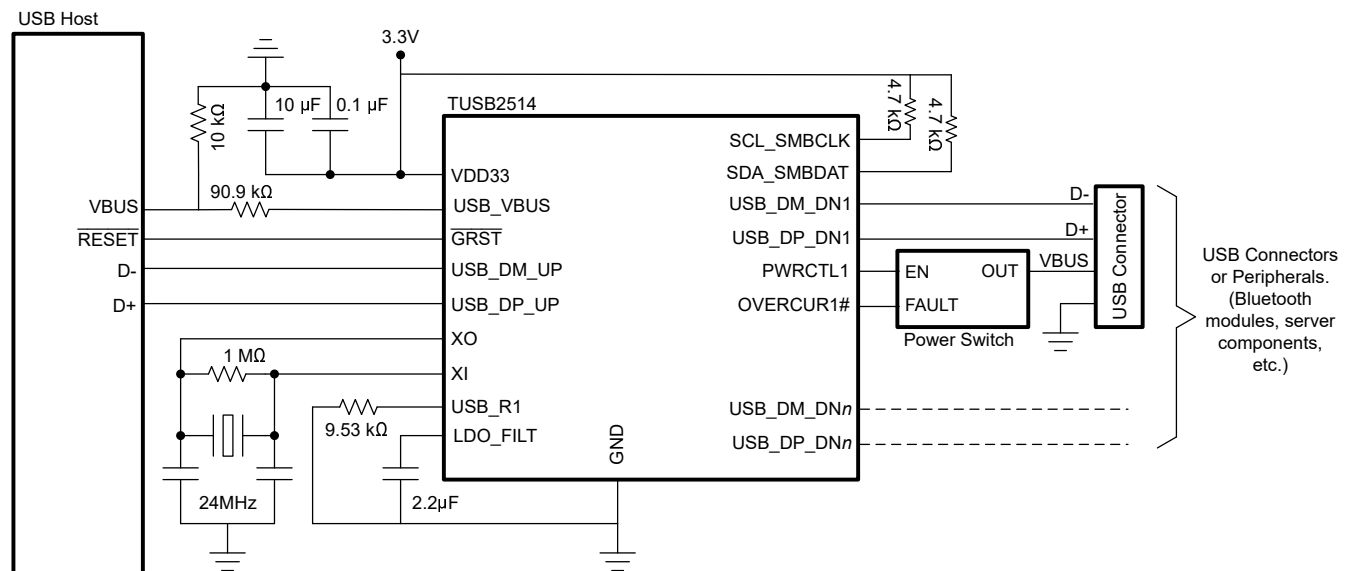


Figure 8-1. Typical Use Case

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 8-1](#).

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD33 supply	3.3V
Upstream port USB support (HS, FS)	HS, FS
Downstream port 1 USB support (HS, FS, LS)	HS, FS, LS
Downstream port 2 USB support (HS, FS, LS)	HS, FS, LS
Downstream port 3 USB support (HS, FS, LS)	HS, FS, LS
Downstream port 4 USB support (HS, FS, LS)	HS, FS, LS
Number of removable downstream ports	4
Number of non-removable downstream ports	0
Full power management of downstream ports	Yes (FULLPWRMGMTZ = 0)
Individual control of downstream port power switch	Yes (GANGED = 0)
Power switch enable polarity	Active high (PWRCTL_POL = 1)
Battery charge support for downstream port 1	Yes
Battery charge support for downstream port 2	Yes
Battery charge support for downstream port 3	Yes
Battery charge support for downstream port 4	Yes
I ² C EEPROM support	No
24MHz clock source	Crystal

8.2.2 Application Curves

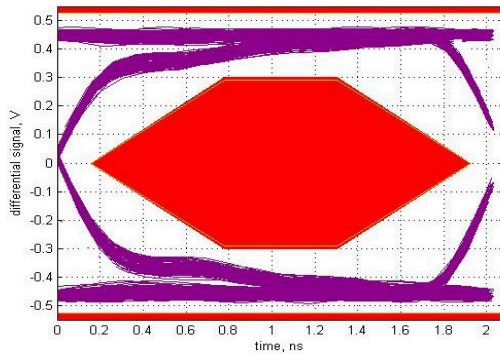


Figure 8-2. High-Speed Upstream Port

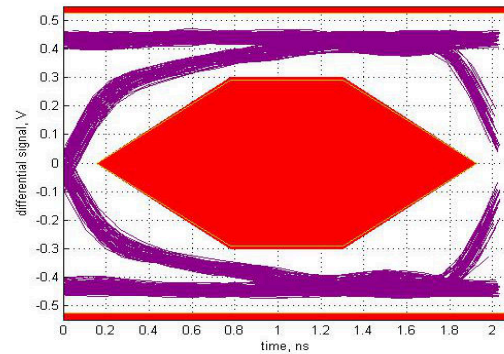


Figure 8-3. High-Speed Downstream Port 1

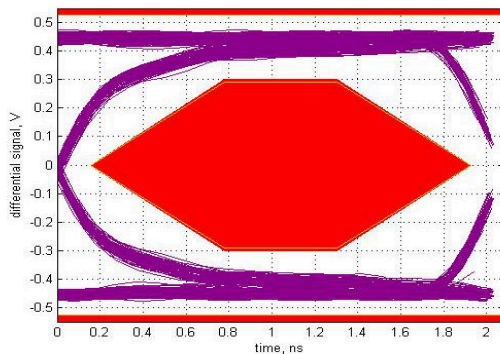


Figure 8-4. High-Speed Downstream Port 2

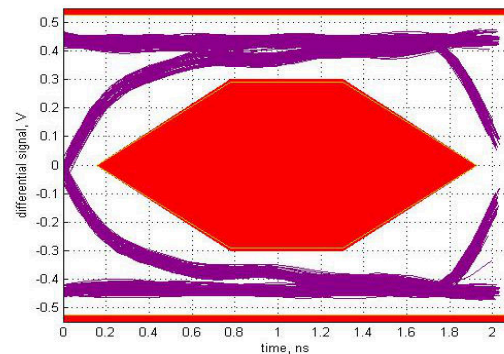


Figure 8-5. High-Speed Downstream Port 3

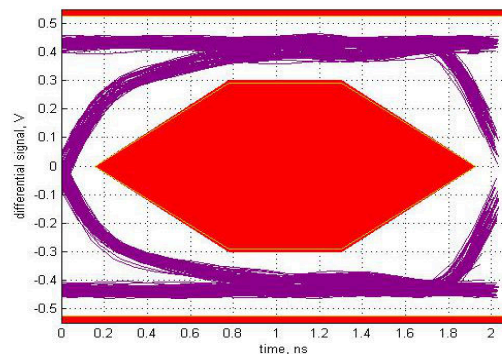


Figure 8-6. High-Speed Downstream Port 4

8.3 Power Supply Recommendations

8.3.1 TUSB2514B Power Supply

Implement V_{DD33} as a single power plane.

- The V_{DD33} pins of the TUSB2514B device supply 3.3V power rail to the I/O of the TUSB2514B device. This power rail can be isolated from other power rails by a ferrite bead to reduce noise.
- All power rails require a 10 μ F capacitor or 1 μ F capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. Place the smaller decoupling capacitors as close to the TUSB2514B power pins as possible with an appropriate grouping of two capacitors of differing values per pin.

8.3.2 Downstream Port Power

- A source capable of supplying 5V and up to 500mA per port must supply the downstream port power, VBUS. The TUSB2514B signals can control the downstream port power switches. Leaving the downstream port power as always enabled is also possible.
- The VBUS of each downstream port requires a large-bulk low-ESR capacitor of 22μF or larger to limit in-rush current.
- TI recommends the ferrite beads on the VBUS pins of the downstream USB port connections for both ESD and EMI reasons. A 0.1μF capacitor on the USB connector side of the ferrite provides a low-impedance path to ground for fast rise time ESD current that might have coupled onto the VBUS trace from the cable.

8.3.3 Ground

TI recommends to use only one board ground plane in the design which provides the best image plane for signal traces running above the plane. Connect the thermal pad of the TUSB2514B and any of the voltage regulators to this plane with vias. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

8.4 Layout

8.4.1 Layout Guidelines

Use the layout guidelines listed in this section for proper PCB layout design.

8.4.1.1 Placement

- Place a 9.53-kΩ ±1% resistor connected to pin USB_R1 as close as possible to the TUSB2514B device.
- Place a 0.1-μF capacitor as close as possible on each V_{DD} and VDD33 power pin.
- Place the ESD and EMI protection devices (if used) as close as possible to the USB connector.
- If a crystal is used, place the crystal as close as possible to the XI and XO pins of the TUSB2514B device.
- Place voltage regulators as far away as possible from the TUSB2514B device, the crystal, and the differential pairs.
- In general, place the large bulk capacitors associated with each power rail as close as possible to the voltage regulators.

8.4.1.2 Package Specific

- The TUSB2514B device package has a 0.5mm pin pitch.
- The TUSB2514B device package has a thermal pad. This thermal pad must be connected to ground through a system of vias.
- Solder mask all vias under device, except for those connected to the thermal pad, to avoid any potential issues with thermal pad layouts.

8.4.1.3 Differential Pairs

This section describes the layout recommendations for all the TUSB2514B device differential pairs: USB_DP_XX, USB_DM_XX.

- The differential pairs must be designed with a differential impedance of 90 Ω ± 10%.
- To minimize crosstalk, TI recommends to keep high-speed signals away from each other. Separate each pair by at least 5 times the signal trace width. Separating with ground as depicted in the layout example also helps minimize crosstalk.
- Route all differential pairs on the same layer adjacent to a solid ground plane.
- Do not route differential pairs over any plane split.
- Adding test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Do not place them in a manner that causes stub on the differential pair.
- Avoid 90° turns in trace. Keep the use of bends in differential traces to a minimum. When bends are used, make sure the number of left and right bends are as equal as possible and that the angle of the bend is ≥135°. This guideline minimizes any length mismatch caused by the bends and therefore minimize the impact bends have on EMI.

- Minimize the trace lengths of the differential pair traces. Eight inches is the maximum recommended trace length for USB 2.0 differential pair signals. Longer trace lengths require very careful routing to ensure proper signal integrity.
- Match the etch lengths of the differential pair traces (that is DP and DM). Make sure the USB 2.0 differential pairs do not exceed 50 mils relative trace length difference.
- Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Place any vias used as close as possible to the TUSB2514B device.
- To ease routing of the USB 2.0 DP and DM pair, the polarity of these pins can be swapped. If this is done, set the appropriate Px_usb2pol register, where x = 0, 1, 2, 3, or 4.
- Do not place power fuses across the differential pair traces.

8.4.2 Layout Example

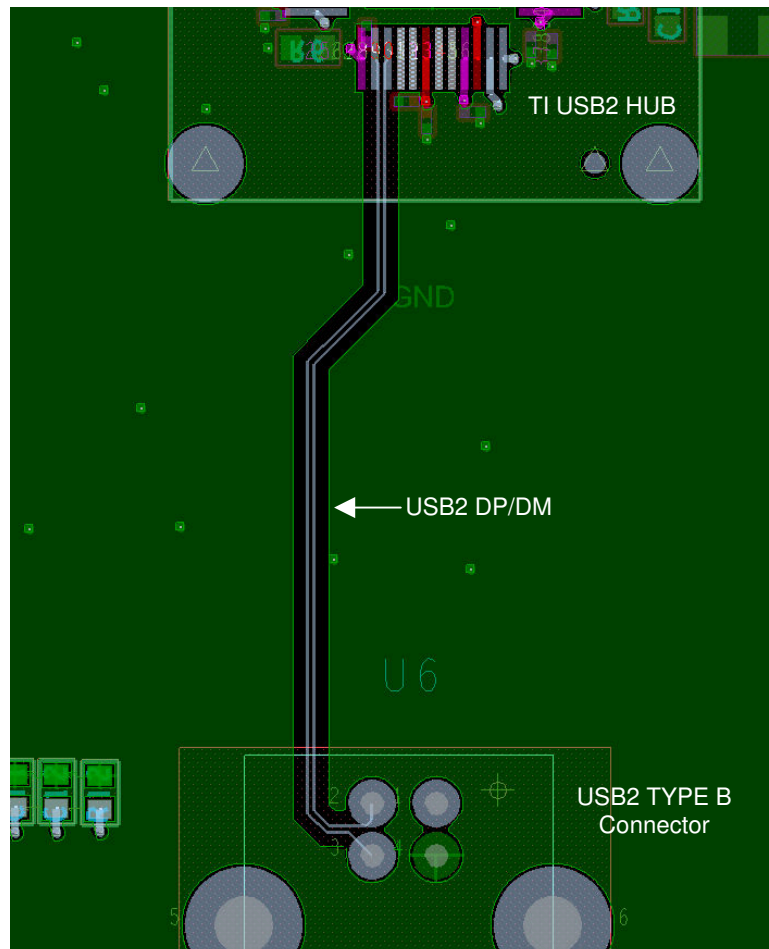


Figure 8-7. Example Routing of Upstream Port

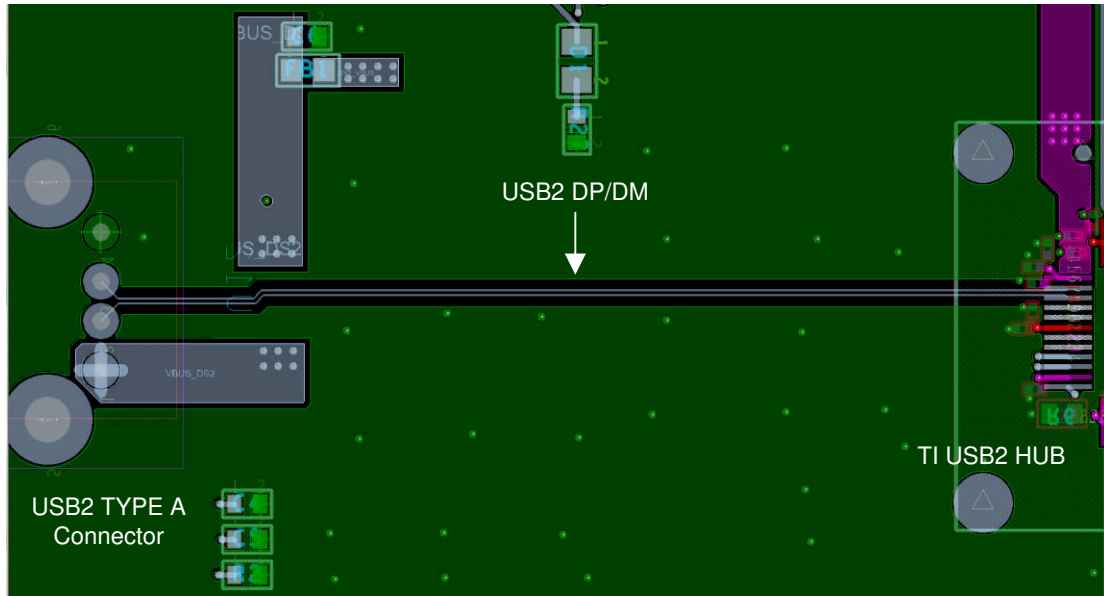


Figure 8-8. Example Routing of Downstream Port

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices application note](#)
- Texas Instruments, [TPS2561 Dual-Channel Precision Adjustable Current-limited Power Switches data sheet](#)
- UM10204 I²C-bus Specification and User Manual

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTUSB2514BRHHR	Active	Preproduction	VQFN (RHH) 36	4000 LARGE T&R	-	Call TI	Call TI	-40 to 85	

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

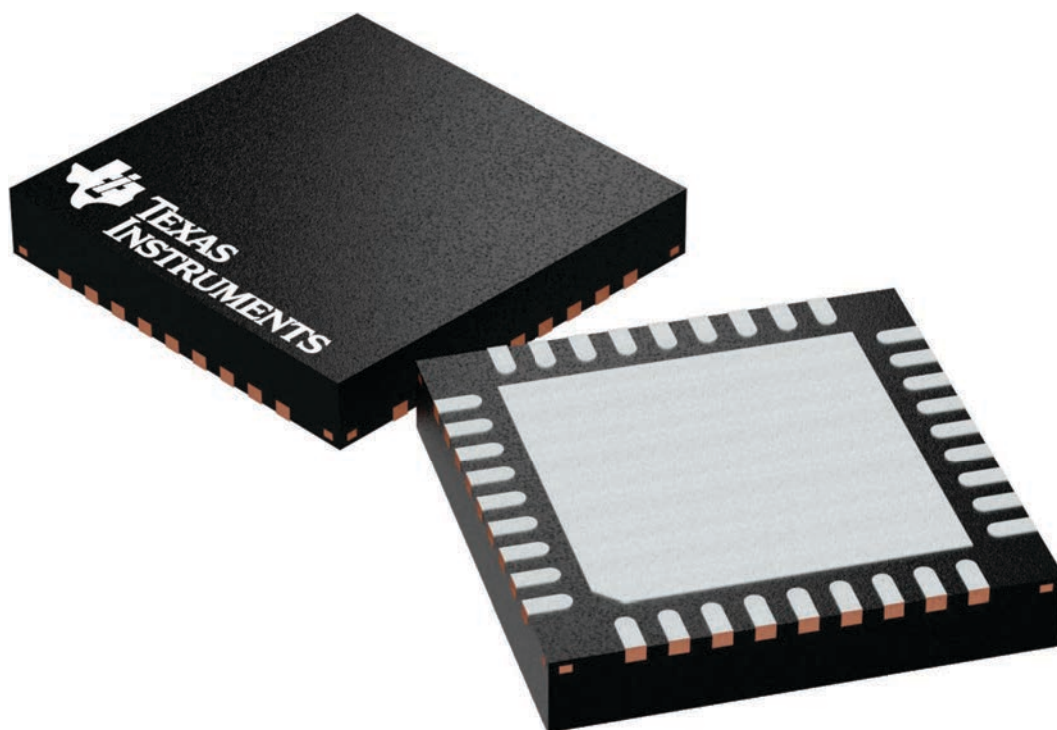
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225440/A

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