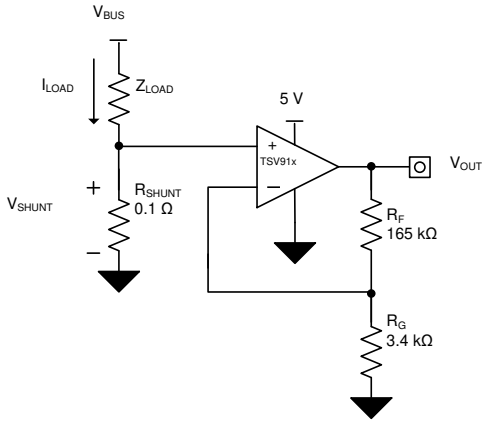
TSV91xA-Q1 Automotive Rail-to-Rail Input or Output, 8-MHz Operational Amplifiers

1 Features

- Rail-to-rail input and output
- Low noise: 18 nV/√Hz at 1 kHz
- Low power consumption: 550 µA (typical)
- High-gain bandwidth: 8 MHz
- Operating supply voltage from 2.5 V to 5.5 V
- Low input bias current: 1 pA (typical)
- Low input offset voltage: 1.5 mV (maximum)
- Low offset voltage drift: ±0.5 µV/°C (typical)
- ESD internal protection: ±4-kV human-body model (HBM)
- Extended temperature range: –40°C to 125°C

2 Applications

- Optimized for AEC-Q100 grade 1 applications
- Infotainment and cluster
- Passive safety
- Body electronics and lighting
- HEV/EV inverter and motor control
- On-board (OBC) and wireless charger
- Powertrain current sensor
- Advanced driver assistance systems (ADAS)
- Single-supply, low-side, unidirectional current-sensing circuit



Low-Side Motor Control

3 Description

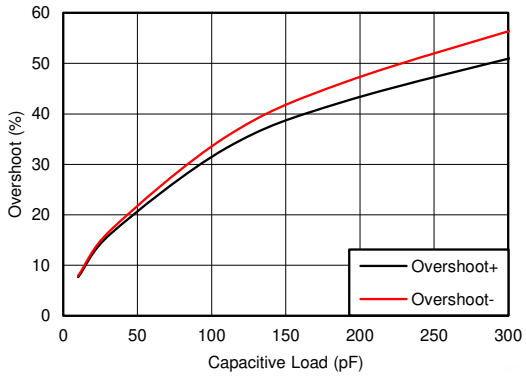
The TSV91xA-Q1 family, which includes single-, dual-, and quad-channel operational amplifiers (op amps), is specifically designed for general-purpose automotive applications. Featuring rail-to-rail input and output (RRIO) swings, wide bandwidth (8 MHz), and low offset voltage (0.3 mV, typical), this family is designed for a variety of applications that require a good balance between speed and power consumption. The op amps are unity-gain stable and feature an ultra-low input bias current, which enables the family to be used in applications with high-source impedance. The low input bias current allows the devices to be used for sensor interfaces, and active filtering.

The robust design of the TSV91xA-Q1 provides ease-of-use to the circuit designer. Features include a unity-gain stable, integrated RFI-EMI rejection filter, no phase reversal in overdrive condition, and high electrostatic discharge (ESD) protection (4-kV HBM).

Device Information

PART NUMBER(1)	CHANNEL COUNT(2)	PACKAGE(1)	PACKAGE SIZE(3)
TSV911A-Q1	Single	DBV (SOT-23, 5)	2.90 mm × 2.80 mm
		DCK (SC70, 5)	2.0 mm × 2.20 mm
TSV912A-Q1	Dual	D (SOIC, 8)	4.90 mm × 6.00 mm
		DGK (VSSOP, 8)	3.00 mm × 4.90 mm
		PW (TSSOP, 8)	3.00 mm × 6.40 mm
TSV914A-Q1	Quad	D (SOIC, 14)	8.65 mm × 6.00 mm
		PW (TSSOP, 14)	5.00 mm × 6.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) See the *Device Comparison* table
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Small-Signal Overshoot vs Load Capacitance

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2021) to Revision C (June 2023)	Page
• Added the SC70 package and 8-pin TSSOP package in *Device Information* table	1
• Removed the preview tag for the SOT-23 package in *Device Information* table	1
• Updated the format of the *Device Information* to include package leads and channel count	1
• Updated the *Device Comparison* table to include newer packages	3
• Added pinout drawings for TSV911A-Q1 in the *Pin Configurations and Functions* section	4
• Added the *Thermal Information: TSV911A-Q1* section	8
• Changed input offset voltage at room temperature from ±1.5 mV to ±1.85 mV in *Electrical Characteristics*	9
• Deleted the *Packages With an Exposed Thermal Pad* section	18

Changes from Revision A (December 2020) to Revision B (February 2021)	Page
• Deleted preview tag from VSSOP package in *Device Information* table	1
• Updated thermal information for DGK (VSSOP) package in *Thermal Information: TSV912A-Q1* table	8

Changes from Revision * (June 2020) to Revision A (December 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Deleted preview tag from TSSOP package in *Device Information* table	1
• Deleted Package, preview note from TSV914-Q1 pinout drawing and *Pin Functions* table	4
• Added note 4 to differential input voltage in *Absolute Maximum Ratings* table	7
• Added thermal information for TSSOP (14) to *Thermal Information: TSV914A-Q1* table	8

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5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS				
		DCK	DBV	D	DGK	PW
TSV911A-Q1	1	5	5	—	—	—
TSV912A-Q1	2	—	—	8	8	8
TSV914A-Q1	4	—	—	14	—	14

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6 Pin Configuration and Functions

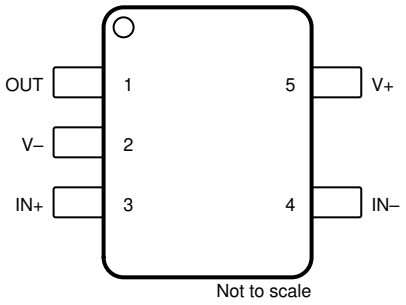


Figure 6-1. TSV911A-Q1 DBV Package, 5-Pin SOT-23 (Top View)

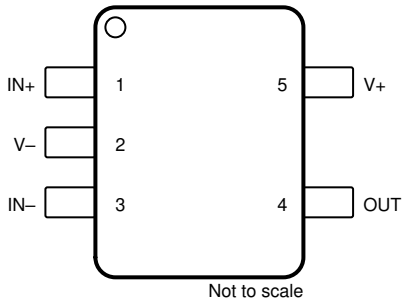


Figure 6-2. TSV911A-Q1 DCK Package, 5-Pin SC70 (Top View)

Table 6-1. Pin Functions: TSV911A-Q1

PIN			TYPE(1)	DESCRIPTION
NAME	SOT-23	SC70		
IN–	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	2	I or —	Negative (low) supply or ground (for single-supply operation)
V+	5	5	I	Positive (high) supply

(1) I = input, O = output

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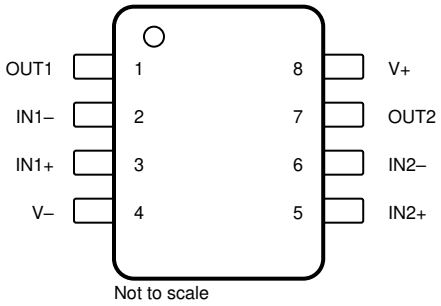


Figure 6-3. TSV912A-Q1 D, PW and DGK Packages, 8-Pin SOIC, TSSOP and VSSOP (Top View)

Table 6-2. Pin Functions: TSV912A-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

(1) I = input, O = output

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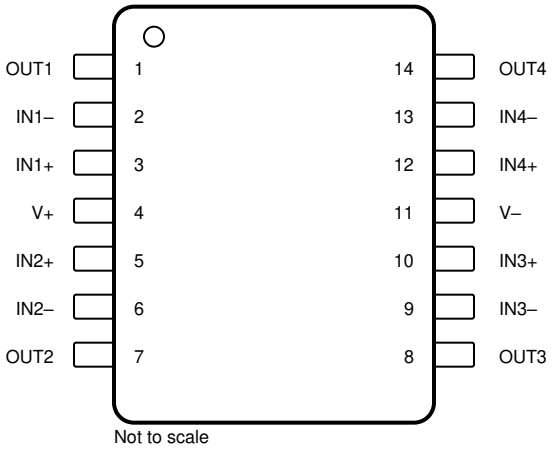


Figure 6-4. TSV914A-Q1 D and PW Packages, 14-Pin SOIC and TSSOP (Top View)

Table 6-3. Pin Functions: TSV914A-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) supply or ground (for single-supply operation)
V+	4	—	Positive (highest) supply

(1) I = input, O = output

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage				6	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential(4)		(V+) – (V–) + 0.2	
	Current(2)		–10	10	mA
Output short-circuit(3)			Continuous		mA
Specified, T_A			–40	125	°C
Junction, T_J				150	°C
Storage, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.
(4) Differential input voltages greater than 0.5 V applied continuously can result in a shift to the input offset voltage above the maximum specification of this parameter. The magnitude of this effect increases as the ambient operating temperature rises.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with ANSI/ESDA/JEDEC JS-001 Specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	2.5	5.5	V
	Specified temperature	–40	125	°C

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7.4 Thermal Information: TSV911A-Q1

THERMAL METRIC[1]		TSV911A-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	232.5	246.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	131.0	157.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.6	95.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	66.5	68.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	99.1	95.0	°C/W

7.5 Thermal Information: TSV912A-Q1

THERMAL METRIC[1]		TSV912A-Q1			UNIT
		D (SOIC)	PW (TSSOP)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.6	205.1	198.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	104.6	93.7	87.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.7	135.7	120.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	55.6	25.0	23.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	99.2	134.0	118.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: TSV914A-Q1

THERMAL METRIC[1]		TSV914A-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.1	133.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	62.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67	76.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.4	13.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	66.6	76.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.7 Electrical Characteristics

V_S (Total Supply Voltage) = (V+) – (V–) = 2.5 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.3	±1.85	mV
		V_S = 5 V T_A = –40°C to 125°C			±3	
dV_{OS}/dT	Drift	V_S = 5 V T_A = –40°C to 125°C		±0.5		µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.5 V – 5.5 V, V_{CM} = (V–)		±7		µV/V
	Channel separation, DC	At DC		100		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 2.5 V to 5.5 V	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C	80	103		dB
		V_S = 5.5 V, V_{CM} = –0.1 V to 5.6 V T_A = –40°C to 125°C	57	75		
		V_S = 2.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C		88		
		V_S = 2.5 V, V_{CM} = –0.1 V to 1.9 V T_A = –40°C to 125°C		70		
INPUT BIAS CURRENT						
I_B	Input bias current			±5		pA
I_{OS}	Input offset current			±5		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	V_S = 5 V, f = 0.1 Hz to 10 Hz		4.77		μV_{PP}
e_n	Input voltage noise density	V_S = 5 V, f = 10 kHz		12		nV/√Hz
		V_S = 5 V, f = 1 kHz		18		
i_n	Input current noise density	f = 1 kHz		23		fA/√Hz
INPUT CAPACITANCE						
C_{ID}	Differential			2		pF
C_{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 2.5 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V R_L = 10 kΩ		100		dB
		V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V R_L = 10 kΩ	104	130		
		V_S = 2.5 V, (V–) + 0.06 V < V_O < (V+) – 0.06 V R_L = 2 kΩ		100		
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V R_L = 2 kΩ		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V_S = 5 V, G = 1		8		MHz
φ_m	Phase margin	V_S = 5 V, G = 1		55		°
SR	Slew rate	V_S = 5 V, G = 1 R_L = 2 kΩ C_L = 100 pF		4.5		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = 1 C_L = 100 pF		0.5		µs
		To 0.01%, V_S = 5 V, 2-V step , G = 1 C_L = 100 pF		1		
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		0.2		µs
THD + N	Total harmonic distortion + noise(1)	V_S = 5 V, V_O = 1 V_{RMS}, G = 1, f = 1 kHz		0.0008%		

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7.7 Electrical Characteristics (continued)

V_S (Total Supply Voltage) = (V+) – (V–) = 2.5 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ			20	mV
		V_S = 5.5 V, R_L = 2 kΩ			60	
I_{SC}	Short-circuit current	V_S = 5 V		±50		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 10 MHz		100		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 mA		550	750	μA
		V_S = 5.5 V, I_O = 0 mA T_A = –40°C to 125°C			1100	

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

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7.8 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

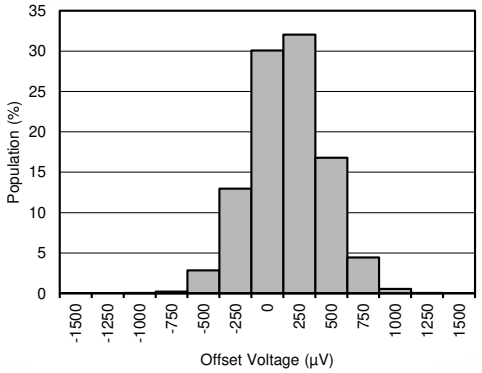
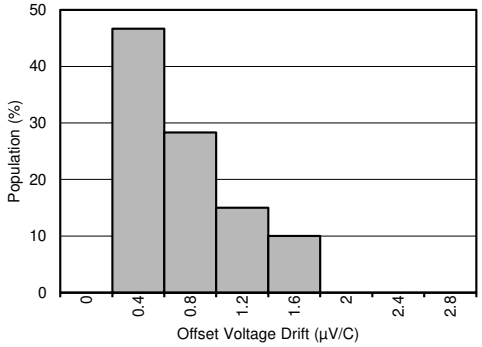


Figure 7-1. Offset Voltage Production Distribution



T_A = –40°C to 125°C

Figure 7-2. Offset Voltage Drift Distribution

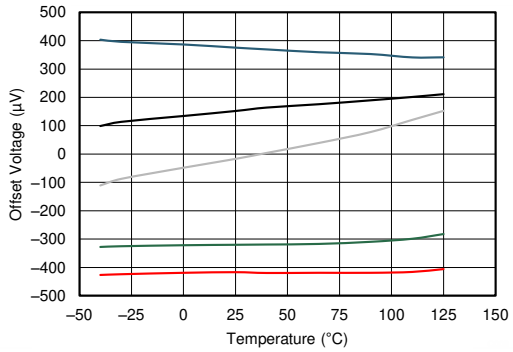
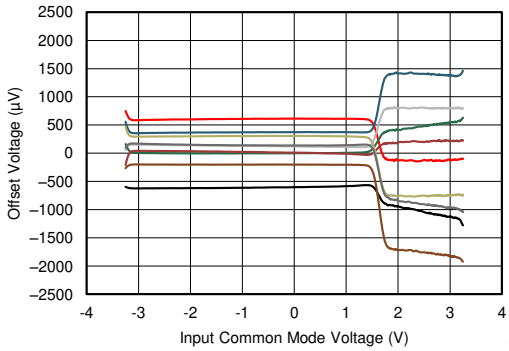
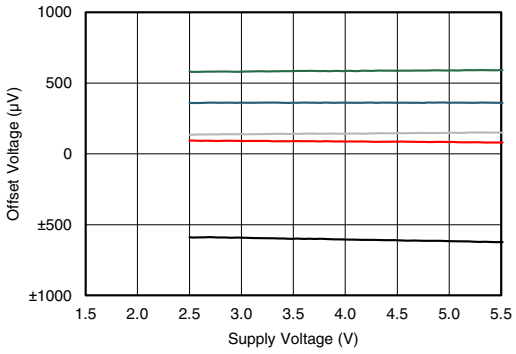


Figure 7-3. Offset Voltage vs Temperature



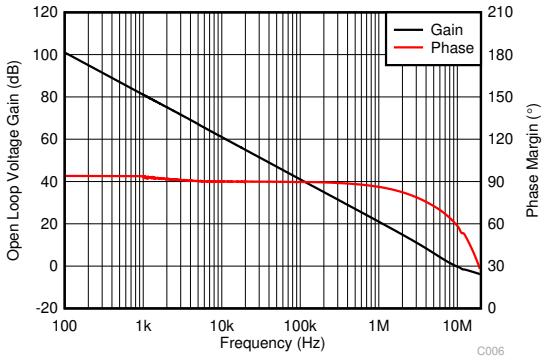
V+ = 2.75 V, V– = –2.75 V

Figure 7-4. Offset Voltage vs Common-Mode Voltage



V_S = 2.5 V to 5.5 V

Figure 7-5. Offset Voltage vs Power Supply



C_L = 10 pF

Figure 7-6. Open-Loop Gain and Phase vs Frequency

7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

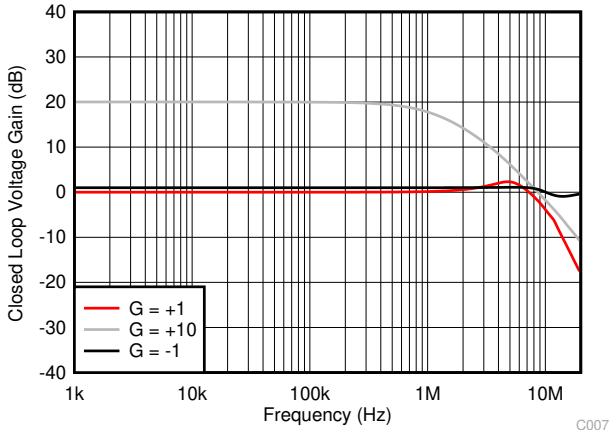


Figure 7-7. Closed-Loop Gain vs Frequency

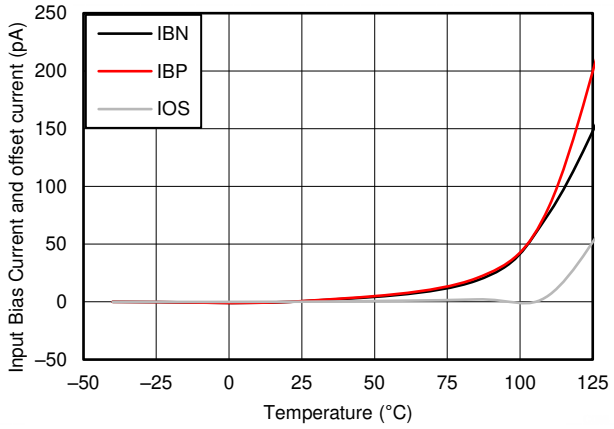
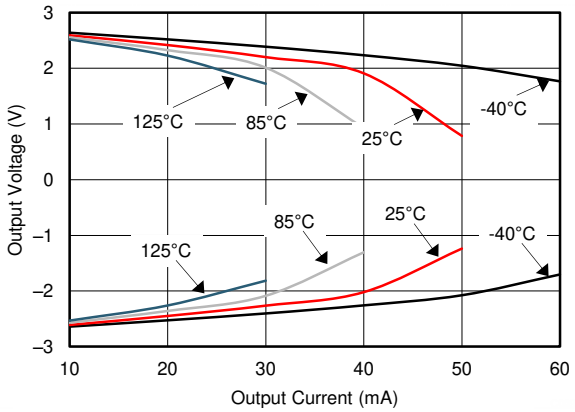


Figure 7-8. Input Bias Current vs Temperature



V+ = 2.75 V, V– = –2.75 V

Figure 7-9. Output Voltage Swing vs Output Current

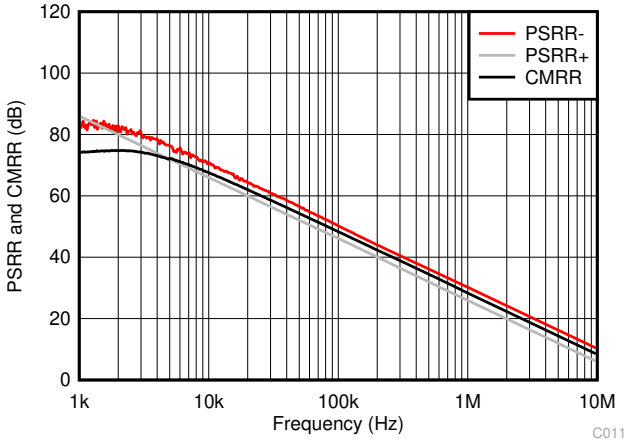
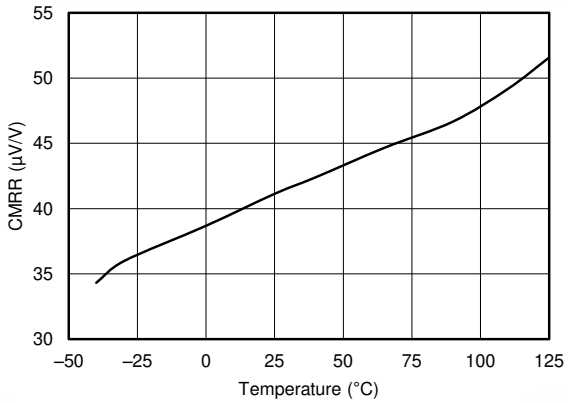


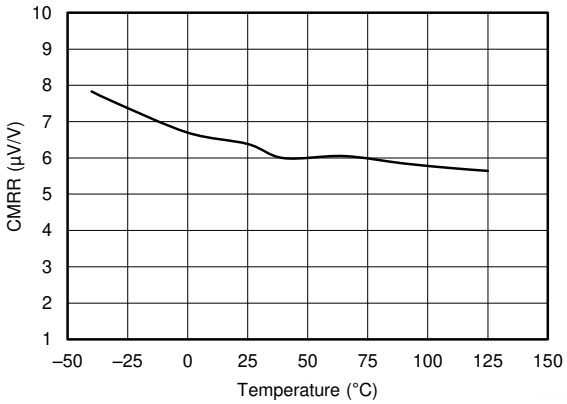
Figure 7-10. CMRR and PSRR vs Frequency (Referred to Input)



V_S = 5.5 V V_{CM} = (V–) – 0.1 V to (V+) + 0.1 V R_L = 10 kΩ

T_A = –40°C to 125°C

Figure 7-11. CMRR vs Temperature



V_S = 5.5 V V_{CM} = (V–) –0.1 V to (V+) –1.4 V R_L = 10 kΩ

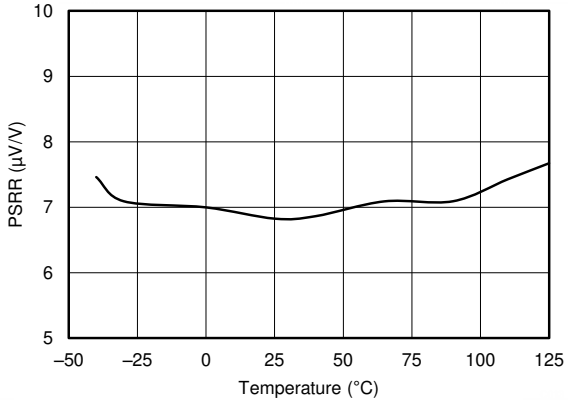
T_A = –40°C to 125°C

Figure 7-12. CMRR vs Temperature

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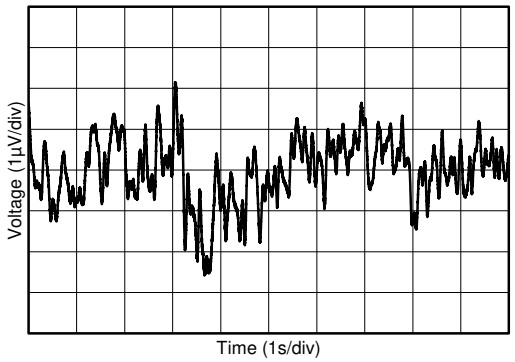
7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 2.5 V to 5.5 V

Figure 7-13. PSRR vs Temperature



V_S = 2.5 V to 5.5 V

Figure 7-14. 0.1-Hz to 10-Hz Input Voltage Noise

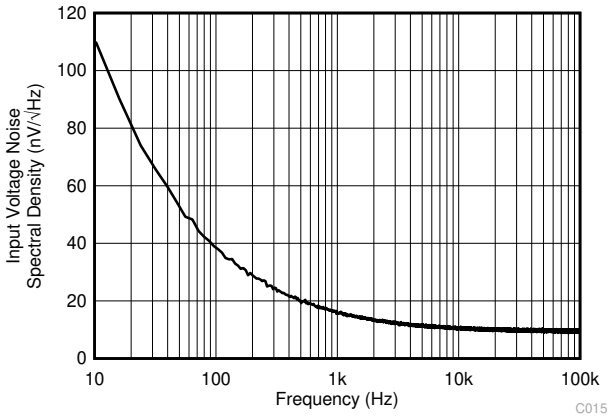
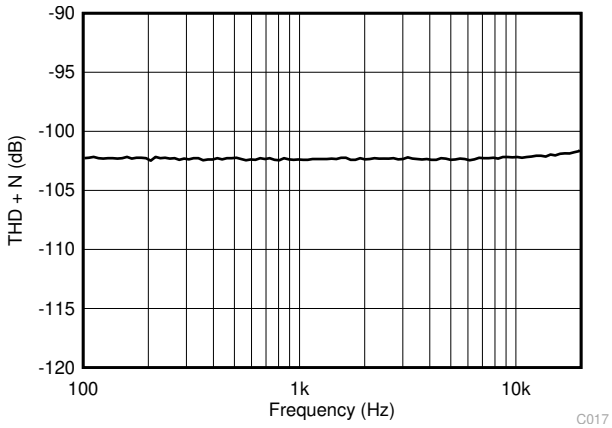
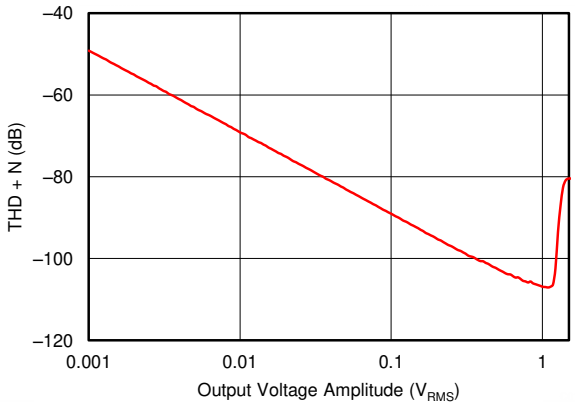


Figure 7-15. Input Voltage Noise Spectral Density vs Frequency



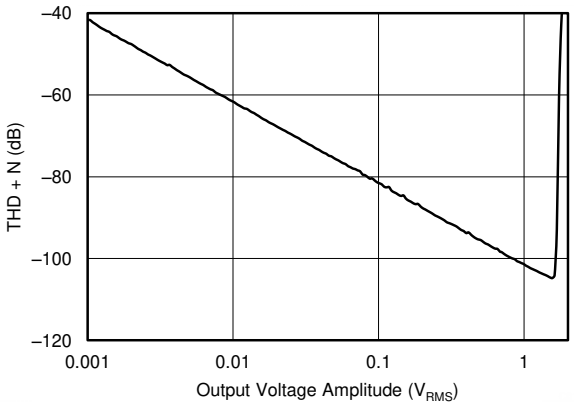
V_S = 5.5 V | V_{CM} = 2.5 V | R_L = 2 kΩ
G = 1 | V_{OUT} = 0.5 V_{RMS} | BW = 80 kHz

Figure 7-16. THD + N vs Frequency



V_S = 5.5 V | V_{CM} = 2.5 V | R_L = 2 kΩ
G = 1 | BW = 80 kHz | f = 1 kHz

Figure 7-17. THD + N vs Amplitude



V_S = 5.5 V | V_{CM} = 2.5 V | R_L = 2 kΩ
G = –1 | BW = 80 kHz | f = 1 kHz

Figure 7-18. THD + N vs Amplitude

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7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

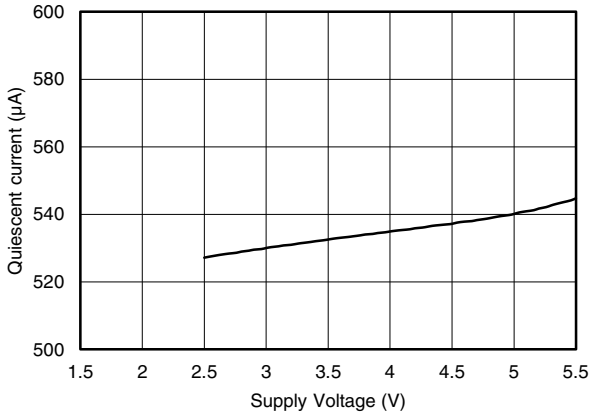


Figure 7-19. Quiescent Current vs Supply Voltage

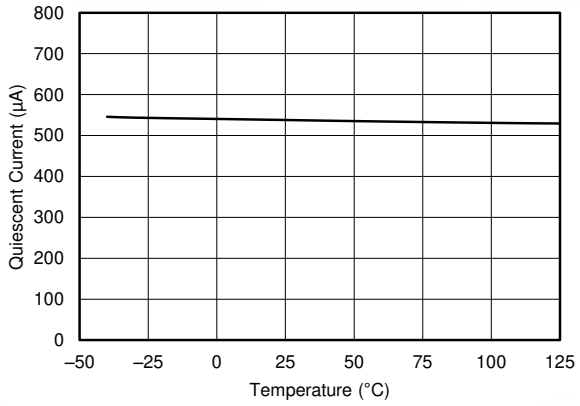


Figure 7-20. Quiescent Current vs Temperature

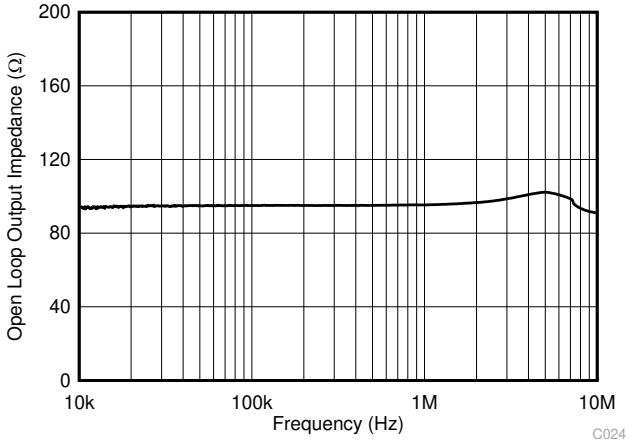
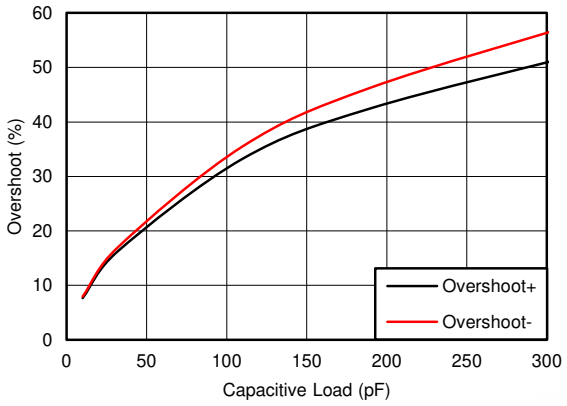
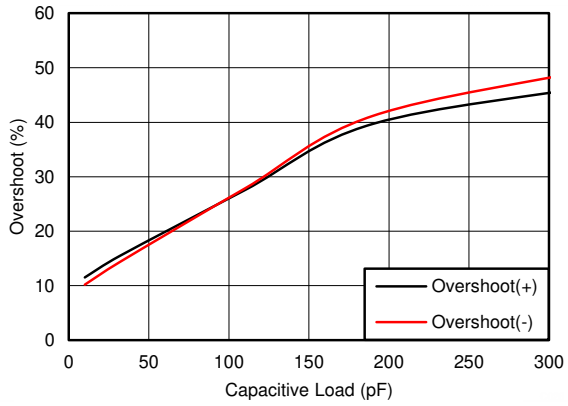


Figure 7-21. Open-Loop Output Impedance vs Frequency



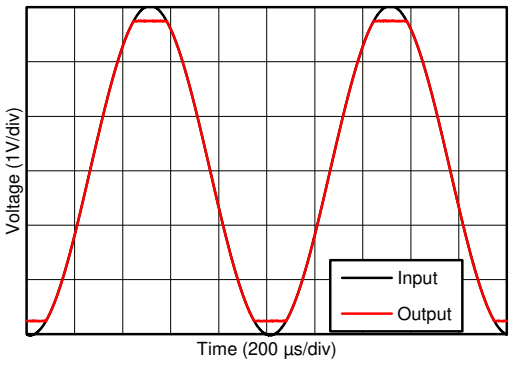
V+ = 2.75 V V– = –2.75 V G = 1 V/V
R_L = 10 kΩ V_{OUT} step = 100 mV_{p-p}

Figure 7-22. Small-Signal Overshoot vs Load Capacitance



V+ = 2.75 V V– = –2.75 V R_L = 10 kΩ
G = –1 V/V V_{OUT} step = 100 mV_{p-p}

Figure 7-23. Small-Signal Overshoot vs Load Capacitance



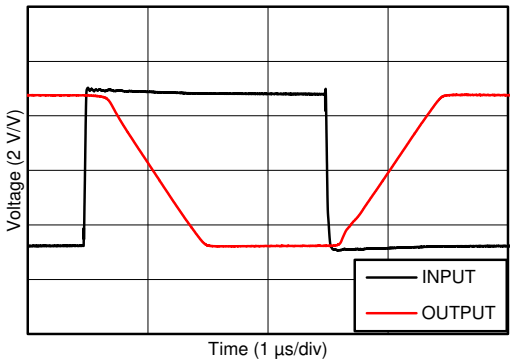
V+ = 2.75 V, V– = –2.75 V

Figure 7-24. No Phase Reversal

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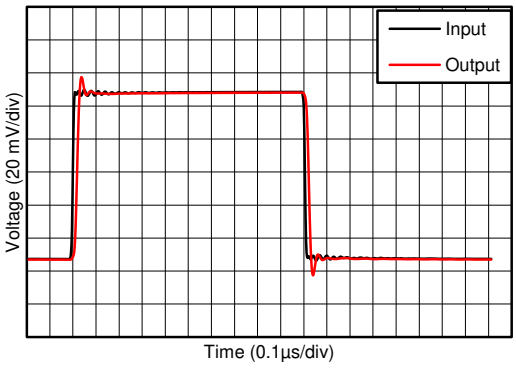
7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



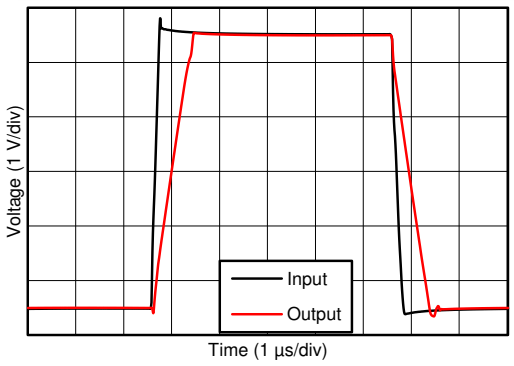
V+ = 2.75 V, V– = –2.75 V, G = –10 V/V

Figure 7-25. Overload Recovery



V+ = 2.75 V, V– = –2.75 V, G = 1 V/V

Figure 7-26. Small-Signal Step Response



V+ = 2.75 V V– = –2.75 V C_L = 100 pF
G = 1 V/V

Figure 7-27. Large-Signal Step Response

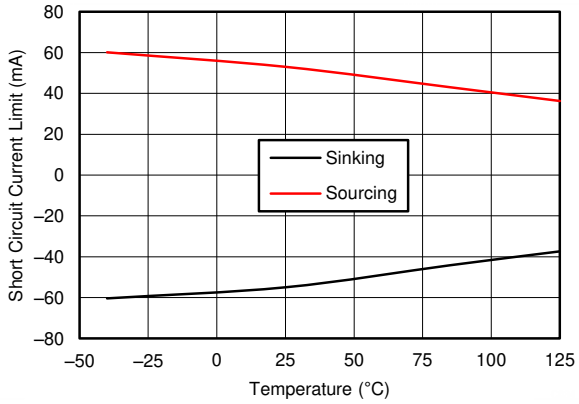
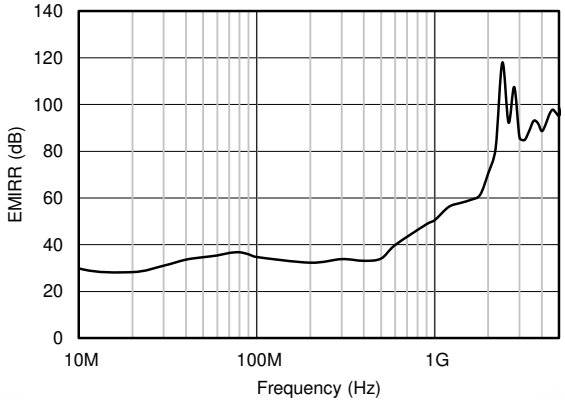
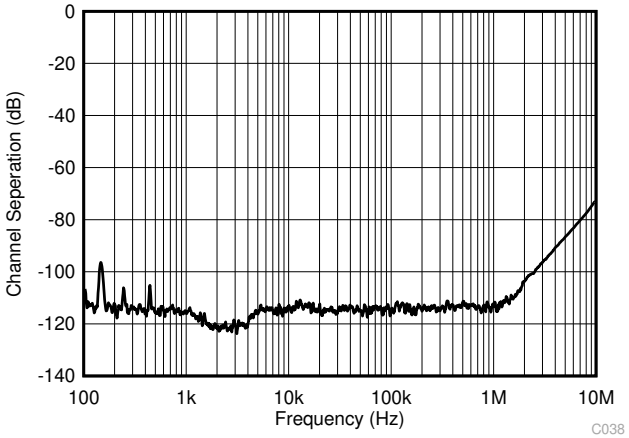


Figure 7-28. Short-Circuit Current vs Temperature



P_{RF} = –10 dBm

Figure 7-29. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



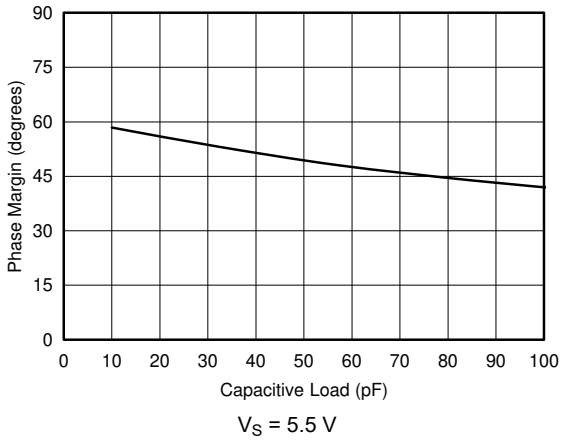
V+ = 2.75 V, V– = –2.75 V

Figure 7-30. Channel Separation vs Frequency

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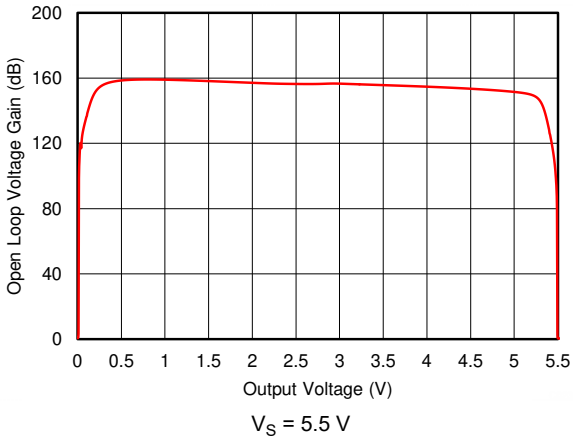
7.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5.5 V

Figure 7-31. Phase Margin vs Capacitive Load



A. V_S = 5.5 V

Figure 7-32. Open Loop Voltage Gain vs Output Voltage

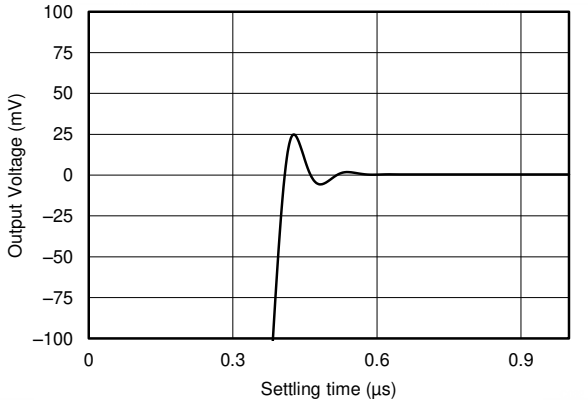


Figure 7-33. Large Signal Settling Time (Positive)

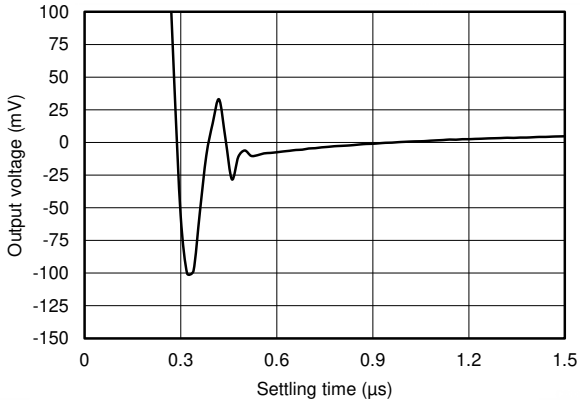


Figure 7-34. Large Signal Settling Time (Negative)

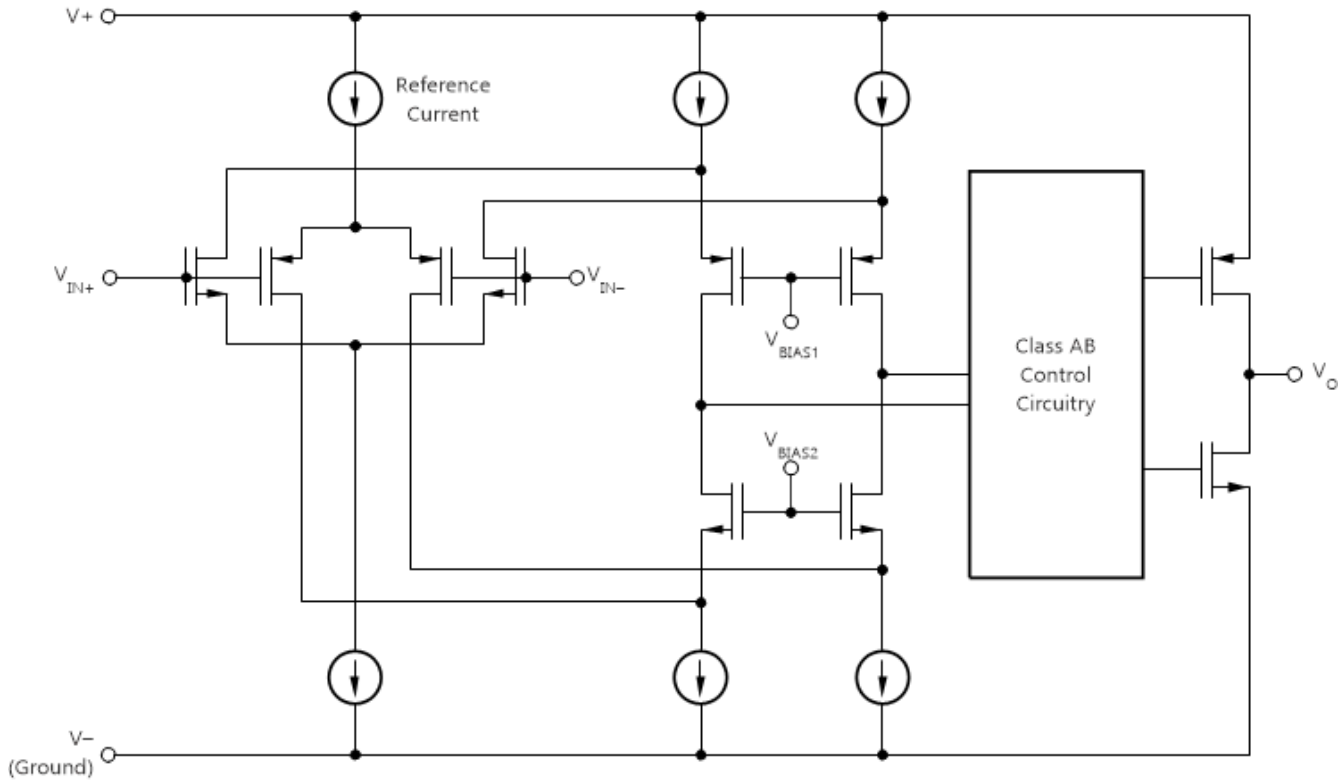
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8 Detailed Description

8.1 Overview

The TSV91xA-Q1 series is a family of low-power, rail-to-rail input and output op amps. These devices operate from 2.5 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose automotive applications. The input common-mode voltage range includes both rails and allows the TSV91xA-Q1 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications and are designed for driving sampling analog-to-digital converters (ADCs).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Rail-to-Rail Input

The input common-mode voltage range of the TSV91xA-Q1 family extends 100 mV beyond the supply rails for the full supply voltage range of 2.5 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 100 mV above the positive supply, whereas the P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

8.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TSV91xA-Q1 series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.3 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TSV91xA-Q1 series is approximately 200 ns.

8.4 Device Functional Modes

The TSV91xA-Q1 family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 2.5 V (±1.25 V) and 5.5 V (±2.75 V).

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TSV91xA-Q1 series features 8-MHz bandwidth and 4.5-V/µs slew rate with only 550 µA of supply current per channel, providing good AC performance at low power consumption. DC applications are well served with a low input noise voltage of 18 nV / √ Hz at 1 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

9.2 Typical Application

Figure 9-1 shows the TSV91xA-Q1 configured in a low-side, motor-control application.

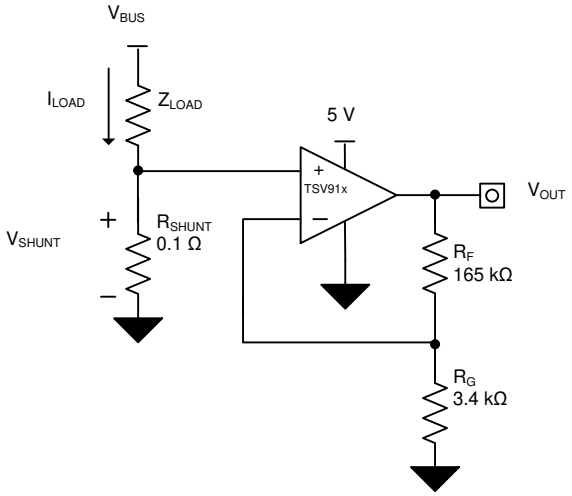


Figure 9-1. TSV91xA-Q1 in a Low-Side, Motor-Control Application

9.2.1 Design Requirements

The design requirements for this design are as follows:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

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9.2.2 Detailed Design Procedure

The transfer function of the circuit in Figure 9-1 is shown in Equation 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

Using Equation 2, R_{SHUNT} is 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TSV91xA-Q1 to produce an output voltage of approximately 0 V to 4.95 V. The gain required by the TSV91xA-Q1 to produce the necessary output voltage is calculated using Equation 3:

$$Gain = \frac{(V_{OUT_MAX} - V_{OUT_MIN})}{(V_{IN_MAX} - V_{IN_MIN})} \quad (3)$$

Using Equation 3, the required gain is calculated to be 49.5 V/V, which is set with resistors R_F and R_G. Equation 4 is used to size the resistors, R_F and R_G, to set the gain of the TSV91xA-Q1 to 49.5 V/V.

$$Gain = 1 + \left(\frac{R_F}{R_G}\right) \quad (4)$$

Selecting R_F as 165 kΩ and R_G as 3.4 kΩ provides a combination that equals roughly 49.5 V/V. Figure 9-2 shows the measured transfer function of the circuit shown in Figure 9-1.

9.2.3 Application Curve

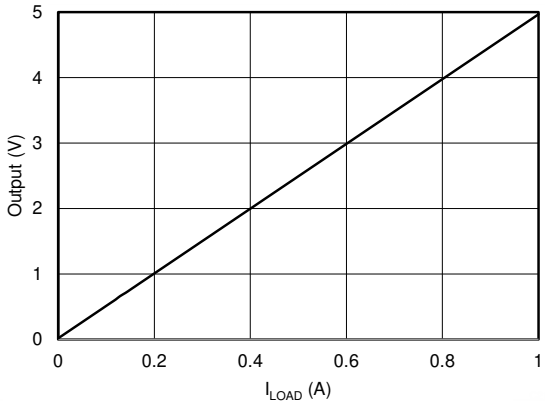


Figure 9-2. Low-Side, Current-Sense, Transfer Function

9.3 Power Supply Recommendations

The TSV91xA-Q1 series is specified for operation from 2.5 V to 5.5 V (±1.25 V to ±2.75 V); many specifications apply from –40°C to 125°C. *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

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Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Example*.

9.3.1 Input and ESD Protection

The TSV91xA-Q1 series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10-mA, as stated in the *Absolute Maximum Ratings* table. Figure 9-3 shows how a series input resistor is added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

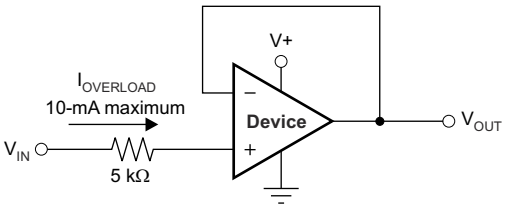


Figure 9-3. Input Current Protection

9.4 Layout

9.4.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 9-5, keeping RF and RG close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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9.4.2 Layout Example

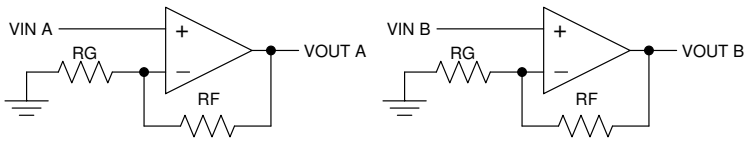


Figure 9-4. Schematic Representation of Layout Example

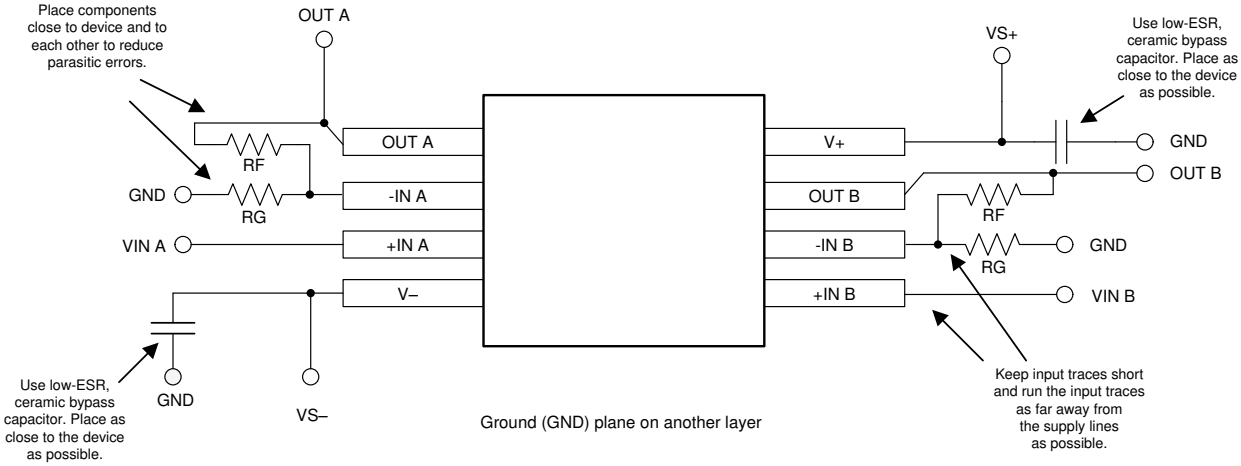


Figure 9-5. Layout Example

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10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSV911AQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1N4
TSV911AQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1N4
TSV911AQDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1N6
TSV911AQDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1N6
TSV912AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	29IT
TSV912AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	29IT
TSV912AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TS912Q
TSV912AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TS912Q
TSV912AQPWRQ1	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TSV912
TSV912AQPWRQ1.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TSV912
TSV914AQDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TSV914AQD
TSV914AQDRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TSV914AQD
TSV914AQPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	T914AQ
TSV914AQPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T914AQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

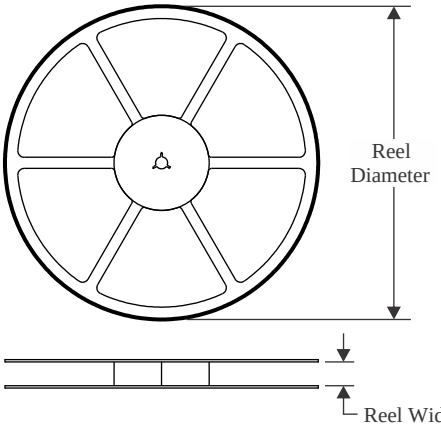
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

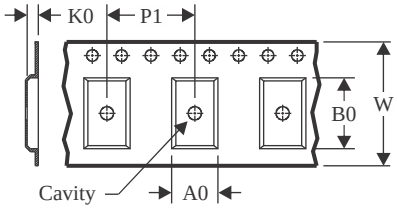
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

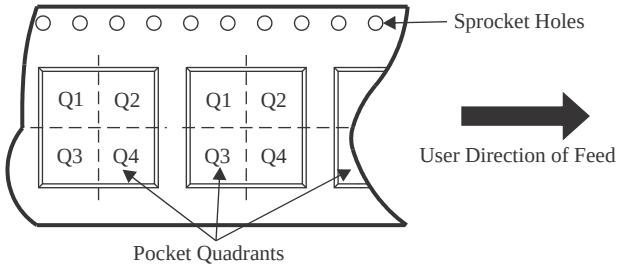


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

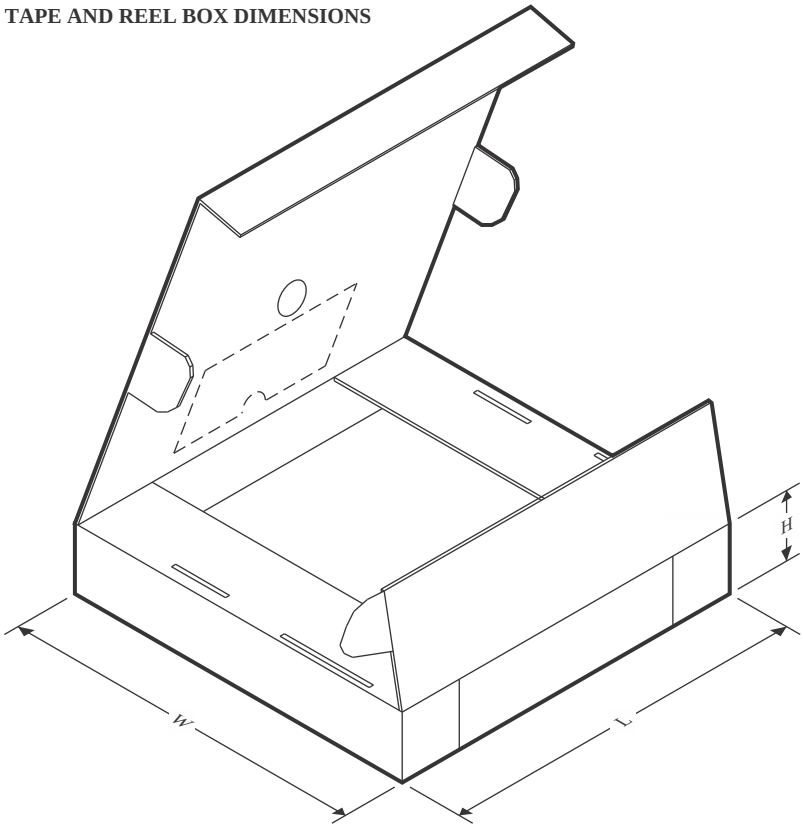
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSV911AQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TSV911AQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TSV911AQDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TSV912AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TSV912AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TSV912AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TSV912AQPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TSV914AQDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TSV914AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TSV914AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

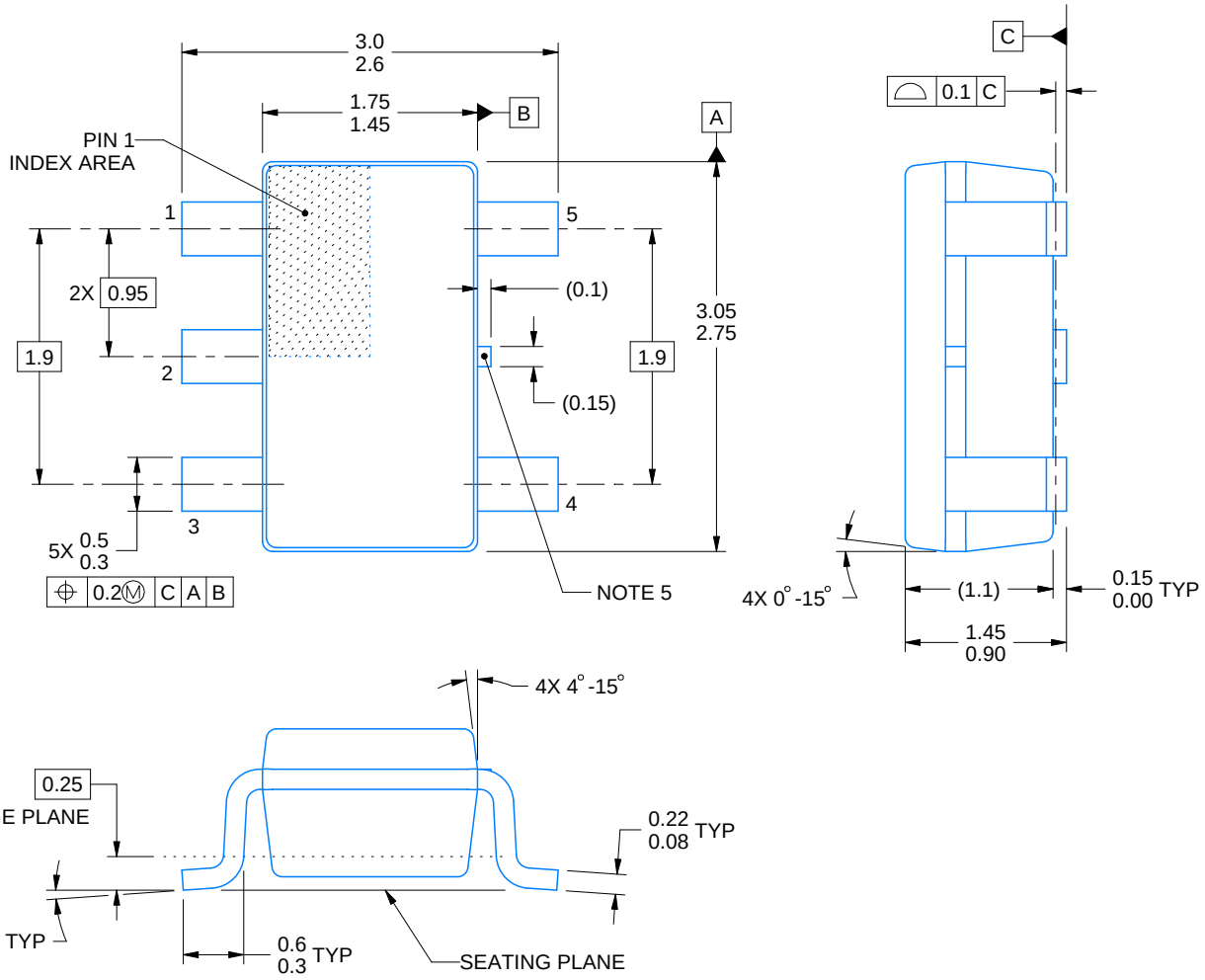
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSV911AQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TSV911AQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TSV911AQDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
TSV912AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TSV912AQDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
TSV912AQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TSV912AQPWRQ1	TSSOP	PW	8	3000	353.0	353.0	32.0
TSV914AQDRQ1	SOIC	D	14	2500	353.0	353.0	32.0
TSV914AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
TSV914AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

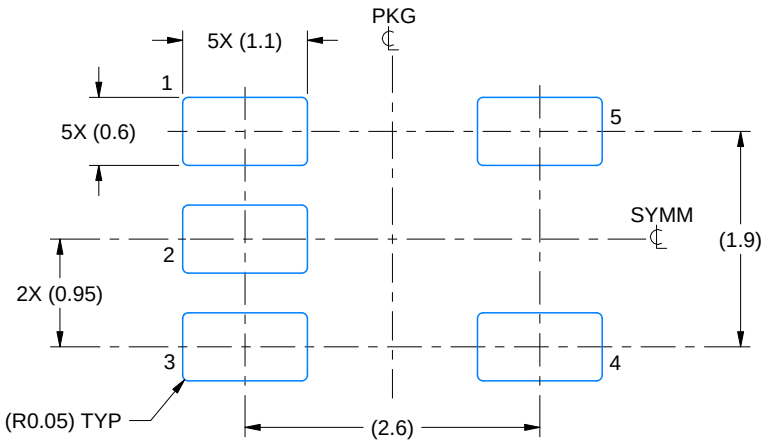
SMALL OUTLINE TRANSISTOR



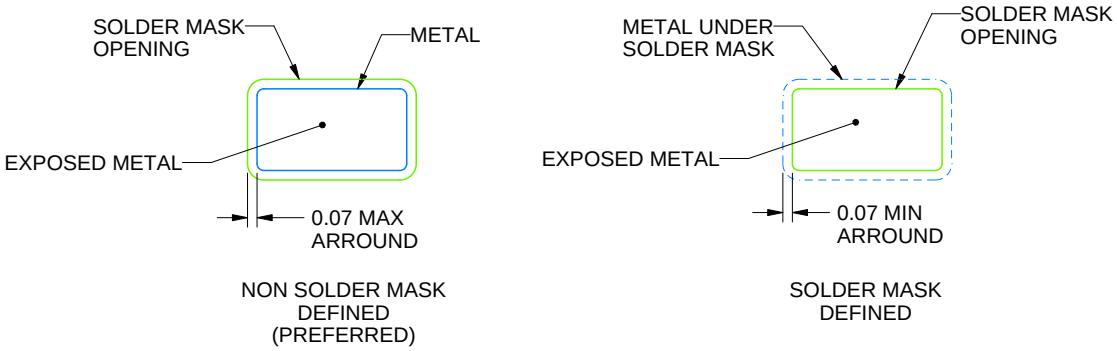
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

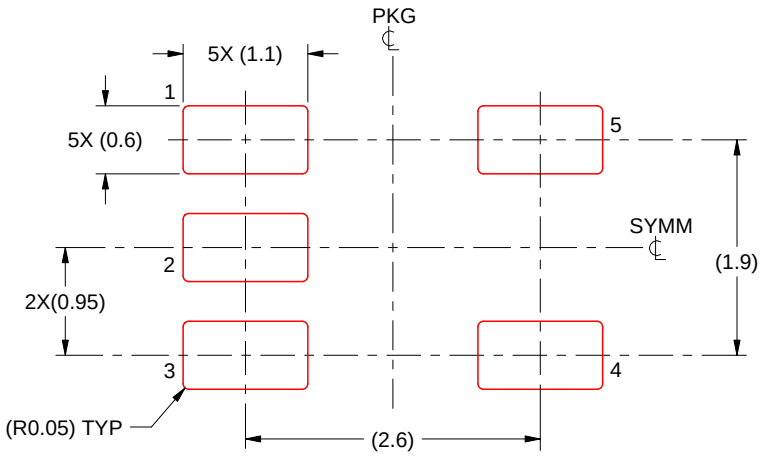


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

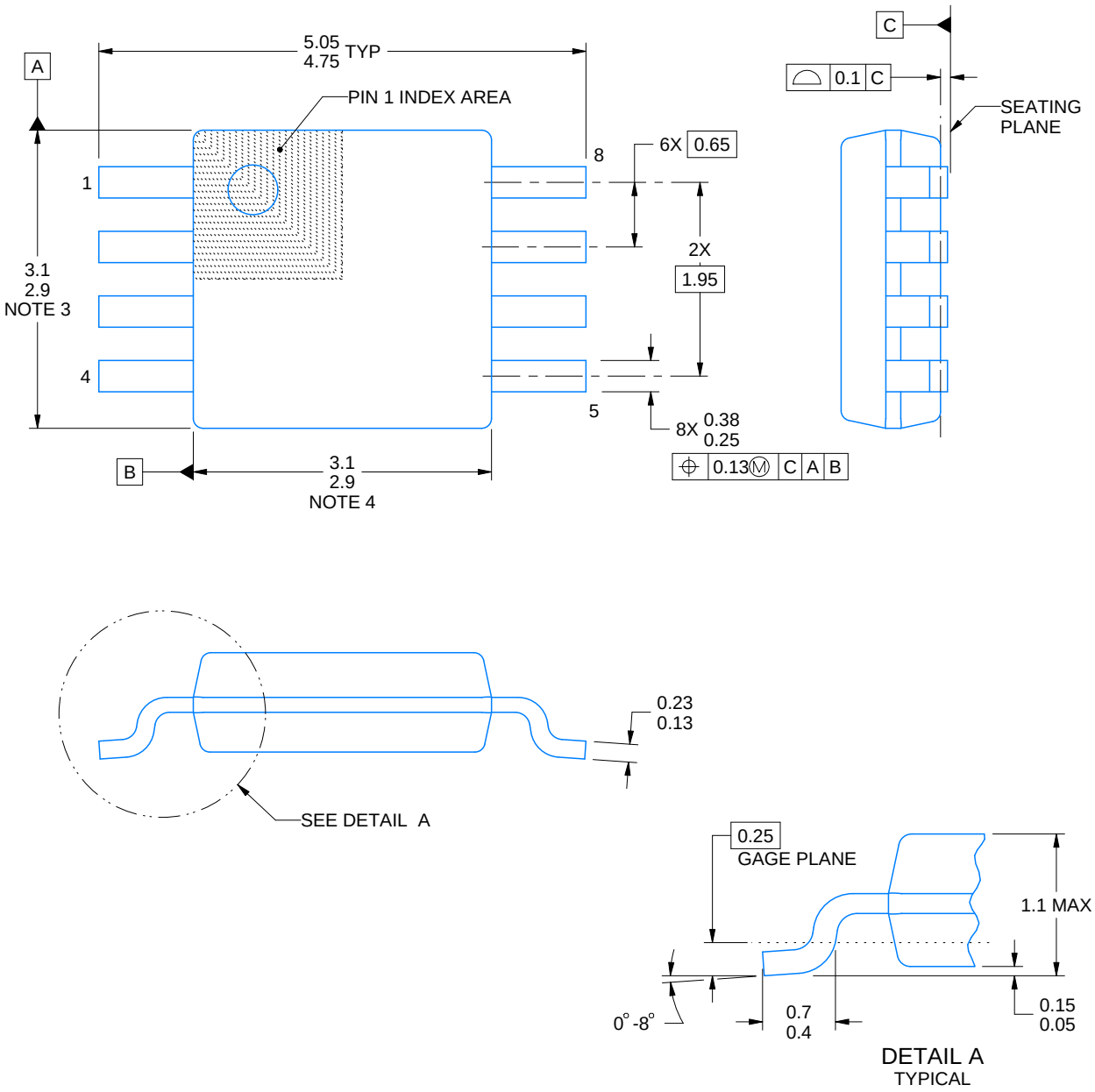
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

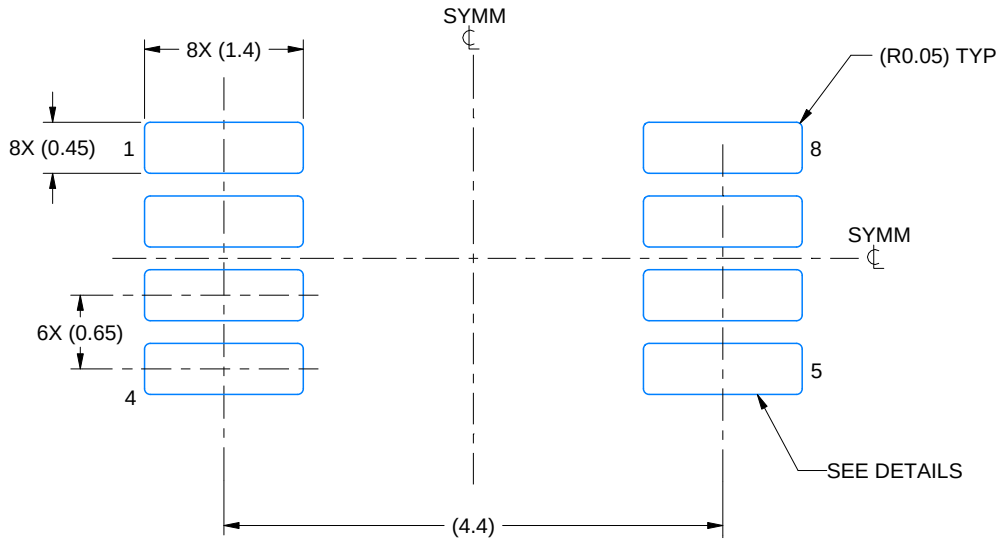
SMALL OUTLINE PACKAGE



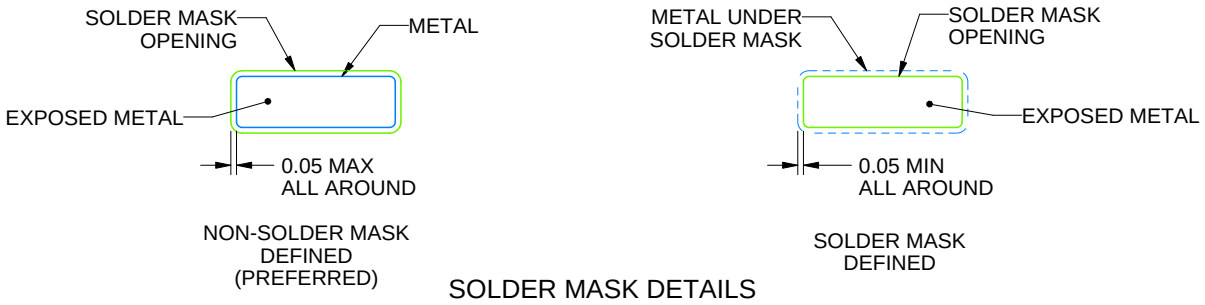
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

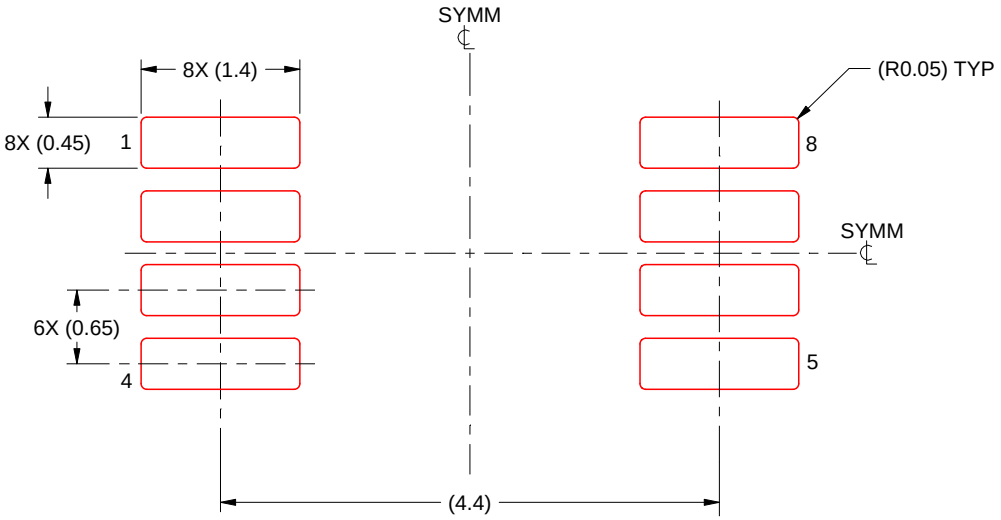


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

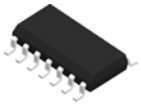


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

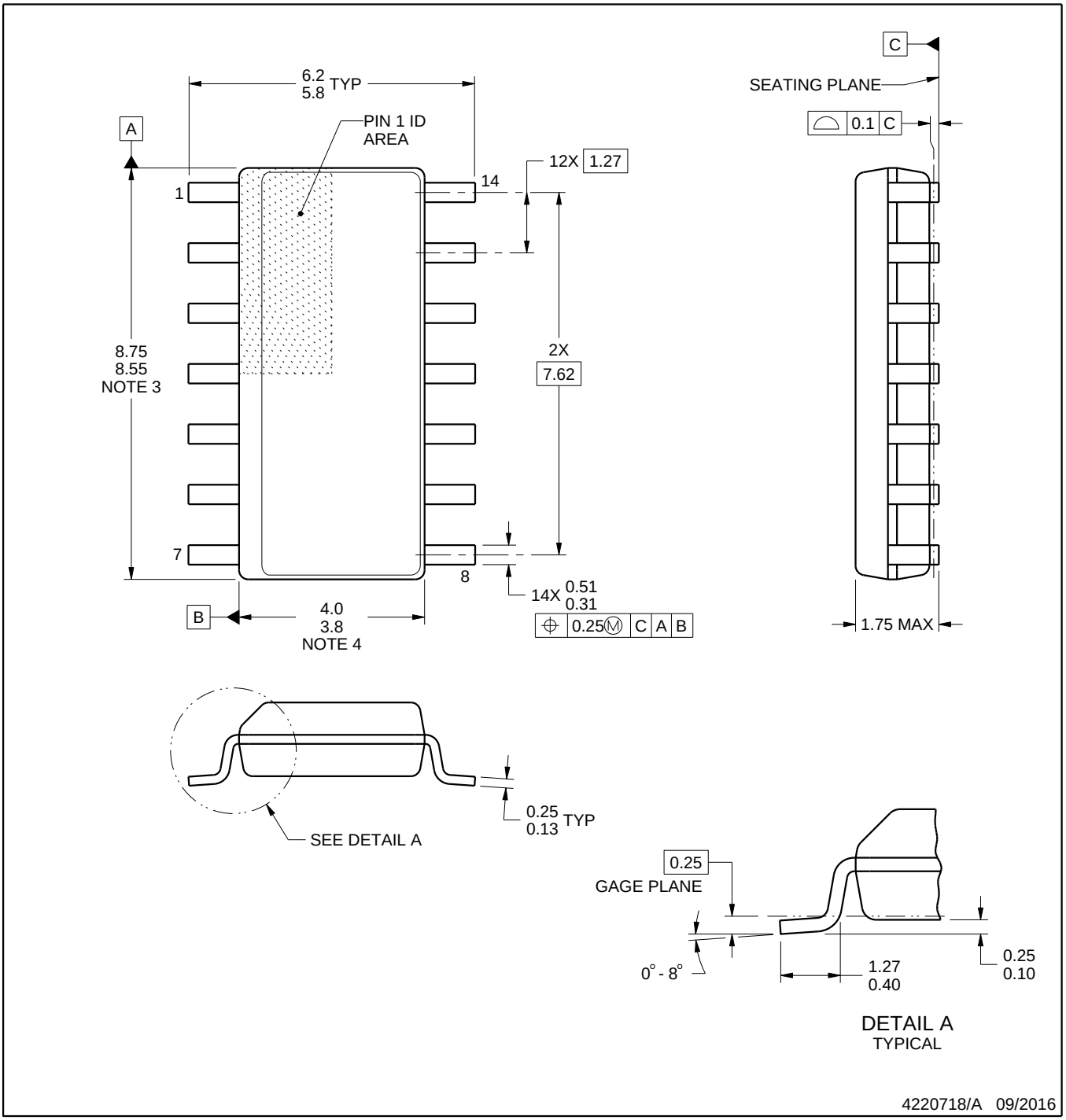


PACKAGE OUTLINE

D0014A

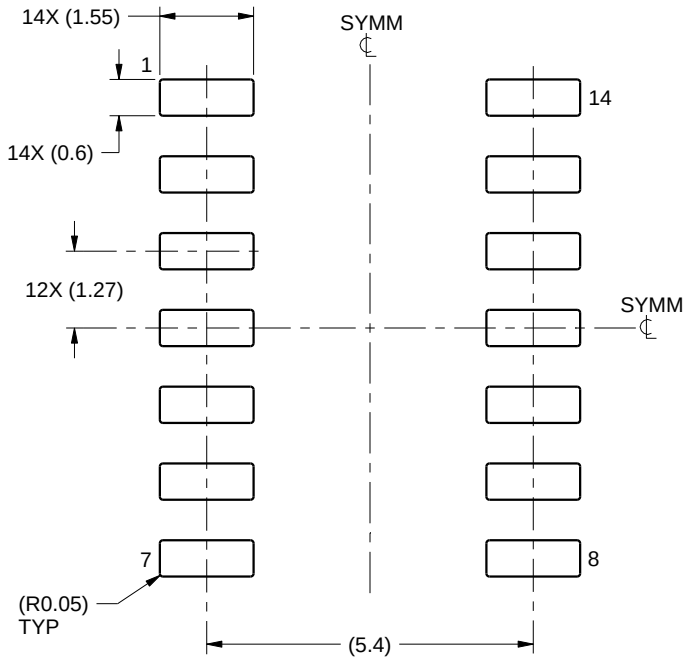
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

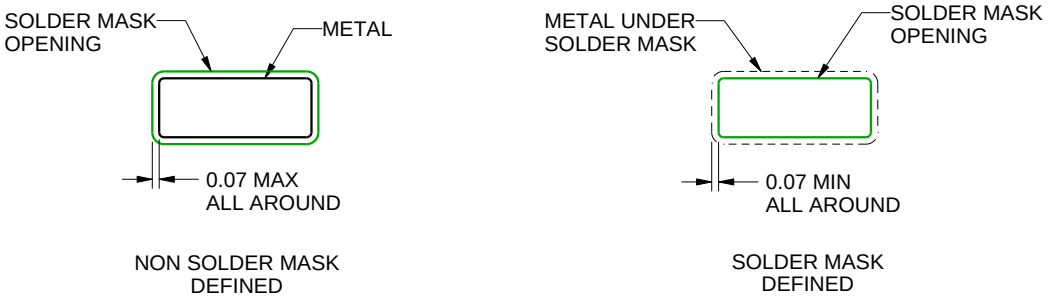


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

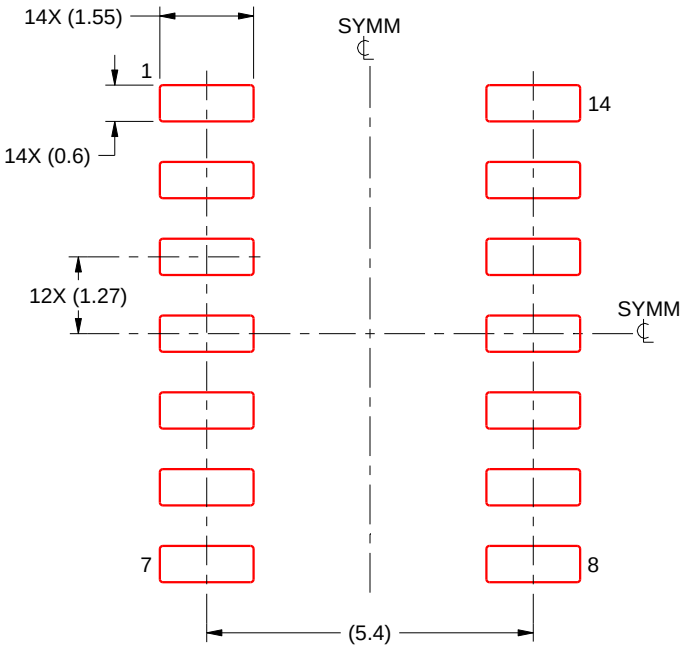
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

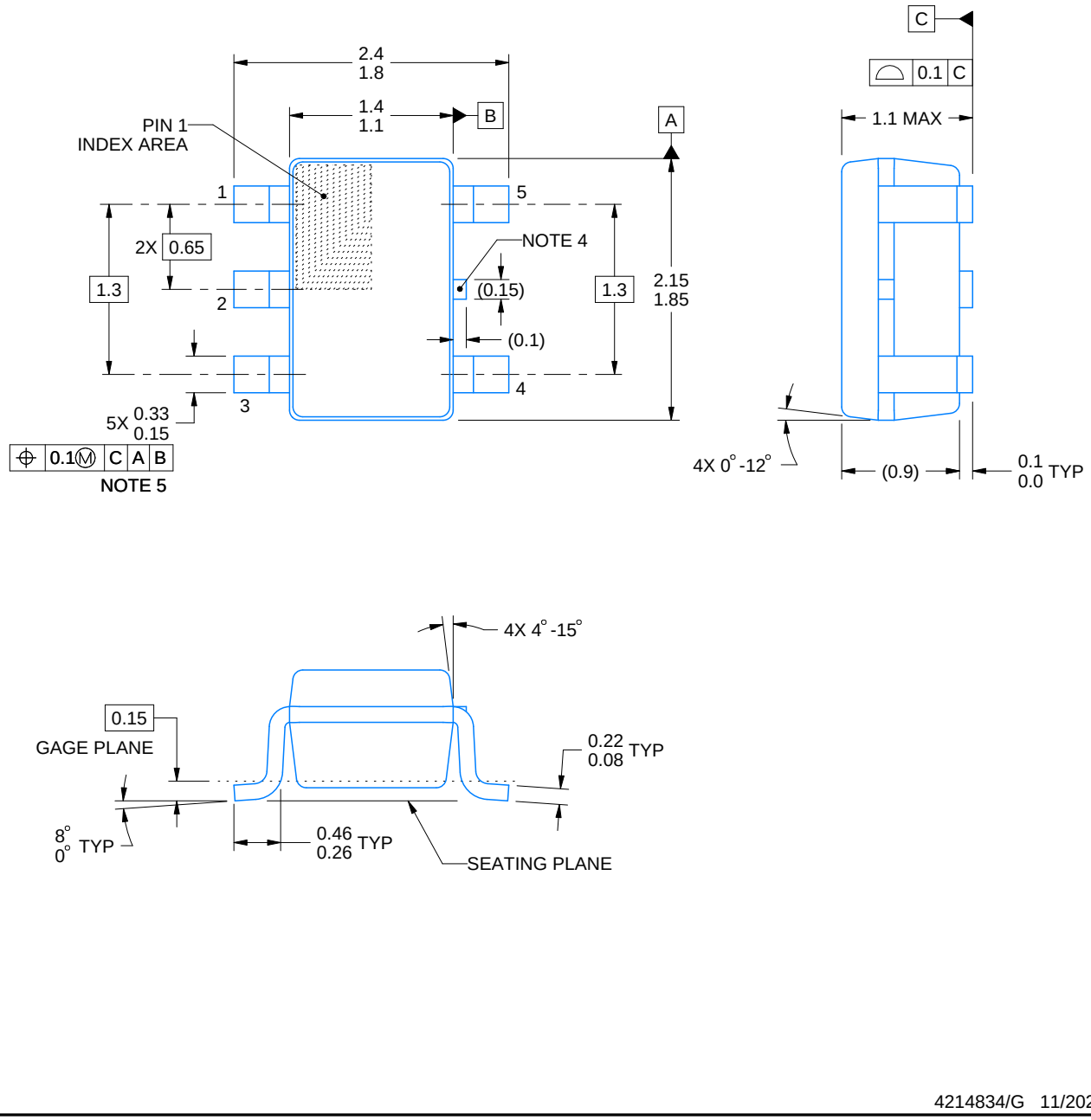
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

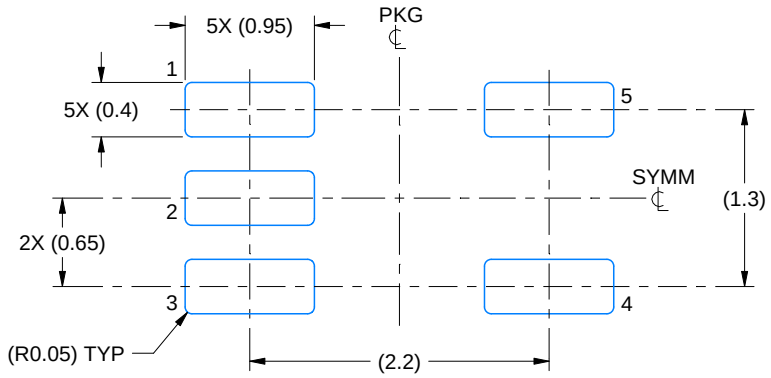
SMALL OUTLINE TRANSISTOR



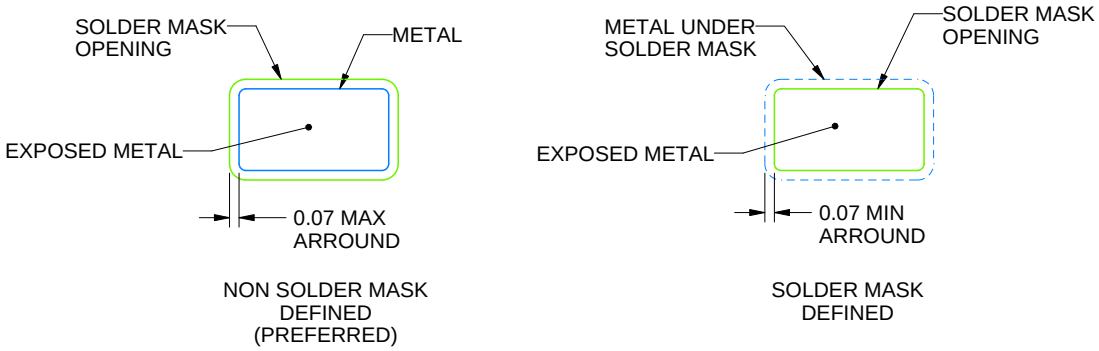
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

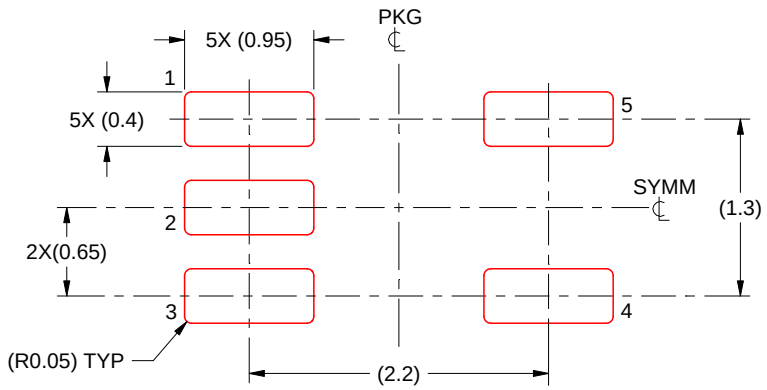


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

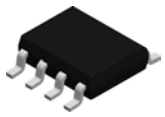


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

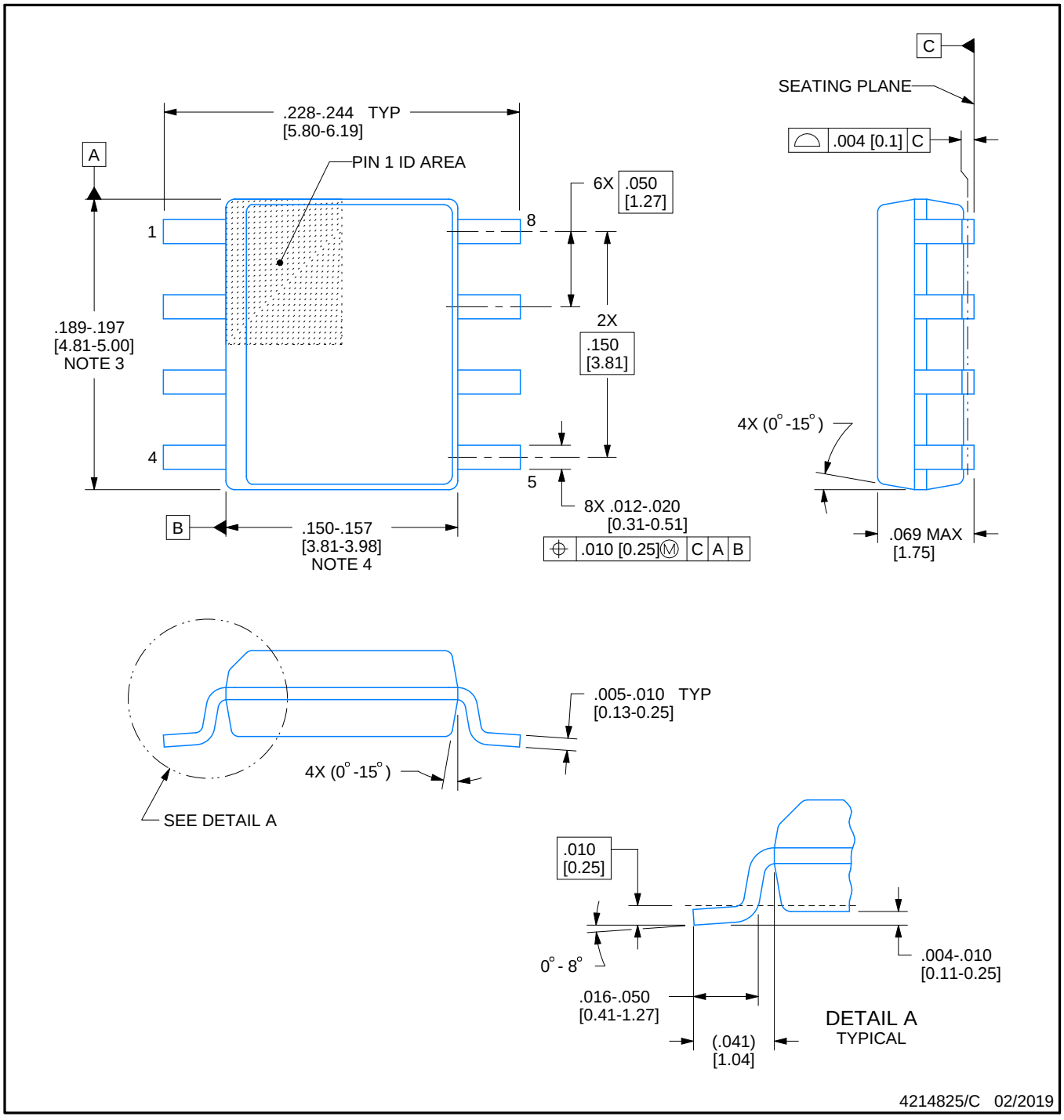


PACKAGE OUTLINE

D0008A

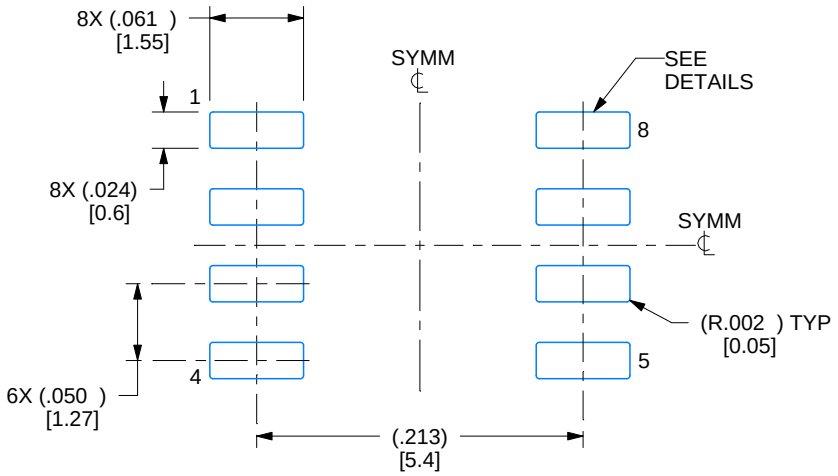
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

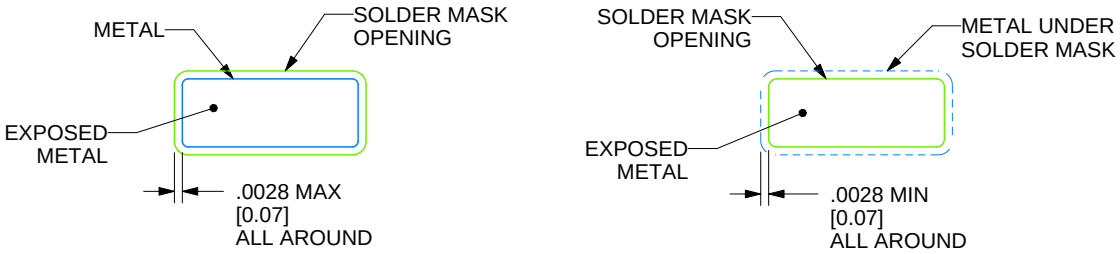


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

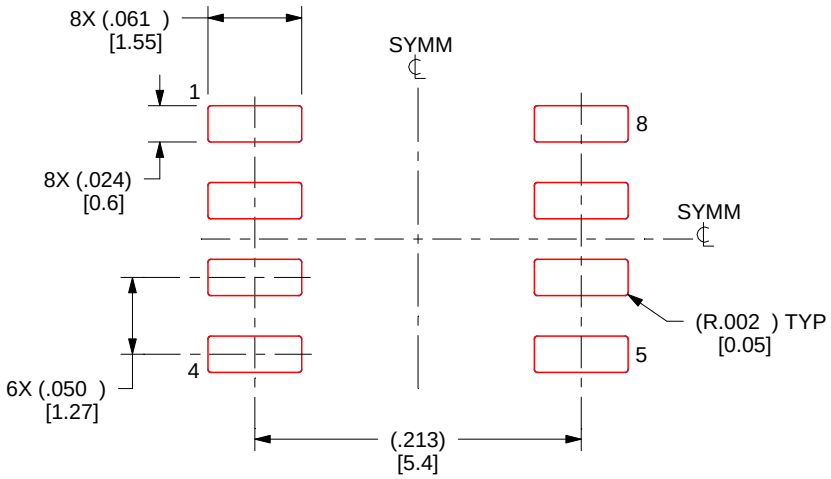
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

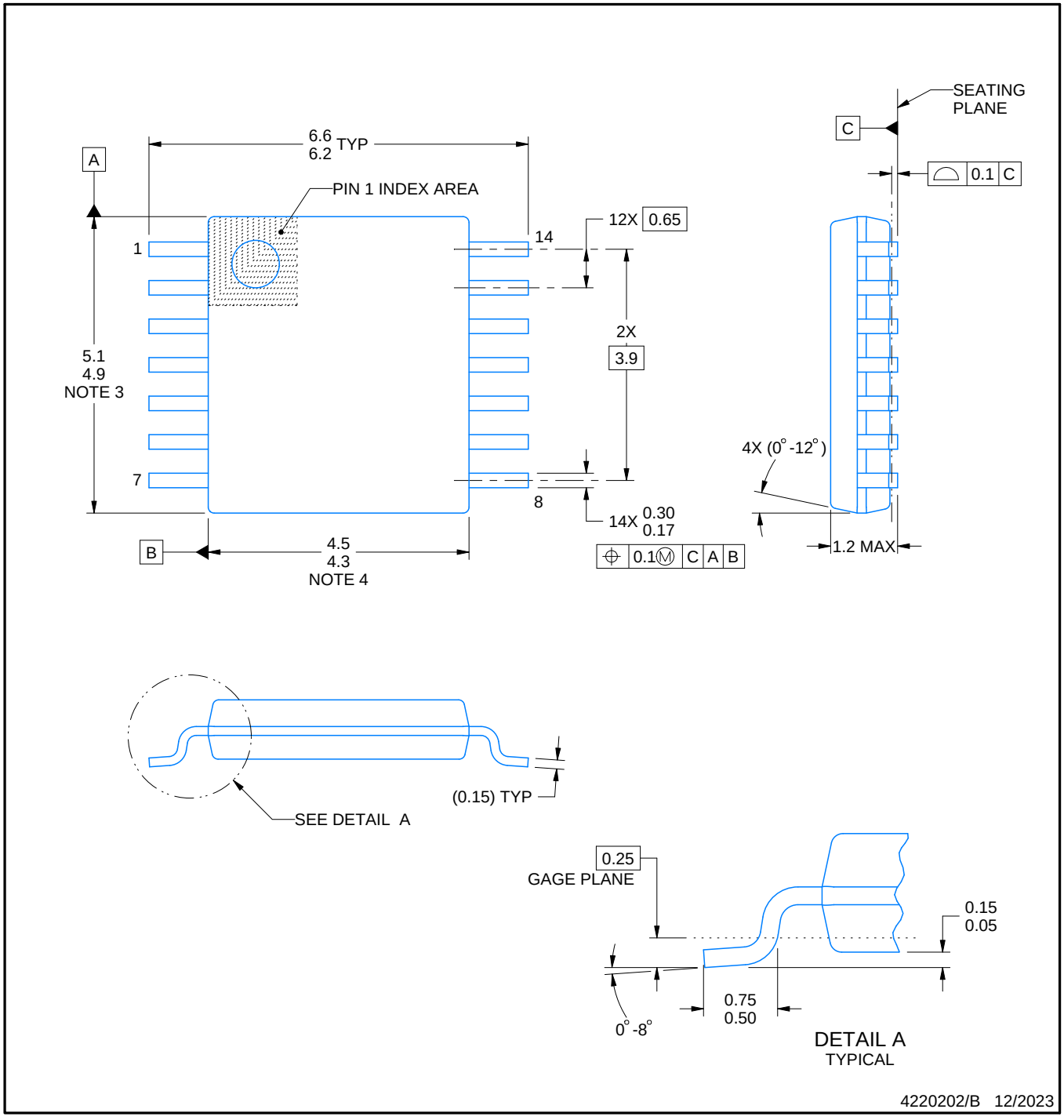
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

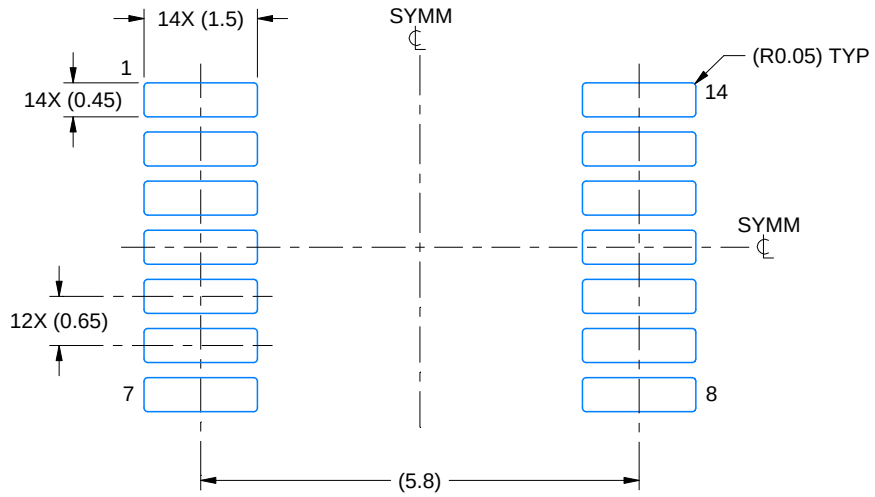
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

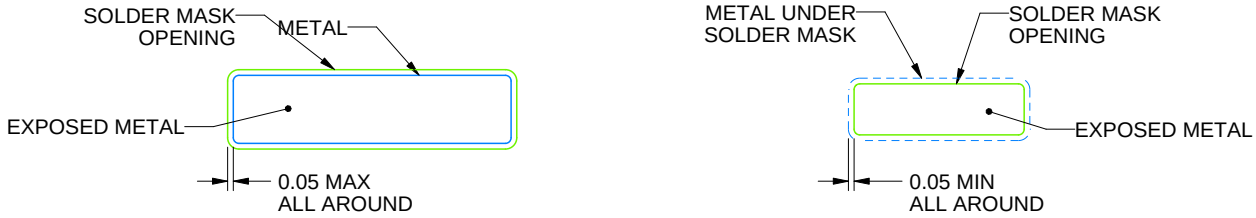


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

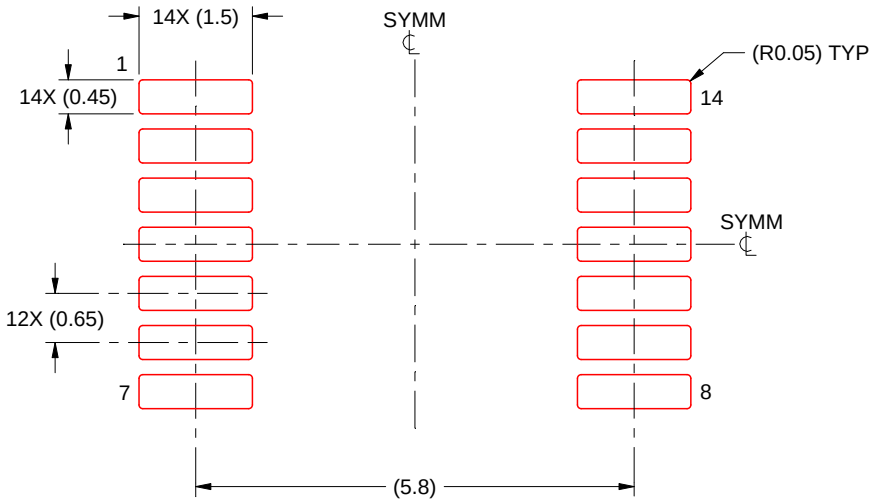


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

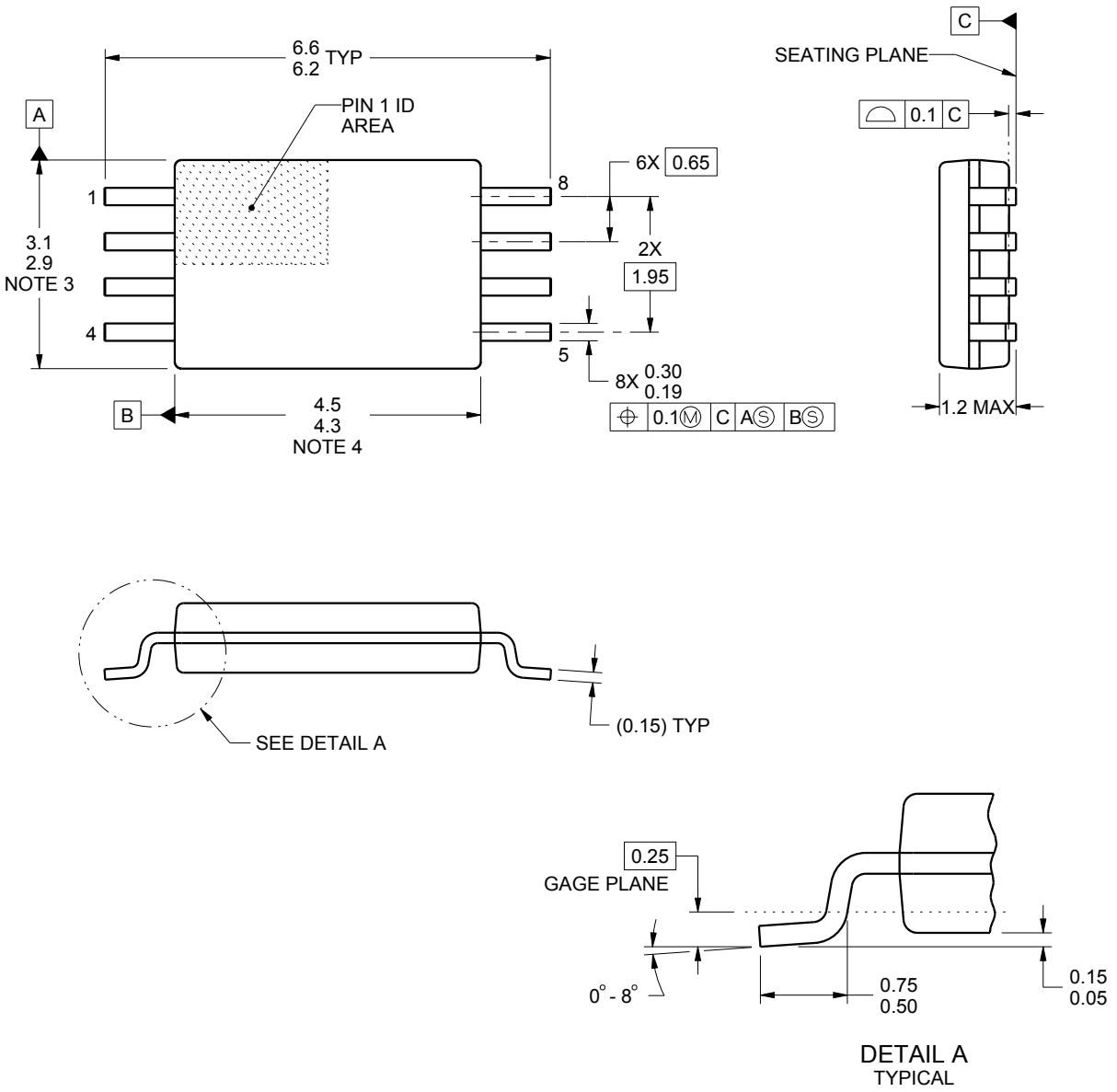
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

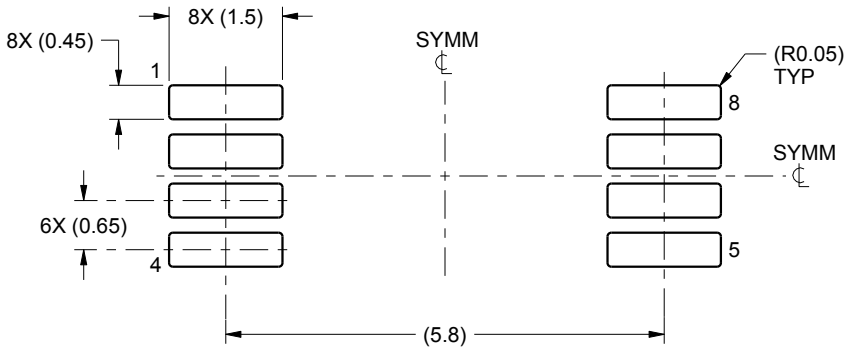
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

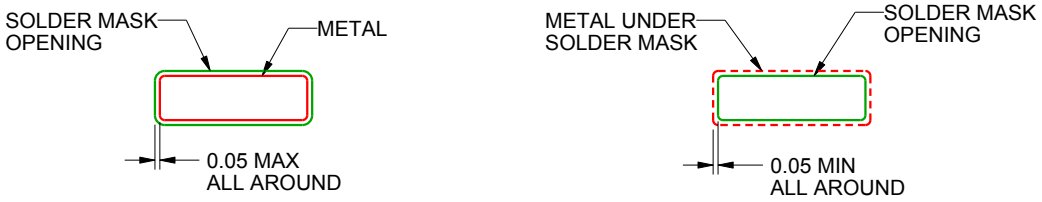


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

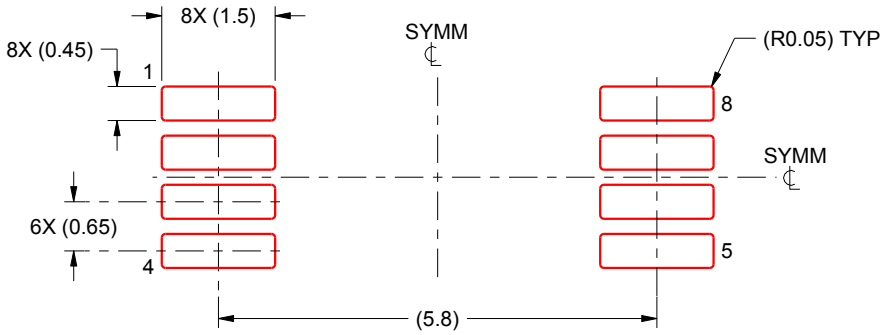


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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