

TSDxx-Q1 Unidirectional TVS Diodes for Automotive Applications in SOD-323 Package

1 Features

- ISO 10605 (330pF, 330Ohm) ESD protection:
 - $\pm 30\text{kV}$ contact discharge
 - $\pm 30\text{kV}$ air gap discharge
- IEC 61000-4-5 surge protection:
 - 7-60A (8/20 μs)
- IO capacitance < 20pF
- Ultra low leakage current: 50nA (maximum)
- Industrial temperature range: -55°C to $+150^{\circ}\text{C}$
- AEC-Q101 qualified
- Industry standard SOD-323 leaded package (2.65mm $\times$ 1.3mm)

2 Applications

- I/O Protection
- Power Line Protection
- [USB VBUS](#)
- [Body Electronics & Lighting](#)
- [Hybrid, Electric, & Powertrain Systems](#)

3 Description

The TSDxx-Q1 are a family of unidirectional TVS protection diodes designed for clamping harmful transients such as ESD and surge. The TSDxx-Q1 are rated to dissipate ESD strikes up to $\pm 30\text{kV}$ (contact and air gap discharge) and also meets the the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

Combining the robust clamping performance and low capacitance of these devices, TSDxx-Q1 are excellent TVS diodes to protect both data and power lines in many different applications.

The TSDxx-Q1 is offered in the industry standard, leaded SOD-323 package to enable easy solderability.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TSDxx-Q1	DYF (SOD-323, 2)	2.65mm $\times$ 1.3mm

(1) For more information, see [Section 9](#).

(2) The package size (length $\times$ width) is a nominal value and includes pins, where applicable.



Functional Block Diagram



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4 Pin Configuration and Functions

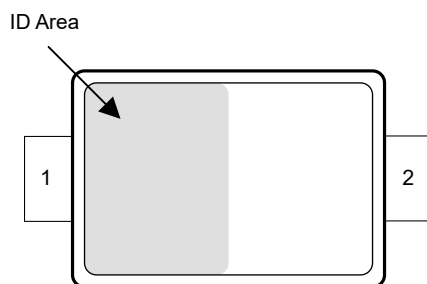


Figure 4-1. DYF Package, 2-Pin SOD-323 (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	IO	I/O	Protected Channel
2	GND	GND	Ground. Connect to ground.

(1) I = input, O = output. GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

Parameter		DEVICE	MIN	MAX	UNIT
P _{PP}	IEC 61000-4-5 power (t _p – 8/20 μs) at 25°C	TSD12-Q1		300	W
		TSD15-Q1		300	W
		TSD18-Q1		300	W
		TSD24-Q1		250	W
		TSD36-Q1		300	W
I _{PP}	IEC 61000-4-5 current (t _p – 8/20 μs) at 25°C	TSD12-Q1		18	A
		TSD15-Q1		15	A
		TSD18-Q1		15	A
		TSD24-Q1		9	A
		TSD36-Q1		7	A
T _A	Ambient Operating Temperature		-55	150	°C
T _{stg}	Storage Temperature		-65	155	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings - AEC Specifications

Parameter		Test Conditions	VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q101-001 ⁽¹⁾	±2500	V
		Charged device model (CDM), per AEC Q101-005 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specification

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 contact discharge	±30000	V
		IEC 61000-4-2 air-gap discharge	±30000	

5.4 ESD Ratings - ISO Specifications

Parameter		Test Conditions		VALUE	UNIT
V _(ESD)	ISO 10605 Electrostatic Discharge	C = 150pF; R = 330Ω	Contact Discharge, all pins	±30000	V
			Air-gap Discharge, all pins	±30000	
		C = 330pF; R = 330Ω	Contact Discharge, all pins	±30000	
			Air-gap Discharge, all pins	±30000	

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T _A	Operating free-air temperature	-55		150	°C

5.6 Thermal Information

THERMAL METRIC ⁽¹⁾		TSD12-Q1 / TSD15-Q1 / TSD18-Q1 / TSD24-Q1 / TSD36-Q1	UNIT
		DYF (SOD-323)	
		2 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	693.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	254.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	566.6	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	78.6	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	552.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.7 Electrical Characteristics - TSD12-Q1

At T_A=25°C (unless otherwise noted) ⁽¹⁾

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V _{RWM}	Reverse stand-off voltage	I _{IO} <50nA, across operating temperature range			12	V
V _{BR}	Breakdown voltage	I _{IO} = 10mA, IO to GND	12.7			V
I _{LEAK}	Reverse leakage current	V _{IO} = 12V, IO to GND		2	20	nA
V _{FWD}	Forward voltage	I _{IO} = 1mA, GND to IO		0.7		V
V _{CLAMP}	Surge clamping voltage, t _p = 8/20μs ⁽²⁾	I _{PP} = 1A, IO to GND			18	V
		I _{PP} = 5A, IO to GND			19	V
		I _{PP} = 18A, IO to GND			23	V
		I _{PP} = 18A, GND to IO			8	V
	TLP clamping voltage, t _p = 100ns	I _{PP} = 16A, IO to GND		17		V
		I _{PP} = 16A, GND to IO		3		V
C _L	Line capacitance	V _{IO} = 0V; f = 1MHz, IO to GND		12		pF

(1) Typical parameters are measured at 25°C

(2) Nonrepetitive current pulse 8 to 20μs exponentially decaying waveform according to IEC 61000-4-5

5.8 Electrical Characteristics - TSD15-Q1

At T_A=25°C (unless otherwise noted) ⁽¹⁾

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V _{RWM}	Reverse stand-off voltage	I _{IO} <50nA, across operating temperature range			15	V
V _{BR}	Breakdown voltage	I _{IO} = 10mA, IO to GND	18.3			V
I _{LEAK}	Reverse leakage current	V _{IO} = 15V, IO to GND		2	20	nA
V _{FWD}	Forward voltage	I _{IO} = 10mA, GND to IO		0.7		V
V _{CLAMP}	Surge clamping voltage, t _p = 8/20μs ⁽²⁾	I _{PP} = 1A, IO to GND			25	V
		I _{PP} = 5A, IO to GND			26	V
		I _{PP} = 15A, IO to GND			31	V
		I _{PP} = 15A, GND to IO			7	V
	TLP clamping voltage, t _p = 100ns	I _{PP} = 16A, IO to GND		23		V
		I _{PP} = 16A, GND to IO		3		V

TSD12-Q1, TSD15-Q1, TSD18-Q1, TSD24-Q1, TSD36-Q1

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At $T_A = 25^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
C_L	Line capacitance	$V_{IO} = 0\text{V}; f = 1\text{MHz}$, IO to GND	12		pF

(1) Typical parameters are measured at 25°C

(2) Nonrepetitive current pulse 8 to $20\mu\text{s}$ exponentially decaying waveform according to IEC 61000-4-5

5.9 Electrical Characteristics - TSD18-Q1

At $T_A = 25^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	$I_{IO} < 50\text{nA}$, across operating temperature range		18	V
V_{BR}	Breakdown voltage	$I_{IO} = 10\text{mA}$, IO to GND	18.5		V
I_{LEAK}	Reverse leakage current	$V_{IO} = 18\text{V}$, IO to GND	2	20	nA
V_{FWD}	Forward voltage	$I_{IO} = 10\text{mA}$, GND to IO	0.7		V
V_{CLAMP}	Surge clamping voltage, $t_p = 8/20\mu\text{s}$ ⁽²⁾	$I_{PP} = 1\text{A}$, IO to GND		25	V
		$I_{PP} = 5\text{A}$, IO to GND		26	V
		$I_{PP} = 15\text{A}$, IO to GND		31	V
		$I_{PP} = 15\text{A}$, GND to IO		7	V
	TLP clamping voltage, $t_p = 100\text{ns}$	$I_{PP} = 16\text{A}$, IO to GND	23		V
		$I_{PP} = 16\text{A}$, GND to IO	3		V
C_L	Line capacitance	$V_{IO} = 0\text{V}; f = 1\text{MHz}$, IO to GND	12		pF

(1) Typical parameters are measured at 25°C

(2) Nonrepetitive current pulse 8 to $20\mu\text{s}$ exponentially decaying waveform according to IEC 61000-4-5

5.10 Electrical Characteristics - TSD24-Q1

At $T_A = 25^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	$I_{IO} < 50\text{nA}$, across operating temperature range		24	V
V_{BR}	Breakdown voltage	$I_{IO} = 10\text{mA}$, IO to GND	24.8		V
I_{LEAK}	Reverse leakage current	$V_{IO} = 24\text{V}$, IO to GND	2	20	nA
V_{FWD}	Forward voltage	$I_{IO} = 10\text{mA}$, GND to IO	0.7		V
V_{CLAMP}	Surge clamping voltage, $t_p = 8/20\mu\text{s}$ ⁽²⁾	$I_{PP} = 1\text{A}$, IO to GND		32	V
		$I_{PP} = 5\text{A}$, IO to GND		36	V
		$I_{PP} = 9\text{A}$, IO to GND		39	V
		$I_{PP} = 9\text{A}$, GND to IO		4	V
	TLP clamping voltage, $t_p = 100\text{ns}$	$I_{PP} = 16\text{A}$, IO to GND	33		V
		$I_{PP} = 16\text{A}$, GND to IO	3		V
C_L	Line capacitance	$V_{IO} = 0\text{V}; f = 1\text{MHz}$, IO to GND	12		pF

(1) Typical parameters are measured at 25°C

(2) Nonrepetitive current pulse 8 to $20\mu\text{s}$ exponentially decaying waveform according to IEC 61000-4-5

5.11 Electrical Characteristics - TSD36-Q1

At $T_A=25^{\circ}\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	$I_{IO} < 50\text{nA}$, across operating temperature range			36	V
V_{BR}	Breakdown voltage	$I_{IO} = 10\text{mA}$, IO to GND	37.1			V
I_{LEAK}	Reverse leakage current	$V_{IO} = 36\text{V}$, IO to GND		2	20	nA
V_{FWD}	Forward voltage	$I_{IO} = 10\text{mA}$, GND to IO		0.7		V
V_{CLAMP}	Surge clamping voltage, $t_p = 8/20\mu\text{s}$ ⁽²⁾	$I_{PP} = 1\text{A}$, IO to GND			44	V
		$I_{PP} = 5\text{A}$, IO to GND			59	V
		$I_{PP} = 7\text{A}$, IO to GND			67	V
		$I_{PP} = 7\text{A}$, GND to IO			4	V
	TLP clamping voltage, $t_p = 100\text{ns}$	$I_{PP} = 16\text{A}$, IO to GND		53		V
		$I_{PP} = 16\text{A}$, GND to IO		3		V
C_L	Line capacitance	$V_{IO} = 0\text{V}$; $f = 1\text{MHz}$, IO to GND		12		pF

(1) Typical parameters are measured at 25°C

(2) Nonrepetitive current pulse 8 to $20\mu\text{s}$ exponentially decaying waveform according to IEC 61000-4-5

5.12 Typical Characteristics

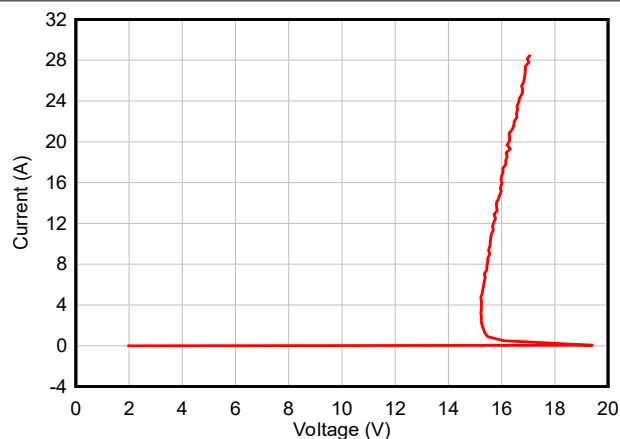


Figure 5-1. Positive TLP Curve - TSD12-Q1

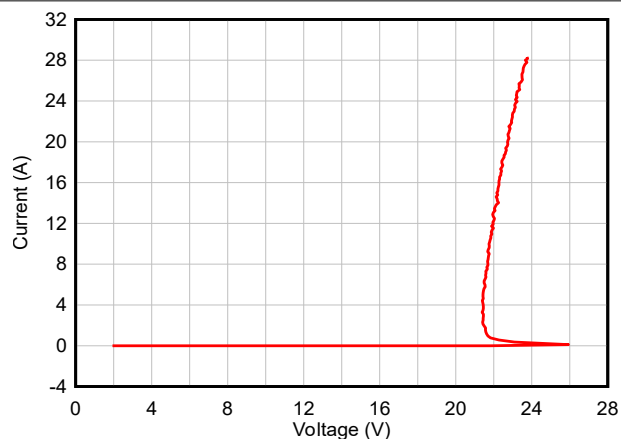


Figure 5-2. Positive TLP Curve - TSD15-Q1

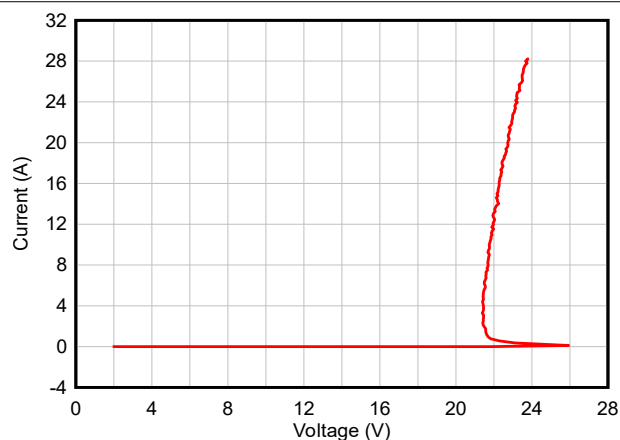


Figure 5-3. Positive TLP Curve - TSD18-Q1

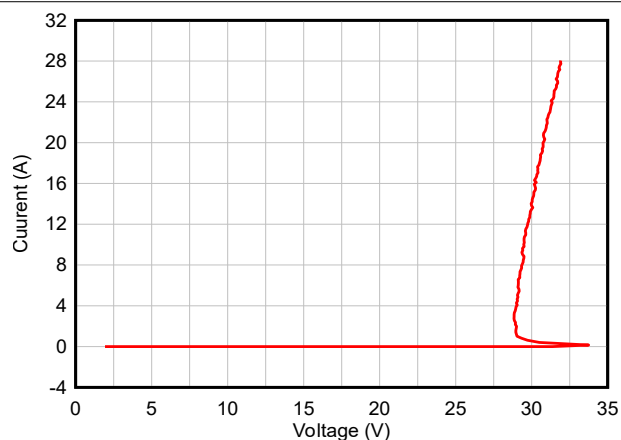


Figure 5-4. Positive TLP Curve - TSD24-Q1

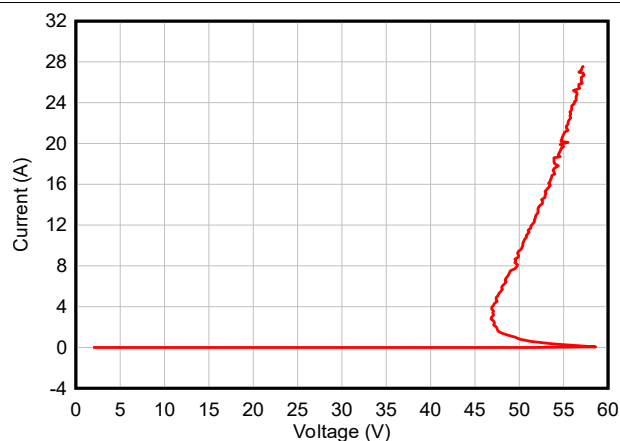


Figure 5-5. Positive TLP Curve - TSD36-Q1

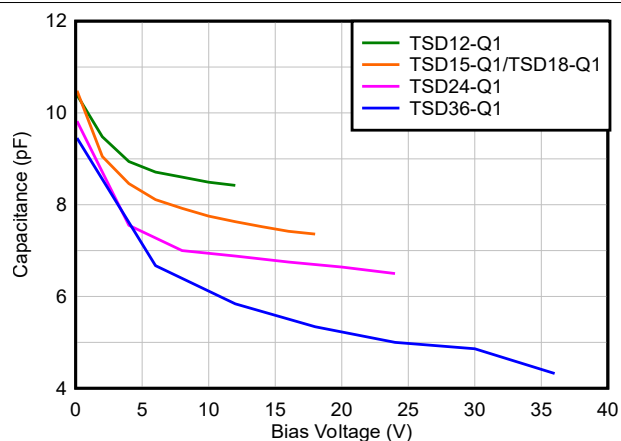


Figure 5-6. Capacitance vs Bias Voltage

5.12 Typical Characteristics (continued)

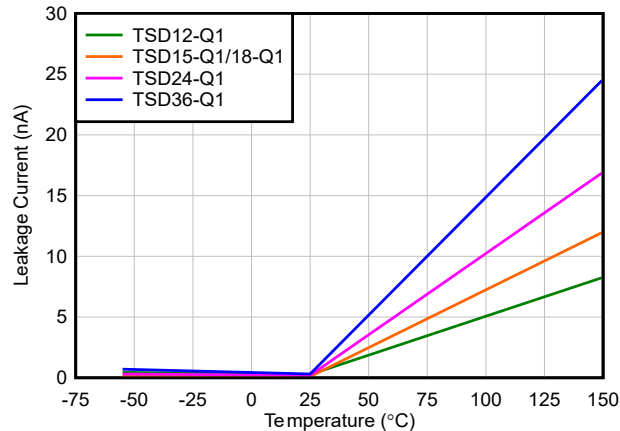


Figure 5-7. Leakage Current vs Temperature

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The TSDxx-Q1 are TVS diodes that provide a path to ground for dissipating transient voltage spikes, such as ESD or surge, on signal lines and power lines. Connect the device in parallel to the down stream circuitry for protection. As the current from the transient passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, refer to the [ESD Packaging and Layout Guide](#).

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Layout Guide application reports](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection Data Sheet](#)

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

DATE	REVISION	NOTES
June 2025	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSD12DYFRQ1	Active	Production	SOT (DYF) 2	3000 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	3JJF
TSD15DYFRQ1	Active	Production	SOT (DYF) 2	3000 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	3MPF
TSD18DYFRQ1	Active	Production	SOT (DYF) 2	3000 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	3JKF
TSD24DYFRQ1	Active	Production	SOT (DYF) 2	3000 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	3H4F
TSD36DYFRQ1	Active	Production	SOT (DYF) 2	3000 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-	3GLF

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

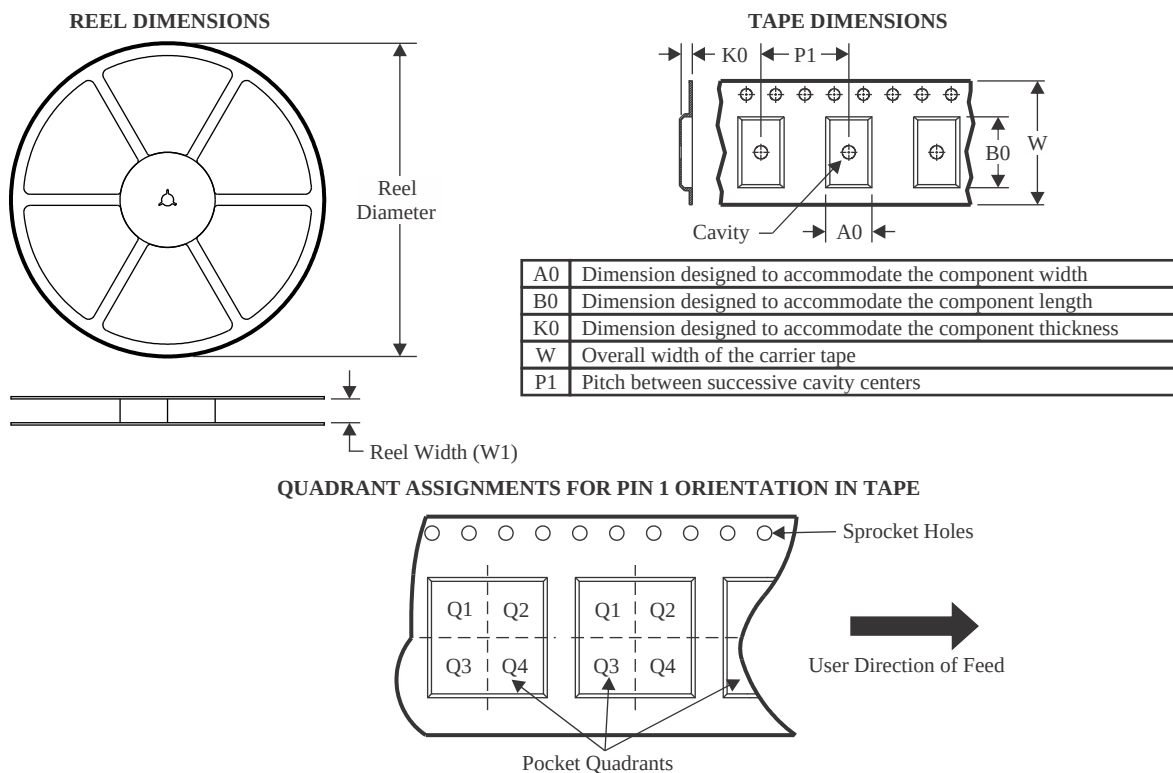
OTHER QUALIFIED VERSIONS OF TSD12-Q1, TSD15-Q1, TSD18-Q1, TSD24-Q1, TSD36-Q1 :

- Catalog : [TSD12](#), [TSD15](#), [TSD18](#), [TSD24](#), [TSD36](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

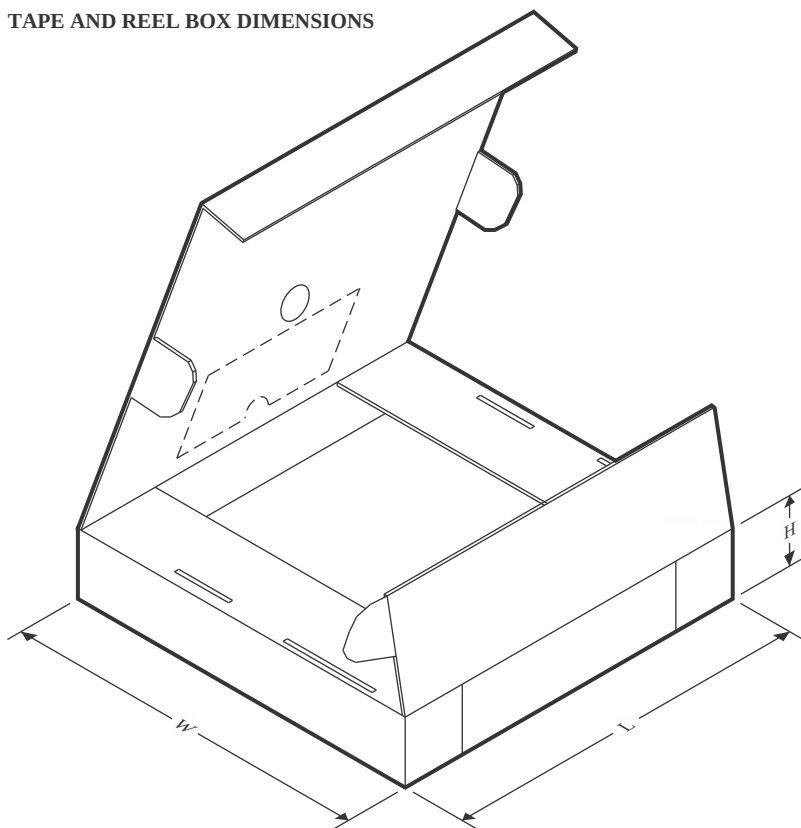
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSD12DYFRQ1	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1
TSD15DYFRQ1	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1
TSD18DYFRQ1	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1
TSD24DYFRQ1	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1
TSD36DYFRQ1	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSD12DYFRQ1	SOT	DYF	2	3000	210.0	200.0	42.0
TSD15DYFRQ1	SOT	DYF	2	3000	210.0	200.0	42.0
TSD18DYFRQ1	SOT	DYF	2	3000	210.0	200.0	42.0
TSD24DYFRQ1	SOT	DYF	2	3000	210.0	200.0	42.0
TSD36DYFRQ1	SOT	DYF	2	3000	210.0	200.0	42.0

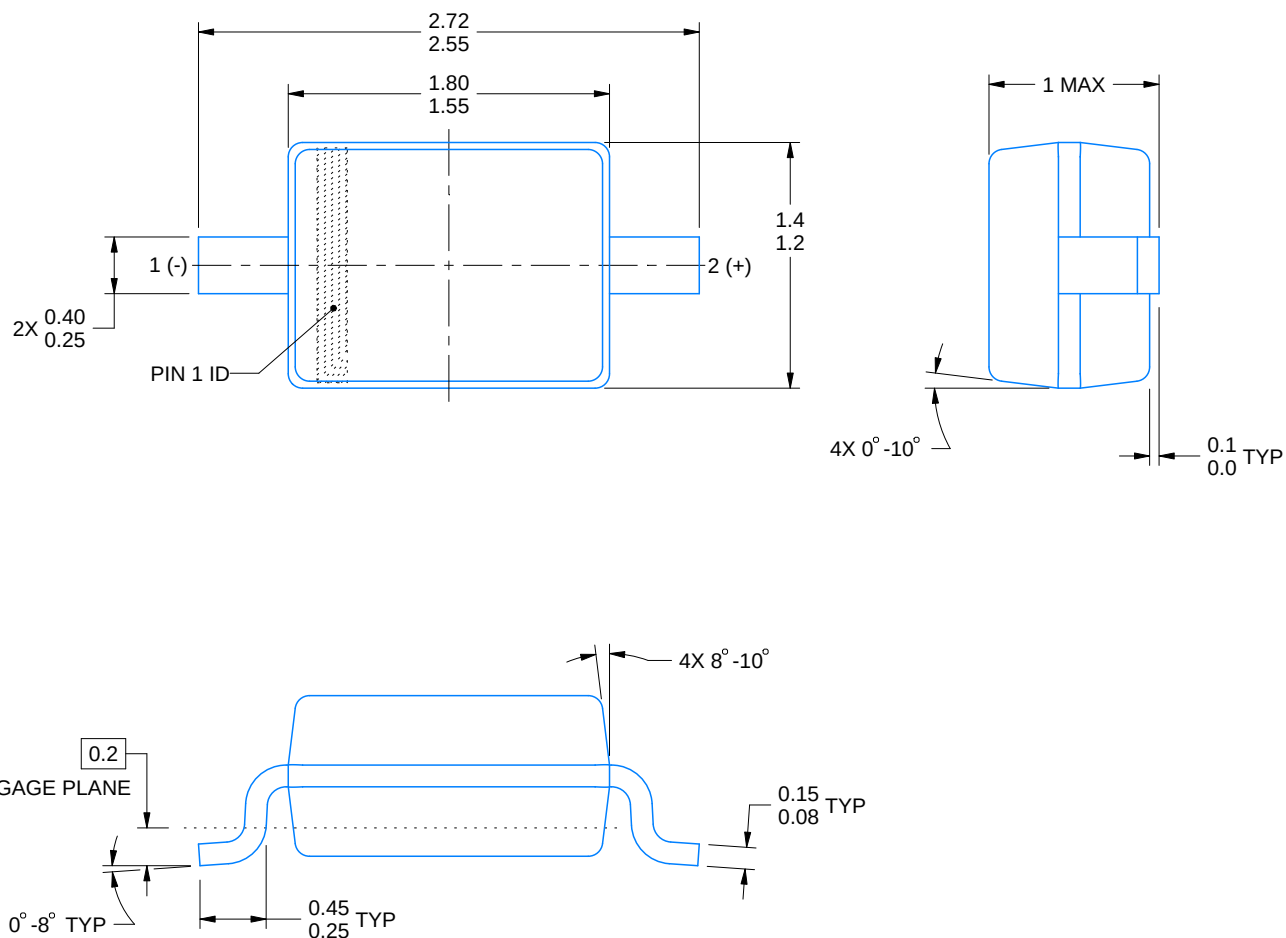
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PACKAGE OUTLINE

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

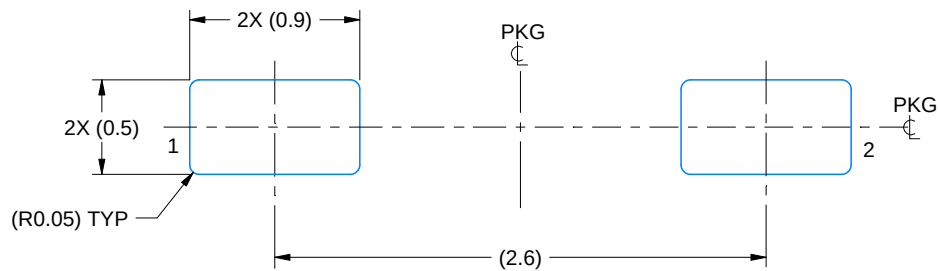
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

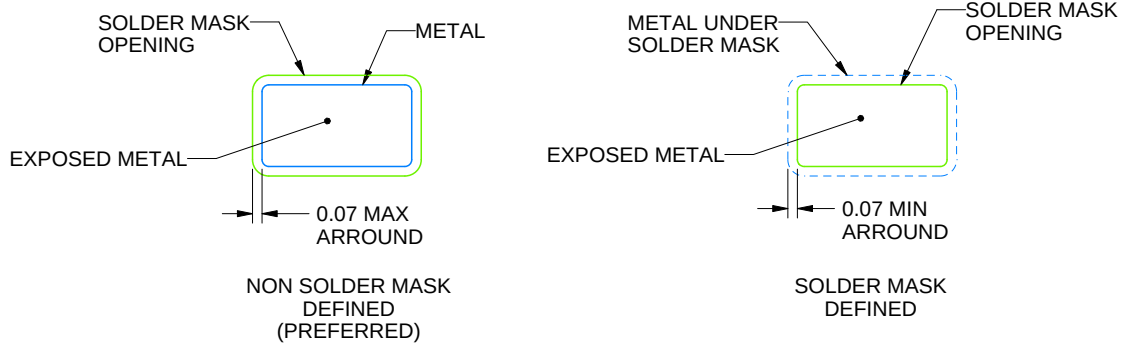
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SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

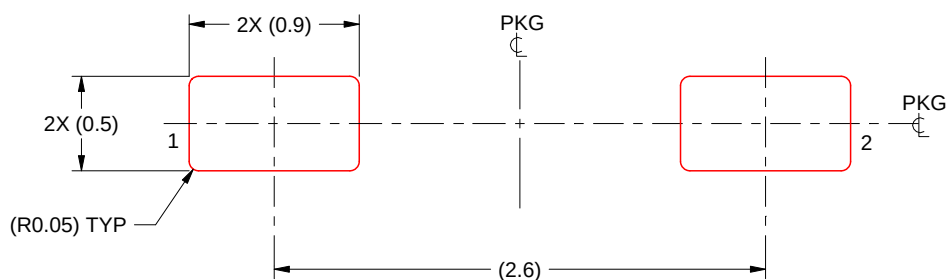
3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYF0002A

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

4228484/D 09/2026

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
6. Board assembly site may have different recommendations for stencil design.

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