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# 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV IEC ESD PROTECTION

#### **FEATURES**

- Qualified for Automotive Applications
- ESD Protection for RS-232 Bus Pins
  - ±15-kV Human Body Model (HBM)
  - ±8 kV (IEC61000-4-2, Contact Discharge)
  - ±15 kV (IEC61000-4-2, Air-Gap Discharge)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V<sub>CC</sub> Supply
- Operates up to 250 kbit/s
- Two Drivers and Two Receivers
- Low Supply Current: 300 μA (Typ)
- External Capacitors: 4 × 0.1 μF
- Accepts 5-V Logic Input With 3.3-V Supply
- Pin Compatible to Alternative High-Speed Device (1 Mbit/s): TRSF3232E

#### (TOP VIEW) $\square$ $V_{cc}$ C1+ □□ 16 15 C1- 🖂 14 C2+ \_\_\_\_ 13 C2- \_\_\_\_ 5 12 V− \_\_\_ 11 DOUT2 \_\_\_ 10 RIN2 \_\_\_ 9

**PW PACKAGE** 

#### DESCRIPTION

The TRS3232E device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV IEC ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/μs driver output slew rate.

#### ORDERING INFORMATION(1)

T <sub>A</sub>	PACK	AGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	TSSOP - PW	Reel of 2000	TRS3232EQPWRQ1	RS32EQ

<sup>(1)</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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## **FUNCTION TABLES**

## Each Driver(1)

INPUT DIN	OUTPUT DOUT
L	Н
Н	L

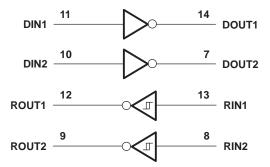
(1) H = high level, L = low level

## Each Receiver<sup>(1)</sup>

INPUT RIN	OUTPUT ROUT
L	Н
Н	L
Open	Н

(1) H = high level, L = low level, Open = input disconnected or connected driver off

## LOGIC DIAGRAM (POSITIVE LOGIC)





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## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>		−0.3 V to 6 V
V+	Positive output supply voltage range <sup>(2)</sup>		−0.3 V to 7 V
V-	Negative output supply voltage range <sup>(2)</sup>		0.3 V to -7 V
V+ - V-	Supply voltage difference <sup>(2)</sup>		
V	Innut velte en vene	Drivers	−0.3 V to 6 V
V <sub>I</sub>	Input voltage range	Receivers	–25 V to 25 V
.,	Outrot vallens van	Drivers	–13.2 V to 13.2 V
Vo	Output voltage range	Receivers	-0.3 V to V <sub>CC</sub> + 0.3 V
$\theta_{JA}$	Package thermal impedance (3)(4)		108°C/W
T <sub>J</sub>	Operating virtual-junction temperature		150°C
T <sub>stg</sub>	Storage temperature range		−65°C to 150°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS(1)

#### See Figure 4

			MIN	NOM	MAX	UNIT
\/	Cumply yeltore	V <sub>CC</sub> = 3.3 V	3	3.3	3.6	V
V <sub>CC</sub>	Supply voltage	V <sub>CC</sub> = 5 V	4.5	5	5.5	V
\/	Driver high-level input voltage, DIN	V <sub>CC</sub> = 3.3 V	2		5.5	V
V <sub>IH</sub>	Diver high-lever input voltage, Div	V <sub>CC</sub> = 5 V	2.4		3.6 5.5	v
$V_{IL}$	Driver low-level input voltage, DIN		0		0.8	V
$V_{I}$	Receiver input voltage		-25		25	<b>V</b>
T <sub>A</sub>	Operating free-air temperature		-40		125	ç

<sup>(1)</sup> Test conditions are C1–C4 = 0.1  $\mu$ F at  $V_{CC}$  = 3.3 V ± 0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at  $V_{CC}$  = 5 V ± 0.5 V.

## **ELECTRICAL CHARACTERISTICS**(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN TYP <sup>(2)</sup>	MAX	UNIT
$I_{CC}$	Supply current	No load, $V_{CC} = 3.3 \text{ V or 5 V}$	0.3	1	mA

Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.

All voltages are with respect to network GND.

Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability. The package thermal impedance is calculated in accordance with JESD 51-7.

All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25 ^{\circ}\text{C}$ .

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#### DRIVER SECTION

## **ELECTRICAL CHARACTERISTICS**(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

	PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{OH}$	High-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND, DIN = GND	5	5.4		٧
$V_{OL}$	Low-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND, DIN = $V_{CC}$	<b>-</b> 5	-5.4		<b>V</b>
$I_{\text{IH}}$	High-level input current	$V_I = V_{CC}$		±0.01	±1	μΑ
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> at GND		±0.01	±1	μΑ
(3)	Short circuit output ourrent	$V_{CC} = 3.6 \text{ V}, V_{O} = 0 \text{ V}$		±35	±60	~ ^
I <sub>OS</sub> (3)	Short-circuit output current	$V_{CC} = 5.5 \text{ V}, V_{O} = 0 \text{ V}$		±35	±60	mA
r <sub>o</sub>	Output resistance	$V_{CC}$ , V+, and V- = 0 V, $V_{O}$ = ±2 V	300	10M		Ω

Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.

## SWITCHING CHARACTERISTICS(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST C	ONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
	Maximum data rate	$C_L$ = 1000 pF, $R_L$ = 3 k $\Omega$ , One DOUT switching, See Figure 1		150	250		kbit/s	
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	$C_L$ = 150 pF to 2500 pF, $R_L$ = 3 k $\Omega$ to 7 k $\Omega$ , See Figure 2			300		ns	
CD(+*)	Slew rate, transition region	$R_L = 3 k\Omega$ to $7 k\Omega$ ,	C <sub>L</sub> = 150 pF to 1000 pF	6		30	1//	
SR(tr)	(see Figure 1)	$V_{CC} = 3.3 \text{ V}$ $C_L = 150 \text{ pF to } 2500 \text{ pF}$		$I_{CC} = 3.3 \text{ V}$ $I_{C} = 150 \text{ pF to } 2500 \text{ pF}$ 4	4		30	V/μs

Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.

#### **ESD PROTECTION**

		TYP	UNIT
	Human-Body Model (HBM)	±15	
Driver outputs (DOUTx)	outputs (DOUTx) IEC61000-4-2, Air-Gap Discharge	±15	kV
	IEC61000-4-2, Contact Discharge	±8	

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All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25 ^{\circ}\text{C}$ . Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

All typical values are at  $V_{CC}$  = 3.3 V or  $V_{CC}$  = 5 V, and  $T_A$  = 25°C. Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

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#### RECEIVER SECTION

## **ELECTRICAL CHARACTERISTICS**(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

	PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -1 \text{ mA}$	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.1		V
$V_{OL}$	Low-level output voltage	I <sub>OL</sub> = 1.6 mA			0.4	V
V	Decitive going input threshold voltage	V <sub>CC</sub> = 3.3 V		1.5	2.4	V
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 5 V		1.8	2.4	V
V	No notice acioni in out through ald coltano	V <sub>CC</sub> = 3.3 V	0.6	1.2		V
V <sub>IT</sub> _	Negative-going input threshold voltage	V <sub>CC</sub> = 5 V	0.8	1.5		V
$V_{hys}$	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.3		V
r <sub>i</sub>	Input resistance	V <sub>I</sub> = ±3 V to ±25 V	3	5	7	kΩ

Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V ± 0.5 V. All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## **SWITCHING CHARACTERISTICS**(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 3)

	PARAMETER	TEST CONDITIONS	TYP <sup>(2)</sup>	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C 450 pF	300	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	$C_L = 150 \text{ pF}$	300	ns
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>		300	ns

<sup>(1)</sup> Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V ± 0.5 V. (2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C. (3) Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

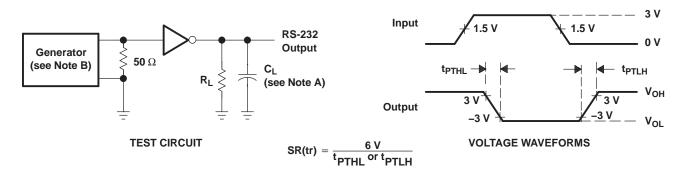
#### **ESD PROTECTION**

		TYP	UNIT
	Human-Body Model (HBM)	±15	
Receiver inputs (RINx)	IEC61000-4-2, Air-Gap Discharge	±15	kV
	IEC61000-4-2, An-Gap Discharge	±8	

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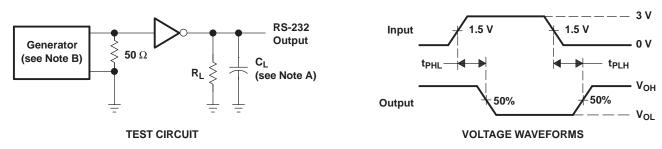
#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \le 10$  ns.  $t_f \le 10$  ns.

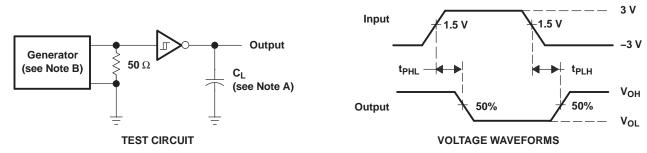
Figure 1. Driver Slew Rate



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \le 10$  ns,  $t_f \le 10$  ns.

Figure 2. Driver Pulse Skew



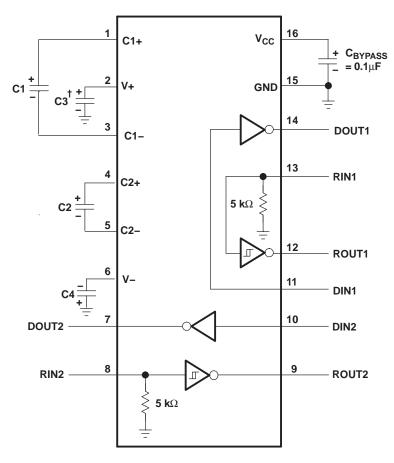
NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_O = 50~\Omega$ , 50% duty cycle,  $t_f \le 10$  ns.  $t_f \le 10$  ns.

Figure 3. Receiver Propagation Delay Times

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## **APPLICATION INFORMATION**



 $<sup>^{\</sup>dagger}$  C3 can be connected to  $V_{CC}\, or \, GND.$ 

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V<sub>CC</sub> vs CAPACITOR VALUES

V <sub>CC</sub>	C1	C2, C3, C4		
$\begin{array}{c} \textbf{3.3 V} \pm \textbf{0.3 V} \\ \textbf{5 V} \pm \textbf{0.5 V} \\ \textbf{3 V to 5.5 V} \end{array}$	0.1 μF 0.047 μF 0.1 μF	0.1 μF 0.33 μF 0.47 μF		

Figure 4. Typical Operating Circuit and Capacitor Values

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TRS3232EQPWRQ1	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RS32EQ
TRS3232EQPWRQ1.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RS32EQ
TRS3232EQPWRQ1.B	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RS32EQ

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF TRS3232E-Q1:

Catalog : TRS3232E

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



## **PACKAGE OPTION ADDENDUM**

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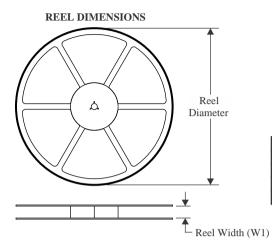
NOTE: Qualified Version Definitions:

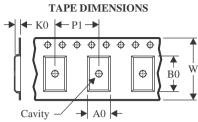
 $_{\bullet}$  Catalog - TI's standard catalog product

## **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3232EQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## **PACKAGE MATERIALS INFORMATION**

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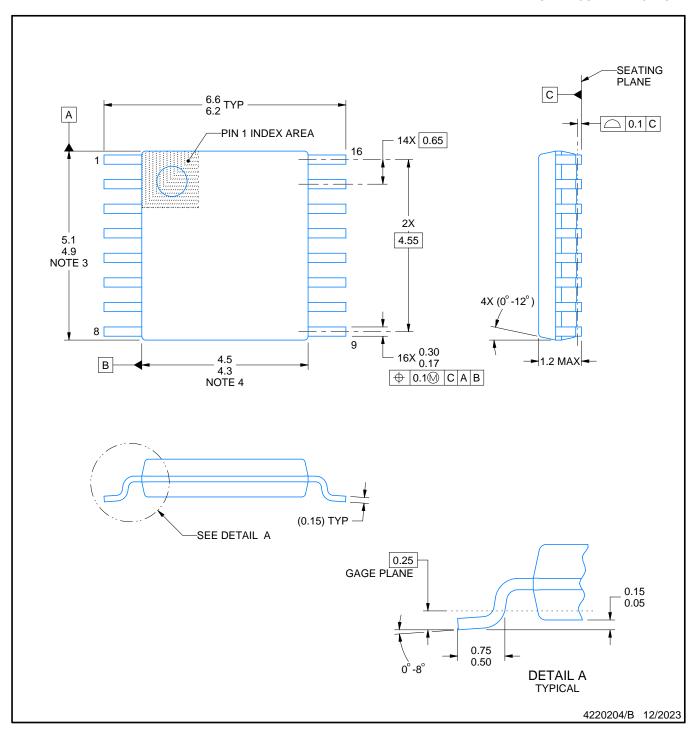


### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
TRS3232EQPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0	



SMALL OUTLINE PACKAGE



#### NOTES:

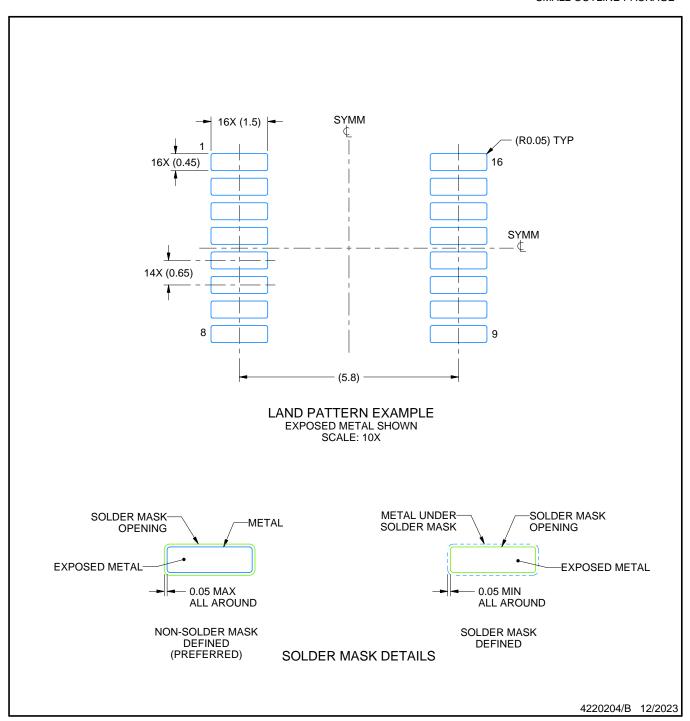
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE

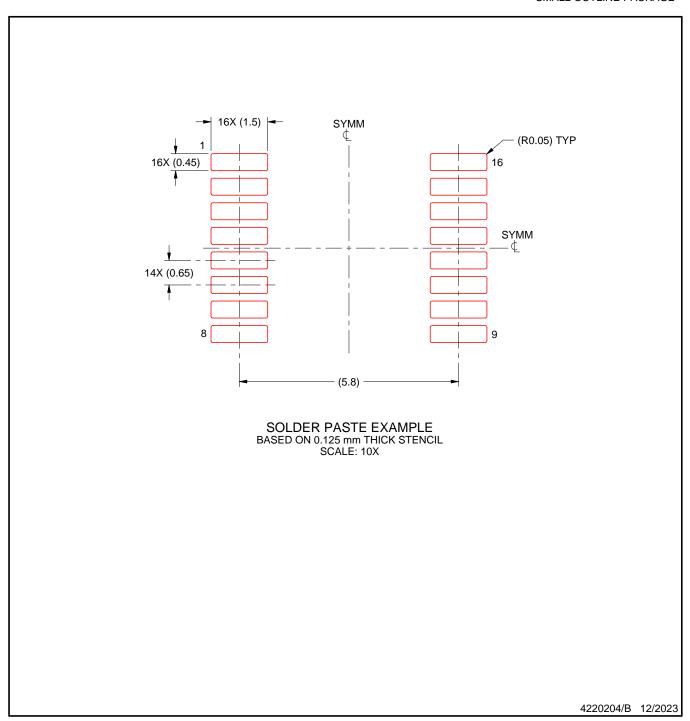


NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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