TPSM8287Cx0 30A, 40A, and 50A, Parallelable Step-Down Power Modules With I²C Interface, Remote Sense, and Telemetry in a MagPack™ Package

ADVANCE INFORMATION

1 Features

- 2.8V to 6V input voltage range
- Up to 50A continuous output current
- ±0.8% output voltage accuracy
- Telemetry for V_{IN}, temperature, V_{OUT}, and I_{OUT}
- Single or multiphase-configuration with configurable phase shift
- 0.4V to 1.0V output voltage range
- Selectable switching frequency
- Optimized load transient operation
  - Fixed frequency DCS-Control
  - Non-synchronous mode for load release voltage suppression
  - Externally adjustable compensation
- I²C-compatible interface with up to 3.4MHz
- Differential remote sense
- Thermal prewarning and thermal shutdown
- Output discharge
- Power-good and interrupt output
- –40°C to 150°C junction temperature range
- Available in 4.5mm × 6.7mm VQFN package
- 85mm² design size

2 Applications

- FPGA, ASIC, and digital core supply
- Optical networks
- Storage
- Aerospace and defense
- Test and measurement

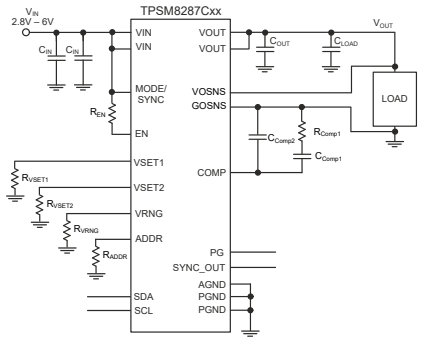
3 Description

The TPSM8287Cx0 devices are a family of pin-to-pin 30A, 40A and 50A synchronous step-down DC/DC converter modules with I²C interface and differential remote sense. Ultra low-resistance power switches allow up to 50A continuous output current at high ambient temperatures. The module can be used in single or multiphase configuration (stack mode). In stacked mode, the modules share a common synchronization signal, phase shift the phase to supply loads with several hundreds of Amperes. The TPSM8287Cx0 family implements a fixed-frequency DCS-Control scheme with adjustable switching frequency and adjustable loop compensation. The flexible switching frequency and high loop bandwidth enable the use of low output capacitance. The module can operate in power-safe mode for maximum efficiency or forced-PWM mode for best transient performance and lowest output voltage ripple. The I²C compatible interface offers several control, monitoring and warning features. The devices feature V_{IN}, V_{OUT}, output current, and temperature readback capability. The VSETx and VRNG pins set the default start-up voltage and the ADDR pin configures the I2C address.

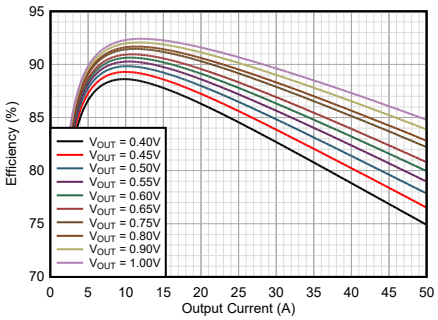
Device Information

PART NUMBER	CURRENT RATING(3)	PACKAGE(1)	PACKAGE SIZE(2)
TPSM8287C30(4)	30A	VCR (QFN-FCMOD, 33)	6.7mm × 4.5mm
TPSM8287C40(4)	40A		
TPSM8287C50	50A		

(1) For more information, see Section 8.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) See the *Device Comparison Table*.
(4) Preview information (not Advance Information).



TPSM8287Cx0 Simplified Schematic



Efficiency TPSM8287C50x (V_{IN} = 3.3V; 833kHz)

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4 Device Comparison Table

ORDERABLE PART NUMBER(1)	OUTPUT CURRENT	DEFAULT f_{SW}	NOMINAL INDUCTANCE
TPSM8287C30TAPVCRR(2)	30A	1.250MHz	70nH ± 20%
TPSM8287C40TAPVCRR(2)	40A	1.250MHz	
TPSM8287C50TAPVCRR	50A	1.250MHz	

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) Preview information (not Advance Information).

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5 Pin Configuration and Functions

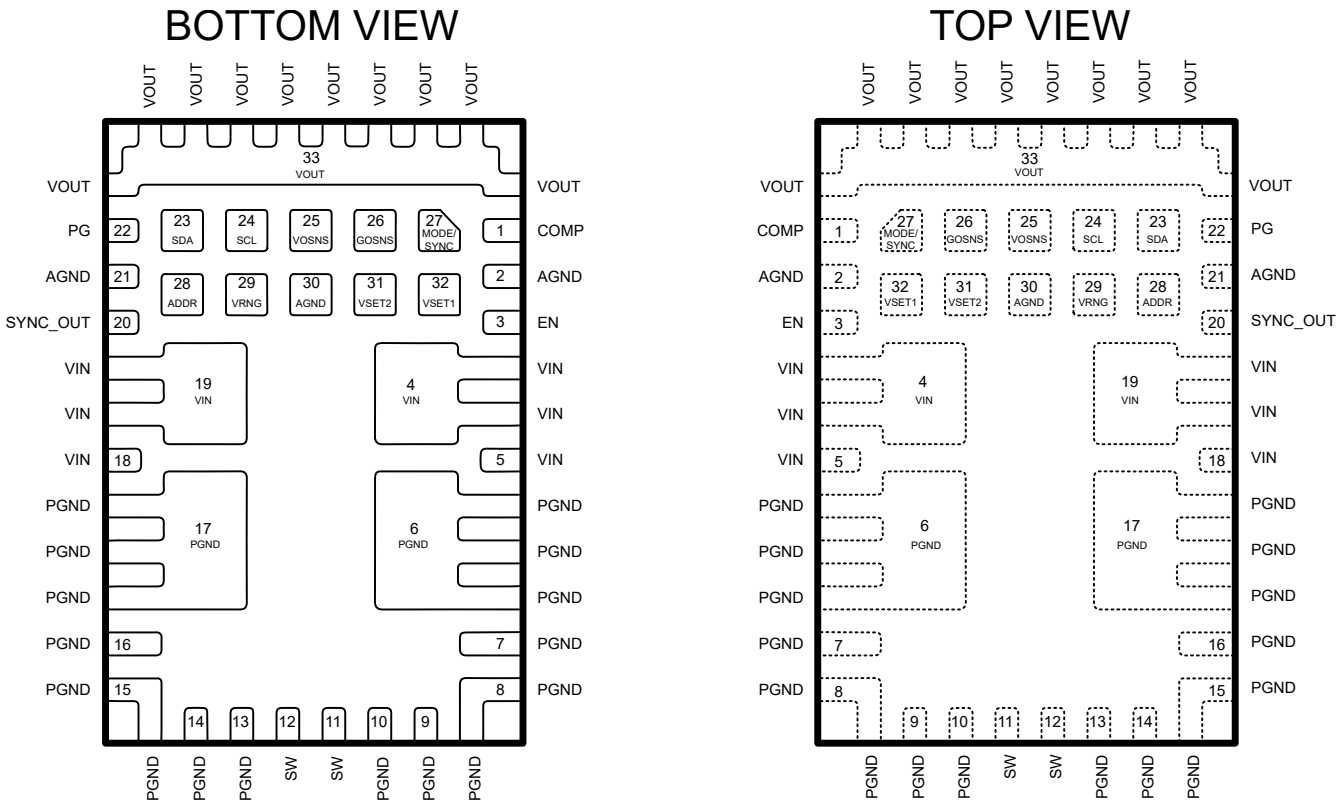


Figure 5-1. VCR Package, 33-Pin QFN-FCMOD

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	COMP	I/O	Device or stack compensation input. A resistor and capacitor from this pin to AGND defines the compensation of the control loop. In stacked operation, connect the COMP pins of all devices together.
2, 21,30	AGND	I/O	Analog Ground pin
3	EN	I/O	This pin is the enable pin of the device. The user must connect to this pin using a series resistor of at least 15kΩ. A low logic level on this pin disables the device, and a high logic level on this pin enables the device. Do not leave this pin unconnected. For stacked operation, connect the EN pins of all stacked devices together with a resistor to the supply voltage or a GPIO of a processor.
4, 5,18, 19	VIN	P	Power supply input. Connect the input capacitor as close as possible between pin VIN and GND.
6, 7, 8, 9, 10, 13, 14, 15, 16, 17	PGND	GND	PGND pins
11, 12	SW	O	This pin is the switch pin of the converter and is connected to the internal Power MOSFETs. This pin can be left floating.
20	SYNC_OUT	I/O	Internal clock output pin. For stacked operation,connect the MODE/SYNC pin of the secondary devices to the SYNC_OUT of the primary device. During start-up, this pin is used to identify primary converter and secondary converters in stacked operation.

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Table 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
22	PG	I/O	Power Good and Interrupt (nINT) open drain output. Low impedance when "power bad" or "interrupt", high impedance when "power good" or "no interrupt". This pin can be left open or be tied to GND when not used in single device operation. In stacked operation interconnect the PG pins of all stacked devices. During start-up, only the PG pin of the primary converter in stacked operation is an open drain output, the secondaries use the pin as an input. After soft start has finished, the pin can be used as an output on all devices.
23	SDA	I/O	I^2C serial data pin. Do not leave this pin floating. Connect a pullup to logic high level.
24	SCL	I	I^2C serial clock pin. Do not leave this pin floating. Connect a pullup resistor to a logic high level.
25	VOSNS	I	Output voltage sense (differential output voltage sensing)
26	GOSNS	I	Output ground sense (differential output voltage sensing)
27	MODE/SYNC	I	The device operates in Auto DCM/CCM mode when this pin is pulled low. If the pin is pulled high, the device runs in forced-PWM mode. Do not leave this pin unconnected. The mode pin can also be used to synchronize the device to an external clock. When used as secondary, connect the MODE/SYNC to the SYNC_OUT of the primary device.
28	ADDR	I	Default setting pin for I2C device address. A resistor or short-circuit to GND or V_{IN} defines the selected address.
29	VRNG	I	Default setting pin for V_{OUT}-range (high or low) combined with transient-asynchronous-mode (on/off). A resistor or short circuit to GND or V_{IN} defines the selected combination.
31	VSET2	I	Default setting pin for target V_{OUT} within selected range through VRNG. A resistor or short circuit to GND or V_{IN} defines the selected output voltage.
32	VSET1	I	Default setting pin for target V_{OUT} within selected range through VRNG. A resistor or short circuit to GND or V_{IN} defines the selected output voltage.
33	VOUT	P	Output voltage pin

(1) I = input, O = output, P = power, GND = ground

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6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Achieving a clean startup by using a DC/DC converter with a precise enable-pin threshold* analog design journal

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.4 Trademarks

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6.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

DATE	REVISION	NOTES
October 2026	*	Initial release

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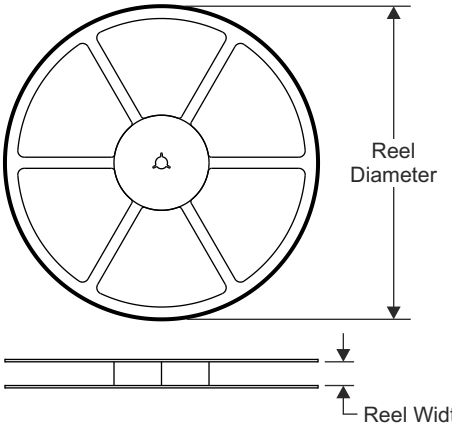
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8 Mechanical, Packaging, and Orderable Information

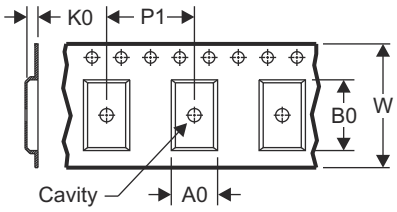
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, see also the left-hand navigation.

8.1 Tape and Reel Information

REEL DIMENSIONS

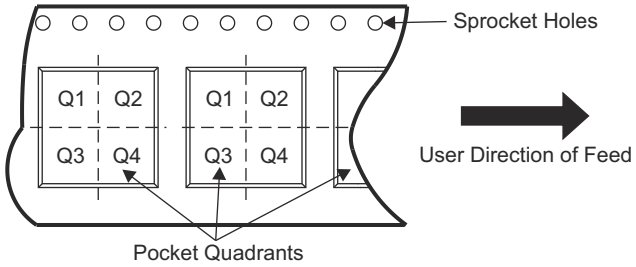


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



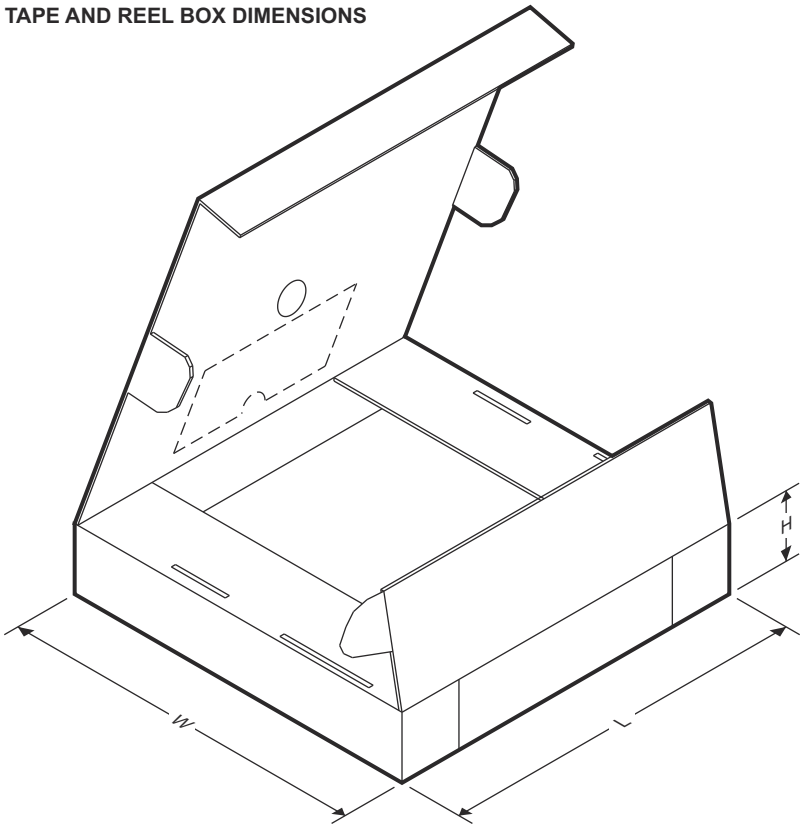
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XPSM8287C50TAPVCRR	QFN-FCMOD	VCR	33	1500	330	12.4	4.8	7	3.2	8	16	Q1

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XPSM8287C50TAPVCRR	QFN-FCMOD	VCR	33	1500	367	367	35

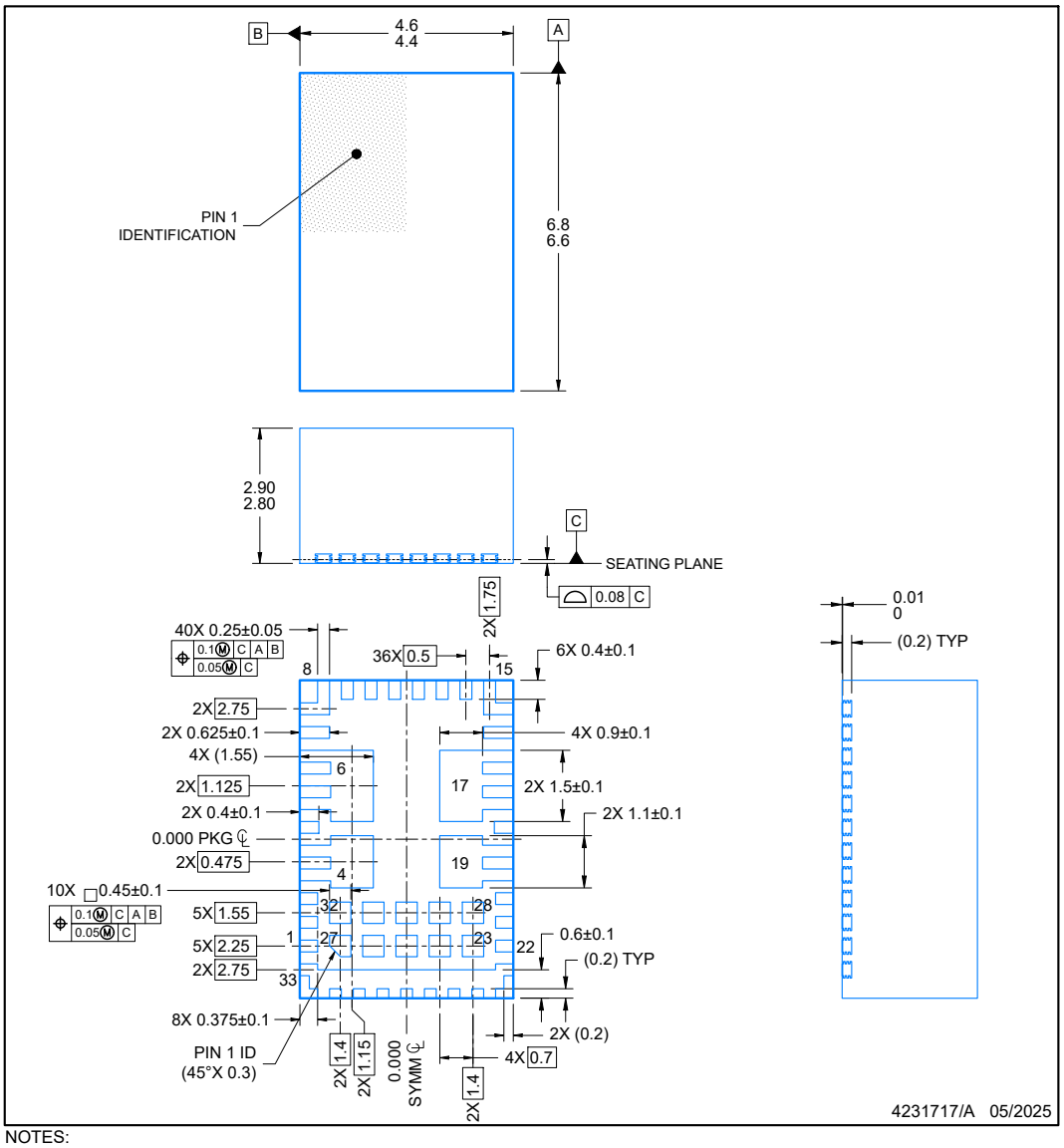
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PACKAGE OUTLINE

VCR0033A

QFN-FCMOD - 2.9 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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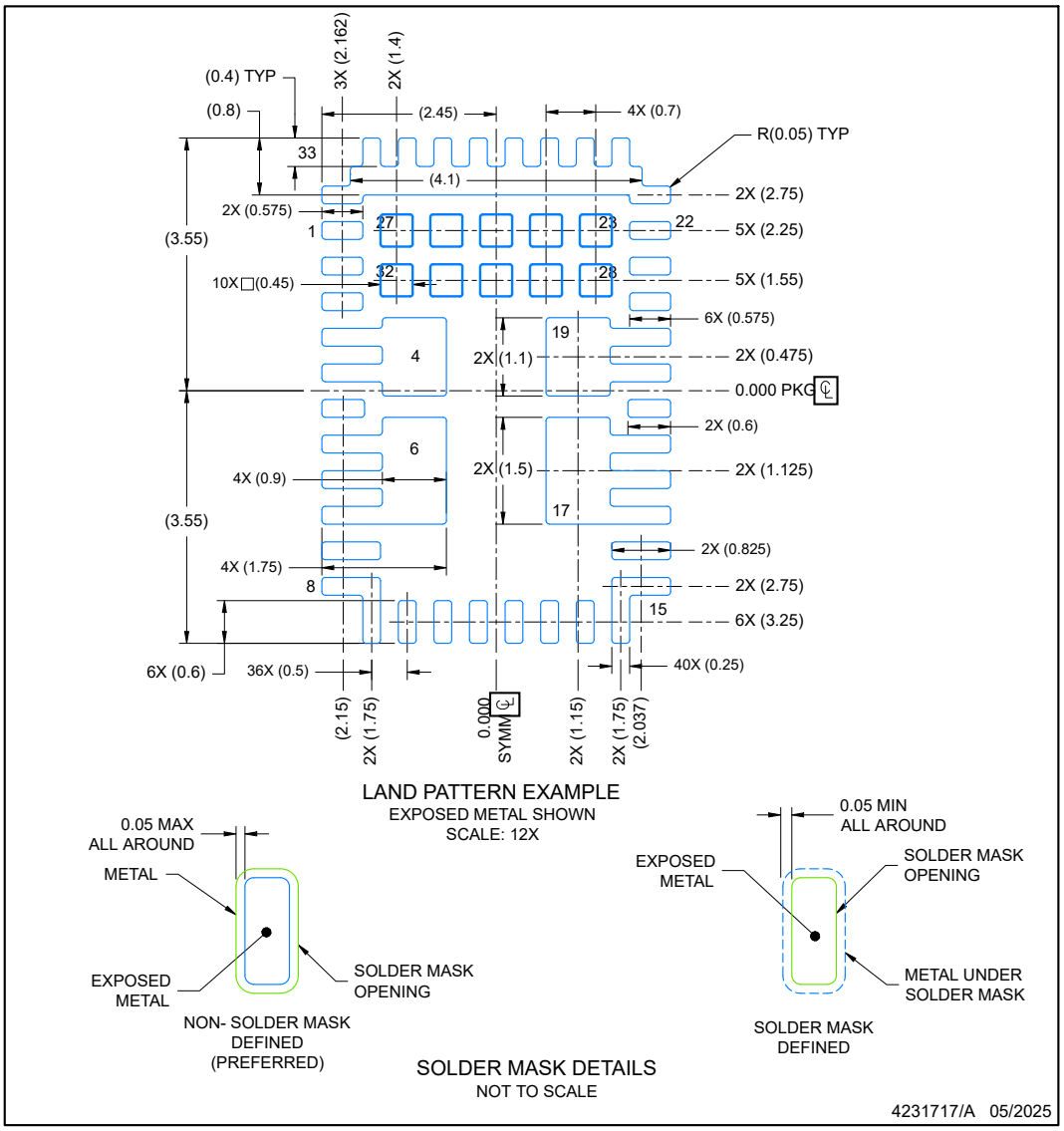
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EXAMPLE BOARD LAYOUT

VCR0033A — **QFN-FCMOD - 2.9 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

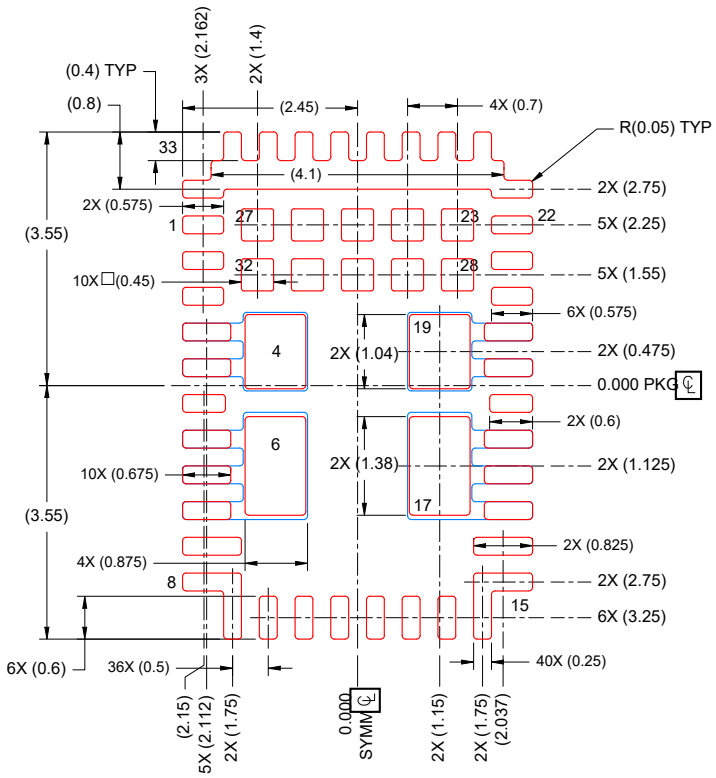
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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EXAMPLE STENCIL DESIGN

VCR0033A — **QFN-FCMOD - 2.9 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PIN 4 & 19 : 86.3%
PIN 6 & 17 : 84.5%

SCALE: 12X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XPSM8287C50TAPVCRR	Active	Preproduction	QFN-FCMOD (VCR) | 33	2500 | LARGE T&R	-			-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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