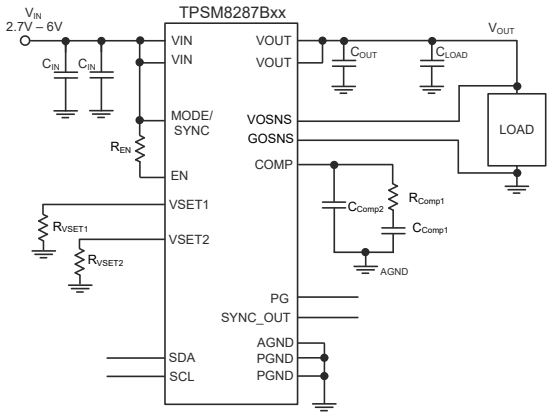
TPSM8287Bxx 2.7V to 6V Input, 15A, 20A, 25A, and 30A, Parallelable, Step-Down Power Modules With I²C Interface and Remote Sense in a MagPack™ Package

1 Features

- ±0.8% output voltage accuracy
- Differential remote sensing
- Parallelable for multiphase operation
- Start-up output voltage and I²C addresses selectable through VSETx pins:
  - 0.4V to 0.775V in 25mV steps
  - 0.8V to 1.55V in 50mV steps
- Output voltage I²C adjustable in 1.25mV steps
- Adjustable external compensation for wide output capacitor range and optimized transient response
- Designed for low EMI requirements
  - MagPack technology shields inductor and IC
  - No bond wire package
  - Optional internal input and output capacitors
  - Simplified layout through parallel input path
  - Optional synchronization to external clock or spread-spectrum operation
- Optional droop compensation through I²C
- Power save mode or forced PWM operation
- Precise enable input threshold
- Power-good output with window comparator
- Active output discharge
- Excellent thermal performance
- -40°C to 125°C operating temperature range
- 3.75mm × 8.0mm QFN package with 0.5mm pitch
- 66mm² design size

2 Applications

- FPGA, ASIC, and SoC digital core supply
- Optical networks
- Test and measurement equipment
- Sensors, imaging, and radar



TPSM8287Bxx Simplified Schematic

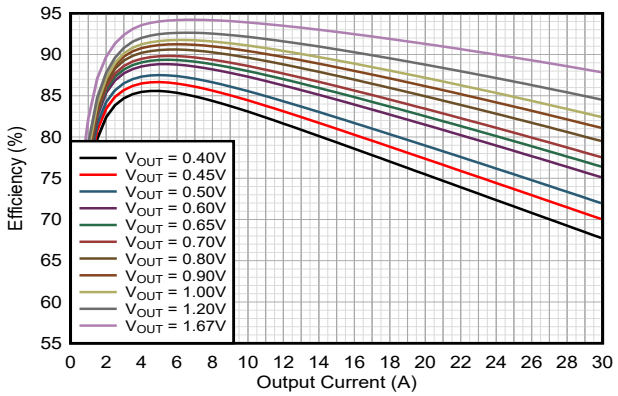
3 Description

The TPSM8287Bxx is a family of pin-to-pin, step-down, DC/DC power modules with differential remote sensing and I²C interface. The power modules use TI's MagPack technology to integrate a synchronous step-down converter, an inductor, input and output capacitors to simplify design, reduce external components and save PCB area. The low-profile and compact design is designed for assembly by standard surface mount equipment. The TPSM8287Bxx family implements an enhanced control scheme that supports fast transients. The TPSM8287Bxx can operate in fixed-frequency or power save mode. The remote sensing feature optimizes voltage regulation at the point-of-load and the device achieves ±0.8% DC voltage accuracy over the entire temperature range. The devices can operate in stacked, paralleled mode to deliver higher output currents or to spread the power dissipation across multiple devices. The I²C-compatible interface offers several control, monitoring, and warning features. The start-up voltage is selectable through the VSETx pins to allow a power-up without an active I²C communication.

Device Information

PART NUMBER(2)	CURRENT RATING	PACKAGE(1)	PACKAGE HEIGHT
TPSM8287B15x	15A	VCH (VQFN, 37)	1.95mm (2.0mm maximum)
TPSM8287B20x	20A		
TPSM8287B25x	25A		
TPSM8287B30x	30A		

(1) For more information, see Section 12.
(2) For available devices, see the *Device Options* table.



Efficiency TPSM8287B30x (V_{IN} = 3.3V; FPWM)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Device Options....3
5 Pin Configuration and Functions....4
6 Specifications....6
6.1 Absolute Maximum Ratings....6
6.2 ESD Ratings....6
6.3 Recommended Operating Conditions....6
6.4 Thermal Information....7
6.5 Electrical Characteristics....7
6.6 I^2C Interface Timing Requirements....10
6.7 Typical Characteristics....12
7 Detailed Description....13
7.1 Overview....13
7.2 Functional Block Diagram....13
7.3 Feature Description....14
7.4 Device Functional Modes....30
7.5 Programming....31
8 Device Registers....35
9 Application and Implementation....41
9.1 Application Information....41
9.2 Typical Application....41
9.3 Typical Application Using Two TPSM8287B30x in Parallel Operation....53
9.4 Power Supply Recommendations....60
9.5 Layout....60
10 Device and Documentation Support....63
10.1 Device Support....63
10.2 Documentation Support....63
10.3 Receiving Notification of Documentation Updates....63
10.4 Support Resources....63
10.5 Trademarks....63
10.6 Electrostatic Discharge Caution....63
10.7 Glossary....63
11 Revision History....64
12 Mechanical, Packaging, and Orderable Information....65

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4 Device Options

Table 4-1. Devices With I²C Interface

ORDERABLE PART NUMBER(1)	OUTPUT CURRENT	START-UP VOLTAGE SELECTION THROUGH VSETx PINS	INTEGRATED CAPACITORS	NOMINAL INDUCTANCE	DEFAULT OPERATING FREQUENCY
TPSM8287B15LAPVCHR(2)	15A	0.4 – 0.775V (in 25mV steps)	C_{IN} = 4 × 22nF C_{OUT} = 2 × 22nF + 2 × 10µF	50nH ± 20%	1.5MHz
TPSM8287B15HAPVCHR(2)	15A	0.8 – 1.55V (in 50mV steps)			
TPSM8287B20LAPVCHR(2)	20A	0.4 – 0.775V (in 25mV steps)			
TPSM8287B20HAPVCHR(2)	20A	0.8 – 1.55V (in 50mV steps)			
TPSM8287B25LAPVCHR(2)	25A	0.4 – 0.775V (in 25mV steps)			
TPSM8287B25HAPVCHR(2)	25A	0.8 – 1.55V (in 50mV steps)			
TPSM8287B30LAPVCHR(3)	30A	0.4 – 0.775V (in 25mV steps)			
TPSM8287B30HAPVCHR(2)	30A	0.8 – 1.55V (in 50mV steps)			
TPSM8287B15LANVCHR	15A	0.4 – 0.775V (in 25mV steps)	no Caps		
TPSM8287B15HANVCHR	15A	0.8 – 1.55V (in 50mV steps)			
TPSM8287B20LANVCHR	20A	0.4 – 0.775V (in 25mV steps)			
TPSM8287B20HANVCHR	20A	0.8 – 1.55V (in 50mV steps)			
TPSM8287B25LANVCHR	25A	0.4 – 0.775V (in 25mV steps)			
TPSM8287B25HANVCHR	25A	0.8 – 1.55V (in 50mV steps)			
TPSM8287B30LANVCHR	30A	0.4 – 0.775V (in 25mV steps)			
TPSM8287B30HANVCHR	30A	0.8 – 1.55V (in 50mV steps)			

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview information (not Production Data).
(3) Advance information (not Production Data).

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5 Pin Configuration and Functions

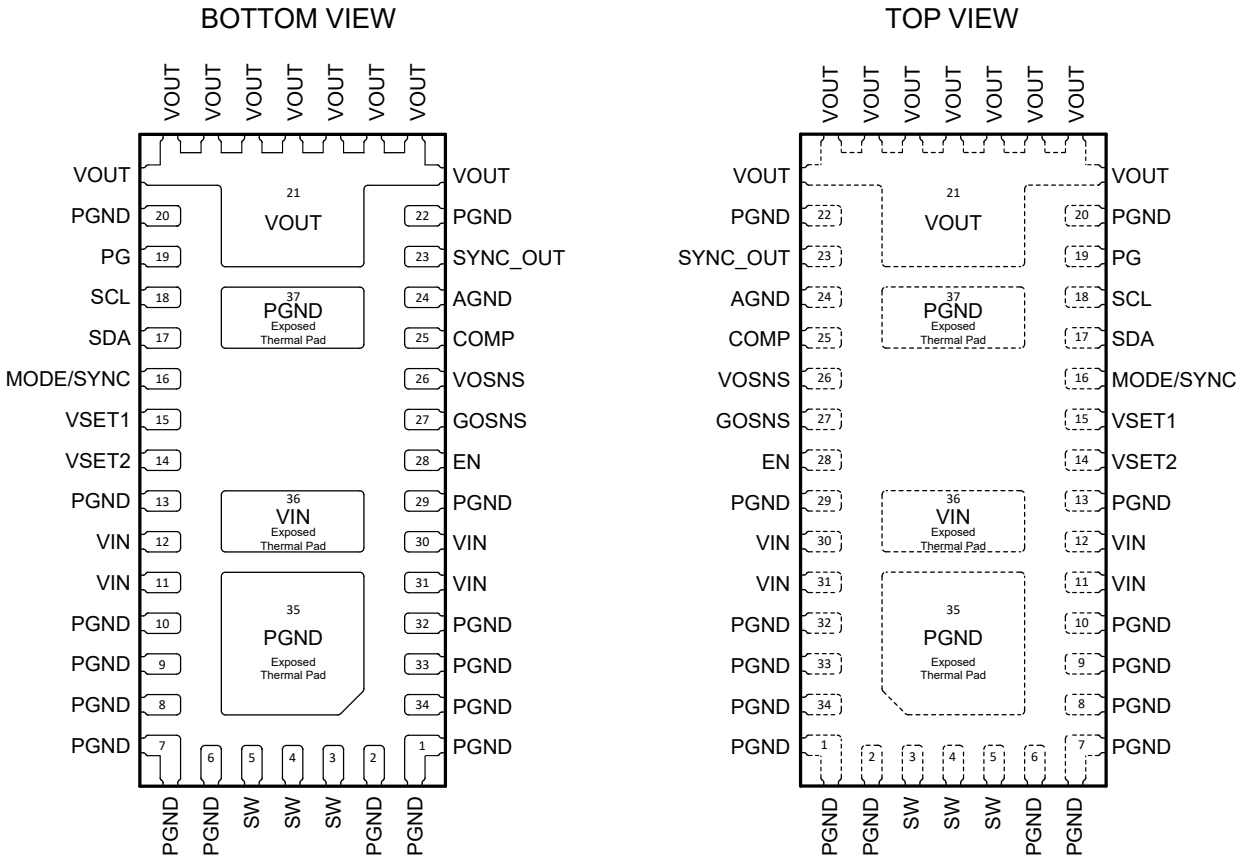


Figure 5-1. TPSM8287Bxx VCH Package, VQFN 37 Pin

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
27	GOSNS	I	Output ground sense (differential output voltage sensing). Connect at the load.
26	VOSNS	I	Output voltage sense (differential output voltage sensing). Connect at the load.
28	EN	I/O	This pin is the enable pin of the device. The user must connect to the pin using a series resistor of at least 15kΩ. A low logic level on this pin disables the device, and a high logic level on this pin enables the device. For stacked operation, connect the EN pins of all stacked devices together with a resistor to the supply voltage or a GPIO of a processor. See *Stacked Operation* for a detailed description.
11, 12, 30, 31	VIN	P	Power supply input. Connect an input capacitor as close as possible between each VIN and PGND (on both sides of the package).
1, 2, 6 – 10, 13, 20, 22, 29, 32 – 34	PGND	GND	Ground pin
21	VOUT	P	Output voltage pin
3 – 5	SW	O	This pin is the switch pin of the converter and is connected to the internal Power MOSFETs. This pin can be left floating.

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Table 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
19	PG	I/O	Open-drain power-good output with window comparator. This pin is pulled to GND while VOUT is outside the power-good threshold. This pin can be left open or tied to GND if not used in single device operation. A pullup resistor can be connected to any voltage not larger than 6.5V. In stacked operation, connect the PG pins of all stacked devices together. Only the PG pin of the primary converter in stacked operation is an open drain output. For devices that are defined as secondary converters in stacked mode, the pin is an input pin. See *Stacked Operation* for a detailed description.
16	MODE/SYNC	I	The device runs in power save mode when this pin is pulled low. If the pin is pulled high, the device runs in forced PWM mode. If unused, this pin can be left floating and an internal pulldown resistor pulls the pin low. The pin can also be used to synchronize the device to an external clock. See Section 7.3.7 for a detailed description.
17	SDA	I/O	I^2C serial data pin. Do not leave floating. Connect a pullup resistor to a logic high level. For secondary devices in stacked operation, or if the I^2C interface is not used, connect the pin to GND.
18	SCL	I	I^2C serial clock pin. Do not leave this pin floating. Connect a pullup resistor to a logic high level. For secondary devices in stacked operation, or if the I^2C interface is not used, connect the pin to GND.
23	SYNC_OUT	I/O	Internal clock output pin for synchronization in stacked mode. Leave this pin floating for single device operation. Connect this pin to the MODE/SYNC pin of the next device in the daisy-chain in stacked operation. *Do not use this pin to connect to a non-TPSM8287Bxx device.* During start-up, this pin is used to identify if a device must operate as a secondary converter in stacked operation. Connect a 47kΩ resistor from this pin to GND to define a secondary converter in stacked operation. See *Stacked Operation* for a detailed description.
15	VSET1	I/O	Start-up output voltage and I^2C address selection pin. A resistor or short circuit to GND or V_{IN} defines the selected output voltage and I^2C address. See Table 7-2.
14	VSET2	I/O	
25	COMP	I/O	Device compensation input. A resistor and capacitor from this pin to AGND define the compensation of the control loop. In stacked operation, connect the COMP pins of all stacked devices together and connect a resistor and capacitor between the common COMP node and AGND.
35, 37	PGND Exposed Thermal Pad	GND	The thermal pad must be soldered to GND to achieve an appropriate thermal resistance and for mechanical stability.
36	VIN Exposed Thermal Pad	P	The thermal pad must be soldered to VIN to achieve an appropriate thermal resistance and for mechanical stability.
24	AGND	GND	Analog Ground. Connect to GND.

(1) I = input, O = output, P = power, GND = ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VSET1, VSET2, EN, MODE/SYNC ,PG, VIN	–0.3	6.5	V
	SW (DC)	–0.3	V_{IN} + 0.3	
	SW (AC, less than 10ns)(3)	–3	10	
	COMP	–0.3	5.0V or V_{IN}(4)	
	VOUT	–0.3	2.5	
	VOSNS	–0.3	1.8	
	SCL, SDA	–0.3	5.5	
	SYNC_OUT	–0.3	2	
	GOSNS	–0.3	0.3	
Current	COMP	–1	1	mA
	SYNC_OUT	–1	1	
	EN		2.5	
	SDA		9	
	PG		10	
Inductance	Parasitic input loop impedance		1.2	nH
T_J	Junction temperature	–40	125	°C
T_{stg}	Storage temperature	–40	125	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal.
(3) While switching.
(4) Whatever value is lower

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		6	V
V_{OUT}	Output voltage range	0.4		1.675V or (V_{IN} – 1.5V)(1)	V
V_{SCL}, V_{SDA}	Nominal pullup voltage on pins SDA and SCL	1.2		5	V
C_{IN}	Effective input capacitance (see Selecting the Input Capacitors)	20			µF
C_{OUT}	Effective output capacitance	47		(2)	µF
C_{PAR}	Parasitic capacitance on VSET1, VSET2 pin			100	pF
C_{PAR}	Parasitic capacitance on SYNC_OUT pin			20	pF

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6.3 Recommended Operating Conditions (continued)

		MIN	NOM	MAX	UNIT
R_{EN}	Pull-up resistance on EN pin	15			kΩ
R_{VSET1}, R_{VSET2}	Resistance on VSETx, if not directly tied to GND or VIN	37.6	47	56.4	kΩ
R_{SYNC_OUT}	Resistor value	37.6	47	56.4	kΩ
I_{SINK_PG}	Sink current at PG pin	0		1	mA
T_J	Operating junction temperature	–40		125	°C

(1) Whatever V_{OUT} value is lower.
(2) The maximum recommended output capacitance depends on the specific operating conditions of an application. Output capacitance values of up to a few millifarads are typically possible.

6.4 Thermal Information

THERMAL METRIC(1)		TPSM8287Bxx VCH (37 PINS)		UNIT
		JEDEC 51-5	EVM	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.8	11.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.2	n/a(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.4	n/a(2)	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.0	n/a(2)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.2	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.2	5.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Not applicable to an EVM.

6.5 Electrical Characteristics

over operating junction temperature (T_J = –40°C to +125°C) and V_{IN} = 2.7V to 6V. Typical values at V_{IN} = 5V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = High, I_{OUT} = 0mA, device not switching, MODE/SYNC = Low, FPWMEN = 0, SINGLE = 1		2	4.6	mA
I_{SD}	Shutdown current	EN = Low, V_{VOUT} = 0V		18	450	µA
$V_{IT+(UVLO)}$	Positive-going UVLO threshold voltage (VIN)		2.5	2.6	2.7	V
$V_{IT-(UVLO)}$	Negative-going UVLO threshold voltage (VIN)		2.4	2.5	2.6	V
$V_{hys(UVLO)}$	UVLO hysteresis voltage (VIN)		80			mV
$V_{IT+(OVLO)}$	Positive-going OVLO threshold voltage (VIN)		6.1	6.3	6.5	V
$V_{IT-(OVLO)}$	Negative-going OVLO threshold voltage (VIN)		6.0	6.2	6.4	V
$V_{hys(OVLO)}$	OVLO hysteresis voltage (VIN)		80			mV
$V_{IT-(POR)}$	Negative-going power-on reset threshold voltage (VIN)		1.4			V

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6.5 Electrical Characteristics (continued)

over operating junction temperature (T_J = –40°C to +125°C) and V_{IN} = 2.7V to 6V. Typical values at V_{IN} = 5V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD}	Thermal shutdown threshold temperature	T_J rising		170		°C
	Thermal shutdown hysteresis			20		°C
T_W	Thermal warning threshold temperature	T_J rising		150		°C
	Thermal warning hysteresis			20		°C
CONTROL and INTERFACE						
V_{IT+}	Positive-going input threshold voltage (EN)		0.97	1.0	1.03	V
V_{IT-}	Negative-going input threshold voltage (EN)		0.87	0.9	0.93	V
V_{hys}	Hysteresis voltage (EN)		95			mV
I_{IH}	High-level input current (EN)	SINGLE = 1			3	µA
I_{IL}	Low-level input current (EN)	SINGLE = 1	–200			nA
V_{IH}	High-level input voltage (MODE/SYNC, VSET1, VSET2, SYNC_OUT, PG)		0.8			V
V_{IH}	High-level input voltage (SDA, SCL)		0.95			V
V_{IL}	Low-level input voltage (MODE/SYNC, VSET1, VSET2, SYNC_OUT, PG)				0.4	V
V_{IL}	Low-level input voltage (SDA, SCL)				0.5	V
R_{IN}	Input resistance to GND on pins MODE/SYNC, EN and PG		2	3	4	MΩ
V_{OL}	Low-level output voltage (SDA)	I_{OL} = 9mA			0.4	V
V_{OL}	Low-level output voltage (SDA)	I_{OL} = 5mA			0.2	V
$C_{IO(SDA/SCL)}$	SDA/SCL pin capacitance			10		pF
I_{LKG}	Input leakage current into SDA, SCL	V_{OH} = 3.3V			200	nA
I_{IL}	Low-level input current (MODE/SYNC)		–100		100	nA
I_{IH}	High-level input current (MODE/SYNC)				3	µA
$t_{d(EN)1}$	Enable delay time when EN tied to V_{IN}	Measured from when EN goes high to when device starts switching, SR_{VIN} = 1V/µs		200	600	µs
$t_{d(EN)2}$	Enable delay time when V_{IN} already applied	Measured from when EN goes high to when device starts switching		40	100	µs
$t_{d(Ramp_PG)}$	Output voltage ramp time for SSTIME = 00	Measured from when device starts switching to rising edge of PG ($t_{d(Ramp)}$ + $t_{d(PG)}$)	0.38	0.54	0.7	ms
	Output voltage ramp time for SSTIME = 01		0.57	0.81	1.05	ms
	Output voltage ramp time for SSTIME = 10, default		0.73	1.04	1.35	ms
	Output voltage ramp time for SSTIME = 11		1.43	2.04	2.65	ms
$f_{(SYNC)}$	Synchronization clock frequency range (MODE/SYNC)	$f_{(SW)nom}$ = 1.5MHz, $D_{(MODE/SYNC)}$ = 45%...55%	1.2		1.8	MHz
$D_{(MODE/SYNC)}$	Duty cycle of synchronization clock frequency (MODE/SYNC)		45		55	%
	Time to lock to external frequency			50		µs
	Phase shift at SYNC_OUT with reference to internal CLK or external CLK	SYNC_OUT_PHASE = 0		120		°

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6.5 Electrical Characteristics (continued)

over operating junction temperature (T_J = –40°C to +125°C) and V_{IN} = 2.7V to 6V. Typical values at V_{IN} = 5V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Phase shift at SYNC_OUT with reference to internal CLK or external CLK	SYNC_OUT_PHASE = 1 (default)		180		°
$V_{T+(UVP)}$	Positive-going power-good threshold voltage (output undervoltage)		94	96	98	%
$V_{T-(UVP)}$	Negative-going power-good threshold voltage (output undervoltage)		92	94	96	%
$V_{T+(OVP)}$	Positive-going power-good threshold voltage (output overvoltage)		104	106	108	%
$V_{T-(OVP)}$	Negative-going power-good threshold voltage (output overvoltage)		102	104	106	%
V_{OL}	Low-level output voltage (PG)	I_{OL} = 1mA		0.012	0.3	V
I_{OH}	High-level output current (PG)	V_{OH} = 5V			3	µA
I_{IH}	High-level input current (PG)	Device configured as secondary device in stacked operation			3	µA
I_{IL}	Low-level input current (PG)	Device configured as secondary device in stacked operation	–1			µA
$t_{d(PG)}$	Deglitch time (PG)	High-to-low or low-to-high transition on the PG pin	34	40	46	µs
OUTPUT						
ΔV_{OUT}	Output voltage accuracy	$V_{IN} \geq V_{OUT}$ + 1.6V, DROOPEN = 0	–0.8		0.8	%
ΔV_{OUT}	Output voltage change from no current to rated current	DROOPEN = 1		±12		mV
	Accuracy of droop compensation voltage; TPSM8287B15xx	device in forced PWM mode	–3.75		3.75	mV
	Accuracy of droop compensation voltage; TPSM8287B20xx	device in forced PWM mode	–3.5		3.5	mV
	Accuracy of droop compensation voltage; TPSM8287B25xx, TPSM8287B30xx	device in forced PWM mode	–3		3	mV
I_{IB}	Input bias current (GOSNS)	EN = High; $V_{(GOSNS)}$ = –100mV to 100mV	–60		3	µA
I_{IB}	Input bias current (VOSNS)	$V_{(VOSNS)}$ = 1.675V, V_{IN} = 6V, DROOPEN = 0	–5.5		5.5	µA
I_{IB}	Input bias current (VOSNS)	$V_{(VOSNS)}$ = 1.675V, V_{IN} = 6V, DROOPEN = 1	–13.2		13.2	µA
V_{ICR}	Input common-mode range (GOSNS)		–100		100	mV
R_{DIS}	Output discharge resistance	$V_{OUT} \leq$ 1V		2.7	9.2	Ω
f_{SW}	Switching frequency (SW)	setting=1.5 MHz, PWM operation	1.35	1.5	1.65	MHz
f_{SSC}	Modulation frequency	SSCEN = 1		fsw/2048		kHz
Δf_{SW}	Switching frequency variation during spread spectrum operation	SSCEN = 1	f_{SW} – 10%		f_{SW} + 10%	
gm	Transconductance of OTA on COMP pin			1.5		mS
τ	Emulated current time constant		11.87	12.5	13.2	µs
ILIM	High-side FET forward switch current limit, DC	TPSM8287B15xx	19	22.5	26	A
ILIM	High-side FET forward switch current limit, DC	TPSM8287B20xx	24	28.5	32	A
ILIM	High-side FET forward switch current limit, DC	TPSM8287B25xx	29	34	39	A

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6.5 Electrical Characteristics (continued)

over operating junction temperature (T_J = –40°C to +125°C) and V_{IN} = 2.7V to 6V. Typical values at V_{IN} = 5V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ILIM	High-side FET forward switch current limit, DC	TPSM8287B30xx	34	39	44	A
ILIM	Low-side FET forward switch current limit, DC	TPSM8287B15xx	15	20	24	A
ILIM	Low-side FET forward switch current limit, DC	TPSM8287B20xx	20	24.5	29	A
ILIM	Low-side FET forward switch current limit, DC	TPSM8287B25xx	24.5	29	33	A
ILIM	Low-side FET forward switch current limit, DC	TPSM8287B30xx	29.5	33.5	38	A
ILIM	Low-side FET negative current limit, DC			–10	–7.5	A
$t_{on, min}$	Minimum on-time of HS FET	V_{IN} = 3.3V		45		ns
$t_{on, min}$	Minimum on-time of HS FET	V_{IN} = 5V		35		ns
	Maximum duty cycle of power stage	DC operation for TPSM8287B25xx only, T_J = 125°C		40		%
	Maximum duty cycle of power stage	DC operation for TPSM8287B30xx only, T_J = 125°C		25		%

6.6 I²C Interface Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
		Fast mode plus			1	MHz
		High-speed mode (write operation), CB – 100pF max			3.4	MHz
		High-speed mode (read operation), CB – 100pF max			3.4	MHz
		High-speed mode (write operation), CB – 400pF max			1.7	MHz
		High-speed mode (read operation), CB – 400pF max			1.7	MHz
t_{HD}, t_{STA}	Hold time (repeated) START condition	Standard mode	4			µs
		Fast mode	0.6			µs
		Fast mode plus	0.26			µs
		High-speed mode	0.16			µs
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			µs
		Fast mode plus	0.5			µs
		High-speed mode, CB – 100pF max	0.16			µs
		High-speed mode, CB – 400pF max	0.32			µs
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4			µs
		Fast mode	0.6			µs
		Fast mode plus	0.26			µs
		High-speed mode, CB – 100pF max	0.06			µs
		High-speed mode, CB – 400pF max	0.12			µs

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6.6 I²C Interface Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SU}, t_{STA}	Setup time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	0.6			µs
		Fast mode plus	0.26			µs
		High-speed mode	0.16			µs
t_{SU}, t_{DAT}	Data setup time	Standard mode	250			ns
		Fast mode	100			ns
		Fast mode plus	50			ns
		High-speed mode, CB – 100pF max	10			ns
t_{HD}, t_{DAT}	Data hold time	Standard mode	0		3.45	µs
		Fast mode	0		0.9	µs
		Fast mode plus	0			µs
		High-speed mode, CB – 100pF max	0		70	ns
		High-speed mode, CB – 400pF max	0		150	ns
t_{RCL}	Rise time of both SDA and SCL signals	Standard mode			1000	ns
		Fast mode	20		300	ns
		Fast mode plus			120	ns
		High-speed mode, CB – 100pF max	10		40	ns
		High-speed mode, CB – 400pF max	20		80	ns
t_{FCL}	Fall time of both SDA and SCL signals (1)	Standard mode			300	ns
		Fast mode	20 × V_{DD}/5.5V		300	ns
		Fast mode plus	20 × V_{DD}/5.5V		120	ns
		High-speed mode, CB – 100pF max	10		40	ns
		High-speed mode, CB – 400pF max	20		80	ns
t_{SU}, t_{STO}	Setup time of STOP Condition	Standard mode	4			µs
		Fast mode	0.6			µs
		Fast mode plus	0.26			µs
		High-Speed mode	0.16			µs
CB	Capacitive load for SDA and SCL	Standard mode			400	pF
		Fast mode			400	pF
		Fast mode plus			550	pF
		High-Speed mode			400	pF
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			µs
		Fast mode	1.3			µs
		Fast mode plus	0.5			µs

(1) V_{DD} is the pullup voltage of SDA and SCL.

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6.7 Typical Characteristics

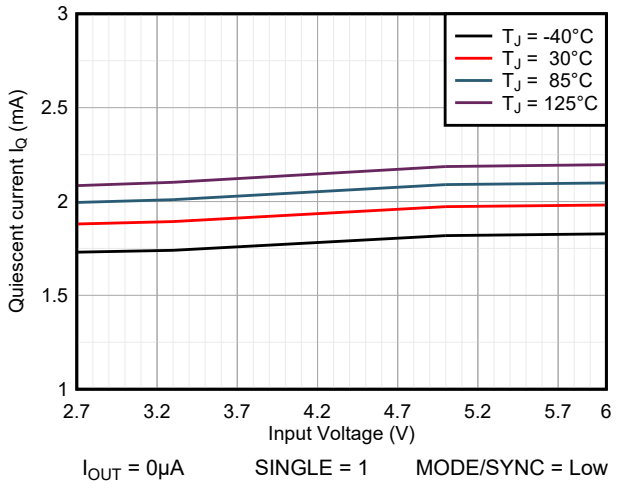


Figure 6-1. Operating Supply Current (Power-Save Mode)

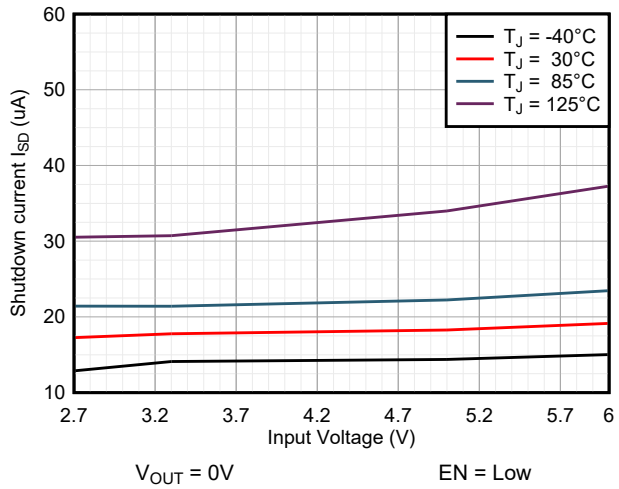


Figure 6-2. Shutdown Current

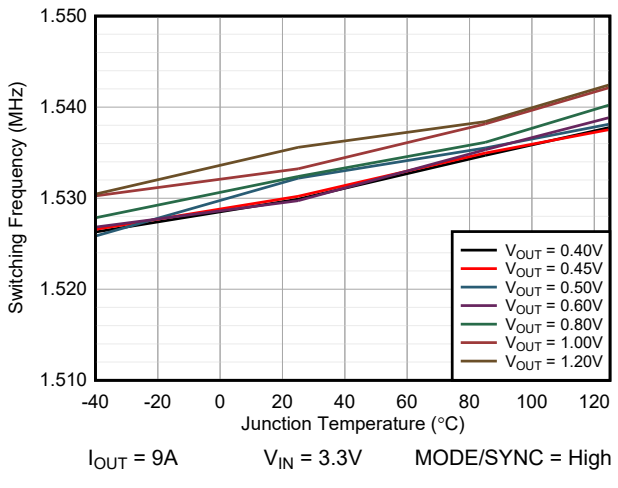


Figure 6-3. TPSM8287Bxx Switching Frequency vs T_J

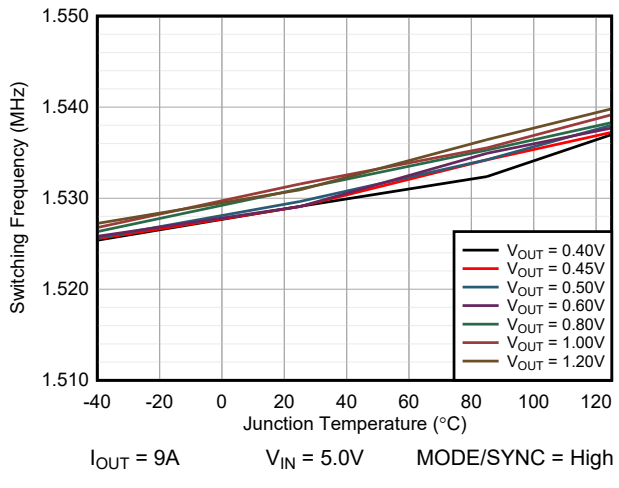


Figure 6-4. TPSM8287Bxx Switching Frequency vs T_J

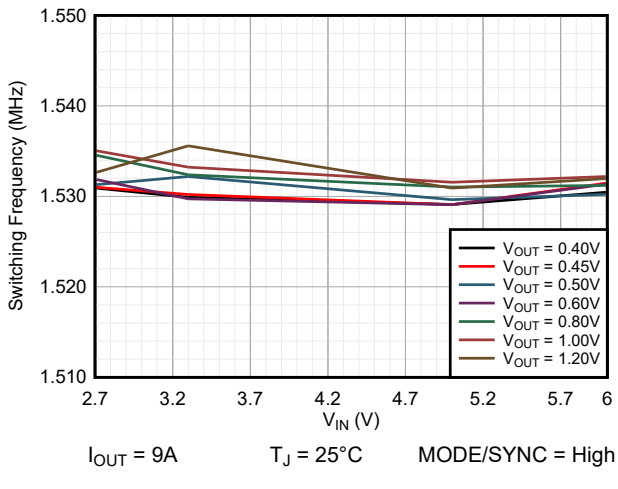


Figure 6-5. TPSM8287Bxx Switching Frequency vs V_{IN}

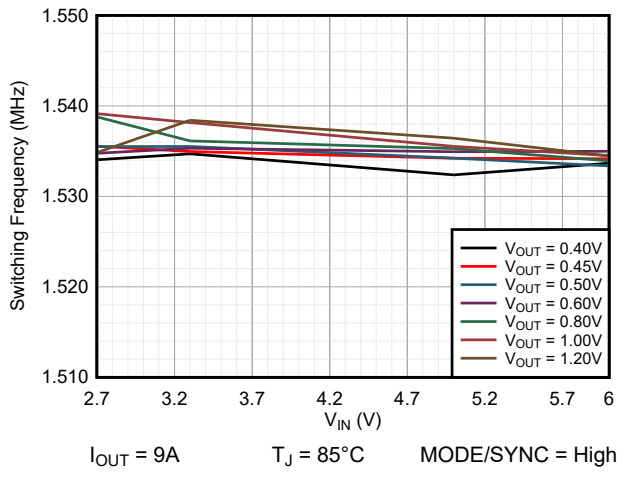


Figure 6-6. TPSM8287Bxx Switching Frequency vs V_{IN}

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7 Detailed Description

7.1 Overview

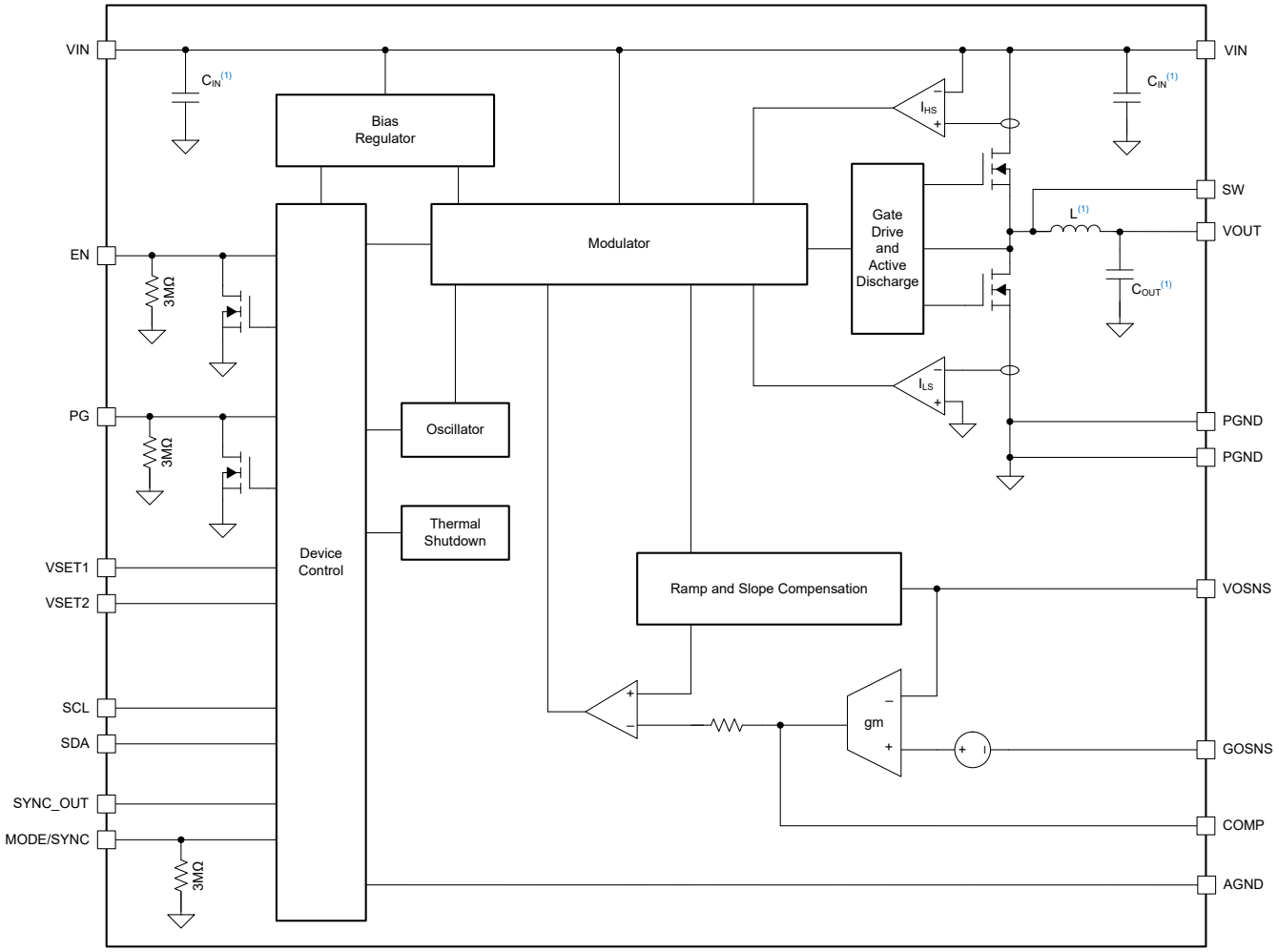
The TPSM8287Bxx synchronous, step-down converter power modules use the fixed-frequency DCS-Control topology to achieve fast transient response during a load step while switching with a fixed frequency during normal operation. This control topology, together with the low output voltage ripple, high DC accuracy, and differential remote sense, makes the devices designed for supplying the cores of modern high-performance processors or other voltage rails with tight regulation requirements.

As the load current decreases, the converter can enter power save mode based on the MODE/SYNC pin, reducing the switching frequency and entering DCM to achieve high efficiency over the entire load current range.

This pin-to-pin compatible family of modules includes 15A, 20A, 25A, and 30A variants. To further increase the output current capability, combine multiple devices in a *stack*. For example, paralleling four 30A devices can provide up to 120A of current.

The TPSM8287Bxx uses MagPack technology to deliver the highest-performance power module design. Leveraging proprietary integrated-magnetics MagPack packaging technology, these power modules deliver industry-leading power density, high efficiency, good thermal performance, ease of use, and reduced EMI emissions.

7.2 Functional Block Diagram



(1) For integrated passive's values, please refer to Section 4.

7.3 Feature Description

7.3.1 Fixed-Frequency DCS-Control Topology

Figure 7-1 shows a simplified block diagram of the fixed-frequency DCS-Control topology used in the TPSM8287Bxx devices. This topology comprises an inner emulated current loop and an outer voltage-regulating loop. The differential remote sense allows for precise voltage regulation at the load. The external compensation allows fine tuning the load transient response for a wide range of output capacitance and load transient requirements.

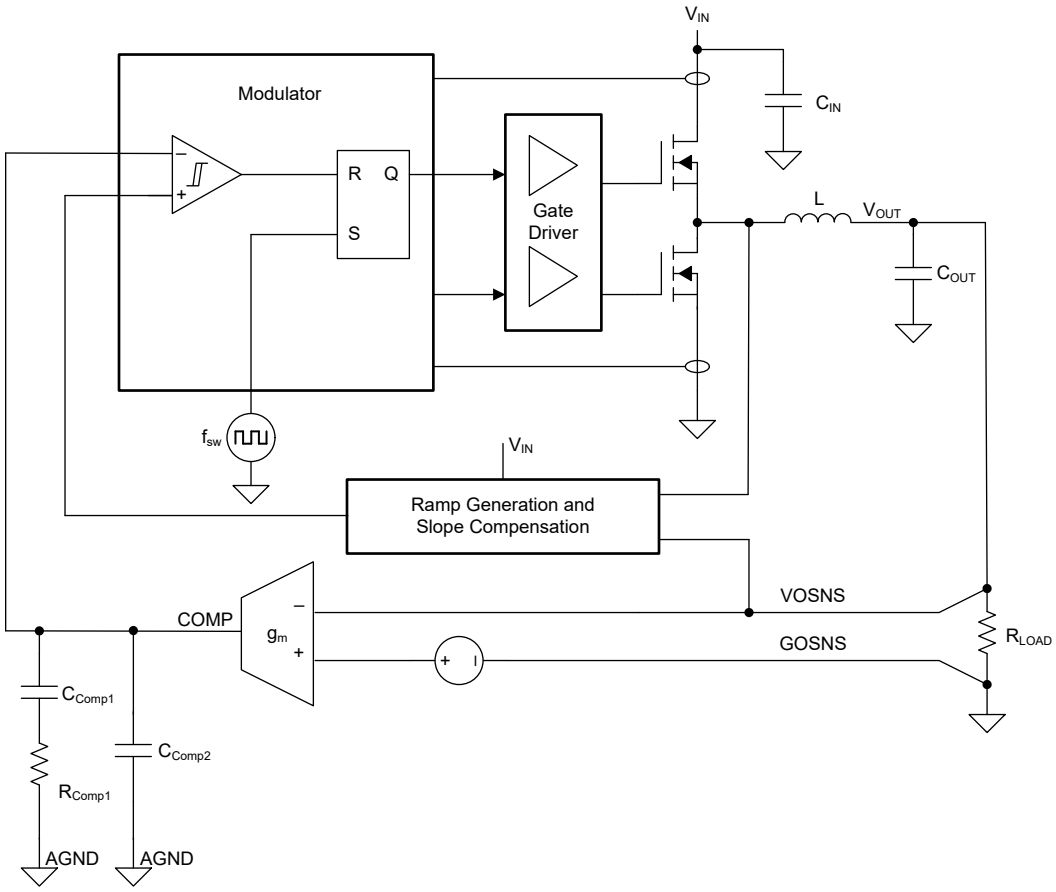


Figure 7-1. Fixed-Frequency DCS-Control Topology (Simplified)

7.3.2 Forced PWM and Power Save Modes

The device can control the inductor current in three different ways to regulate the output:

- Pulse-width modulation with continuous inductor current (PWM-CCM)
- Pulse-width modulation with discontinuous inductor current (PWM-DCM)
- Pulse-frequency modulation with discontinuous inductor current and pulse skipping (PFM-DCM)

The on-time in PWM-CCM is set by Equation 1. For very small output voltages, a minimum on time ($t_{on,\ min}$) reduces the switching frequency from the set value. Even when the minimum on-time is reached, the device maintains proper output voltage regulation by extending the off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (1)$$

During PWM-CCM operation, the device switches at a constant frequency and the inductor current is continuous (see Figure 7-2). PWM operation achieves the lowest output voltage ripple and the best transient performance.

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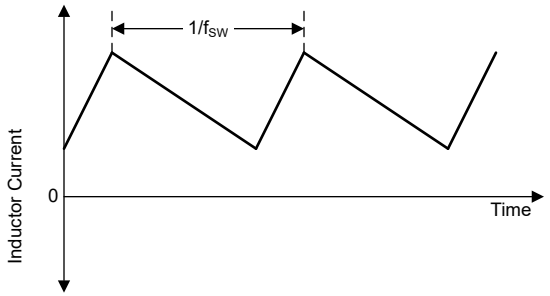


Figure 7-2. Continuous Conduction Mode (PWM-CCM) Current Waveform

During PWM-DCM operation the device switches at a constant frequency and the inductor current is discontinuous (see Figure 7-3). In this mode, the device controls the peak inductor current to maintain the selected switching frequency while still being able to regulate the output.

Equation 2 calculates the output current threshold at which the device changes from PWM-CCM to PWM-DCM:

$$I_{OUT(\mathrm{CCM-DCM})} = \frac{V_{IN} \times t_{ON}}{2} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L} \quad (2)$$

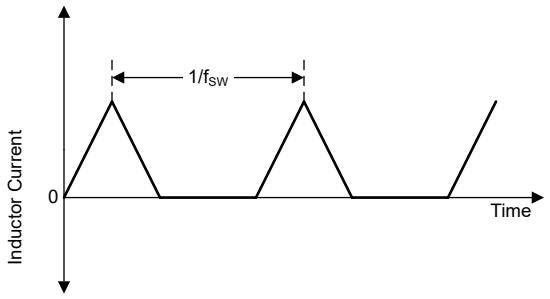


Figure 7-3. Discontinuous Conduction Mode (PWM-DCM) Current Waveform

During PFM-DCM operation, the device keeps the peak inductor current constant (at a level corresponding to the minimum on-time ($t_{on,\ min}$) of the converter) and skips pulses to regulate the output (see Figure 7-4). The switching pulses that occur during PFM-DCM operation are synchronized to the internal clock.

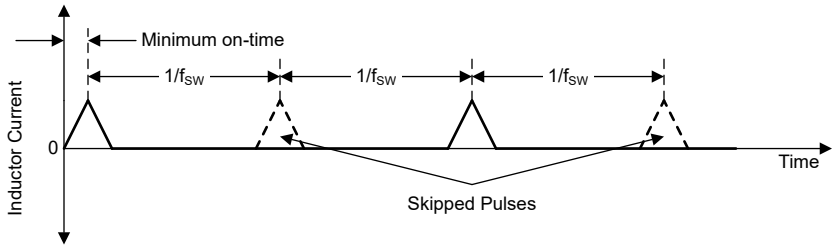


Figure 7-4. Discontinuous Conduction Mode (PFM-DCM) Current Waveform

Equation 3 calculates the output current threshold at which the device changes from PWM-DCM to PFM-DCM:

$$I_{OUT(PFM-entry)} = \frac{V_{IN} \times \ ton, \ min}{2} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L} \quad (3)$$

Figure 7-5 shows how the PWM-DCM to PFM-DCM threshold typically varies with V_{IN} and V_{OUT}.

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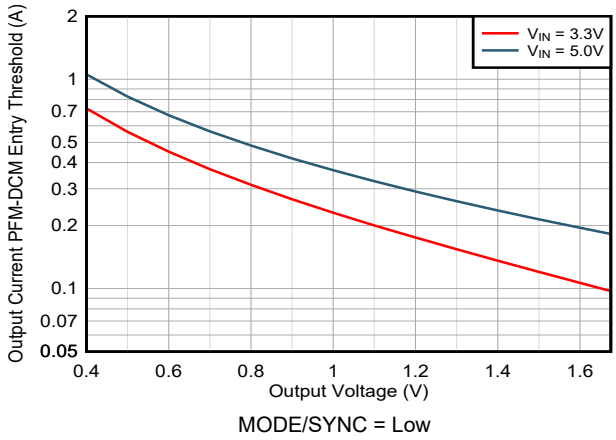


Figure 7-5. PFM-DCM Entry Threshold TPSM8287Bxx

Configure the device to use either forced PWM mode (FPWM) or power save mode (PSM):

- In forced PWM mode, the device uses PWM-CCM at all times.
- In power save mode, the device uses PWM-CCM at medium and high loads, PWM-DCM at light loads, and PFM-DCM at very light loads. Transitions between the different operating modes are seamless.

the following table shows the function table of the MODE/SYNC pin and the FPWMEN bit in the CONTROL1 register, which controls the operating mode of the device.

Table 7-1. FPWM Mode and Power Save Mode Selection

SSCEN Bit	FPWMEN Bit	MODE/SYNC PIN	OPERATING MODE	REMARK
0	0	Low	PSM	Do not use in a stacked configuration
1	0	Low	PSM	
0	1	X	FPWM	
0	X	High	FPWM	
X	X	Sync clock	FPWM	See Section 7.3.7
1	1	X	FPWM	See Section 7.3.8
1	X	High	FPWM	

7.3.3 Precise Enable

The Enable (EN) pin is bidirectional and has two functions. See Figure 7-6:

- As an input, the pin enables and disables the DC/DC converter in the device.
- In a stacked configuration, the pin is an output and provides a SYSTEM_READY signal to other devices.

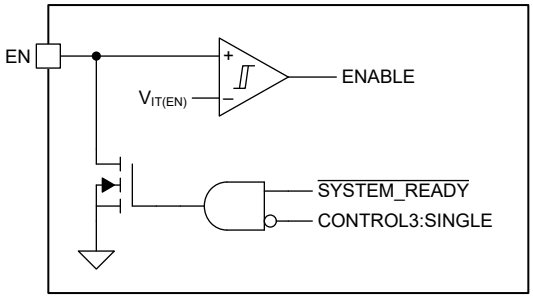


Figure 7-6. Enable Functional Block Diagram

Because there is an internal open-drain transistor connected to the EN pin, do not drive this pin directly from a low-impedance source. Instead, use a > 15kΩ resistor to limit the current flowing into the EN pin.

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When power is first applied to the VIN pin, the device pulls the EN pin low until the default register settings from nonvolatile memory are loaded and the state of the VSETx and SYNC_OUT pins is read. The device re-initializes only if the input voltage drops below the POR (Power On Reset) threshold. The device also pulls EN low if a fault, such as thermal shutdown or overvoltage lockout, occurs. In a stacked configuration, all devices share a common enable signal, which means that the DC/DC converters in the stack cannot start to switch until *all* devices in the stack have completed the initialization. Similarly, a fault in one or more devices in the stack disables *all* converters in the stack (see Section 7.3.16).

In standalone (non-stacked) applications, set SINGLE = 1 in the CONTROL3 register to disable the active pulldown of the EN pin. Fault conditions have no effect on the EN pin when SINGLE = 1. (Note that the EN pin is *always* pulled down during device initialization.) In stacked applications, make sure that SINGLE = 0. Setting SINGLE = 1 also disables the SYNC_OUT pin.

When the internal $\overline{\text{SYSTEM_READY}}$ signal is low (that is, initialization is complete and there are no fault conditions), the internal open-drain transistor is high impedance and the EN pin functions like a standard input: a high level on the EN pin enables the DC/DC converter in the device and a low level disables the DC/DC converter. The I^2C interface is enabled as soon as the device has completed the initialization and is not affected by the state of the internal ENABLE or $\overline{\text{SYSTEM_READY}}$ signals.

A low level on the EN pin forces the device into shutdown. During shutdown, the MOSFETs in the power stage are off, the internal control circuitry is disabled, and the device consumes less than 18µA (typical). Do not leave the EN pin floating.

The precise enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the EN pin. The Precise Enable input also allows the user to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a precise power-up delay. See *Achieving a clean startup by using a DC/DC converter with a precise enable-pin threshold* analog design journal analog design journal for more details.

7.3.4 Start-Up

When the voltage on the VIN pin exceeds the positive-going UVLO threshold, the device initializes as follows:

- The device pulls the EN pin low
- The device enables the internal reference voltage
- The device reads the state of the VSETx and SYNC_OUT pins
- The device loads the default values into the device registers

When initialization is complete, the device enables I^2C communication and releases the EN pin. The external circuitry controlling the EN pin now determines the behavior of the device:

- If the EN pin is low, the device is disabled:
  - The user can write to and read from the device registers
  - The power stage does not operate (high-impedance).
- If the EN pin is high, the device is enabled:
  - The user can write to and read from the device registers
  - After a short delay, the power stage starts switching
  - The converter ramps up the output voltage

Figure 7-7 shows the start-up sequence when the EN pin is pulled up to V_{IN} through a resistor.

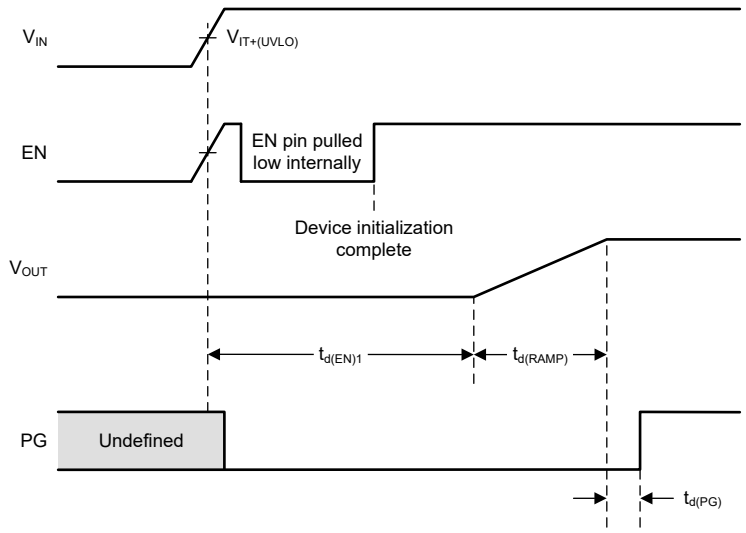


Figure 7-7. Start-Up Timing When EN is Pulled Up to V_{IN}

Figure 7-8 shows the start-up sequence when an external signal is connected to the EN pin.

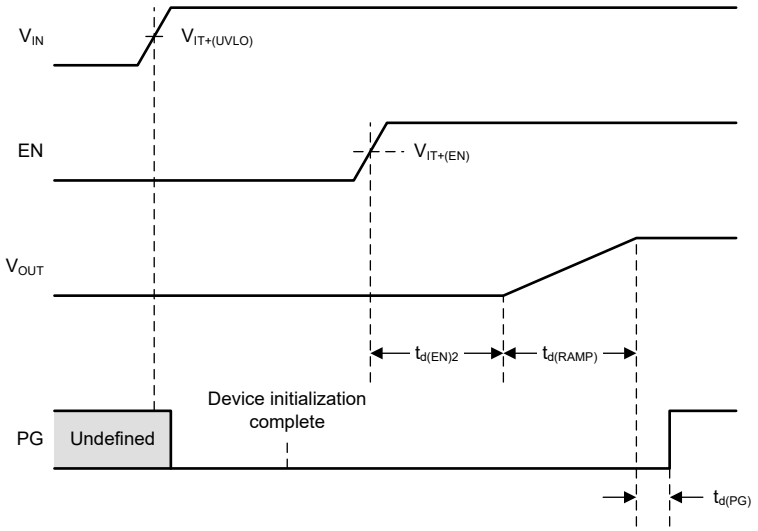


Figure 7-8. Start-Up Timing When an External Signal is Connected to the EN Pin

The SSTIME[1:0] bits in the CONTROL2 register select the duration of the soft-start ramp:

- $t_{d(Ramp)}$ = 500µs
- $t_{d(Ramp)}$ = 0.77ms
- $t_{d(Ramp)}$ = 1ms (default)
- $t_{d(Ramp)}$ = 2ms

The device ignores new values during the soft-start sequence for the following parameters:

- Output voltage setpoint (VSET[7:0])
- Output voltage range (VRANGE[1:0])
- Soft-start time (SSTIME[1:0])

If the user changes the value of VSET[7:0] during soft start, the device first ramps to the value that VSET[7:0] had when the soft-start sequence began. When soft start is complete, the device ramps up or down to the new value.

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During start-up, the device does not sink current to make sure that the output voltage follows the configured ramp rate to the target output voltage. With this, the device can start up into a prebiased output. In this case, only a portion of the internal voltage ramp is seen externally (see Figure 7-9).

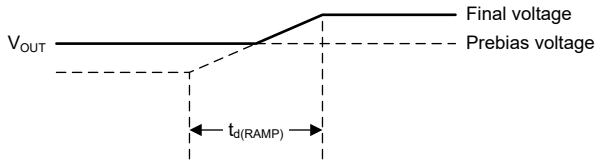


Figure 7-9. Start-Up into a Prebiased Output

7.3.5 Output Voltage Setting

7.3.5.1 Output Voltage Setpoint

During initialization, the device reads the state of the VSETx pins and selects the default output voltage according to Table 7-2. Note that the VSETx pins also select the I^2C target address of the device and the setting of the VRANGE bits located in register CONTROL2. The VSETx pins are only read during a power cycle of VIN or by setting RESET = 1 through the I^2C interface. Changing the configuration after VIN is present does not affect the content of the registers or the I^2C address. Make sure that there is no stray current path connected to the VSETx pins and that the parasitic capacitance between the VSETx pins and GND is less than 100pF. For proper operation, the input voltage needs to be at least 1.5V above the selected output voltage.

Table 7-2. Start-Up Output Voltage and I^2C Address

VSET1	VSET2	I^2C ADDRESS	TPSM8287BxxL VOUT VOLTAGE(1)	TPSM8287BxxH VOUT VOLTAGE(2)
GND	GND	0x45	400mV	800mV
GND	47kΩ to GND	0x44	425mV	850mV
GND	47kΩ to VIN	0x47	450mV	900mV
GND	VIN	0x46	475mV	950mV
47kΩ to GND	GND	0x45	500mV	1000mV
47kΩ to GND	47kΩ to GND	0x44	525mV	1050mV
47kΩ to GND	47kΩ to VIN	0x47	550mV	1100mV
47kΩ to GND	VIN	0x46	575mV	1150mV
47kΩ to VIN	GND	0x45	600mV	1200mV
47kΩ to VIN	47kΩ to GND	0x44	625mV	1250mV
47kΩ to VIN	47kΩ to VIN	0x47	650mV	1300mV
47kΩ to VIN	VIN	0x46	675mV	1350mV
VIN	GND	0x45	700mV	1400mV
VIN	47kΩ to GND	0x44	725mV	1450mV
VIN	47kΩ to VIN	0x47	750mV	1500mV
VIN	VIN	0x46	775mV	1550mV

(1) The device sets VRANGE = 01b.
(2) The device sets VRANGE = 10b.

If the user programs new output voltage setpoints (VOUT[7:0]), output voltage range (VRANGE[1:0]), or soft-start time (SSTIME[1:0]) settings when the device has already begun the soft-start sequence, the device ignores the new values until the soft-start sequence is complete. The output voltage ramps up to the target value set by the VSETx pins, before ramping up or down to any new value programmed to the device over the I^2C interface. When changing VOUT[7:0], VRAMP[1:0], or SSTIME[1:0] while EN is low, the device uses the new values the next time the device is enabled.

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7.3.5.2 Output Voltage Range

The device has four different output voltage ranges. The VRANGE[1:0] bits in the CONTROL2 register control which range is active (see Table 7-3). The default output voltage range is determined by the VSETx pins.

Table 7-3. Voltage Ranges

VRANGE[1:0]	VOLTAGE RANGE
0b00	0.4V to 0.71875V in 1.25mV steps
0b01	0.4V to 1.0375V in 2.5mV steps
0b10	0.4V to 1.675V in 5mV steps
0b11	0.4V to 1.675V in 5mV steps

Every change to the VRANGE[1:0] bits must be followed by a write to the VSET register – even if the value of the VSET[7:0] bits does not change. This sequence is necessary for the device to start to use the new voltage range.

7.3.5.3 Non-Default Output Voltage Setpoint

If none of the output voltage setpoints in Table 7-2 are a good choice for the application, the user can change the output voltage through I^2C *before enabling* the device. After the EN pin is pulled high, the device starts up and ramps to the desired output voltage set in the VSET register. A change of the device settings through I^2C while the device is ramping is only performed after the initial ramp is completed. Storing these new device settings in the device nonvolatile memory is not possible.

7.3.5.4 Dynamic Voltage Scaling (DVS)

If the user changes the output voltage setpoint while the device is operating, the device ramps up or down to the new voltage setting in a controlled way.

The VRAMP[1:0] bits in the CONTROL1 register set the slew rate when the device ramps from one voltage to another during DVS (see Table 7-4). The ramp rate is independent of the setting of the VRANGE[1:0] bits.

Table 7-4. Dynamic Voltage Scaling Slew Rate

VRAMP[1:0]	DVS SLEW RATE
0b00 (default)	10mV/µs
0b01	5mV/µs
0b10	1.25mV/µs
0b11	0.5mV/µs

If the MODE/SYNC pin is low and FPWMEN = 0, the slew rate can be less at low output currents because the device does not actively transfer energy back from the output capacitor to the input. At higher load currents the device controls the slew rate by transferring energy to the output.

Note that ramping the output to a higher voltage requires additional output current, so that during DVS the converter must generate a total output current given by:

$$I_{OUT} = I_{OUT(DC)} + C_{OUT} \times \frac{dV_{OUT}}{dt} \quad (4)$$

where:

- I_{OUT} is the total current the converter must generate while ramping to a higher voltage
- $I_{OUT(DC)}$ is the DC load current
- C_{OUT} is the total output capacitance
- dV_{OUT}/dt is the slew rate of the output voltage (programmable in the range 0.5mV/µs to 10mV/µs)

For correct operation, make sure that the total output current during DVS does not exceed the rated current of the device.

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7.3.5.5 Droop Compensation

Droop compensation scales the nominal output voltage based on the output current. This action is done such that the output voltage is set to a higher value with no output current and to a lower value than the nominal value with the maximum output current. Droop compensation therefore provides a higher margin during a load transient and helps keep the output voltage within a certain tolerance band in case of a heavy load step, or allows the use of less output capacitance, to meet the same tolerance band. The voltage scaling vs output current depends on the output current version of the device. Figure 7-10 shows the behavior. Droop compensation is enabled by the DROOPEN bit in the CONTROL3 register. Enabling droop compensation must be done while the device is disabled, otherwise a transient output voltage deviation can occur.

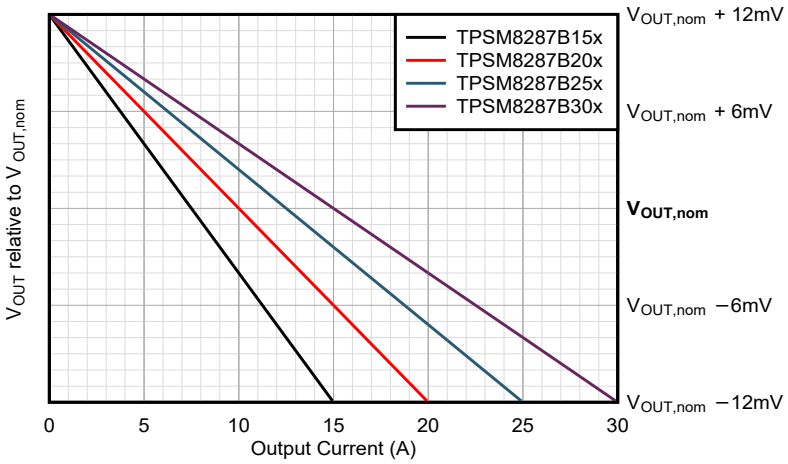


Figure 7-10. Voltage Scaling With Output Current

7.3.6 Compensation (COMP)

The COMP pin is the connection point for an external compensation network. A series-connected resistor and capacitor to AGND is sufficient for typical applications and provides enough scope to optimize the loop response for a wide range of operating conditions.

When using multiple devices in a stacked configuration, all devices share a common compensation network, and the COMP pin makes sure equal current sharing between them (see Section 7.3.16).

7.3.7 Mode Selection / Clock Synchronization (MODE/SYNC)

A high level on the MODE/SYNC pin selects forced PWM operation. A low level on the MODE/SYNC pin selects power-save operation, in which the device automatically transitions between PWM and PFM according to the load conditions.

If applying a valid clock signal to the MODE/SYNC pin, the device synchronizes the switching cycles to the external clock and automatically selects forced PWM operation. When applying a frequency modulated clock to the MODE/SYNC pin, the device also follows this action. This action can be useful in applications where the converter must follow an external spread spectrum modulation.

The MODE/SYNC pin is logically ORed with the FPWMEN bit in the CONTROL1 register. Setting either high enables FPWM (see Section 7.3.2).

When multiple devices are used in a stacked, parallel configuration to increase the output current, the clock signal from the primary device must cascade through all devices in a daisy chain configuration. The SYNC_OUT pin of the previous device must connect to the MODE/SYNC pin of the next device in the chain (see Section 7.3.16).

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7.3.8 Spread Spectrum Clocking (SSC)

The device has a spread spectrum clocking function which can reduce electromagnetic interference (EMI). When the SSC function is active, the device modulates the switching frequency to approximately ±10% around the nominal value. The frequency modulation has a triangular characteristic (see Figure 7-11).

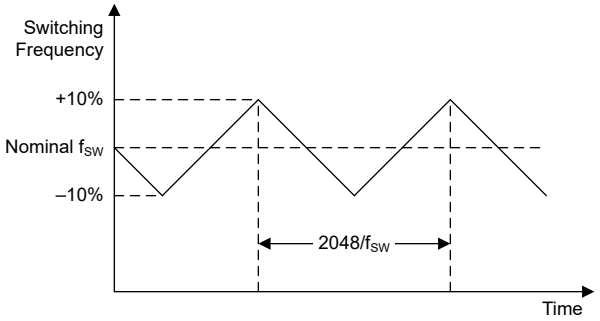


Figure 7-11. Spread Spectrum Clocking Behavior

To use the SSC function, make sure that:

- SSCEN = 1 in the CONTROL1 register
- The device is not synchronized to an external clock

TI recommends to use FPWM operation when using SSC, but SSC is available with PSM operation. To disable the SSC function, make sure that SCCEN = 0 in the CONTROL1 register.

7.3.9 Output Discharge

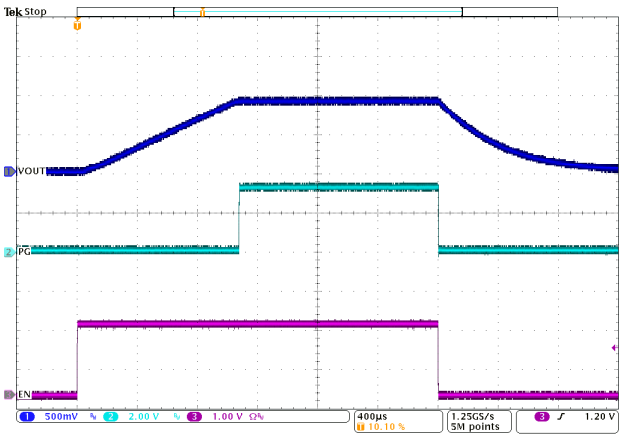
The device has an output discharge function which makes sure a defined ramp down of the output voltage when the device is disabled. The discharge stays on after the output is discharged. The output discharge function is enabled when DISCHEN = 1 in the CONTROL1 register.

If output discharge is enabled, the device discharges the output under the following conditions:

- A low level is applied to the EN pin
- SWEN = 0 in the CONTROL1 register
- A thermal shutdown event occurs
- An UVLO event occurs
- An OVLO event occurs

The discharge resistor is about 2.7Ohm (typical). Figure 7-12 shows an example of the typical discharge behavior.

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V_{IN} = 5.0V; R_{Load} = 9.1Ω; VOUT = 0.9V discharge to 0V

Figure 7-12. Output Discharge

The output discharge function is not available until the device has been enabled at least once after applying VIN. The output discharge functions until VIN drops to around 1.8V.

In a stacked configuration, the discharge is always active in the secondary devices. Please refer to Table 7-6.

7.3.10 Undervoltage Lockout (UVLO)

The device has an undervoltage lockout function which disables the device if the supply voltage is too low for correct operation. The negative-going threshold of the UVLO function is 2.5V (typical). If the supply voltage decreases below this value, the device stops switching and, if DISCHEN = 1 in the CONTROL1 register, turns on the output discharge. In addition, the EN pin is pulled low, which disables all other devices in the stack.

The device automatically starts switching again – the device begins a new soft-start sequence – when the supply voltage is higher than 2.6V (typical).

7.3.11 Overvoltage Lockout (OVLO)

The device has an overvoltage lockout function that disables the DC/DC converter if the supply voltage is too high for correct operation. The positive-going threshold of the OVLO function is 6.3V (typical). If the supply voltage increases above this value, the device stops switching, sets the PBOV bit in the STATUS register and, if DISCHEN = 1 in the CONTROL1 register, turns on the output discharge. In addition, the EN pin is pulled low, which disables all other devices in the stack.

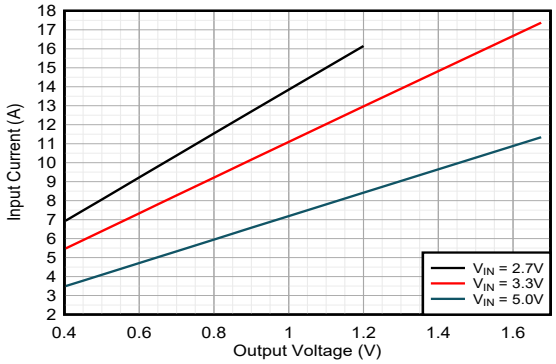
The device automatically starts switching again – the device begins a new soft-start sequence – when the supply voltage falls below 6.2V (typical).

7.3.12 Overcurrent Protection

7.3.12.1 Cycle-by-Cycle Current Limiting

The TPSM8287Bxx module is protected against overload and short circuit events. If the inductor current exceeds the high-side current limit, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. The high-side MOSFET turns on again only if the current in the low-side MOSFET has decreased below the low-side current limit. These current limits are designed to prevent the inductor of going into saturation. Figure 7-13 shows the typical input current in current limit.

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T_A = 25°C; HICCUP = 0

Figure 7-13. TPSM8287B30x Input Current in Current Limit

The low-side MOSFET also contains a negative current limit to prevent excessive current from flowing back through the inductor to the input. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off. In this scenario, both MOSFETs are off until the start of the next cycle. The negative current limit is only active in forced PWM mode.

7.3.12.2 Hiccup Mode

Hiccup mode reduces the power dissipation during an overload event. To enable hiccup operation, make sure that HICCUPEN = 1 in the CONTROL1 register. If hiccup operation is enabled and the high-side switch current hits the high-side current limit threshold on 32 consecutive switching cycles, the device:

- Stops switching for 128µs, after which the device automatically starts switching again (starts a new soft-start sequence)
- Sets the HICCUP bit in the STATUS register
- Pulls the PG pin low. The PG pin stays low until the overload condition goes away and the device can start up and regulate the output voltage. The PG pin has 40µs (typical) deglitch time, which delays the rising edge of the power-good signal.

Hiccup operation continues – in a repeating sequence of 32 cycles in current limit, followed by a pause of 128µs, followed by a soft-start attempt – for as long as the output overload condition exists.

Reading the STATUS register when the overload condition no longer exists clears the HICCUP bit. Figure 7-14 shows three cycles of hiccup operation, at which point the over load is removed and the device continues in normal operation.

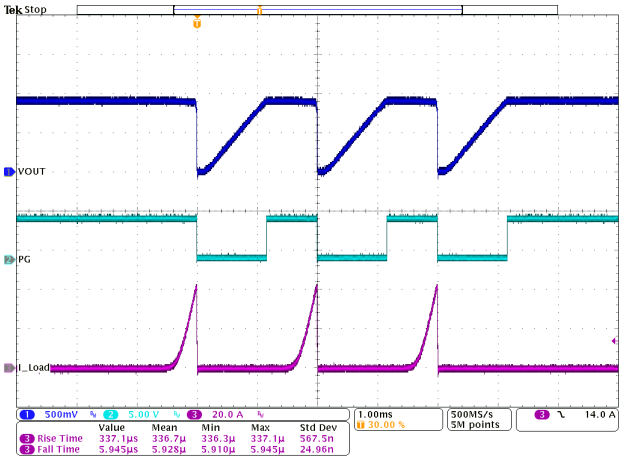


Figure 7-14. Hiccup Current Limit

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7.3.12.3 Current-Limit Mode

To enable current-limit mode, make sure that HICCUPEN = 0 in the CONTROL1 register.

When current limit operation is enabled, the device limits the high-side switch current cycle-by-cycle for as long as the overload condition exists. If the device limits the high-side switch current for four or more consecutive switching cycles,the device sets ILIM = 1 in the STATUS register.

Reading the STATUS register when the overload condition no longer exists clears the ILIM bit.

7.3.13 Power Good (PG)

The Power-Good (PG) pin is bidirectional and has two functions:

- In a standalone configuration, and in the primary device of a stacked configuration, the PG pin is an open-drain output that indicates the status of the converter or stack.
- In a secondary device of a stacked configuration, the PG pin is an input that detects when the soft-start sequence is complete.

7.3.13.1 Power-Good Standalone, Primary Device Behavior

The primary purpose of the PG pin is to indicate if the output voltage is in regulation, but the PG pin also indicates if the device is in thermal shutdown or disabled. The following table summarizes the behavior of the PG pin in a standalone or primary device.

Table 7-5. Power-Good Function Table

V_{IN}	EN	V_{OUT}	SOFT START	PGBLNKDVS	T_J	PG
V_{IN} < 2V	X	X	X	X	X	Undefined
$V_{IT-(UVLO)} \geq V_{IN} \geq 2V$	X	X	X	X	X	Low
$V_{IT-(OVLO)} > V_{IN} > V_{IT+(UVLO)}$	L	X	X	X	X	Low
	H	X	Active	X	X	Low
		$V_{OUT} > V_{T+(OVP)}$ or $V_{OUT} < V_{T-(UVP)}$	Inactive	0	X	Low
				1 (DVS inactive)		
		X		1 (DVS active)	$T_J < T_{SD}$	Hi-Z
		$V_{T-(OVP)} > V_{OUT} > V_{T+(UVP)}$		X		Hi-Z
		X	X	X	$T_J > T_{SD}$	Low
$V_{IN} > V_{IT+(OVLO)}$	X	X	X	X	X	Low

Figure 7-16 shows a functional block diagram of the power-good function in a standalone or primary device. A window comparator monitors the output voltage, and the output of the comparator goes high if the output voltage is either less than 94% (typical) or greater than 106% (typical) of the nominal output voltage. The output of the window comparator is deglitched – the typical deglitch time is 40µs (see Figure 7-15) – and then used to drive the open-drain PG pin.

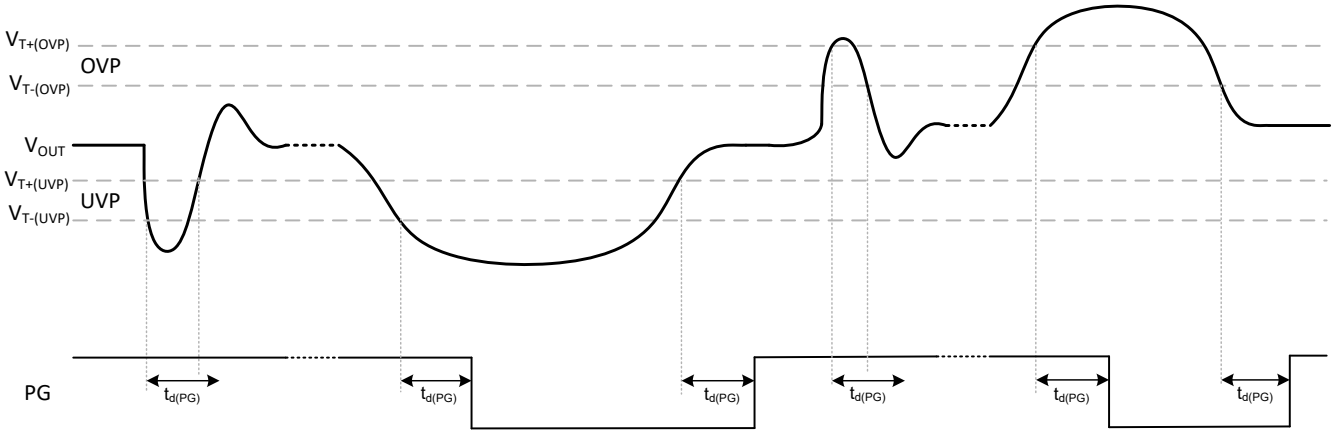


Figure 7-15. Power-Good Transient and Delay Behavior

If an output under or overvoltage event occurs, the device sets the PBUV or PBOV bits in the STATUS register, respectively. The device clears the PBOV and PBUV bits if the user reads the STATUS register after the power-bad condition no longer exists.

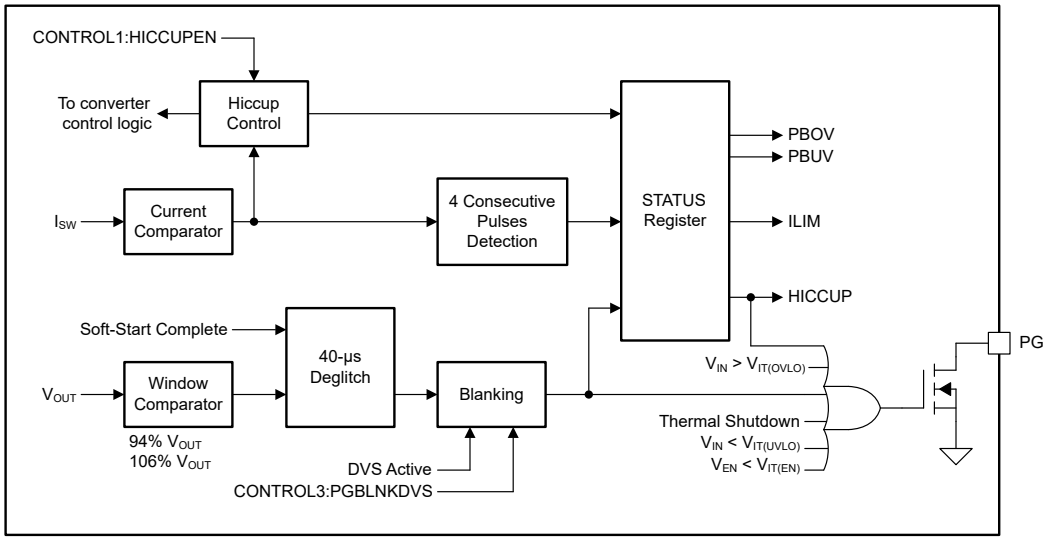


Figure 7-16. Power-Good Functional Block Diagram (Standalone, Primary Device)

During DVS activity, the voltage reference for the window comparator follows the ramping output voltage setpoint. During a DVS in FPWM mode, PG normally does not go low because the device actively drives the output voltage up or down to follow the DVS ramp. In power save mode, PG can go low on the ramp down, if there is not sufficient load to pull down the output voltage fast enough to remain within the limits of the window comparator. In both FPWM and power save mode, setting PGBLNKDVS = 1 in the CONTROL3 register forces the device to ignore the output of the power-good window comparator for the duration of the DVS ramping time (as set by the VRAMP[1:0] bits in the CONTROL1 register), keeping the PG pin high-impedance. After the DVS time has passed, PG again reflects the output of the window comparator.

Note that the PG pin is always low – regardless of the output of the window comparator – when:

- The device is in thermal shutdown
- The device is in Hiccup mode
- The device is disabled
- The device is in undervoltage or overvoltage lockout (UVLO or OVLO)
- The device is in soft start

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7.3.13.2 Power-Good Secondary Device Behavior

In a stacked, parallel configuration, the PG signal is used to communicate between the devices. During device initialization, all devices in the stack pull the PG signal low. After each device completes the initialization, only the primary device controls the PG signal and holds the signal low until soft start is completed.

The secondary devices monitor the voltage level of the PG signal. When the PG signal is low, the secondary devices can not sink current until the primary device releases the PG signal. The external pullup resistor pulls PG high and the secondary devices operate in FPWM from that point onwards.

In case of a fault condition, the secondary device does not drive the PG signal but uses the EN pin to deactivate the whole stack. In this case, the primary converter pulls the PG signal low. For details, see Table 7-6.

7.3.14 Remote Sense

The device has two pins, VOSNS and GOSNS, to remotely sense the output voltage. Remote sensing lets the converter sense the output voltage directly at the point-of-load and increases the accuracy of the output voltage regulation. These sense lines must be routed in parallel and away from noisy signals. Connect the sense lines to the lowest impedance point on the output bus, which must be the center of the output capacitor bank closest to the load.

In a stacked configuration, VOSNS and GOSNS of all secondary devices can be either connected to the local output capacitor or to the AGND pin. For further details, see Section 7.3.16.

7.3.15 Thermal Warning and Shutdown

The device has a two-level overtemperature detection function.

If the junction temperature rises above the thermal warning threshold of 150°C (typical), the device sets the TWARN bit in the STATUS register. The device clears the TWARN bit if the STATUS register is read after the junction temperature fell below the TWARN threshold of 130°C (typical).

If the junction temperature rises above the thermal shutdown threshold of 170°C (typical), the device:

- Stops switching
- Pulls down the EN pin (if SINGLE = 0 in the CONTROL3 register)
- Enables the output discharge (if DISCHEN = 1 in the CONTROL1 register)
- Sets the TSHUT bit in the STATUS register
- Pulls the PG pin low

If the junction temperature then falls below the thermal shutdown threshold of 150°C (typical), the device:

- Starts switching again, starting with a new soft-start sequence
- Releases the EN pin (high impedance)
- Releases the PG pin (high-impedance)

The device clears the TSHUT bit if the user reads the STATUS register after the junction temperature fell below the TSHUT threshold of 150°C (typical).

In a stacked configuration, in which all devices share a common enable signal, a thermal shutdown condition in one device disables the entire stack. When the hot device cools down, the whole stack automatically starts switching again.

7.3.16 Stacked Operation

The user can connect multiple devices in parallel in what is known as a "stack" to increase output current capability, to reduce device junction temperature or the output voltage ripple. For example, paralleling four 30A devices can provide up to 120A of current. More devices can be stacked, as long as the PCB layout maintains the integrity of the shared signals between the modules.

A stack comprises one *primary* device and one or more *secondary* devices. During initialization, each device monitors the SYNC_OUT pin to determine if the device must operate as a primary device or a secondary device:

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- If there is a 47kΩ resistor between the SYNC_OUT pin and ground, the device operates as a secondary device.
- If the SYNC_OUT pin is high impedance, the device operates as a primary device.

The following figure shows the recommended interconnections in a stack of two TPSM8287Bxx devices.

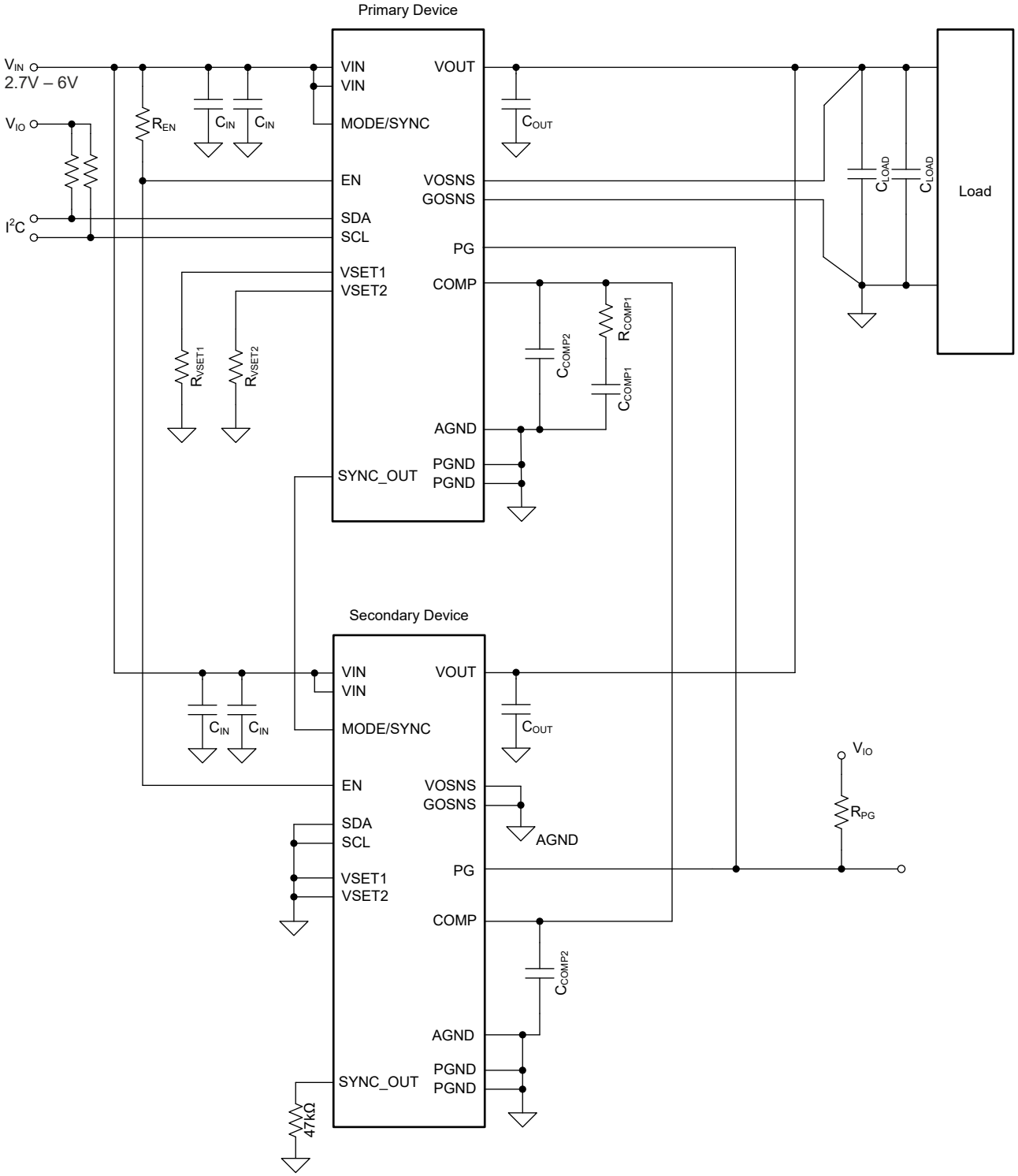


Figure 7-17. Two TPSM8287Bxx Devices in a Stacked Configuration

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The key points to note are:

- All the devices in the stack share a common enable signal, which must be pulled up with a resistance of at least 15kΩ.
- All secondary devices must connect a 47kΩ resistor between the SYNC_OUT pin and ground.
- All the devices in the stack share a common power-good signal, which must be pulled up with a resistor to a logic high level.
- All the devices in the stack share a common compensation signal.
- In case many devices are stacked, the parasitic capacitance of the COMP trace can affect the loop performance. To decouple this trace capacitance from the primary device and the compensation network, a unity gain buffer can be used between the primary and all secondary devices.
- VOSNS and GOSNS of the primary device must be connected to the capacitor at the load
- VOSNS and GOSNS of the secondary devices can either be connected to the output capacitor at the device or alternatively both pins can be tied to AGND. Do not leave these pins floating.
- Connect each device AGND pin to the local GND net, and then connect each of these local GND nets to the common GND plane.
- The same device part number (with the same output current)must be used for all devices in the stack.
- The primary device must be configured for forced PWM operation (secondary devices are automatically configured for forced PWM operation).
- A stacked configuration can support synchronization to an external clock or spread-spectrum clocking.
- Only the VSETx pins of the primary device are used to set the default output voltage. The VSETx pins of secondary devices are not used and must be connected to ground.
- The SDA and SCL pins of secondary devices are not used and must be connected to ground.
- A stacked configuration uses a daisy-chained clocking signal, in which each device switches with a phase offset relative to the previous device in the daisy-chain. This phase offset can be configured to approximately 180° (default) or 120° through the SYNC_OUT_PHASE bit in the CONTROL2 register. To daisy-chain the clocking signal, connect the SYNC_OUT pin of the primary device to the MODE/SYNC pin of the first secondary device. Connect the SYNC_OUT pin of the first secondary device to the MODE/SYNC pin of the second secondary device. Continue this connection scheme for all devices in the stack to daisy-chain them together.
- Hiccup overcurrent protection must not be used in a stacked configuration.
- For output voltages >=1.2V, reduce the maximum output current per phase by 1A to account for current balancing inaccuracy.

In a stacked configuration, the common enable signal also acts as a SYSTEM_READY signal (see Section 7.3.3). Each device in the stack can pull the EN pin low during device start-up or when a fault occurs. Thus, the stack is only enabled when all devices have completed the start-up sequence and are fault-free. A fault in any one device disables the whole stack for as long as the fault condition exists.

During start-up, the primary converter pulls the COMP pin low for as long as the enable signal (SYSTEM_READY) is low. When the enable signal goes high, the primary device actively controls the COMP pin and all converters in the stack follow the COMP voltage. During start-up, each device in the stack pulls the PG pin low while the device initializes. When initialization is complete, each secondary device in the stack sets the PG pin to high impedance and the primary device alone controls the state of the PG signal. The PG pin goes high when the stack has completed the start-up ramp and the output voltage is within the power-good window. The secondary converters in the stack detect the rising edge of the power-good signal and switch to FPWM operation. After the stack has successfully started up, the primary device controls the power-good signal in the normal way.

Functionality During Stacked Operation

Some device features are not available during stacked operation, or are only available in the primary converter. Table 7-6 summarizes the available functionality during stacked operation.

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Table 7-6. Functionality During Stacked Operation

FUNCTION	PRIMARY DEVICE	SECONDARY DEVICE	REMARK
UVLO	Yes	Yes	Common enable signal
OVLO	Yes	Yes	Common enable signal
OCP – current limit	Yes	Yes	Individual device
OCP – hiccup OCP	No	No	Do not use during stacked operation
Thermal shutdown	Yes	Yes	Common enable signal
Power Good (window comparator)	Yes	No	Primary device only
I^2C interface	Yes	No	Primary device only
DVS	Through I^2C	No	Voltage loop controlled by primary device only
SSC	Through I^2C	Yes, through primary device	Daisy-chained from primary device to secondary devices
SYNC	Yes	Yes, through primary device	Synchronization clock applied to primary device and daisy-chained from primary device to secondary devices
Precise enable	No	No	Only binary enable
Output discharge	Through I^2C	Yes	Always enabled in secondary devices

Fault Handling During Stacked Operation

In a stacked configuration, there are some faults that only affect individual devices, and other faults that affect all devices. For example, if one device enters current limit, only that device is affected. But a thermal shutdown or undervoltage lockout event in one device disables all devices through the shared enable (SYSTEM_READY) signal. Table 7-7 summarizes the fault handling during stacked operation.

Table 7-7. Fault Handling During Stacked Operation

FAULT CONDITION	DEVICE RESPONSE	SYSTEM RESPONSE
UVLO	Enable signal pulled low	New soft start
OVLO		
Thermal shutdown		
Current limit	Enable signal remains high	Error amplifier clamped
External CLK applied to MODE/SYNC fails	SYNC_OUT and power-stage switch to internal oscillator	Normal operation at the default switching frequency. Secondary devices remain properly phase-shifted.

7.4 Device Functional Modes

7.4.1 Power-On Reset (POR)

The device operates in POR mode when the supply voltage is less than the POR threshold ($V_{IT-(POR)}$).

In POR mode, no functions are available and the device resets the registers to the default values.

The device leaves POR mode and enters UVLO mode when the supply voltage increases above the POR threshold.

7.4.2 Undervoltage Lockout

The device operates in UVLO mode when the supply voltage is between the POR and UVLO thresholds.

If the device enters UVLO mode from POR mode, no functions are available. If the device enters UVLO mode from standby mode, the output discharge function is available. The I^2C interface is not available in UVLO mode.

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The device leaves UVLO mode and enters POR mode when the supply voltage decreases below the POR threshold. The device leaves UVLO mode and enters standby mode when the supply voltage increases above the UVLO threshold.

7.4.3 Standby

The device operates in standby mode when the supply voltage is greater than the UVLO threshold, the device has finished initialization and any of the following conditions is true:

- A low level is applied to the EN pin
- SWEN = 0 in the CONTROL1 register
- The device junction temperature is greater than the thermal shutdown threshold
- The supply voltage is greater than the OVLO threshold

The following functions are available in standby mode:

- I^2C interface
- Output discharge
- Power good

The device leaves standby mode and enters UVLO mode when the supply voltage decreases below the UVLO threshold. The device leaves standby mode and enters on mode when all of the following conditions are true:

- A high-level is applied to the EN pin
- SWEN = 1 in the CONTROL1 register
- The device junction temperature is below the thermal shutdown threshold
- The supply voltage is below the OVLO threshold

7.4.4 On

The device operates in On mode when the supply voltage is greater than the UVLO threshold and all of the following conditions are true:

- A high-level is applied to the EN pin
- SWEN = 1 in the CONTROL1 register
- The device junction temperature is below the thermal shutdown threshold
- The supply voltage is below the OVLO threshold
- The device has finished initialization

All functions are available in On mode.

The device leaves pn mode and enters UVLO mode when the supply voltage decreases below the UVLO threshold. The device leaves on mode and enters the standby mode when any of the following conditions is true:

- A low level is applied to the EN pin
- SWEN = 0 in the CONTROL1 register
- The device junction temperature is greater than the thermal shutdown threshold
- The supply voltage is greater than the OVLO threshold

7.5 Programming

7.5.1 Serial Interface Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see I^2C-Bus Specification and User Manual, Revision 6, 4 April 2014). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All I^2C-compatible devices connect to the I^2C bus through open drain I/O pins, SDA, and SCL. A *controller*, usually a microcontroller or a digital signal processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A *target* receives and transmits data on the bus under control of the controller.

The TPSM8287Bxx device operates as a target and supports the following data transfer *modes*, as defined in the I^2C-Bus Specification: standard mode (100kbps), fast mode (400kbps), fast mode plus (1Mbps), and high-speed mode (3.4Mbps). The interface adds flexibility to the power supply design, enabling most functions

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to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the input voltage remains above $V_{IT-(POR)}$.

The data transfer protocol for standard and fast modes is exactly the same, therefore the modes are referred to as F/S-mode in this document. The protocol for high-speed mode is different from F/S-mode, and is referred to as HS mode. The device supports 7-bit addressing; general call addresses are not supported.

The state of the VSETx pins during power-up defines the I^2C target address of the device (see Table 7-2).

TI recommends that the I^2C controller initiates a STOP condition on the I^2C bus after the initial power up of the SDA and SCL pullup voltages to make sure a reset of the I^2C engine.

7.5.2 Standard-, Fast-, Fast-Mode Plus Protocol

The controller initiates a data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 7-18. All I^2C-compatible devices must recognize a start condition.

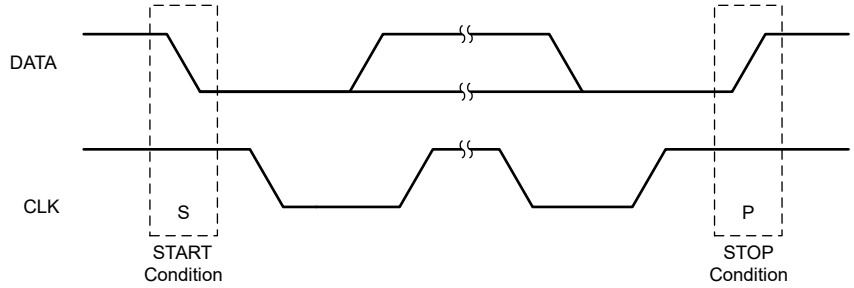


Figure 7-18. START and STOP Conditions

The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/$\overline{W}$ on the SDA line. During all transmissions, the controller makes sure that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 7-19). All devices recognize the address sent by the controller and compare the address to the internal fixed addresses. Only the target with a matching address generates an acknowledge (see Figure 7-20) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the controller knows that communication link with a target has been established.

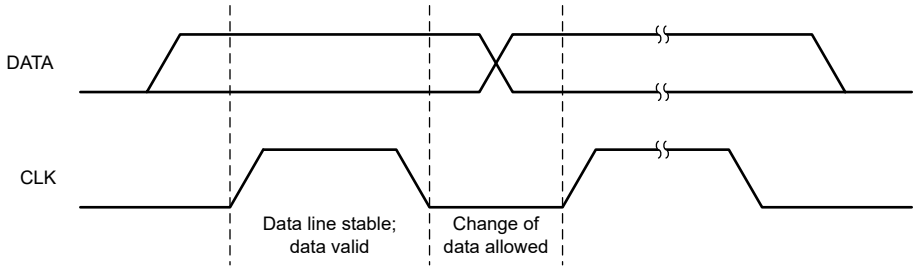


Figure 7-19. Bit Transfer on the Serial Interface

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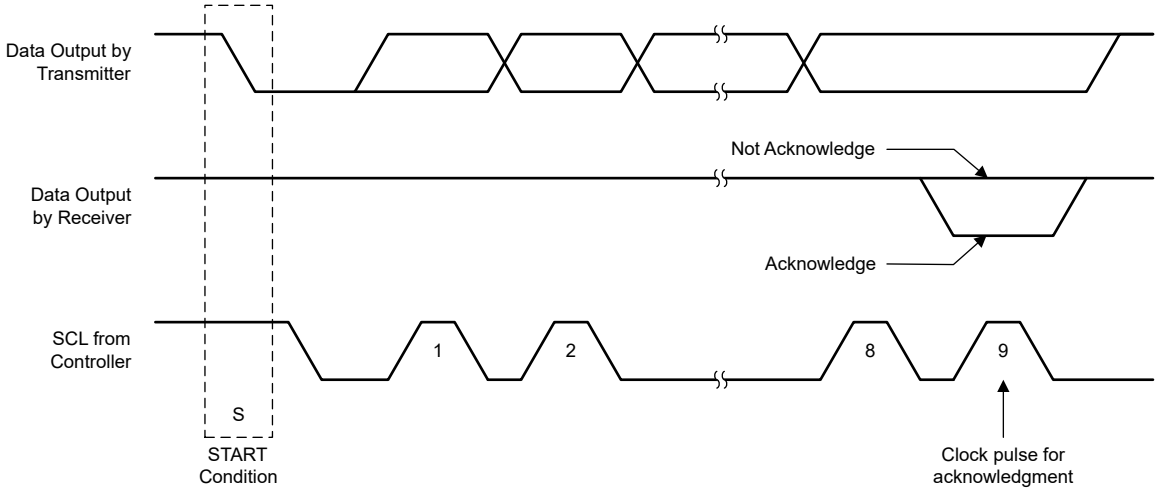


Figure 7-20. Acknowledge on the I²C Bus

The controller generates further SCL cycles to either transmit data to the target (R/$\overline{W}$ bit 0) or receive data from the target (R/$\overline{W}$ bit 1). In either case, the target must acknowledge the data sent by the controller. So an acknowledge signal can either be generated by the controller or by the target, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (see Figure 7-21).

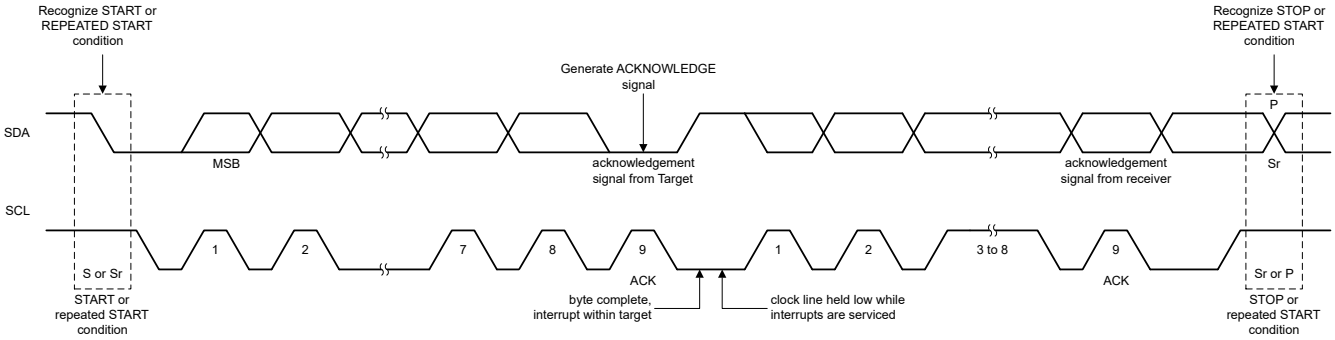


Figure 7-21. Bus Protocol

To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 7-18). This action releases the bus and stops the communication link with the addressed target. All I²C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and the devices wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 0x00 being read out.

7.5.3 I²C HS-Mode Protocol

The controller generates a start condition followed by a valid serial byte containing HS controller code 00001XXX. This transmission is made in F/S-mode at no more than 400kbps. No device is allowed to acknowledge the HS controller code, but all devices must recognize the HS controller code and switch the internal setting to support 3.4Mbps operation.

The controller then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the target devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions must be used to secure the bus in HS-mode.

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Attempting to read data from register addresses not listed in this section results in 0x00 being read out.

7.5.4 I²C Update Sequence

A start condition, a valid I²C address, a register address byte, and a data byte are required for a single update. After the receipt of each byte, the receiving device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the target. The target performs an update on the falling edge of the acknowledge signal that follows the LSB byte.



Figure 7-22. *Write* Data Transfer Format in Standard-, Fast, Fast-Plus Modes

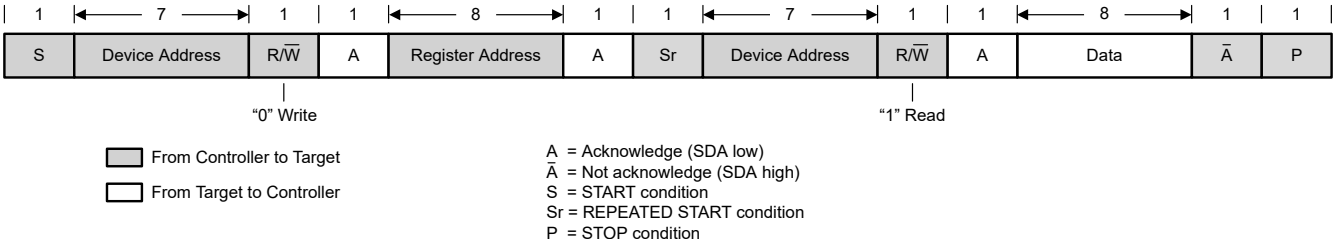


Figure 7-23. *Read* Data Transfer Format in Standard-, Fast, Fast-Plus Modes

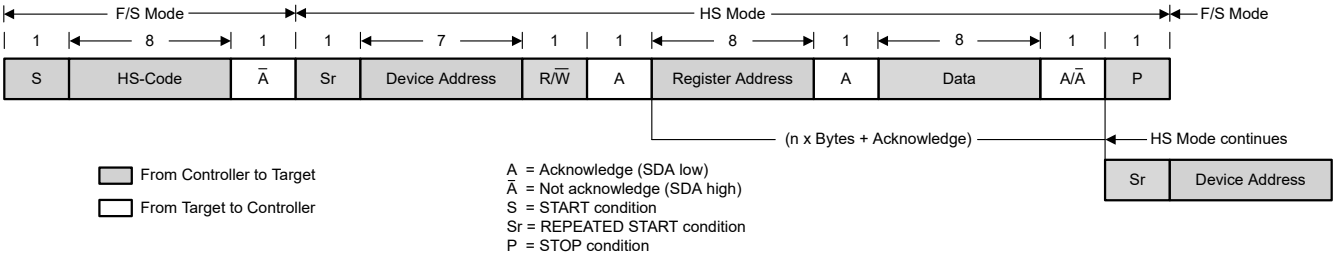


Figure 7-24. Data Transfer Format in HS-Mode

7.5.5 I²C Register Reset

The I²C registers can be reset by:

- Pulling the input voltage below $V_{IT-(POR)}$ (see Section 7.4.1).
- Setting the RESET bit in the CONTROL register. When RESET = 1, all registers are reset to the default values and a new start-up begins immediately. After $t_{d(EN)2}$, all I²C registers can be accessed again.

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8 Device Registers

Table 8-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 8-1 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. DEVICE Registers

Offset	Acronym	Register Name	Section
0h	VSET	Output Voltage Setpoint	Section 8.1
1h	CONTROL1	Control 1	Section 8.2
2h	CONTROL2	Control 2	Section 8.3
3h	CONTROL3	Control 3	Section 8.4
4h	STATUS	Status	Section 8.5

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1 VSET Register (Offset = 0h) [Reset = XXh]

VSET is shown in Figure 8-1 and described in Table 8-3.

Return to the Summary Table.

This register controls the output voltage setpoint

Figure 8-1. VSET Register

7	6	5	4	3	2	1	0
VSET							
R/W-xxxxxxxxb							

Table 8-3. VSET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VSET	R/W	xxxxxxxxb	Output voltage setpoint (see also the range-setting bits in the CONTROL2 register). Range 1: Output voltage setpoint = 0.4V + VSET[7:0] × 1.25mV Range 2: Output voltage setpoint = 0.4V + VSET[7:0] × 2.5mV Range 3: Output voltage setpoint = 0.4V + VSET[7:0] × 5mV The state of the VSETx pins during power up determines the reset value.

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8.2 CONTROL1 Register (Offset = 1h) [Reset = 28h]

CONTROL1 is shown in Figure 8-2 and described in Table 8-4.

Return to the Summary Table.

This register controls various device configuration options

Figure 8-2. CONTROL1 Register

7	6	5	4	3	2	1	0
RESET	SSCEN	SWEN	FPWMEN	DISCHEN	HICCUPEN	VRAMP	
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b	R/W-00b	

Table 8-4. CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	R/W	0b	Reset device. 0b = No effect 1b = Resets all registers to the default values. The device then performs another initialization. Reading this bit always returns 0.
6	SSCEN	R/W	0b	Spread spectrum clocking enable. 0b = SSC operation disabled 1b = SSC operation enabled
5	SWEN	R/W	1b	Software enable. 0b = Switching disabled (register values retained) 1b = Switching enabled (without the enable delay)
4	FPWMEN	R/W	0b	Forced-PWM enable. 0b = Power-save operation enabled 1b = Forced-PWM operation enabled This bit is logically ORed with the MODE/SYNC pin: If a high level or a synchronization clock is applied to the the MODE/SYNC pin, the device operates in Forced-PWM, regardless of the state of this bit.
3	DISCHEN	R/W	1b	Output discharge enable. 0b = Output discharge disabled. 1b = Output discharge enabled.
2	HICCUPEN	R/W	0b	Hiccup operation enable. 0b = Hiccup operation disabled 1b = Hiccup operation enabled. Do not enable Hiccup operation during stacked operation
1-0	VRAMP	R/W	00b	Output voltage ramp speed when changing from one output voltage setting to another. 00b = 10mV/µs 01b = 5mV/µs 10b = 1.25mV/µs 11b = 0.5mV/µs

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8.3 CONTROL2 Register (Offset = 2h) [Reset = 1Xh]

CONTROL2 is shown in Figure 8-3 and described in Table 8-5.

Return to the Summary Table.

This register controls various device configuration options

Figure 8-3. CONTROL2 Register

7	6	5	4	3	2	1	0
RESERVED			SYNC_OUT_PHASE	VRANGE		SSTIME	
R-0b			R/W-1b	R/W-xxb		R/W-10b	

Table 8-5. CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved for future use. To ensure compatibility with future device variants, program these bits to 0.
4	SYNC_OUT_PHASE	R/W	1b	Phase shift of SYNC_OUT with reference to internal clk or external clk applied at MODE/SYNC. 0b = SYNC_OUT is phase shifted by 120° 1b = SYNC_OUT is phase shifted by 180° The phase relation of 180° is only valid from the primary to the first secondary converter.
3-2	VRANGE	R/W	xxb	Output voltage range. 00b = 0.4V to 0.71875V in 1.25-mV steps 01b = 0.4V to 1.0375V in 2.5-mV steps 10b = 0.4V to 1.675V in 5-mV steps 11b = 0.4V to 1.675V in 5-mV steps The state of the VSETx pins during power up determines the reset value.
1-0	SSTIME	R/W	10b	Soft-start ramp time. 00b = 0.5ms 01b = 0.77ms 10b = 1ms 11b = 2ms

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8.4 CONTROL3 Register (Offset = 3h) [Reset = 00h]

CONTROL3 is shown in Figure 8-4 and described in Table 8-6.

Return to the Summary Table.

This register controls various device configuration options

Figure 8-4. CONTROL3 Register

7	6	5	4	3	2	1	0
RESERVED					DROOPEN	SINGLE	PGBLNKDVS
R-0b					R/W-0b	R/W-0b	R/W-0b

Table 8-6. CONTROL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved for future use. To ensure compatibility with future device variants, program these bits to 0.
2	DROOPEN	R/W	0b	Droop compensation enable. 0b = droop compensation disabled 1b = droop compensation enabled
1	SINGLE	R/W	0b	Single operation. This bit controls the internal EN pulldown and SYNCOUT functions. 0b = EN pin pulldown and SYNC_OUT enabled. Increases I_Q by 600µA typical. 1b = EN pin pulldown and SYNC_OUT disabled. Do not set during stacked operation
0	PGBLNKDVS	R/W	0b	Power-good blanking during DVS. 0b = PG pin reflects the output of the window comparator 1b = PG pin is high impedance during DVS

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8.5 STATUS Register (Offset = 4h) [Reset = 02h]

STATUS is shown in Figure 8-5 and described in Table 8-7.

Return to the Summary Table.

This register returns the device status flags

Figure 8-5. STATUS Register

7	6	5	4	3	2	1	0
RESERVED		HICCUP	ILIM	TWARN	TSHUT	PBUV	PBOV
R-0b		R-0b	R-0b	R-0b	R-0b	R-1b	R-0b

Table 8-7. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0b	Reserved for future use. To ensure compatibility with future device variants, ignore these bits.
5	HICCUP	R	0b	Hiccup. This bit reports whether a hiccup event occurred since the last time the STATUS register was read. 0b = No hiccup event occured 1b = A hiccup event occurred
4	ILIM	R	0b	Current limit. This bit reports whether a current limit event occurred since the last time the STATUS register was read. 0b = No current limit event occured 1b = A current limit event occurred
3	TWARN	R	0b	Thermal warning. This bit reports whether a thermal warning event occurred since the last time the STATUS register was read. 0b = No thermal warning event occurred 1b = A thermal warning event occurred
2	TSHUT	R	0b	Thermal shutdown. This bit reports whether a thermal shutdown event occurred since the last time the STATUS register was read. 0b = No thermal shutdown event occurred 1b = A thermal shutdown event occurred
1	PBUV	R	1b	Power-bad undervoltage. This bit reports whether a power-bad event (output voltage too low) occurred since the last time the STATUS register was read. 0b = No power-bad undervoltage event occurred 1b = A power-bad undervoltage event occurred
0	PBOV	R	0b	Power-bad overvoltage. This bit reports whether a power-bad event (output voltage too high) occurred since the last time the STATUS register was read. 0b = No power-bad overvoltage event occurred 1b = A power-bad overvoltage event occurred

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following section discusses selection of the external components to complete the power supply design for a typical application. This section gives a good starting point for further tuning the design to improve the transient performance or to reduce the output capacitors to match application requirements. During this optimization, simulations of the power distribution network, with the parasitic components, must be considered. See *TPSM8287B-COMPONENT-CALCULATOR* for a spreadsheet component calculator with the following calculations.

The use of the droop compensation feature can further reduce the required output capacitance or narrow the output voltage window during load steps. For details, see Section 7.3.5.5.

The required power inductor is integrated inside the TPSM8287Bxx, as shown in the block diagram. The integrated shielded inductor inductance and tolerance are found in Section 4. All TPSM8287Bxx versions are pin-to-pin and BOM-to-BOM compatible.

9.2 Typical Application

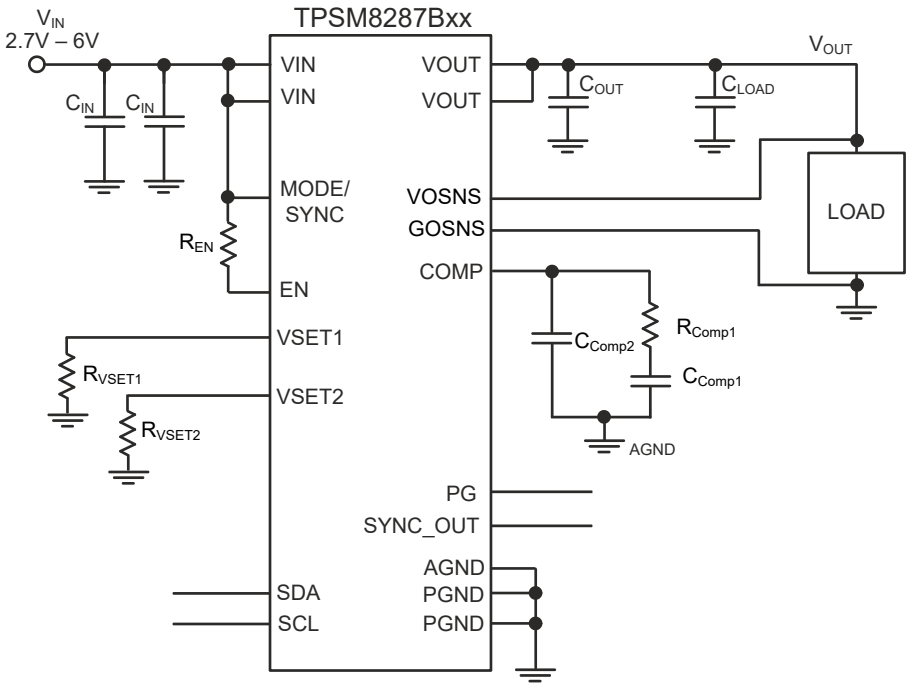


Figure 9-1. Typical Application Schematic

Table 9-1. List of Components

REFERENCE	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER(1)
C_{Comp1}	15nF	Ceramic Capacitor, X7R	Std	Std
C_{OUT}	2 × 22µF	Ceramic Capacitor, 6.3V, X6S, size 0603	GRM188C80J226ME01D	Murata
C_{LOAD}	2 × 10µF	Ceramic Capacitor, 4V, X6S, size 0402	GRM155C80G106ME18D	Murata
C_{LOAD}	2 × 22µF	Ceramic Capacitor, 6.3V, X6S, size 0603	GRM188C80J226ME01D	Murata
C_{LOAD}	47µF	Ceramic Capacitor, 4V, X6S, size 0603	GRM188C80G476ME01D	Murata
C_{IN}	4 × 22µF	Ceramic Capacitor, 10V, X6S, size 0603	GRM188C81A226ME01D	Murata
R_{Comp1}	301Ω	Resistor 1%, 0.1W	Std	Std
R_{VSET1}, R_{VSET2}	Set per Table 7-2	Resistor 5%, 0.1W	Std	Std
R_{EN}	15kΩ	Resistor 5%, 0.1W	Std	Std

(1) See the *Third-Party Products Disclaimer*.

9.2.1 Design Requirements

The following table lists the operating parameters for this application example with the TPSM8287B30LAPx device.

Table 9-2. Design Parameters

SYMBOL	PARAMETER	VALUE
V_{IN}	Input voltage	2.7V – 6.0V
V_{OUT}	Output voltage	0.60V
TOL_{VOUT}	Output voltage tolerance allowed by the application	±5.0%
TOL_{DC}	Output voltage tolerance of the TPSM8287Bxx (DC accuracy)	±0.8%
$\Delta I_{OUT(step)}$	Output current load step	±3.0A
t_t	Load step transition time	1µs
f_{SW}	Switching frequency	1.5MHz
L	Integrated inductor	50nH
TOL_{IND}	Integrated inductor tolerance	±20%
g_m	Error amplifier transconductance	1.5mS
τ	Emulated current time constant	12.5µs
BW_T	Target loop bandwidth	200kHz
N_Φ	Number of paralleled devices (phases)	1

Preliminary Calculations

The maximum allowable deviation of the power supply is ±5.0%. The DC accuracy of the TPSM8287Bxx is specified as ±0.8%, and therefore the maximum output voltage variation during a transient is given by:

$$\Delta V_{OUT} = \pm V_{OUT} \times (TOL_{VOUT} - TOL_{DC}) \quad (5)$$

$$\Delta V_{OUT} = \pm 0.6 \times (5.0\% - 0.8\%) = \pm 25.2mV \quad (6)$$

Equation 7 calculates the peak-to-peak inductor current ripple, which is the greatest at the maximum input voltage:

$$I_{L(PP)} = \frac{V_{OUT}}{V_{IN(max)}} \left(\frac{V_{IN(max)} - V_{OUT}}{L \times f_{sw} \times N\Phi} \right) \quad (7)$$

$$I_{L(PP)} = \frac{0.6}{6.0} \left(\frac{6.0 - 0.6}{50 \times 10^{-9} \times 1.5 \times 10^{6} \times 1} \right) = 7.2A \quad (8)$$

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The maximum load step occurs when the load step from the application occurs at exactly the same time as the peak (or trough) of the inductor ripple current, and is given by:

$$\Delta I_{OUT(max)} = \Delta I_{OUT(step)} + \frac{\Delta I_{L(PP)}}{2} \quad (9)$$

$$\Delta I_{OUT(max)} = 3.0 + \frac{7.2}{2} = 6.6A \quad (10)$$

9.2.2 Detailed Design Procedure

The following subsections describe how to calculate the external components required to meet the specified transient requirements of a given application. The calculations include the worst-case variation of components and use the RMS method to combine the variation of uncorrelated parameters.

See *TPSM8287B-COMPONENT-CALCULATOR* for a spreadsheet component calculator with the following calculations.

9.2.2.1 Selecting the Input Capacitors

The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. TI recommends a X7R multilayer ceramic capacitor (MLCC) for best filtering and must be placed between both VIN and PGND pins, as close as possible to those pins. For applications with ambient temperatures below 85°C, a capacitor with X5R dielectric can be used. Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Select the right capacitor carefully in combination with considering the package size and voltage rating. Depending on the device version, up to four high frequency input capacitors are contained inside the module to reduce EMI, shrink the overall design size and to simplify the board layout. Because those integrated capacitors target high frequencies, four additional external capacitors with a minimum effective capacitance of 5µF each are required. For device versions without the integrated input capacitors, TI recommends to place high frequency capacitors as close as possible to the module, to reduce the parasitic inductance of the input loop. For details on which device versions have integrated input capacitors, please refer toSection 4. When selecting the input capacitors, make sure that the total input loop impedance toward the module is below 1.2nH.

The TPSM8287Bxx devices feature a *butterfly* or parallel layout with two pairs of VIN and PGND pins on opposite sides of the package. This feature allows the input capacitors to be placed symmetrically on the PCB so that the electromagnetic fields cancel each other out, thereby reducing EMI. In addition, the parasitic loop inductance between the input capacitors and the IC is reduced through this pinout.

The duty cycle of the converter is given by:

$$D = \frac{V_{OUT}}{\eta \times V_{IN}} \quad (11)$$

where:

- V_{IN} is the input voltage.
- V_{OUT} is the output voltage.
- η is the efficiency.

$$D = \frac{0.60}{0.75 \times 2.7} = 0.296 \quad (12)$$

Equation 13 shows the value of input capacitance needed to meet any system-level input voltage ripple requirement. For this example, the lowest input voltage and highest load current are used to generate a worst case input voltage ripple of 100mV.

$$C_{IN} = \frac{D \times (1 - D) \times I_{OUT}}{V_{IN(PP)} \times f_{sw}} \quad (13)$$

where:

- D is the duty cycle.
- f_{sw} is the switching frequency.
- I_{OUT} is the output current.

$$C_{IN} = \frac{0.296 \times (1 - 0.296) \times 30.0}{0.1 \times 1.5 \times 10^{6}} = 42\mu F \quad (14)$$

The value of C_{IN} calculated with Equation 13 is the *effective* capacitance after all derating, tolerance, and aging effects have been considered.

9.2.2.2 Selecting the Target Loop Bandwidth

The control loop bandwidth measures how quickly the device responds to a change in output voltage. With the TPSM8287Bxx external compensation, the loop bandwidth is adjustable to balance the tradeoff of a fast response versus stability and ringing. The R_{Comp1} resistor and output capacitance are the primary means of adjusting the loop bandwidth.

TI recommends setting the target loop bandwidth to 200kHz for a simple design. If strong load transients are expected in the application, the target bandwidth can be set as high as ¼ of the switching frequency. A target bandwidth of 200kHz is used for this example design.

9.2.2.3 Selecting the Compensation Resistor

Use Equation 15 to calculate the recommended value of compensation resistor, R_{Comp1}:

$$R_{Comp1} = \frac{1}{g_m}\left(\frac{\pi \times \Delta I_{OUT(step)} \times L}{4 \times \tau \times \Delta V_{OUT} \times N\Phi}\right)(1 + TOL_{IND}) \quad (15)$$

$$R_{Comp1} = \frac{1}{1.5 \times 10^{-3}}\left(\frac{\pi \times 3.0 \times 50 \times 10^{-9}}{4 \times 12.5 \times 10^{-6} \times 25.2 \times 10^{-3} \times 1}\right)(1 + 20\%) = 299.2\Omega \quad (16)$$

Picking a standard component above the calculated value, a 301Ω resistor is chosen in this example. The selected value must be used for the further calculations.

9.2.2.4 Selecting the Output Capacitors

In practice, the total output capacitance is typically comprised of a combination of different capacitors, in which larger capacitors provide the load current at lower frequencies and smaller capacitors provide the load current at higher frequencies to satisfy the load impedance requirements. The value, type, and location of the output capacitors are typically defined by the load. TI recommends X7R multilayer ceramic capacitors (MLCCs) for best filtering and must be placed between both VOUT and PGND pins, as close as possible to those pins. For applications with ambient temperatures below 85°C, capacitors with an X5R dielectric can be used. Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Select the right capacitors carefully in combination with considering the package size and voltage rating. The below calculations use the effective value of the total output capacitance.

The TPSM8287Bxx devices feature a *butterfly* or *parallel* layout with VOUT and PGND pins on opposite sides of the package. This feature allows the output capacitors to be placed symmetrically on the PCB such that the electromagnetic fields cancel each other out, thereby reducing EMI. Additionally, some device variants of the TPSM8287Bxx integrate two high frequency and two bulk output capacitors to further reduce the area of the output loops and reduce the required external capacitance. Those two integrated bulk capacitors can be considered to have a minimum effective capacitance of 7µF each. For details on which device versions have integrated output capacitors, please refer toSection 4.

The TPSM8287Bxx device is optimized to support harsh load transients. The device external loop compensation tunes the loop response to the desired response with a given output capacitance. The below calculations create designs that meet the load step specified in Table 9-2. These calculations typically result in total output capacitances of several hundred µF.

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Best output voltage regulation is achieved when the TPSM8287Bxx device, the output capacitors, and load are placed very close to each other, keeping the distance and added inductance between the device and load to the absolute minimum.

In case this placement cannot be achieved, then most of the total capacitance must be located at the load, with just two capacitors located at the TPSM8287Bxx device. TI recommends that the capacitance located at the load to be at least equal to the amount of the capacitance located at the device.

If the application does not contain harsh load transients, then smaller values of output capacitances are possible. Do not use output capacitances below the minimum values in *Recommended Operating Conditions*.

The transient response of the converter is defined by one of two criteria:

- The slew rate of the current through the inductor, in which case the feedback loop of the converter saturates.
- The loop bandwidth, in which the converter stays in regulation, and the loop does not saturate ($BW_\tau < f_{SW} / 4$)

Which of the above criteria applies in any given application depends on the operating conditions and component values used. Calculate the output capacitance for both cases and select the higher of the two values.

If the converter remains in regulation, the minimum required output capacitance is given by:

$$C_{OUT(min)(reg)} = \left(\frac{\tau \times g_m \times R_{Comp1}}{2 \times \pi \times \frac{L}{N\Phi} \times BW_\tau} \right) \left(1 + \sqrt{TOL_{IND}^2 + TOL_{fSW}^2} \right) \quad (17)$$

$$C_{OUT(min)(reg)} = \left(\frac{12.5 \times 10^{-6} \times 1.5 \times 10^{-3} \times 301}{2 \times \pi \times \frac{50 \times 10^{-9}}{1} \times 200 \times 10^3} \right) \left(1 + \sqrt{20\%^2 + 10\%^2} \right) = 110\mu F \quad (18)$$

If the converter loop saturates, the minimum output capacitance is given by:

$$C_{OUT(min)(sat)} = \frac{1}{\Delta V_{OUT}} \left(\frac{L \times \Delta I_{OUT(max)}^2}{2 \times V_{OUT} \times N\Phi} - \frac{\Delta I_{OUT(step)} \times t_t}{2} \right) (1 + TOL_{IND}) \quad (19)$$

$$C_{OUT(min)(sat)} = \frac{1}{25 \times 10^{-3}} \left(\frac{50 \times 10^{-9} \times 6.6^2}{2 \times 0.6 \times 1} - \frac{3.0 \times 1 \times 10^{-6}}{2} \right) (1 + 20\%) = 15\mu F \quad (20)$$

In this case, choose $C_{OUT(min)(reg)}$ = 110µF as the larger of the two values for the output capacitance.

Table 9-1 lists the output capacitors chosen. 2 × 22µF capacitors are placed close to the IC, giving a minimum effective capacitance of about 15µF each. A combination of 2 × 10µF, 2 × 22µF and 1 × 47µF capacitors are placed near the load to provide a low impedance for load transients and low output voltage ripple. These capacitors yield about 99µF of effective capacitance. Device variants with capacitors integrated inside the module provide an additional 14µF. Together, the 113µF of effective capacitance is very close to the required minimum value calculated above. For further calculations, use C_{OUT_eff} = 113µF.

Equation 21 checks that most of the output capacitance is placed at the load. If the ratio is less than 1, increase the capacitance at the load or place the device, output capacitance, and load next to each other such that there is no separation between the output capacitances.

$$\frac{C_{LOAD_eff}}{C_{Converter_eff} + C_{Integrated_eff}} > 1 \quad (21)$$

$$\frac{69 \times 10^{-6}}{2 \times 15 \times 10^{-6} + 14 \times 10^{-6}} > 1 = \text{True} \quad (22)$$

Equation 23 calculates the output voltage ripple, based on the effective output capacitance value.

$$V_{OUT(p-p)} = \frac{I_{L(PP)}}{8 \times C_{OUT_eff} \times f_{sw}} \quad (23)$$

$$V_{OUT(p-p)} = \frac{7.2}{8 \times 113 \times 10^{-6} \times 1.5 \times 10^{6}} = 5.3mV \quad (24)$$

The ripple can be slightly higher in the application, due to the ESR and ESL in the output capacitors and the application board parasitics.

9.2.2.5 Selecting the Compensation Capacitor, C_{Comp1}

First, use Equation 25 to calculate the bandwidth of the loop:

$$BW = \frac{\tau \times g_m \times R_{Comp1}}{2\pi \times \frac{L}{N\Phi} \times C_{OUT_eff}} \quad (25)$$

$$BW = \frac{12.5 \times 10^{-6} \times 1.5 \times 10^{-3} \times 301}{2\pi \times \frac{50 \times 10^{-9}}{1} \times 113 \times 10^{-6}} = 159kHz \quad (26)$$

Use Equation 27 to calculate the recommended value of C_{Comp1}.

$$C_{Comp1} = \frac{2}{\pi \times BW \times R_{Comp1}} \quad (27)$$

$$C_{Comp1} = \frac{2}{\pi \times 159 \times 10^{3} \times 301} = 13.3nF \quad (28)$$

The closest standard value is 15nF.

9.2.2.6 Selecting the Compensation Capacitor, C_{Comp2}

The compensation capacitor, C_{Comp2}, is an optional capacitor that TI recommends the user include to bypass high-frequency noise away from the COMP pin. The value of this capacitor is not critical; 10pF or 22pF capacitors are recommended for typical applications.

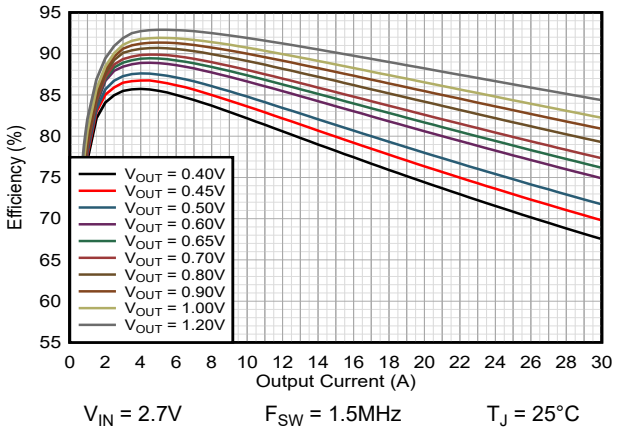
This capacitor can be made larger to suppress high-frequency zeros or resonances that occur in the system output voltage routing and decoupling network. The following equation calculates the pole created by C_{Comp2}.

$$f_{pole} = \frac{1}{2 \times \pi \times R_{Comp1} \times C_{Comp2}} \quad (29)$$

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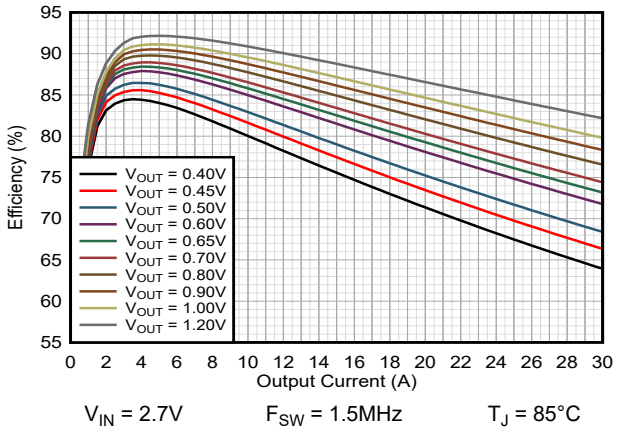
9.2.3 Application Curves

V_{IN} = 5.0V, V_{OUT} = 0.9V, T_A = 25°C, BOM = Table 9-1, unless otherwise noted.



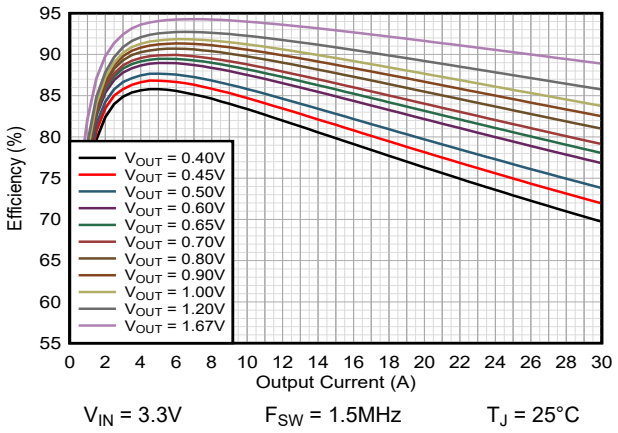
V_{IN} = 2.7V F_{SW} = 1.5MHz T_J = 25°C

Figure 9-2. Efficiency TPSM8287B30xx FPWM



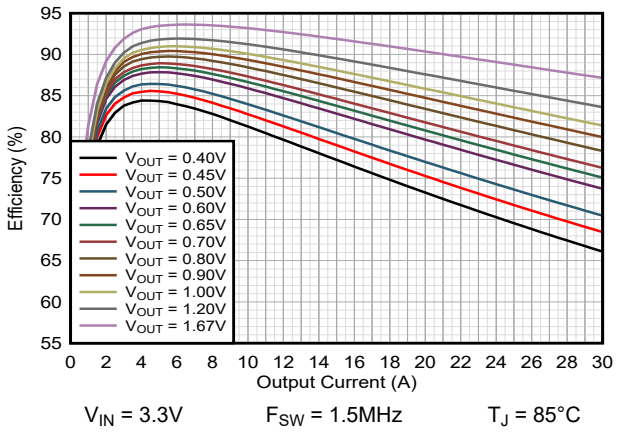
V_{IN} = 2.7V F_{SW} = 1.5MHz T_J = 85°C

Figure 9-3. Efficiency TPSM8287B30xx FPWM



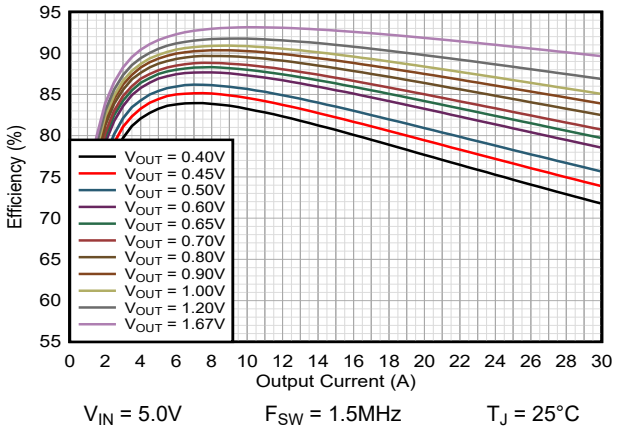
V_{IN} = 3.3V F_{SW} = 1.5MHz T_J = 25°C

Figure 9-4. Efficiency TPSM8287B30xx FPWM



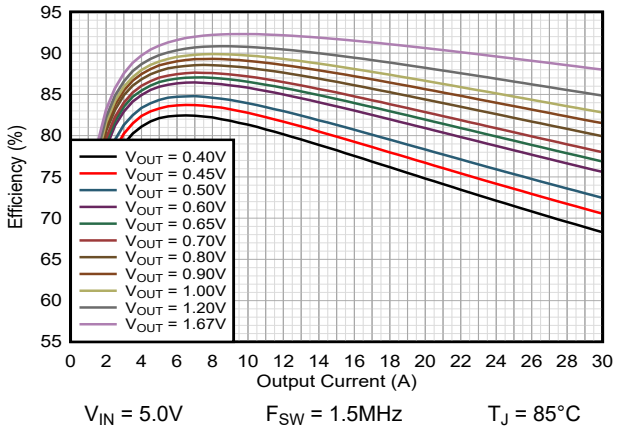
V_{IN} = 3.3V F_{SW} = 1.5MHz T_J = 85°C

Figure 9-5. Efficiency TPSM8287B30xx FPWM



V_{IN} = 5.0V F_{SW} = 1.5MHz T_J = 25°C

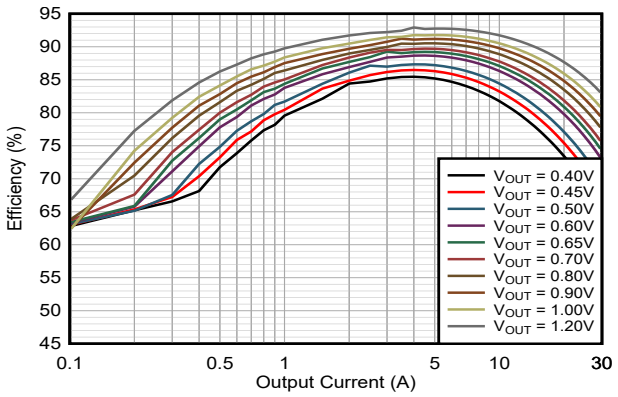
Figure 9-6. Efficiency TPSM8287B30xx FPWM



V_{IN} = 5.0V F_{SW} = 1.5MHz T_J = 85°C

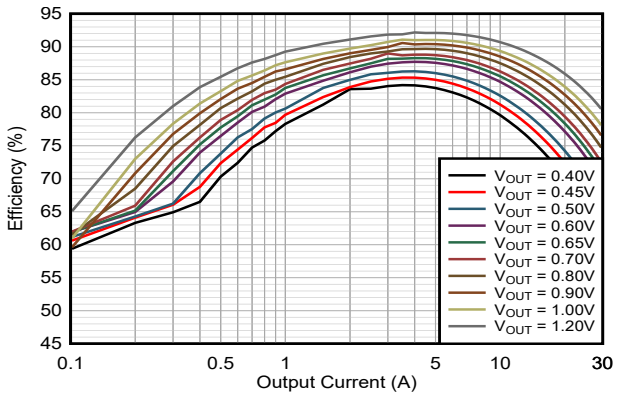
Figure 9-7. Efficiency TPSM8287B30xx FPWM

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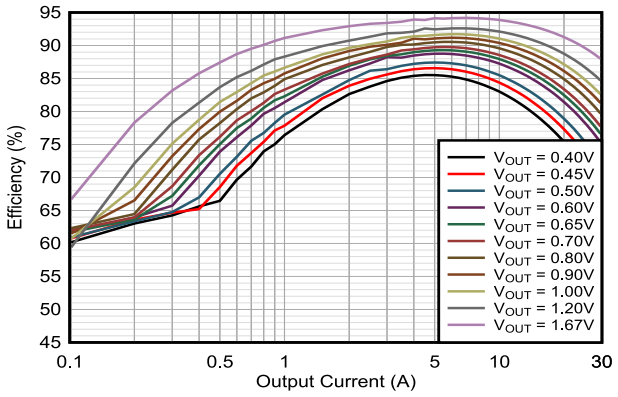
V_{IN} = 2.7V F_{SW} = 1.5MHz T_A = 25°C

Figure 9-8. Efficiency TPSM8287B30xx PSM



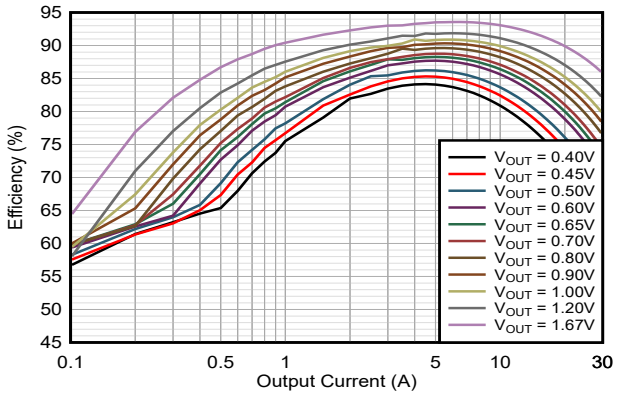
V_{IN} = 2.7V F_{SW} = 1.5MHz T_A = 85°C

Figure 9-9. Efficiency TPSM8287B30xx PSM



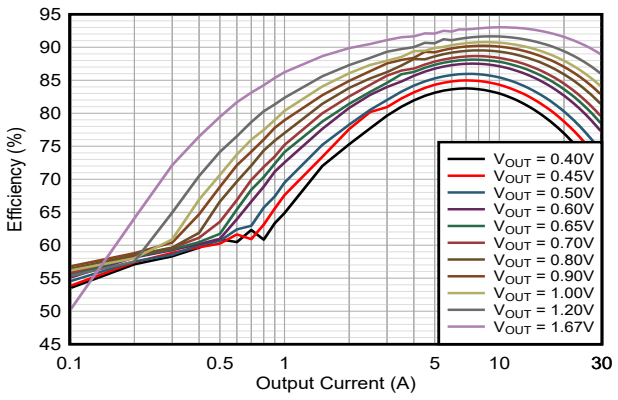
V_{IN} = 3.3V F_{SW} = 1.5MHz T_A = 25°C

Figure 9-10. Efficiency TPSM8287B30xx PSM



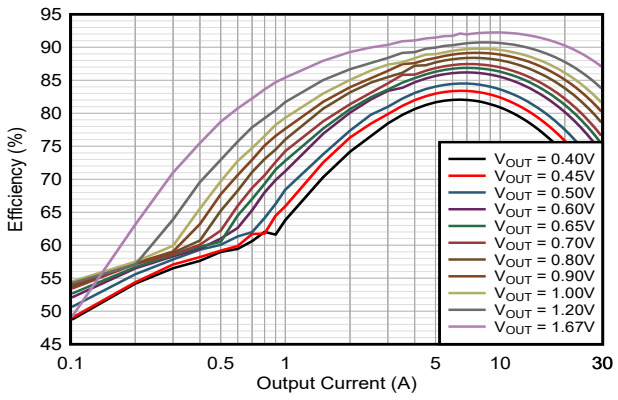
V_{IN} = 3.3V F_{SW} = 1.5MHz T_A = 85°C

Figure 9-11. Efficiency TPSM8287B30xx PSM



V_{IN} = 5.0V F_{SW} = 1.5MHz T_A = 25°C

Figure 9-12. Efficiency TPSM8287B30xx PSM



V_{IN} = 5.0V F_{SW} = 1.5MHz T_A = 85°C

Figure 9-13. Efficiency TPSM8287B30xx PSM

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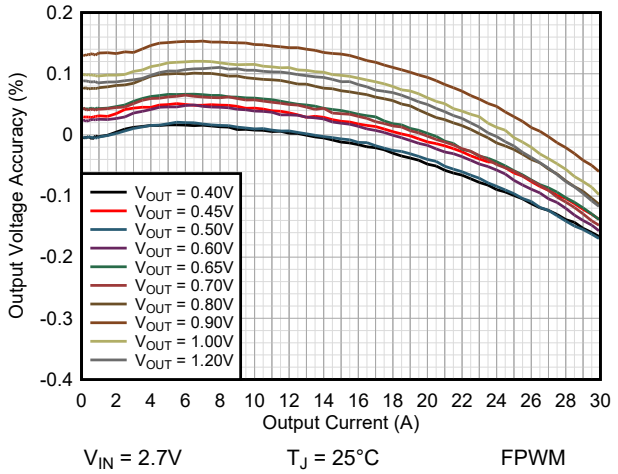


Figure 9-14. Load Regulation TPSM8287B30xx

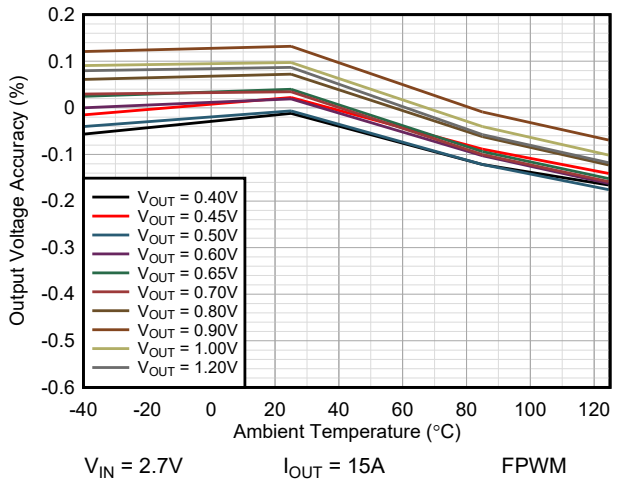


Figure 9-15. Vout Accuracy vs Temperature TPSM8287B30xx

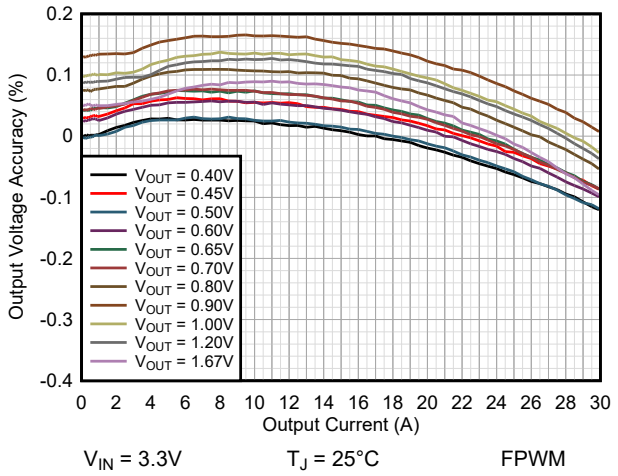


Figure 9-16. Load Regulation TPSM8287B30xx

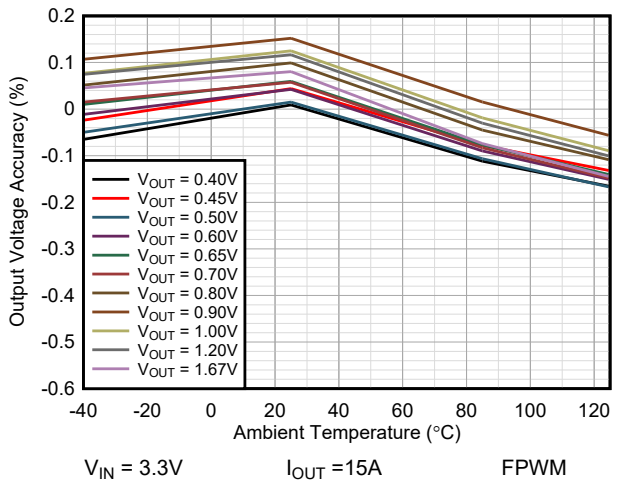


Figure 9-17. Vout Accuracy vs Temperature TPSM8287B30xx

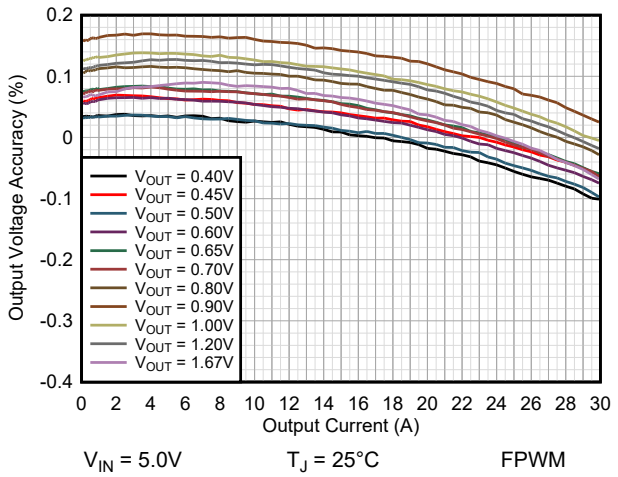


Figure 9-18. Load Regulation TPSM8287B30xx

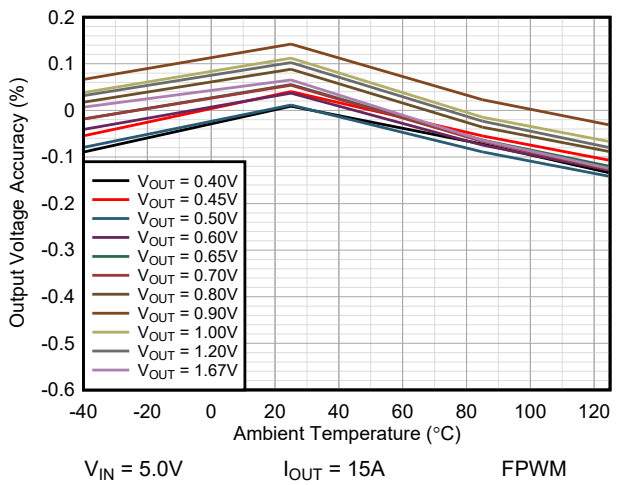
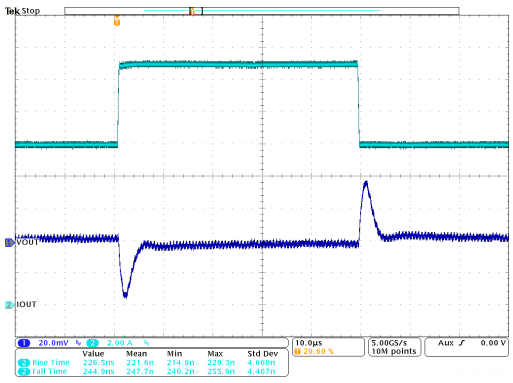


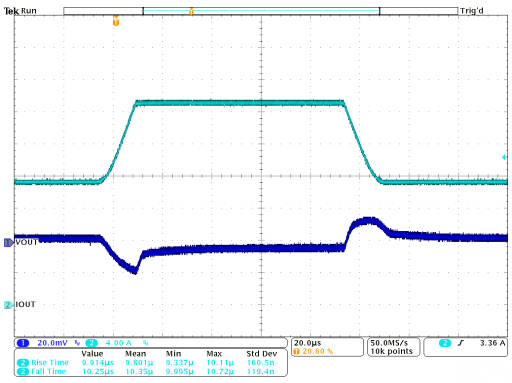
Figure 9-19. Vout Accuracy vs Temperature TPSM8287B30xx

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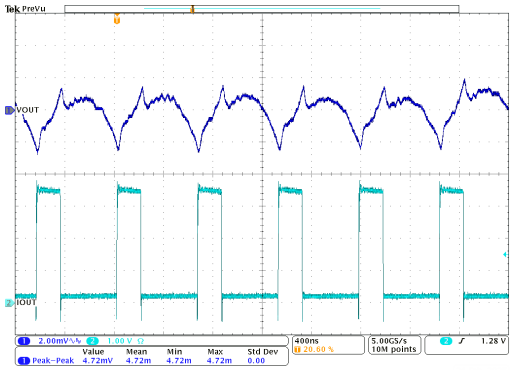
Vout=0.9V $C_{OUT(eff)}$=100µF Iout=10A→15A→10A (22A/µs)

Figure 9-20. Load Transient TPSM8287B30HAPx



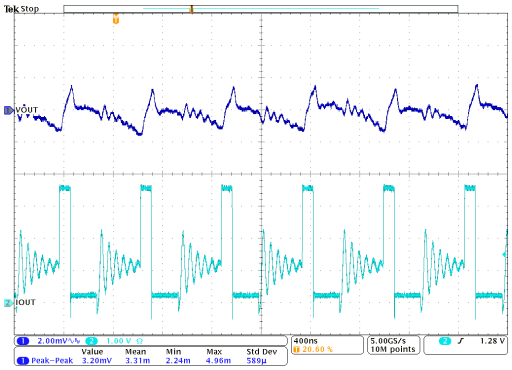
Vout=0.9V $C_{OUT(eff)}$=100µF Iout=15A→25A→15A (1A/µs)

Figure 9-21. Load Transient TPSM8287B30HAPx



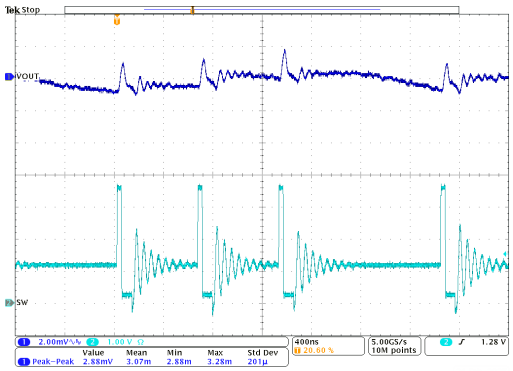
Vout = 0.9V I_{OUT} = 15A

Figure 9-22. PWM-CCM Operation TPSM8287B30HAPx



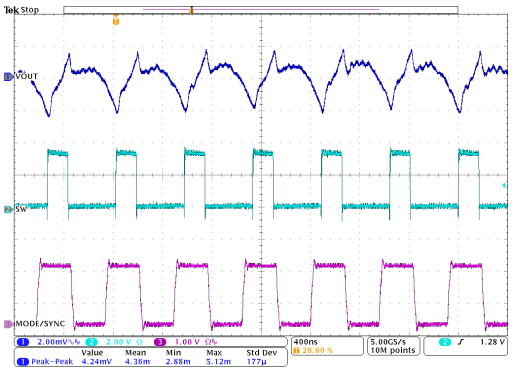
Vout = 0.9V I_{OUT} = 1A

Figure 9-23. PWM-DCM Operation TPSM8287B30HAPx



Vout = 0.9V I_{OUT} = 100mA

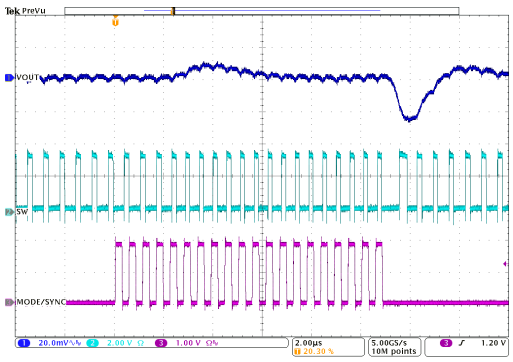
Figure 9-24. PFM-DCM Operation TPSM8287B30HAPx



I_{OUT} = 15A $f_{(SYNC)}$ = 1.8MHz

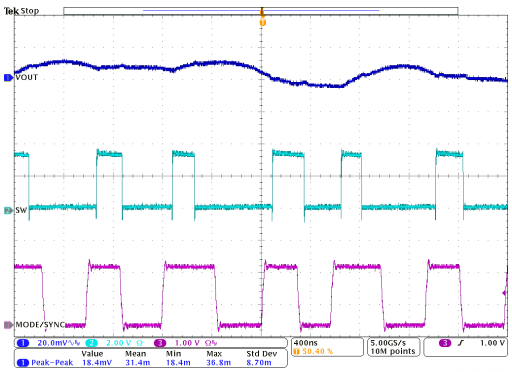
Figure 9-25. Synchronization to an External Clock TPSM8287B30HAPx

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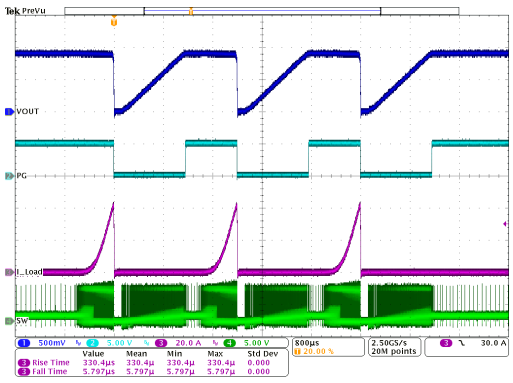
I_{OUT} = 15A V_{OUT} = 0.9V $f_{(SYNC)}$ = 1.8MHz

Figure 9-26. Adding and Removing an External Clock TPSM8287B30HAPx



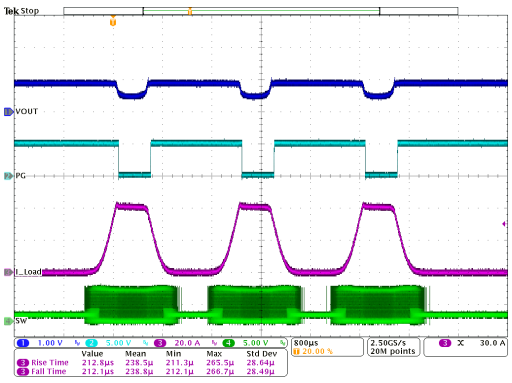
I_{OUT} = 15A V_{OUT} = 0.9V $f_{(SYNC)}$ = 1.2 to 1.8MHz (random)

Figure 9-27. Synchronization to a Random External Clock TPSM8287B30HAPx



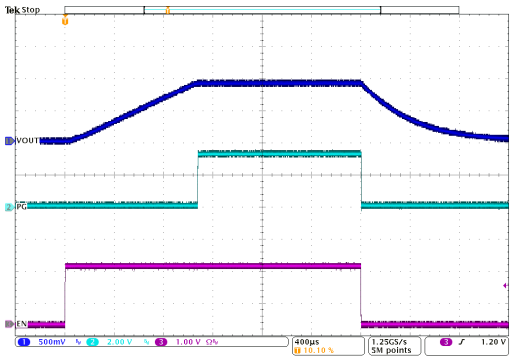
V_{IN} = 5.0V

Figure 9-28. Current Limit (Hiccup = 1)



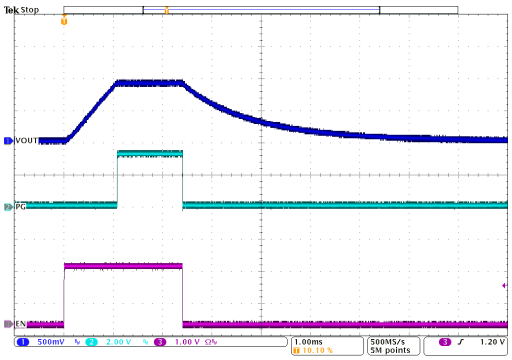
V_{IN} = 5.0V

Figure 9-29. Current Limit (Hiccup = 0)



V_{OUT} = 0.9V Load = 9.1Ω

Figure 9-30. Start-Up and Shutdown using EN Pin (DISCHEN = 1)



V_{OUT} = 0.9V Load = 9.1Ω

Figure 9-31. Start-Up and Shutdown using EN Pin (DISCHEN = 0)

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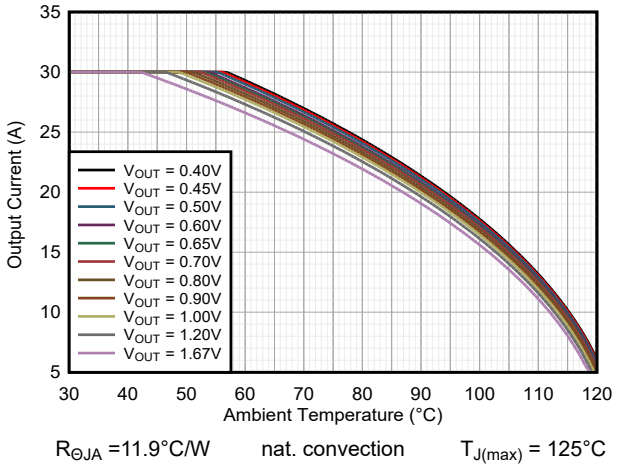


Figure 9-32. Safe Operating Area TPSM8287B30xx V_{IN} = 3.3V

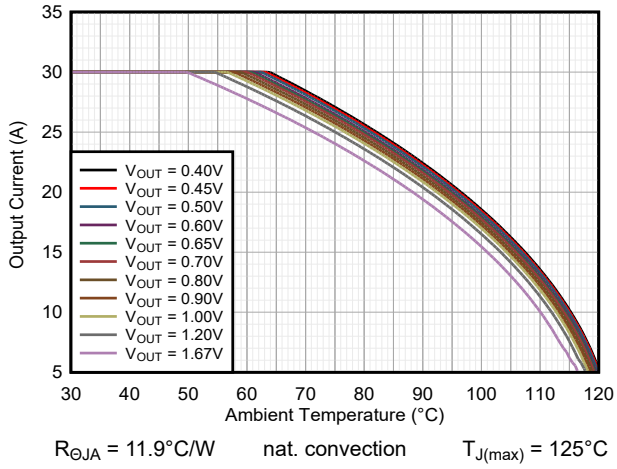


Figure 9-33. Safe Operating Area TPSM8287B30xx V_{IN} = 5.0V

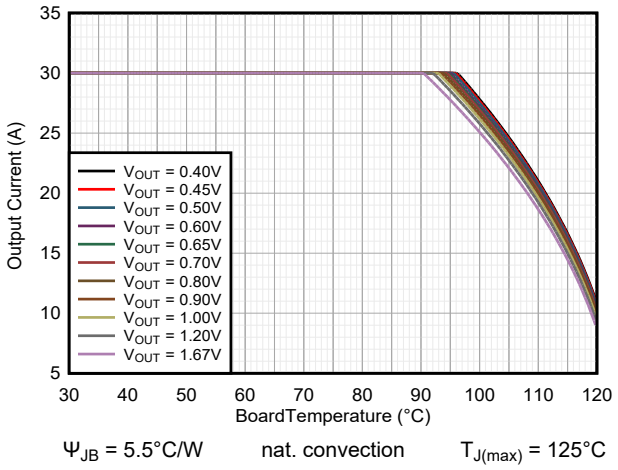


Figure 9-34. Safe Operating Area TPSM8287B30xx V_{IN} = 3.3V

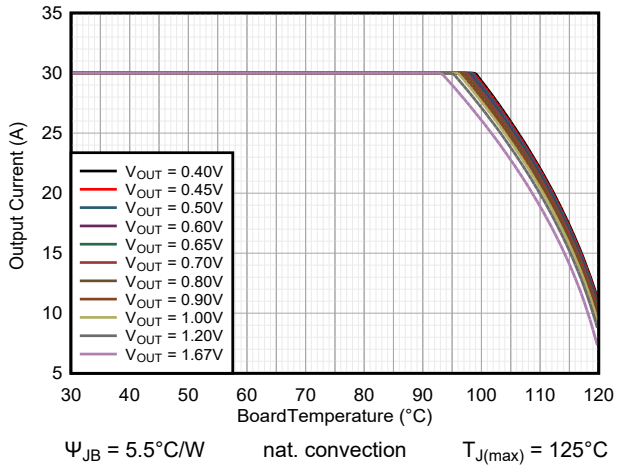


Figure 9-35. Safe Operating Area TPSM8287B30xx V_{IN} = 5.0V

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9.3 Typical Application Using Two TPSM8287B30x in Parallel Operation

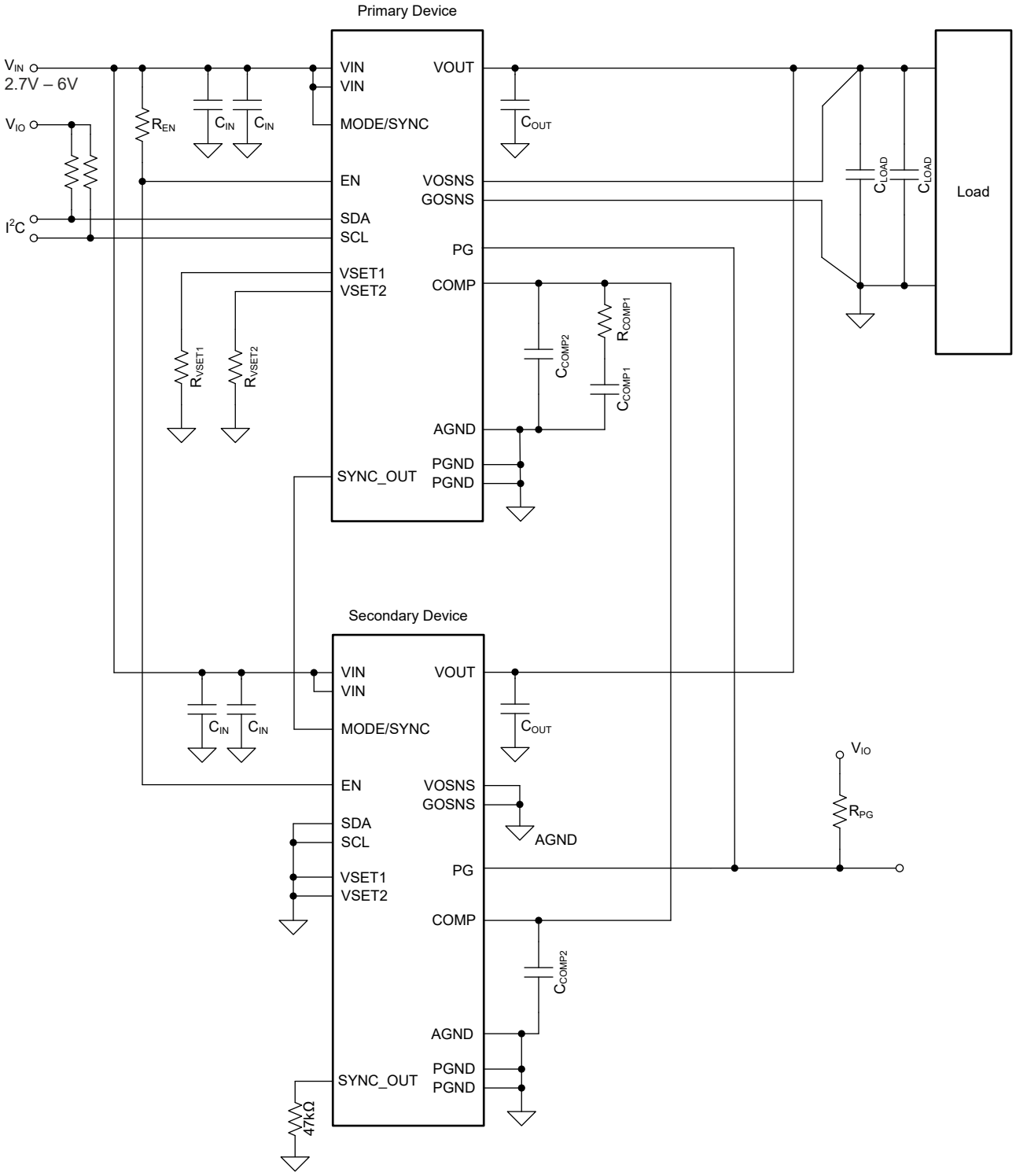


Figure 9-36. Typical Application Schematic

Table 9-3. List of Components

REFERENCE	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER (1)
C_{Comp1}	3.9nF	Ceramic Capacitor, X7R	Std	Std
C_{OUT}	4 × 22µF	Ceramic Capacitor, 6.3V, X6S, size 0603	GRM188C80J226ME01D	Murata
C_{LOAD}	6 × 47µF	Ceramic Capacitor, 4V, X6S, size 0603	GRM188C80G476ME01D	Murata
C_{LOAD}	4 × 10µF	Ceramic Capacitor, 4V, X6S, size 0402	GRM155C80G106ME18D	Murata
C_{IN}	8 × 22µF	Ceramic Capacitor, 10V, X6S, size 0603	GRM188C81A226ME01D	Murata
R_{Comp1}	604Ω	Resistor 1%, 0.1 W	Std	Std
R_{VSET1}, R_{VSET2}	Set per Table 7-2	Resistor 5%, 0.1 W	Std	Std
R_{EN}	15kΩ	Resistor 5%, 0.1 W	Std	Std
R_{SYNC_OUT}	47kΩ	Resistor 5%, 0.1 W	Std	Std

9.3.1 Design Requirements

The following table lists the operating parameters for this application example with two TPSM8287Bxx devices working in parallel to increase the output current.

Table 9-4. Design Parameters

SYMBOL	PARAMETER	VALUE
V_{IN}	Input voltage	2.7V – 6.0V
V_{OUT}	Output voltage	0.60V
TOL_{VOUT}	Output voltage tolerance allowed by the application	±5.0 %
TOL_{DC}	Output voltage tolerance of the TPSM8287Bxx (DC accuracy)	±0.8%
$\Delta I_{OUT(step)}$	Output current load step	±12.0A
t_t	Load step transition time	1µs
f_{SW}	Switching frequency	1.5MHz
L	Integrated inductor	50nH
TOL_{IND}	Integrated inductor tolerance	±20 %
g_m	Error amplifier transconductance	1.5mS
τ	Emulated current time constant	12.5µs
BW_T	Target loop bandwidth	375kHz
N_Φ	Number of paralleled devices (phases)	2

Preliminary Calculations

The maximum allowable deviation of the power supply is ±5.0%. The DC accuracy of the TPSM8287Bxx is specified as ±0.8%, and therefore the maximum output voltage variation during a transient is given by:

$$\Delta V_{OUT} = \pm V_{OUT} \times (TOL_{VOUT} - TOL_{DC}) \quad (30)$$

$$\Delta V_{OUT} = \pm V_{OUT} \times (5.0\% - 0.8\%) = \pm 25.2mV \quad (31)$$

Equation 32 calculates the peak-to-peak inductor current ripple, which is the greatest at the maximum input voltage:

$$I_{L(PP)} = \frac{V_{OUT}}{V_{IN(max)}}\left(\frac{V_{IN(max)} - V_{OUT}}{L \times f_{sw} \times N\Phi}\right) \quad (32)$$

$$I_{L(PP)} = \frac{0.6}{6.0}\left(\frac{6.0 - 0.6}{50 \times 10^{-9} \times 1.5 \times 10^{6} \times 2}\right) = 3.6A \quad (33)$$

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The maximum load step occurs when the load step from the application occurs at exactly the same time as the peak (or trough) of the inductor ripple current, and is given by:

$$\Delta I_{OUT(max)} = \Delta I_{OUT(step)} + \frac{\Delta I_{L(PP)}}{2} \quad (34)$$

$$\Delta I_{OUT(max)} = 12.0 + \frac{3.6}{2} = 13.8A \quad (35)$$

9.3.2 Detailed Design Procedure

The following subsections describe how to calculate the external components required to meet the specified transient requirements of a given application. The calculations include the worst-case variation of components and use the RMS method to combine the variation of uncorrelated parameters.

9.3.2.1 Selecting the Input Capacitors

The TPSM8287Bxx devices feature a *butterfly* or parallel layout with two pairs of VIN and PGND pins on opposite sides of the package.

The duty cycle of the converter is given by:

$$D = \frac{V_{OUT}}{\eta \times V_{IN}} \quad (36)$$

$$D = \frac{0.60}{0.75 \times 2.7} = 0.296 \quad (37)$$

Equation 38 shows the value of input capacitance needed to meet any system-level input voltage ripple requirement. For this example, the lowest input voltage and highest load current are used to generate a worst case input voltage ripple of 100mV.

$$C_{IN} = \frac{D \times (1 - D) \times I_{OUT}}{V_{IN(PP)} \times f_{sw}} \quad (38)$$

$$C_{IN} = \frac{0.296 \times (1 - 0.296) \times 60.0}{0.1 \times 1.5 \times 10^{6}} = 83.4\mu F \quad (39)$$

The value of C_{IN} calculated with Equation 38 is the *effective* capacitance after all derating, tolerance, and aging effects have been considered. In this parallel configuration, distributing the calculated input capacitance equally across all phases is important.

9.3.2.2 Selecting the Target Loop Bandwidth

The control loop bandwidth measures how quickly the device responds to a change in output voltage. With the TPSM8287Bxx external compensation, the loop bandwidth is adjustable to balance the tradeoff of a fast response versus stability and ringing. The R_{Comp1} resistor and output capacitance are the primary means of adjusting the loop bandwidth.

TI recommends setting the target loop bandwidth to 200kHz for a simple design. If strong load transients are expected in the application, the target bandwidth can be set as high as ¼ of the switching frequency. A target bandwidth of 375kHz is used for this example design.

9.3.2.3 Selecting the Compensation Resistor

Use Equation 40 to calculate the recommended value of compensation resistor, R_{Comp1}:

$$R_{Comp1} = \frac{1}{g_m}\left(\frac{\pi \times \Delta I_{OUT(step)} \times L}{4 \times \tau \times \Delta V_{OUT} \times N\Phi} - 1\right)(1 + TOL_{IND}) \quad (40)$$

$$R_{Comp1} = \frac{1}{1.5 \times 10^{-3}}\left(\frac{\pi \times 12.0 \times 50 \times 10^{-9}}{4 \times 12.5 \times 10^{-6} \times 25.2 \times 10^{-3} \times 2} - 1\right)(1 + 20\%) = 598.4\Omega \quad (41)$$

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Picking a standard component above the calculated value, a 604Ω resistor is chosen in this example. The selected value must be used for the further calculations.

9.3.2.4 Selecting the Output Capacitors

If the converter remains in regulation, the minimum required output capacitance is given by:

$$C_{OUT(min)(reg)} = \left(\frac{\tau \times g_m \times R_{Comp1}}{2 \times \pi \times \frac{L}{N\Phi} \times BW_\tau}\right)\left(1 + \sqrt{TOL_{IND}{}^2 + TOL_{fSW}{}^2}\right) \quad (42)$$

$$C_{OUT(min)(reg)} = \left(\frac{12.5 \times 10^{-6} \times 1.5 \times 10^{-3} \times 604}{2 \times \pi \times \frac{50 \times 10^{-9}}{2} \times 375 \times 10^{3}}\right)\left(1 + \sqrt{20\%^2 + 10\%^2}\right) = 235\mu F \quad (43)$$

If the converter loop saturates, the minimum output capacitance is given by:

$$C_{OUT(min)(sat)} = \frac{1}{\Delta V_{OUT}}\left(\frac{L \times \Delta I_{OUT(max)}{}^2}{2 \times V_{OUT} \times N\Phi} - \frac{\Delta I_{OUT(step)} \times t_t}{2}\right)(1 + TOL_{IND}) \quad (44)$$

$$C_{OUT(min)(sat)} = \frac{1}{25.2 \times 10^{-3}}\left(\frac{50 \times 10^{-9} \times 13.8^2}{2 \times 0.6 \times 2} - \frac{13.8 \times 1 \times 10^{-6}}{2}\right)(1 + 20\%) = -97\mu F \quad (45)$$

The negative result for $C_{OUT(min)(sat)}$ indicates that the loop does not saturate, with the given load transient, and that the response is limited by the bandwidth. In this case, choose $C_{OUT(min)(reg)}$ = 235µF as the larger of the two values for the output capacitance.

Table 9-3 lists the output capacitors chosen. 2 × 22µF capacitors are placed close to each of the two modules, giving a minimum effective capacitance of about 15µF each. Six 47µF capacitors and four 10µF are placed near the load to approximate the total decoupling capacitance required by a typical load. Each of the 47µF capacitors yields about 27µF of effective capacitance and each of the 10µF capacitors yields about 6µF. Device variants with capacitors integrated inside the module provide additional 2 × 14µF of effective capacitance. Together, the 274µF of effective capacitance is greater than the required minimum value calculated above. For further calculations, use C_{OUT_eff} = 274µF.

Equation 46 checks that most of the output capacitance is placed at the load. If the ratio is less than 1, increase the capacitance at the load or place the device, output capacitance, and load next to each other such that there is no separation between the output capacitances.

$$\frac{C_{LOAD_eff}}{C_{Converter_eff} + C_{Integrated_eff}} > 1 \quad (46)$$

$$\frac{6 \times 27 \times 10^{-6} + 4 \times 6 \times 10^{-6}}{4 \times 15 \times 10^{-6} + 4 \times 7 \times 10^{-6}} > 1 = \text{True} \quad (47)$$

Equation 48 calculates the output voltage ripple, based on the effective output capacitance value.

$$V_{OUT(p-p)} = \frac{I_{L(PP)}}{8 \times C_{OUT_eff} \times f_{sw}} \quad (48)$$

$$V_{OUT(p-p)} = \frac{3.6}{8 \times 274 \times 10^{-6} \times 1.5 \times 10^{6}} = 1.1mV \quad (49)$$

The ripple is slightly higher in the application due to the ESR and ESL in the output capacitors and the application board parasitics.

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9.3.2.5 Selecting the Compensation Capacitor, C_{Comp1}

First, use Equation 50 to calculate the bandwidth of the loop:

$$BW = \frac{\tau \times g_m \times R_{Comp1}}{2\pi \times \frac{L}{N\Phi} \times C_{OUT_eff}} \quad (50)$$

$$BW = \frac{12.5 \times 10^{-6} \times 1.5 \times 10^{-3} \times 604}{2\pi \times \frac{50 \times 10^{-9}}{2} \times 274 \times 10^{-6}} = 263.1\text{kHz} \quad (51)$$

Use Equation 52 to calculate the recommended value of C_{Comp1}.

$$C_{Comp1} = \frac{2}{\pi \times BW \times R_{Comp1}} \quad (52)$$

$$C_{Comp1} = \frac{2}{\pi \times 263.1 \times 10^{3} \times 604} = 4\text{nF} \quad (53)$$

The closest standard value is 3.9nF.

9.3.2.6 Selecting the Compensation Capacitor, C_{Comp2}

The compensation capacitor, C_{Comp2}, is an optional capacitor that TI recommends the user include to bypass high-frequency noise away from the COMP pin. The value of this capacitor is not critical; 10pF or 22pF capacitors are recommended for typical applications.

This capacitor can be made larger to suppress high-frequency zeros or resonances that occur in the system output voltage routing and decoupling network. The following equation calculates the pole created by C_{Comp2}.

$$f_{pole} = \frac{1}{2 \times \pi \times R_{Comp1} \times C_{Comp2}} \quad (54)$$

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9.3.3 Application Curves

V_{IN} = 5.0V, V_{OUT} = 0.6V, T_A = 25°C, BOM = Table 9-3, 2 × TPSM8287B30Lx in parallel operation, unless otherwise noted.

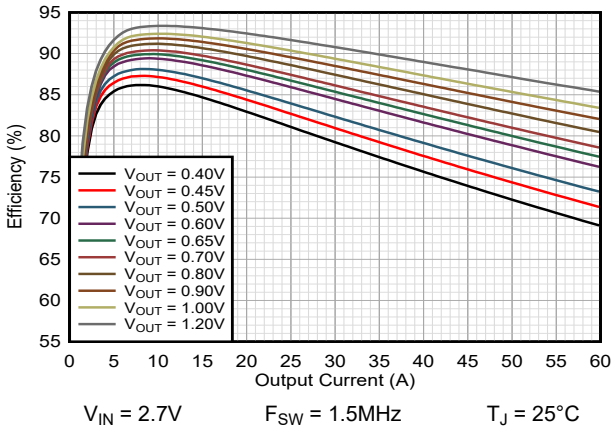


Figure 9-37. Efficiency TPSM8287B30xx FPWM

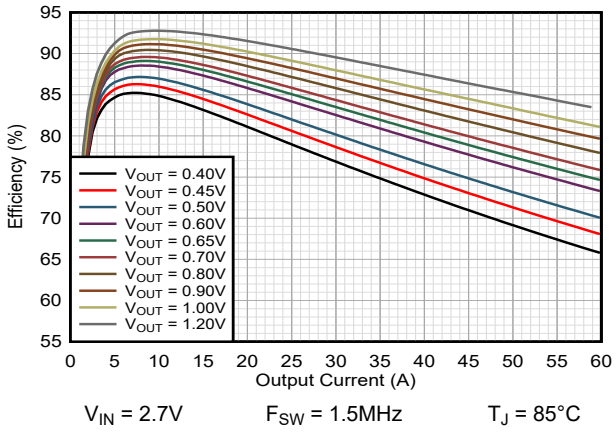


Figure 9-38. Efficiency TPSM8287B30xx FPWM

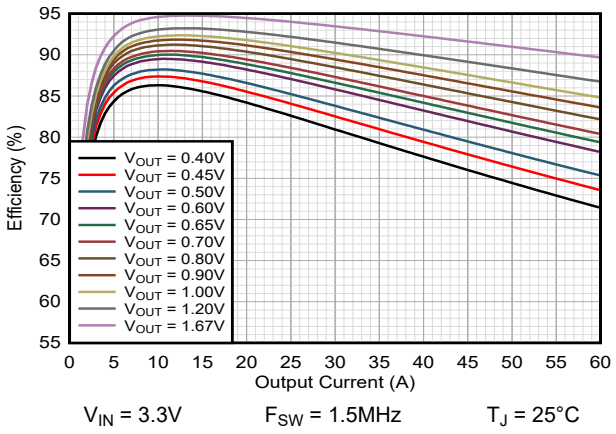


Figure 9-39. Efficiency TPSM8287B30xx FPWM

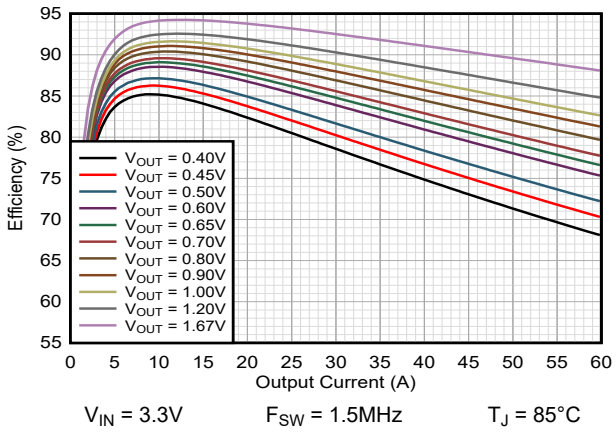


Figure 9-40. Efficiency TPSM8287B30xx FPWM

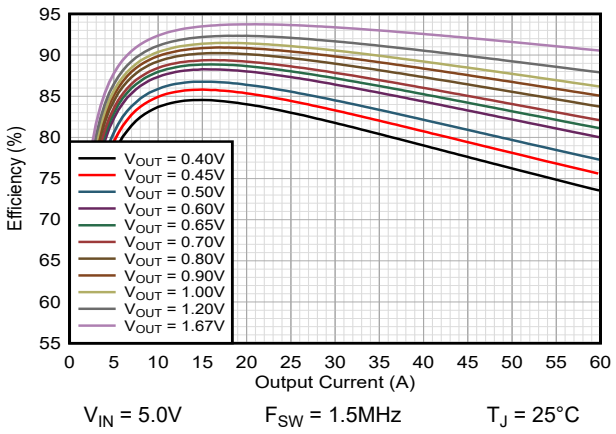


Figure 9-41. Efficiency TPSM8287B30xx FPWM

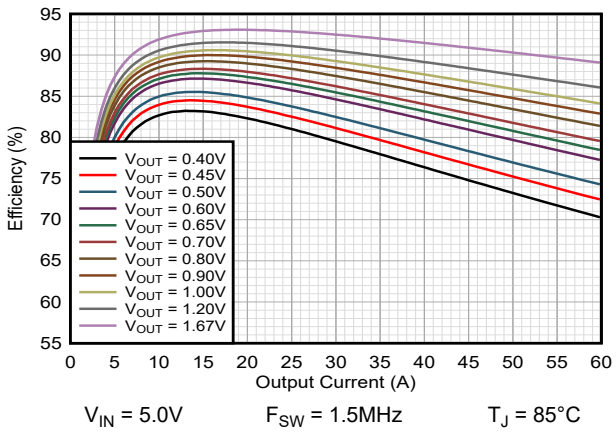
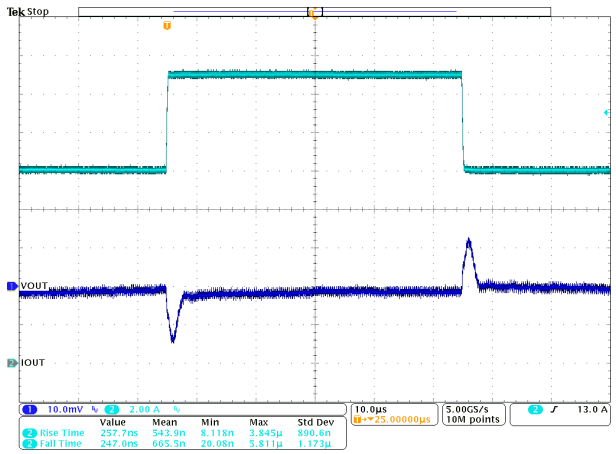


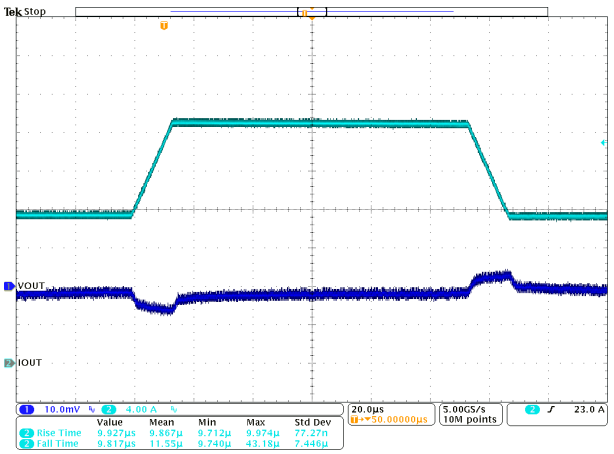
Figure 9-42. Efficiency TPSM8287B30xx FPWM

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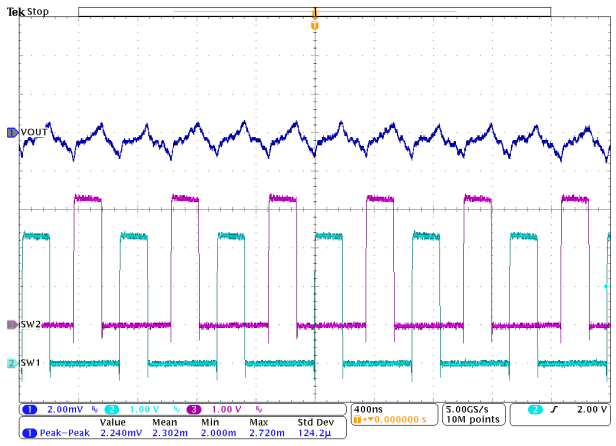
V_{OUT}=0.9V $C_{OUT(eff)}$=274µF I_{OUT}=10A→15A→10A

Figure 9-43. Load Transient TPSM8287B30HAPx



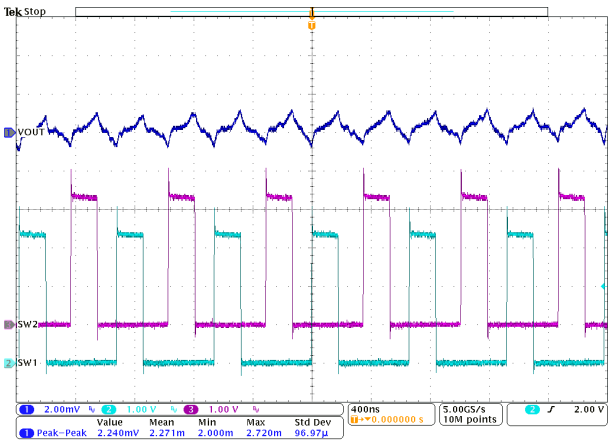
V_{OUT}=0.9V $C_{OUT(eff)}$=274µF I_{OUT}=15A→25A→15A

Figure 9-44. Load Transient TPSM8287B30HAPx



V_{OUT} = 0.9V I_{OUT}= 15A

Figure 9-45. PWM-CCM Operation TPSM8287B30HAPx



V_{OUT} = 0.9V I_{OUT}= 1A

Figure 9-46. PWM-CCM Operation TPSM8287B30HAPx

9.4 Power Supply Recommendations

The TPSM8287Bxx family has no special requirements for the input power supply. The output current rating of the input power supply must be rated according to the supply voltage and current requirements of the TPSM8287Bxx. For proper operation, the input voltage must be at least 1.5V above the selected output voltage.

9.5 Layout

9.5.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM8287Bxx demands careful attention to make sure of best performance. A poor layout can lead to issues like the following:

- Bad line and load regulation
- Instability
- Increased EMI radiation
- Noise sensitivity

Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal for a detailed discussion of general best practices. The following are specific recommendations for the TPSM8287Bxx:

- Place the input capacitors as close as possible to the VIN and PGND pins of the device. This placement is the most critical component placement. Route the input capacitors directly to the VIN and PGND pins avoiding vias.
- Place the output capacitors close to the VOUT and PGND pins and route them directly avoiding vias.
- Place the IC close to the load to minimize the power loss from voltage drop on the output and to minimize parasitic inductance between the output capacitors at the TPSM8287Bxx and those at the load.
- Use vias under the exposed thermal pads to improve thermal performance. Directly connect the PGND pins to the exposed thermal pad with copper on the top PCB layer.
- Route the VOSNS and GOSNS remote sense lines as a differential pair and connect them to the lowest impedance point at the load. Do not route the VOSNS and GOSNS traces close to any switch nodes, the input capacitors, clock signals, or other aggressor signals.
- Connect the compensation components between COMP and AGND. Do not connect the compensation components directly to power ground.
- Place the VSETx resistors (and SYNC_OUT resistor in the secondary devices) close to the TPSM8287Bxx to minimize parasitic capacitance.
- In the stacked configuration, route COMP directly to keep COMP short and avoid noisy aggressor signals.
- Refer to Figure 9-47 for an example of component placement, routing, and thermal design.

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9.5.2 Layout Example

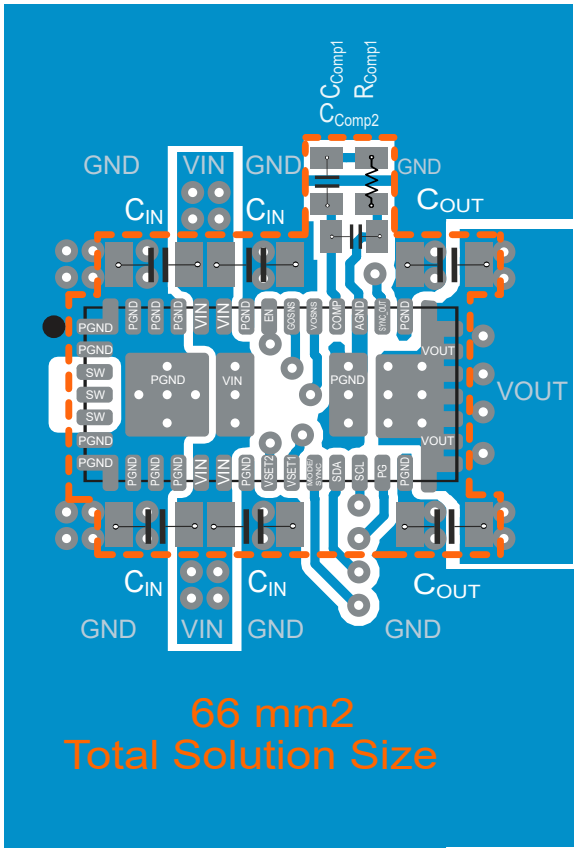


Figure 9-47. Layout Example

9.5.2.1 Thermal Considerations

The TPSM8287Bxx power module temperature must be kept less than the maximum rating of 125°C. The following are three basic approaches for enhancing thermal performance:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the approximate module temperature of the TPSM8287Bxx, apply the typical efficiency stated in this data sheet to the desired application condition to compute the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by the thermal resistance. For a known board temperature use Ψ_{JB}, and for a known ambient temperature use $R_{\Theta JA}$. The thermal parameters depend on PCB construction, layout and airflow.

Using this method to compute the maximum device temperature, the Safe Operating Area (SOA) graphs demonstrates the required derating in maximum output current at high ambient temperatures for the EVM. For more details on how to use the thermal parameters in real applications, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note and *Semiconductor and IC Package Thermal Metrics* application note.

The thermal values in *Thermal Information* used the recommended land pattern, shown at the end of this data sheet, including the vias as shown. The TPSM8287Bxx was simulated on a PCB defined by JEDEC 51-7. The vias on the two PGND Exposed Thermal Pads were connected to copper on other PCB layers, while the remaining vias were not connected to other layers.

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10 Device and Documentation Support

10.1 Device Support

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10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Achieving a clean startup by using a DC/DC converter with a precise enable-pin threshold* analog design journal
- Texas Instruments, *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

Changes from Revision A (December 2025) to Revision B (October 2026)	Page
• Changed TPSM8287BxxxANVCHR from Preview to Production Data	3

Changes from Revision * (March 2025) to Revision A (December 2025)	Page
• Updated the *Features*, *Electrical Characteristics* table, *Feature Description*, *Application Information*, and *Design Requirements* table to the production data specifications	3
• Added new device spins to the data sheet in the *Device Options* table	3

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM8287B15HANVCHR	Active	Production	QFN-FCMOD (VCH) | 37	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM8B15HAN
TPSM8287B30HANVCHR	Active	Production	QFN-FCMOD (VCH) | 37	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM8B30HAN
TPSM8287B30LANVCHR	Active	Production	QFN-FCMOD (VCH) | 37	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM8B30LAN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

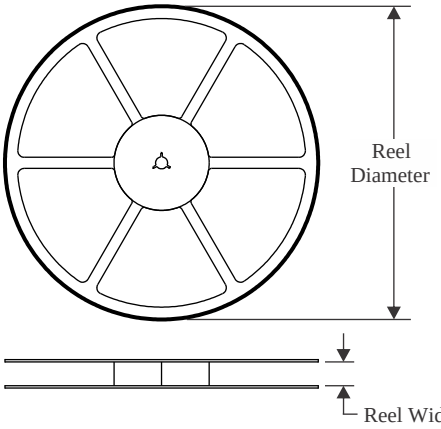
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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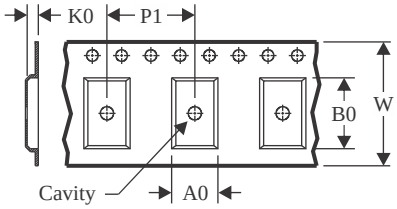
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

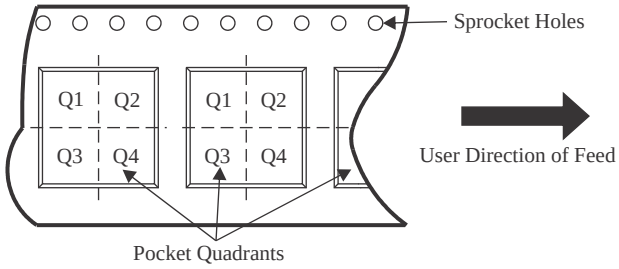


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

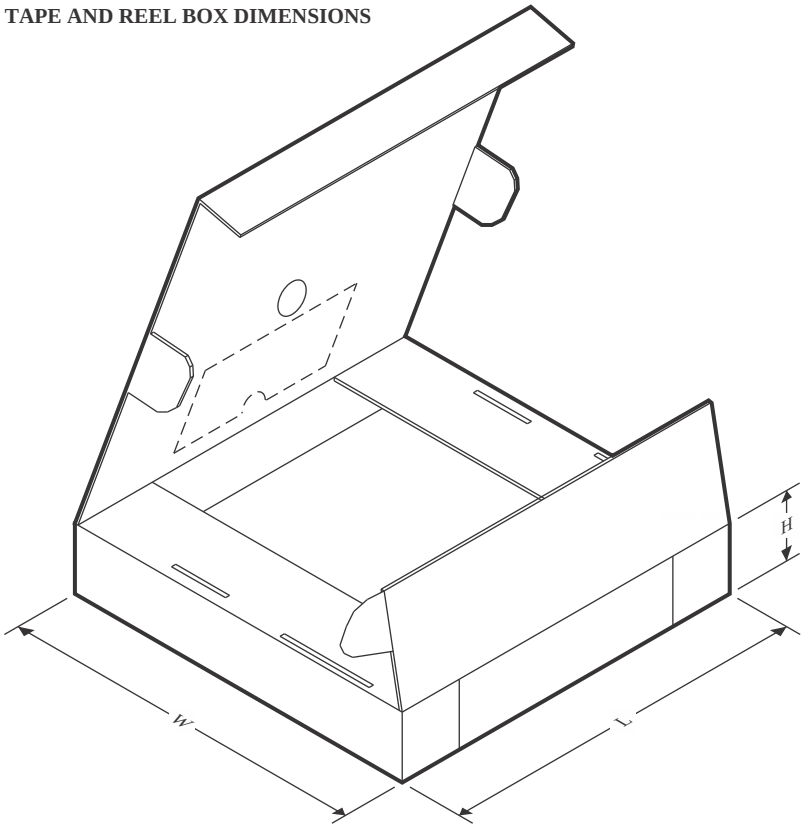
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM8287B15HANVCHR	QFN-FCMOD	VCH	37	2500	330.0	16.4	4.05	3.5	2.4	8.0	16.0	Q2
TPSM8287B30HANVCHR	QFN-FCMOD	VCH	37	2500	330.0	16.4	4.05	3.5	2.4	8.0	16.0	Q2
TPSM8287B30LANVCHR	QFN-FCMOD	VCH	37	2500	330.0	16.4	4.05	3.5	2.4	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM8287B15HANVCHR	QFN-FCMOD	VCH	37	2500	367.0	367.0	38.0
TPSM8287B30HANVCHR	QFN-FCMOD	VCH	37	2500	367.0	367.0	38.0
TPSM8287B30LANVCHR	QFN-FCMOD	VCH	37	2500	367.0	367.0	38.0

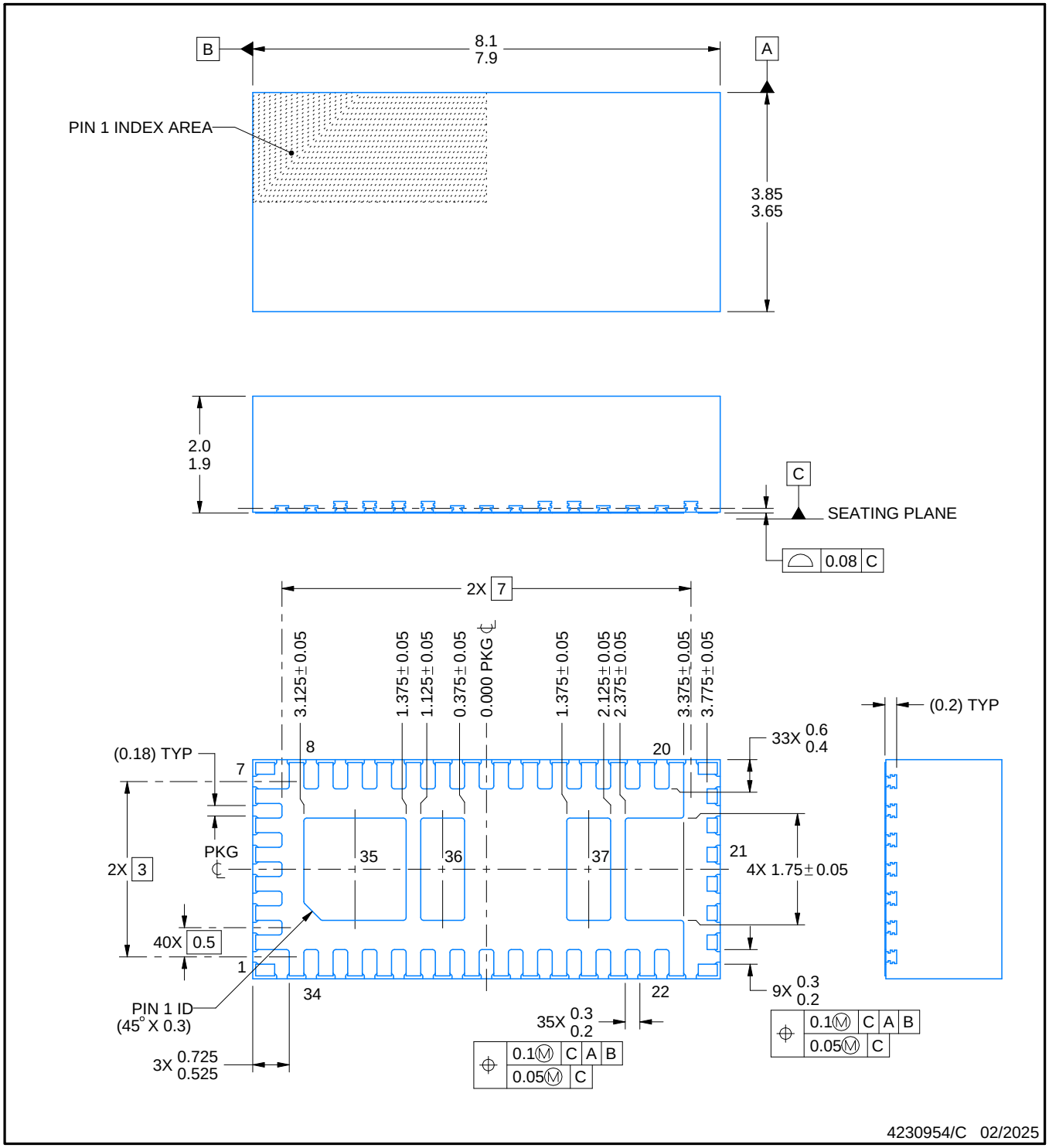
VCH0037A



PACKAGE OUTLINE

VQFN - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

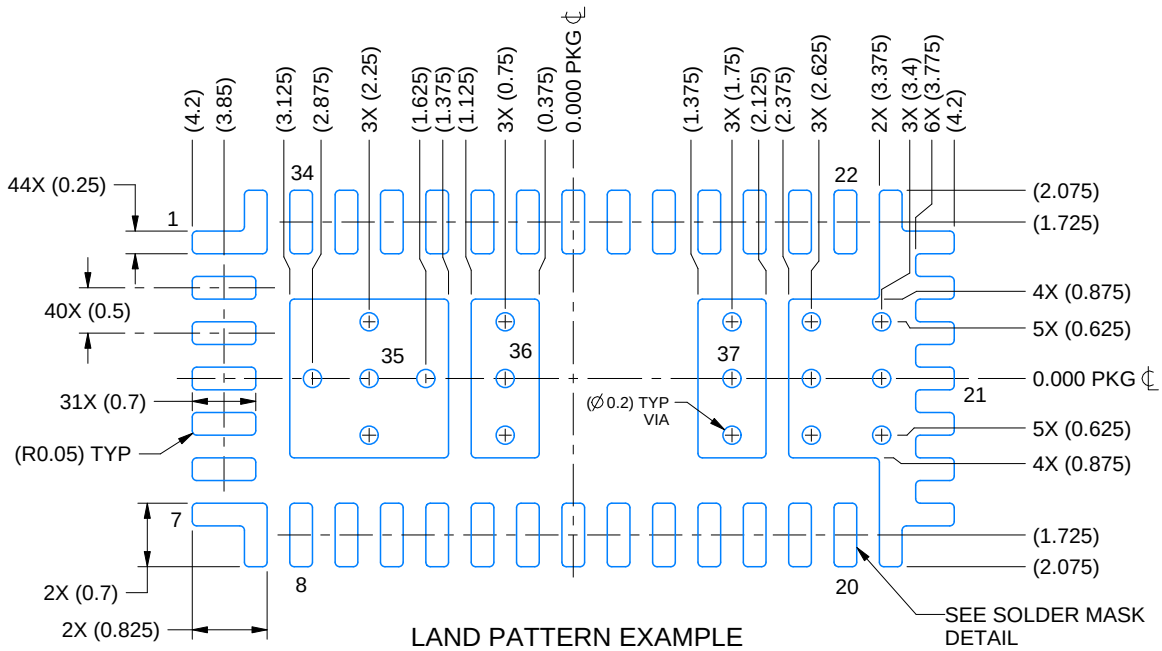
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

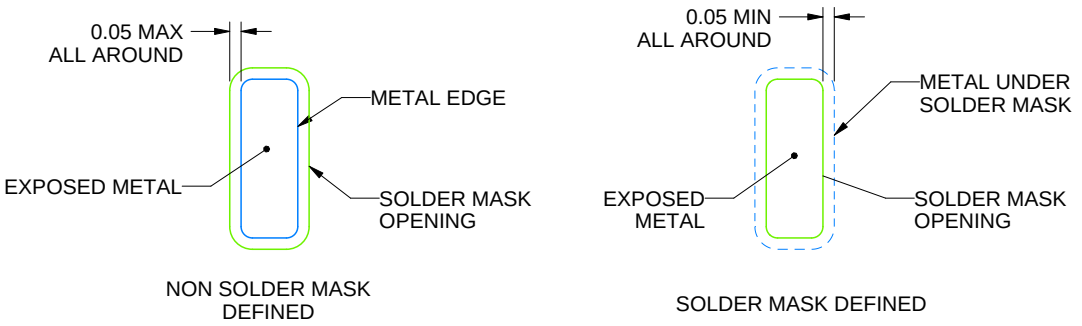
VCH0037A

VQFN - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

4230954/C 02/2025

NOTES: (continued)

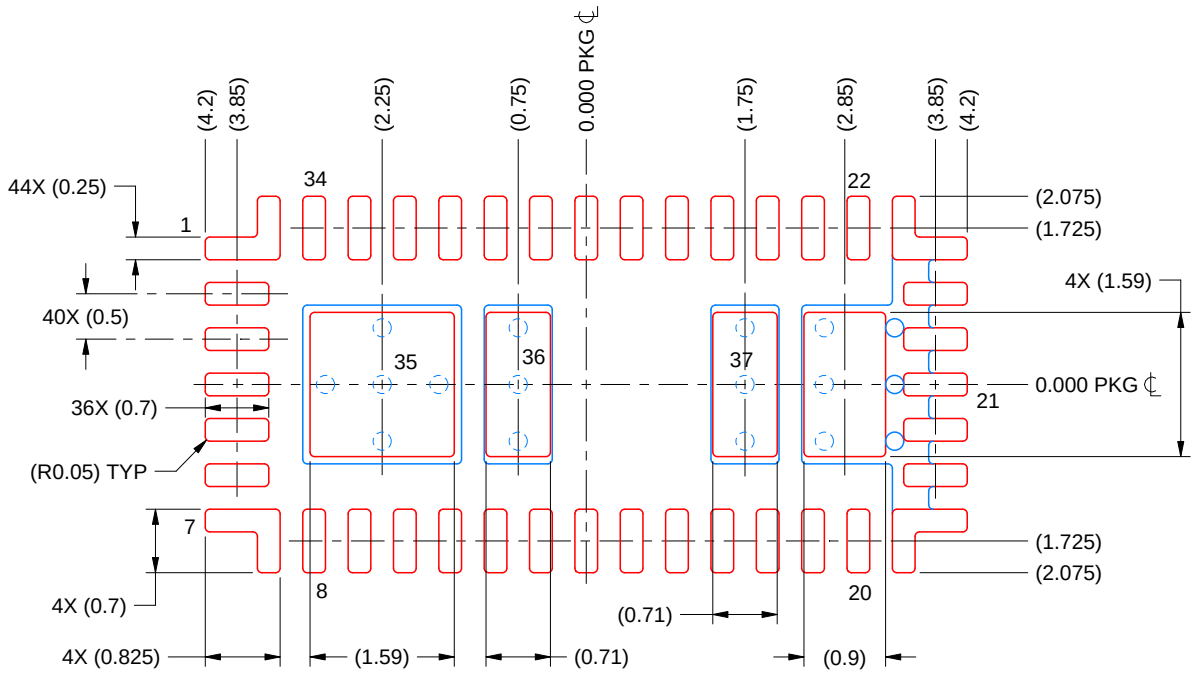
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VCH0037A

VQFN - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 21: 77%
PAD 35: 83%
PADS 36 & 37: 86%

4230954/C 02/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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