

TPS7H6200-SEP Radiation-Tolerant 52A GaN Half-Bridge Power Stage with Low-Side Current Sense

1 Features

- Total ionizing dose (TID) characterized up to 50krad(Si)
- Destructive Single Event Effects (DSEE) characterized
 - Single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune up to linear energy transfer LET = 43MeV·cm²/mg
- Single Event Effects characterized
 - Single-event functional interrupt (SEFI) and single-event transient (SET) characterized up to LET = 43MeV·cm²/mg
- Available in military (–55°C to 125°C) temperature
- 3.2mΩ (typ) high side FET R_{DS(on)}, 1mΩ low side FET R_{DS(on)}
- High efficiency (V_{PVIN} = 12V, V_{VOU}T = 0.8V, f_{SW} = 500kHz, T_A = 25°C, L = 200nH, DCR = 180mΩ):
 - η = 89.6% at 20A
 - η = 87.2% at 40A
 - η = 84.9% at 52A
- 52A maximum continuous current
- Integrated low-side current sense
 - Total RSS accuracy of 14.5% for nominal load currents greater than 40A
- Fault pin indicator for overcurrent, overtemperature, or UVLO detection
- DrMOS 3.3V and 5V PWM input signal compatibility
- Integrated overtemperature and overcurrent protection

2 Applications

- Point of load supply
- Communications payload
- Radar imaging payload

3 Description

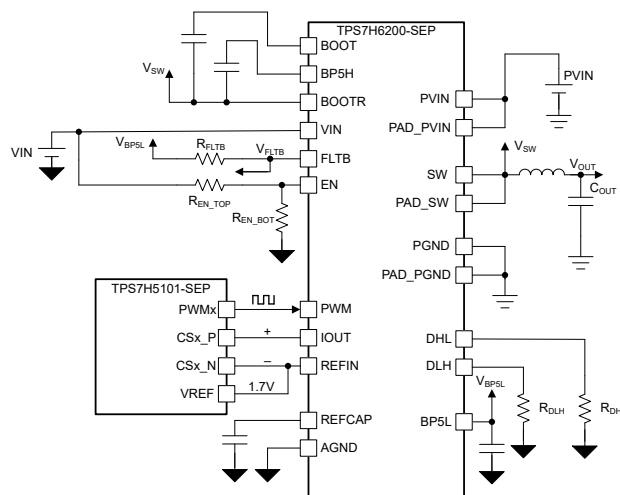
The TPS7H6200-SEP is a 15V e-mode GaN power-FET with integrated gate driver featuring tri-state PWM compatibility, integrated low side current sense, overtemperature protection, and overcurrent protection.

The GaN FET half-bridge die combines the high-side and low-side GaN FETs on one substrate, minimizing parasitic inductance. The device is asymmetrically sized for point-of-load voltage conversion, 1mΩ on the low side and 3mΩ on the high side, optimizing performance and efficiency for typical input to output conversion ratios. As a result, the TPS7H6200-SEP can achieve efficiencies exceeding 89.6% at a typical load of 20A.

Device Information

PART NUMBER⁽¹⁾	Grade	Package⁽²⁾
TPS7H6200MVEJTNSP ⁽³⁾	SEP	49-pin WQFN-FCRLF 6.00mm × 6.00mm Mass = 72.9mg

- (1) For additional information, see [Device Options Table](#)
- (2) Dimension and mass values are nominal
- (3) Advance Information



Typical Application

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4 Device Options Table

Generic Part Number	Radiation Rating ⁽¹⁾	Grade ⁽²⁾	Package	Orderable Part Number
TPS7H6200-SEP	TID of 50krad(Si) RLAT, DSEE free to 43MeV·cm ² /mg	Space Enhanced Plastic	49in plastic WQFN-FCRLF (VEJ)	TPS7H6200VEJMTNSP

- (1) TID is total ionizing dose, RLAT is radiation lot acceptance testing, and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
- (2) For additional information about part grade, view [SLBY235](#)

5 Pin Configuration and Functions

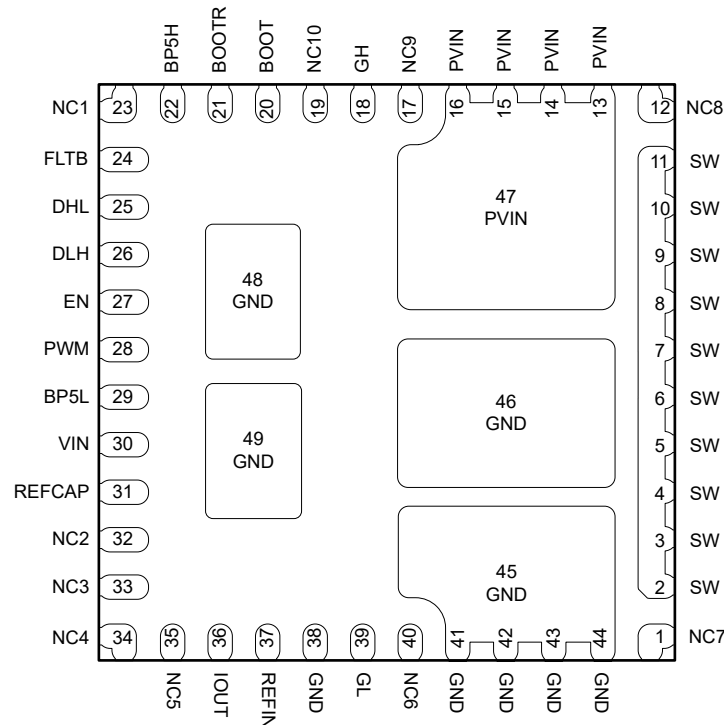


Figure 5-1. TPS7H6200-SEP 49-Pin VEJ0049A, WQFN-FCRL Package (Top View)

Table 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
BOOT	20	P	High-side bootstrap supply input. This pin provides the floating supply voltage required for the high-side gate driver. Connect a 100nF ceramic capacitor between the BOOT and BOOTR pins.
BOOTR	21	P	High-side bootstrap return. This pin serves as the return path for the high-side gate driver and is internally tied to the SW (Switch) node.
BP5H	22	P	The high-side 5.5V LDO output requires a 1μF ceramic capacitor connected to BP5H and BOOTR. Place the capacitor as close to the package as possible and avoid adding external loads. For bottom-side mounting, use multiple in-pad vias to minimize parasitic inductance.
BP5L	29	P	Low-side 5.5V linear regulator output: Connect a 1μF ceramic capacitor between BP5L and GND, placing the component as close to the package as possible. Connections to DHL and DLH, as well as a pull-up to FLT, are permitted; however, the current draw from BP5L must not exceed 100μA. Do not connect any additional components to the BP5L pin. If the capacitor is mounted on the bottom side of the PCB, use multiple in-pad vias to minimize parasitic inductance.
DHL	25	I	High-side to low-side dead-time set. Connect a 10kΩ resistor from DHL to GND to set the dead-time. Additional options are described in Section 9.2.2.2
DLH	26	I	Low-side to high-side dead-time set. Connect a 10kΩ resistor from DLH to GND to set the dead-time. Additional options are described in Section 9.2.2.2
EN	27	I	Enable. Driving this terminal to logic high enables the device; driving the terminal to logic low disables the device. Optionally, a resistor divider from VIN to GND can be used to set the device turn-on level.

Table 5-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
FLT_B	24	O	Fault pin. An open-drain pin that asserts low when an overcurrent event, overtemperature, or UVLO entry event is detected. Connect a 10kΩ pull-up resistor to a 5V supply or to BP5L.
GH	18	O	High-side gate pin. This pin provides access to the gate of the high-side GaN FET for debugging and testing purposes. Do not connect sensing or external networks to this pin during operation.
GL	39	O	Low-side gate pin. This pin provides access to the gate of the low-side GaN FET for debugging and testing purposes. Do not connect sensing or external networks to this pin during operation.
GND	38, 41 to 46, 48 to 49	G	Driver signal return, connected internally to the source terminal of the low-side GaN FET; pins 41 to 46 are in the high current path.
IOUT	36	O	Output of current sensing amplifier. $V(IOUT) - V(REFIN)$ is proportional to the phase current.
NC1	23	—	No connect. Used to anchor the package to the PCB. Pin NC1 is internally pulled to a voltage. TI recommends to connect NC1 to GND, optionally NC1 can be left floating.
NC2	32	—	No connect. Pin NC2 is internally pulled to a voltage. TI recommends to connect NC2 to GND, optionally NC2 can be left floating.
NC3	33	—	No connect. Pin NC3 is internally pulled down to GND. TI recommends to connect NC3 to GND, optionally NC3 can be left floating.
NC4	34	—	No connect. Used to anchor the package to the PCB. Pin NC4 is internally pulled down to GND. TI recommends to connect NC4 to GND, optionally NC4 can be left floating.
NC5	35	—	No connect. Pin NC5 is internally pulled down to GND. TI recommends to connect NC5 to GND, optionally NC5 can be left floating.
NC6	40	—	No connect. Pin NC6 is not internally connected to the device. TI recommends to connect NC6 to GND to prevent charge build up; however, NC6 can be left floating.
NC7	1	—	No connect. Used to anchor the package to the PCB. Pin NC7 is not internally connected to the device. TI recommends to connect NC7 to GND or SW to prevent charge build up; optionally NC7 can be left floating.
NC8	12	—	No connect. Used to anchor the package to the PCB. Pin NC8 is not internally connected to the device, TI recommends to connect NC8 to PVIN or SW to prevent charge build up; optionally NC8 can be left floating.
NC9	17	—	No connect. Pin NC9 is not internally connected to the device. TI recommends to connect NC9 to GND or PVIN to prevent charge build up; optionally pin NC9 can be left floating.
NC10	19	—	No connect. Pin NC10 is not internally connected to the device. TI recommends to connect NC10 to GND or PVIN to prevent charge buildup; optionally, NC10 can be left floating.
PVIN	13 to 16, 47	P	Internally connected to the high side GaN FETs drain terminal; this connection is part of the high current path.
PWM	28	I	Tri-state input from external controller. Logic-low turns-on the low-side FET, logic-high turns-on the high-side FET, and tri-state turns off both FETs
REFCAP	31	O	1.2V internal reference. Requires a 470nF external capacitor to GND.
REFIN	37	I	External reference voltage input for the IOUT current sense output. Apply a 1V to 2V reference voltage.
SW	2 to 11	P	Switch-node pins connecting the high-side source to the low-side drain, connect to the output inductor. This connection forms part of the high current path.
VIN	30	P	Supply voltage for internal gate drive circuitry.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	VIN, PVIN	−0.3	17	V
	EN, PWM	−0.3	7.5	
	REFIN	−0.3	BP5L + 0.3	
	BOOT	−0.3	33	
Output voltage	BP5L, DHL, DLH, FLTb	−0.3	7.5	V
	BP5H - SW	−0.3	33	
	REFCAP	−0.3	1.9	
	SW	−3.5	17	
	IOUT	−0.3	BP5L + 0.5	
Output current	$I_{SW(pulse)}$, single-pulse drain current $t_p < 80\mu s$		125	A
T _J	Operating junction temperature	−55	150	°C
T _{STG}	Storage temperature, T _{stg}	−65	150	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±500	V
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±250	V

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
Input Voltage	VIN		8.5		15	V
	PVIN		4.5		15	
	EN		0		5	
	PWM		0		5	
	REFIN		1	1.7	2	
	V _{IH}	PWM input voltage, logic-high	3			
	V _{IL}	PWM input voltage, logic-low			0.7	
	V _{MID}	PWM input voltage, logic tri-state	1.5		1.8	
Output Voltage	FLTB		0		5	V
	BOOT		V _{SW} +5V		V _{SW} +14V	
	SW		–3		15	
Output Current	I _{OUT(CONT)}	Output current (DC Average)			52	A
	I _{HS(RMS)}	High-side GaN FET RMS current			12.5	
	I _{LS(RMS)}	Low-side GaN FET RMS current			50.5	
	I _{CS(range)}	Current sense range	–20		90	ns
	t _{ON(min)}	Minimum input pulse duration	10			
	Operating junction temperature		–55		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7H6200-SEP	UNIT
		WQFN	
		49 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	23.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	8.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	1.3	°C/W
R _{θJC(HS)(bot)}	Junction-to-case high-side FET (PVIN pad) ⁽²⁾	3.8	°C/W
R _{θJC(LS)(bot)}	Junction-to-case low-side FET (GND pad) ⁽²⁾	1.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	7.1	°C/W
Ψ _{θJT}	Junction-to-top characterization parameter	1.0	°C/W
Ψ _{θJB}	Junction-to-board characterization parameter	7.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the [SPRA953](#) application note
(2) Junction-to-case bottom thermal resistance of the associated thermal pad

6.5 Electrical Characteristics

8.5V ≤ VIN ≤ 15V, R_{DLH} = R_{DHL} = 10kΩ, -55°C ≤ T_A ≤ 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
GAN POWER FETs								
r _{DS(on)(ls)}	Low-side R _{DS(on)}	V _{PWM} = 5V I _{SW_PGND} = 5A	T _A = −55°C		0.8	1.2	mΩ	
			T _A = 25°C		1	1.5		
			T _A = 125°C		1.5	2		
V _{SD(ls)}	Low-side source-drain (GND to SW) third quadrant voltage	I _{SW_GND} = −2A			1.5	3	V	
r _{DS(on)(hs)}	High-side R _{DS(on)}	V _{EN} = 5V I _{VIN_SW} = 2A	T _A = −55°C		2.4	3.6	mΩ	
			T _A = 25°C		3.2	4		
			T _A = 125°C		4.27	5.2		
V _{SD(hs)}	High-side source-drain (SW to PVIN) third quadrant voltage	I _{VIN_SW} = −2A			1.5	3	V	
SUPPLY CURRENTS								
I _{SHDN}	Shutdown current	EN = 0V BOOT = 10V			12	20	mA	
I _{BOOT}	BOOT current	SW = 12V, BOOT = 22V			5.5	8	mA	
I _{OP}	Operating current	PVIN = 0V Duty cycle = 10%	f _{SW} = 100kHz		12	40	mA	
			f _{SW} = 500kHz		26	60		
			f _{SW} = 1MHz		45	90		
INTERNAL REGULATORS								
V _{BP5L}	Low-side 5V regulator output voltage	C _{BP5L} = 1μF, I _{BP5L} = 37.5mA, V _{BOOT} = V _{IN} −3.5V		5	5.5	5.9	V	
V _{BP5H}	High-side 5V regulator output voltage	C _{BP5H} = 1μF I _{BP5H} = 3mA V _{BOOT} = V _{IN} -3.5V	10V ≤ V _{IN} ≤ 15V	4.9	5.5	5.9	V	
			8.5V ≤ V _{IN} ≤ 10V	3.3	5.4	5.7		
REFCAP	REFCAP voltage	C _{REF} = 470nF		1.16	1.2	1.23	V	
UVLO and ENABLE								
BP5H _R	BP5H UVLO rising threshold	C _{BP5H} = 1μF		3.2	3.41	3.61	V	
BP5H _F	BP5H UVLO falling threshold			3.1	3.25	3.4		
BP5H _H	BP5H UVLO hysteresis			0.17				
BP5L _R	BP5L UVLO rising threshold	C _{BP5L} = 1μF		3.95	4.16	4.3	V	
BP5L _F	BP5L UVLO falling threshold			3.81	3.96	4.21		
BP5L _H	BP5L UVLO hysteresis			0.2				
V _{VIN(TH)_UVLO R}	VIN UVLO rising threshold	EN = 5V	V _{IN(rising)} to V _{GL} = 1.5V	7.7	8	8.3	V	
V _{VIN(TH)_UVLO F}	VIN UVLO falling threshold		V _{IN(falling)} to V _{GL} = 1.5V	7.5	7.8	8.1		
V _{UVLOHYST_VI N}	VIN UVLO hysteresis			0.2				
t _{UVLO(delay)}	UVLO propagation delay	EN = 5V, V _{IN(rising)} = 6.9V to V _{GL} = 1.5V		0.2			1	ms
V _{EN_TH(rising)}	Enable rising threshold (turn-on)	V _{PWM} = 0V	V _{EN(rising)} to V _{GL} = 1.5V	0.564	0.596	0.644	V	
V _{EN_TH(falling)}	Enable falling threshold (turn-off)		V _{EN(falling)} to V _{GL} = 1.5V	0.464	0.496	0.536		
V _{EN(HYS)}	Enable threshold hysteresis			0.1				
t _{EN(delay)}	Enable propagation delay	EN high to V _{GL} = 1.5V, PWM = 0V		8			20	μs
I _{EN(LKG)}	Enable input leakage current	V _{EN} = 7V		1			20	nA

6.5 Electrical Characteristics (continued)

8.5V ≤ VIN ≤ 15V, R_{DLH} = R_{DHL} = 10kΩ, -55°C ≤ T_A ≤ 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE						
G _{IOUT}	Current sense gain		4.5	5	5.5	mV/A
I _{ABS(OS)}	Absolute current sense offset error		−4.2		4.2	A
V _{IOUT_DR}	I _{OUT} dynamic range voltage, V _{REFIN} − V _{IOUT}	−20A ≤ I _{D(LS)} ≤ 90A	−175		600	mV
BOOTSTRAP						
V _{SD(BOOT)}	Source-drain voltage, internal bootstrap FET	I _{BST} = 100mA	1	2.2	3.5	V
OVERTEMPERATURE PROTECTION						
T _{OTPR}	Over temperature rising threshold			175		°C
T _{OTPF}	Over temperature falling threshold			145		°C
OVERCURRENT PROTECTION						
I _{SRC_OC(enter)}	Sourcing overcurrent limit, enter			105		A
I _{OC(exit)}	Sourcing overcurrent limit, exit			95		
I _{SRC_OC(HYS)}	Sourcing overcurrent limit, hysteresis			15		
I _{SNK_OC(enter)}	Sinking overcurrent limit, enter			−20		
FAULT						
V _{IN,min_FLT}	Minimum VIN voltage for valid FLTB output	Measured when V _{FLT} ≤ 0.5V at 100μA		3		V
I _{FLT(LKG)}	Fault leakage current	V _{FLT} = 7V		50	425	nA
V _{FLT(OL)}	Fault logic-low output	I _{FLT} = 1mA			0.2	V
DEAD-TIME						
t _{DLH}	Dead time low-to-high ⁽¹⁾	V _{DLH} = BP5L = 5.5V	6	12	19	ns
		R _{DLH} = 10kΩ	2	7	13	
t _{DHL}	Dead time high-to-low ⁽¹⁾	V _{DHL} = BP5L = 5.5V	2	7	16	ns
		R _{DHL} = 10kΩ	2	7	13	
PWM						
I _{PWM(IH)}	PWM sinking current	V _{PWM} = 5V		500		μA
I _{PWM(IL)}	PWM sourcing current	V _{PWM} = 0V		−500		μA
V _{PWM(rising_TH)}	PWM rising threshold voltage		2	2.3	2.7	V
V _{PWM(falling_TH)}	PWM falling threshold voltage		0.7	1.1	1.3	
V _{MID}	PWM tri-state voltage			1.8		

6.5 Electrical Characteristics (continued)

8.5V ≤ VIN ≤ 15V, R_{DLH} = R_{DHL} = 10kΩ, -55°C ≤ T_A ≤ 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING						
t _{p(HL)(GL)}	Low-side gate (GL) logic-high to logic-low propagation delay ⁽¹⁾	V _{PWM} = 3V to V _{GL} = 1.5V		78	133	ns
t _{p(LH)(GL)}	Low-side gate (GL) logic-low to logic-high propagation delay ⁽¹⁾	V _{PWM} = 0.8V to V _{GL} = 1.5V		90	120	
t _{p(HL)(GH)}	High-side gate (GH), referenced to SW, logic-high to logic-low propagation delay ⁽¹⁾	V _{PWM} = 0.8V to V _{GH_SW} = 1.5V		81	116	
t _{p(LH)(GH)}	High-side gate (GH), referenced to SW, logic-low to logic-high propagation delay ⁽¹⁾	V _{PWM} = 3V to V _{GH_SW} = 1.5V		88	118	
t _{d(SW)(LH)}	Switch-node rising delay time ⁽¹⁾	V _{PWM} = 0.8V to V _{SW} = 1.2V		85		ns
t _{d(SW)(HL)}	Switch-node falling delay time ⁽¹⁾	V _{PWM} = 3V to V _{SW} = 10.8V		87		
t _{p(L3)}	Tri-state enter, logic-low to tri-state propagation delay ⁽¹⁾	V _{PWM} 0V to 1.7V, V _{GL} = 1.5V		96	140	ns
t _{p(3H)}	Tri-state exit, tri-state to logic-high propagation delay ⁽¹⁾	V _{PWM} 1.7V to 5V, V _{GH_SW} = 1.5V		126	190	
t _{p(H3)}	Tri-state enter, logic-high to tri-state propagation delay ⁽¹⁾	V _{PWM} 5V to 1.7V, V _{GH_SW} = 1.5V		123	145	
t _{p(3L)}	Tri-state exit, tri-state to logic-low propagation delay ⁽¹⁾	V _{PWM} 1.7V to 0V, V _{GL} = 1.5V		140	197	
t _{3HT(L3)}	Tri-state hold-off time, logic-low to tri-state enter ⁽¹⁾		10	24		ns
t _{3HT(H3)}	Tri-state hold-off time, logic-high to tri-state enter ⁽¹⁾		10	24		
t _{d(PWM-SW)(L3)}	Switch-node tri-state enter from logic-low to tri-state ⁽¹⁾	V _{PWM} = 1.7V to V _{SW} = -0.8V		105		ns
t _{d(PWM-SW)(3H)}	Switch-node tri-state exit from tri-state to logic-high ⁽¹⁾	V _{PWM} = 3V to V _{SW} = 1.2V		150		
t _{d(PWM-SW)(H3)}	Switch-node tri-state enter from logic-high to tri-state ⁽¹⁾	V _{PWM} = 1.7V to V _{SW} = 10.8V		80		
t _{d(PWM-SW)(3L)}	Switch-node tri-state exit from tri-state to logic-low ⁽¹⁾	V _{PWM} = 0.7V to V _{SW} = 0V		120		

(1) See measurement diagram in [Parameter Measurement Information](#)

6.6 Typical Characteristics

VIN = 12V, PVIN = 12V, TA = 25°C, RDLH = RDHL = 10kΩ, CREF = 470nF

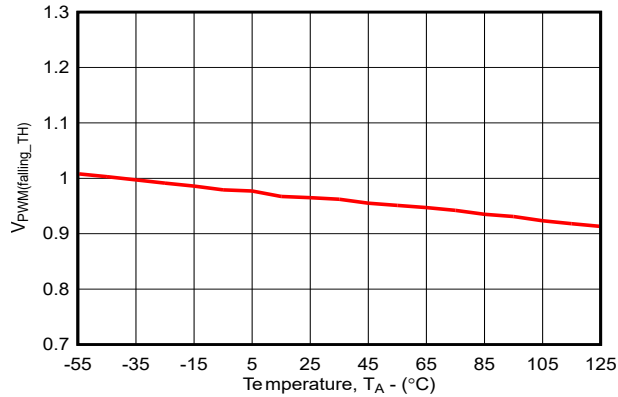


Figure 6-1. PWM Falling Threshold Voltage, V_{PWM(falling_TH)} Vs Temperature

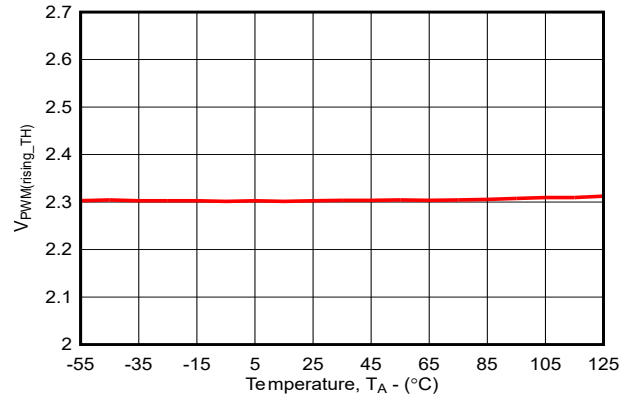


Figure 6-2. PWM Rising Threshold Voltage, V_{PWM(rising_TH)} Vs Temperature

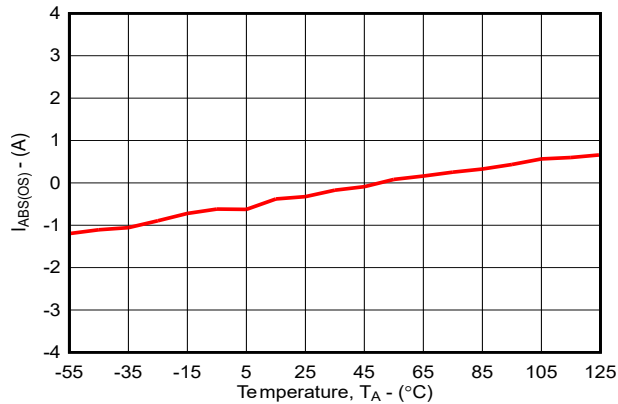


Figure 6-3. Absolute Current Sense Offset, I_{ABS(OS)} Vs Temperature

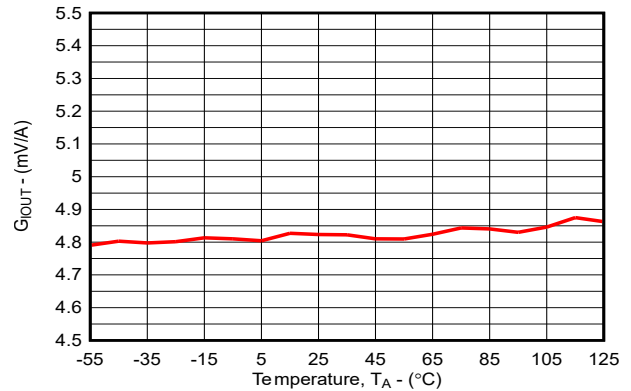


Figure 6-4. Current Sense Gain, G_{IONT} Vs Temperature

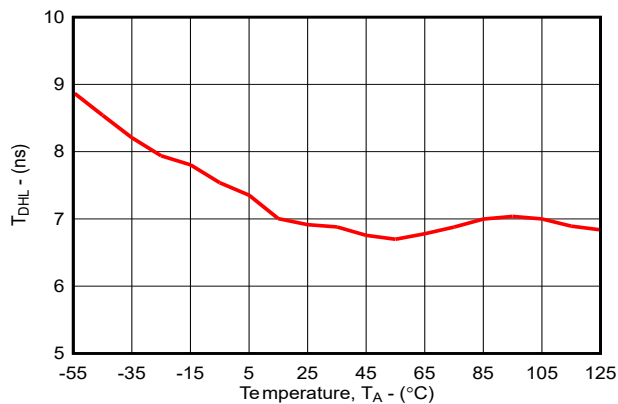


Figure 6-5. Dead-time High-Low, t_{DHL} Vs Temperature

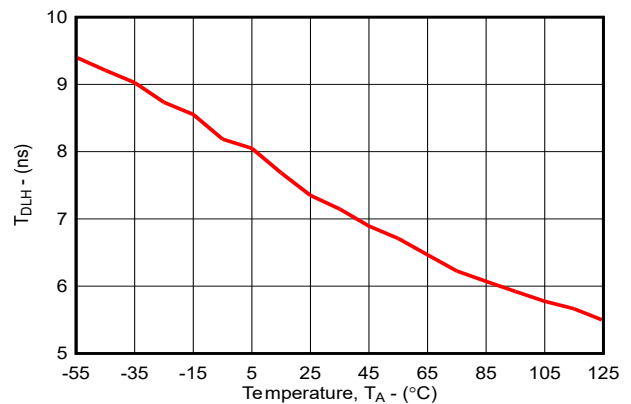


Figure 6-6. Dead-time Low-High, t_{DLH} Vs Temperature

6.6 Typical Characteristics (continued)

VIN = 12V, PVIN = 12V, TA = 25°C, RDLH = RDHL = 10kΩ, CREF = 470nF

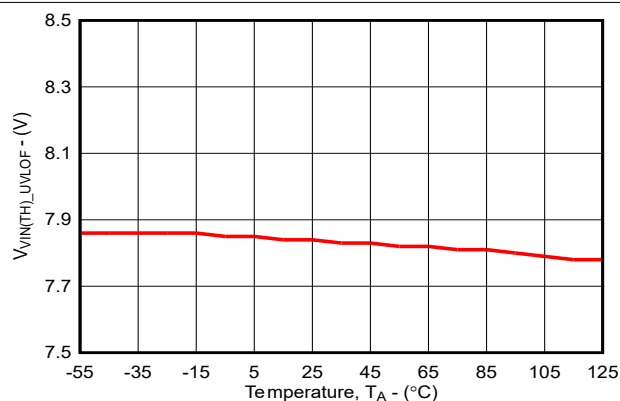


Figure 6-7. VIN ULVO Falling Threshold, VVIN(TH)_UVLOF Vs Temperature

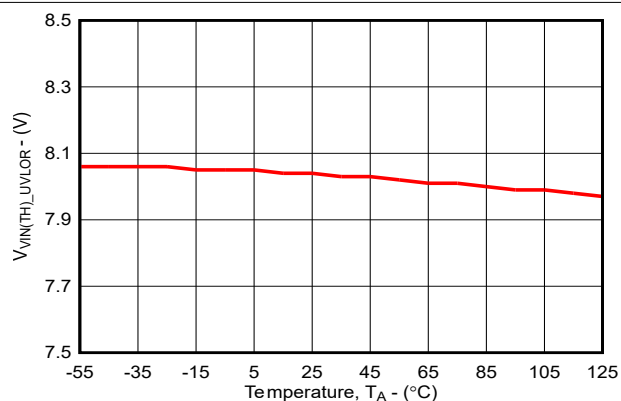


Figure 6-8. VIN ULVO Rising Threshold, VVIN(TH)_UVLOR Vs Temperature

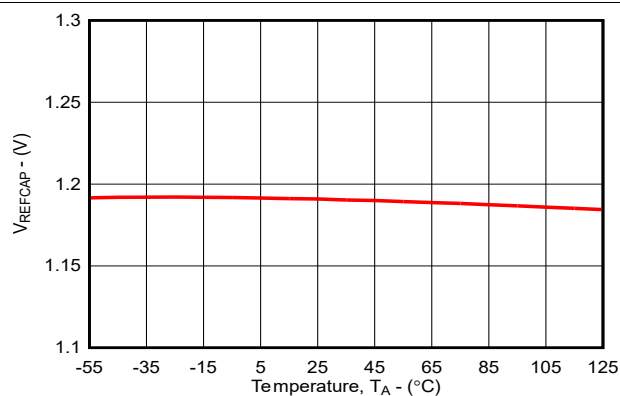


Figure 6-9. REFCAP Voltage, VREFCAP Vs Temperature

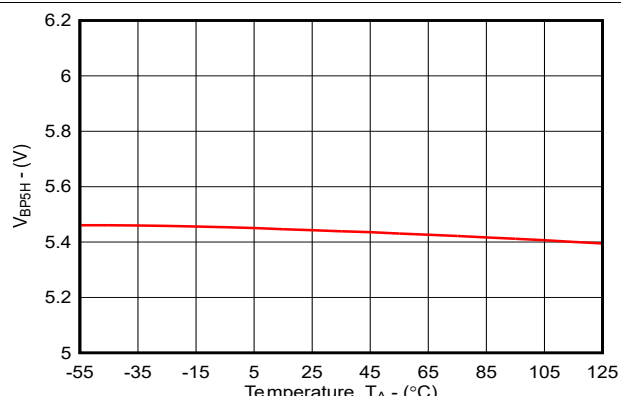


Figure 6-10. High-Side Regulator Voltage, VBP5H Vs Temperature

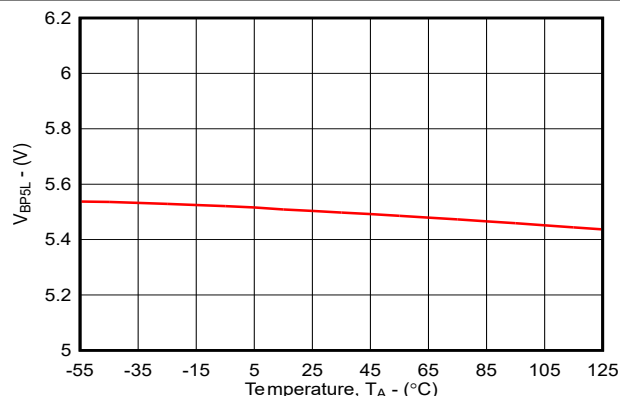
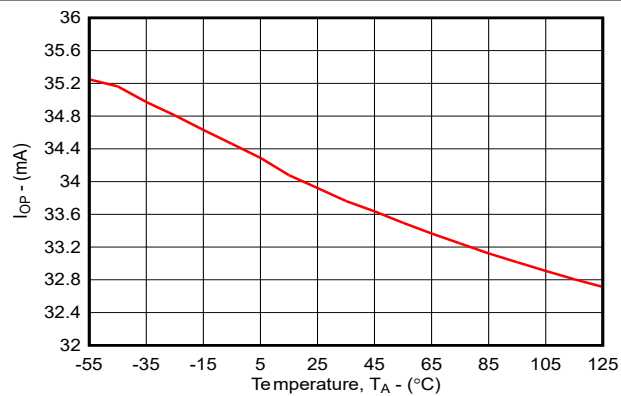


Figure 6-11. Low-Side Regulator Voltage, VBP5L Vs Temperature



fsw = 500kHz VPVIN = 0V

Figure 6-12. Operating Current, IOP Vs Temperature

6.6 Typical Characteristics (continued)

VIN = 12V, PVIN = 12V, TA = 25°C, RDLH = RDHL = 10kΩ, CREF = 470nF

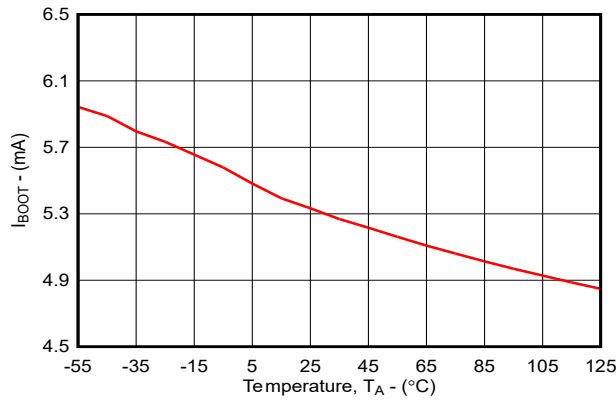


Figure 6-13. BOOT Current, IBOOT Vs Temperature

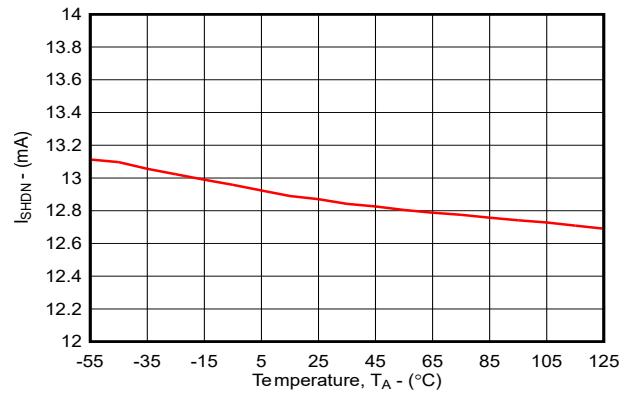


Figure 6-14. Shutdown Current, ISHDN Vs Temperature

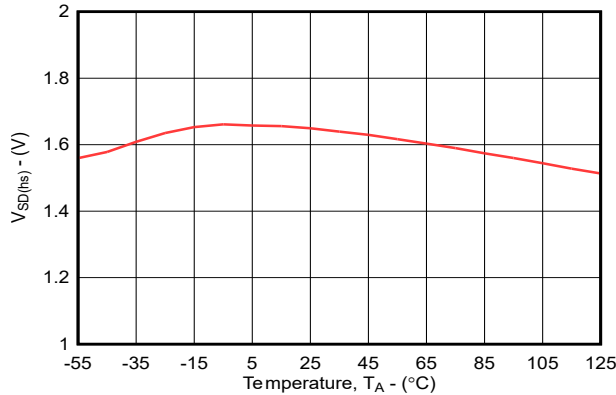


Figure 6-15. High-Side Source-Drain Voltage, VSD Vs Temperature

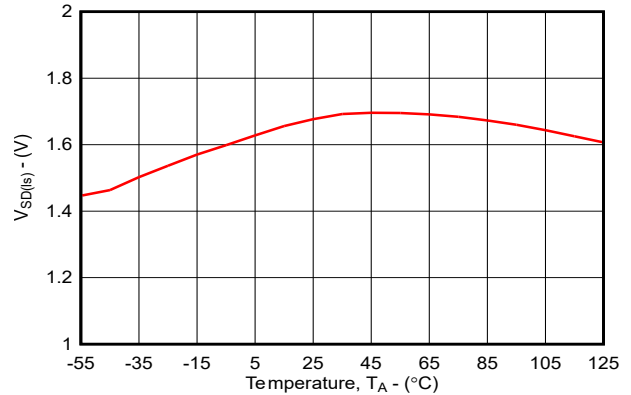


Figure 6-16. Low-Side Source-Drain Voltage, VSD vs Temperature

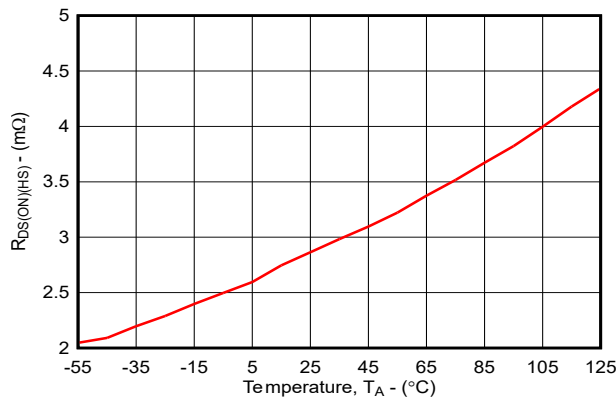


Figure 6-17. High-Side Drain-Source Resistance, RDS(on)(hs) vs Temperature

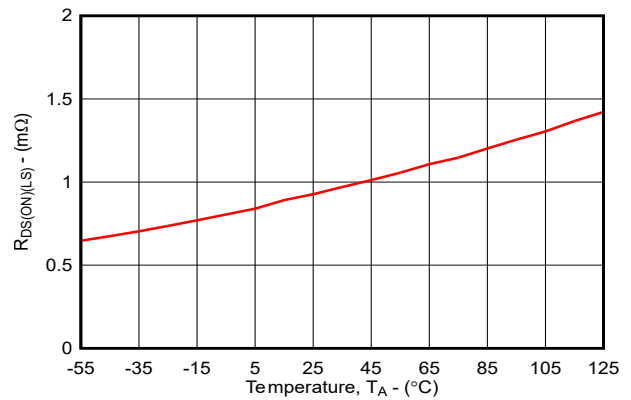


Figure 6-18. Low-Side Drain-Source Resistance, RDS(on)(ls) vs Temperature

6.6 Typical Characteristics (continued)

VIN = 12V, PVIN = 12V, TA = 25°C, RDLH = RDHL = 10kΩ, CREF = 470nF

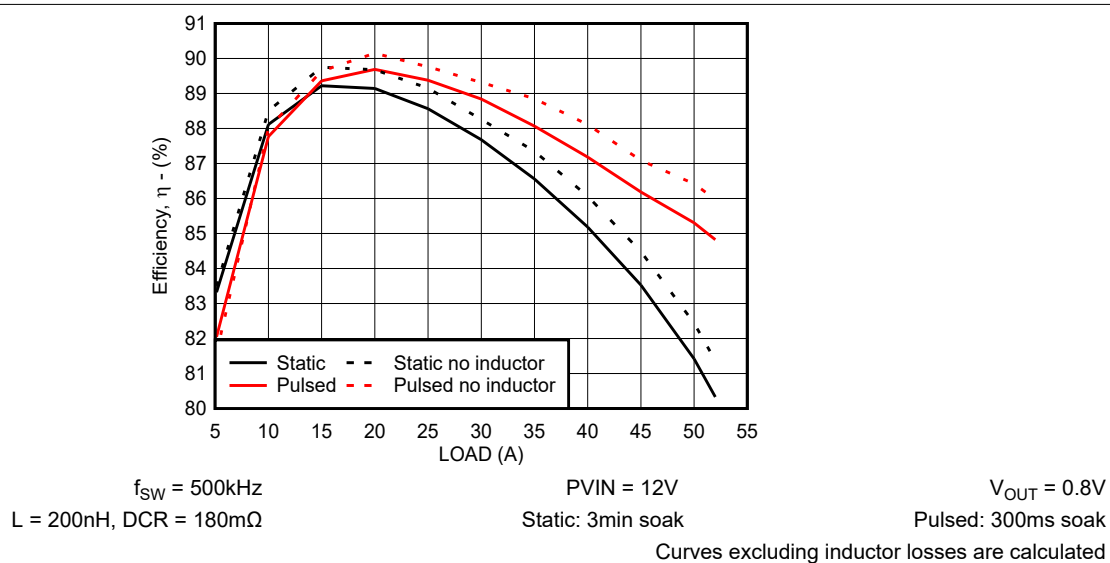


Figure 6-19. Efficiency vs Output Current

7 Parameter Measurement Information

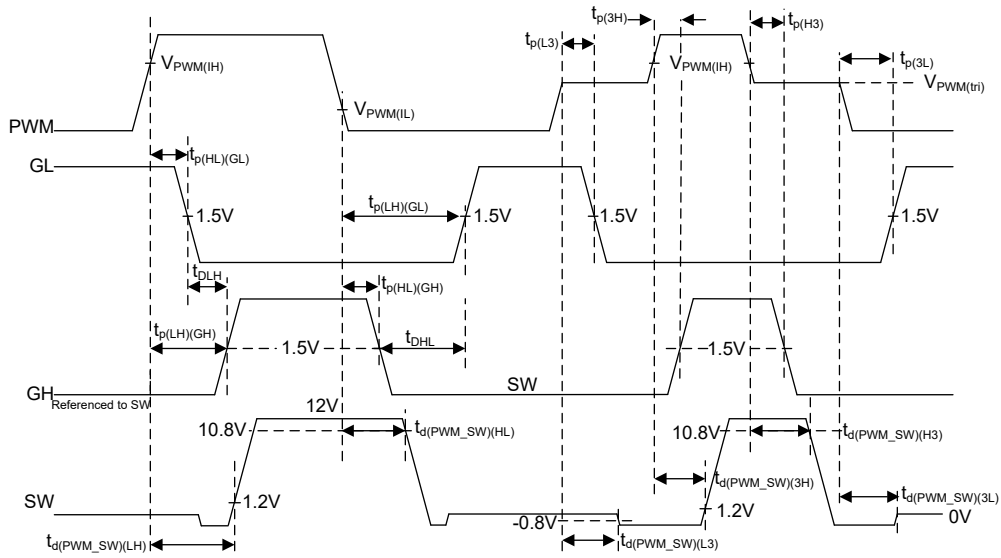


Figure 7-1. Timing Measurement

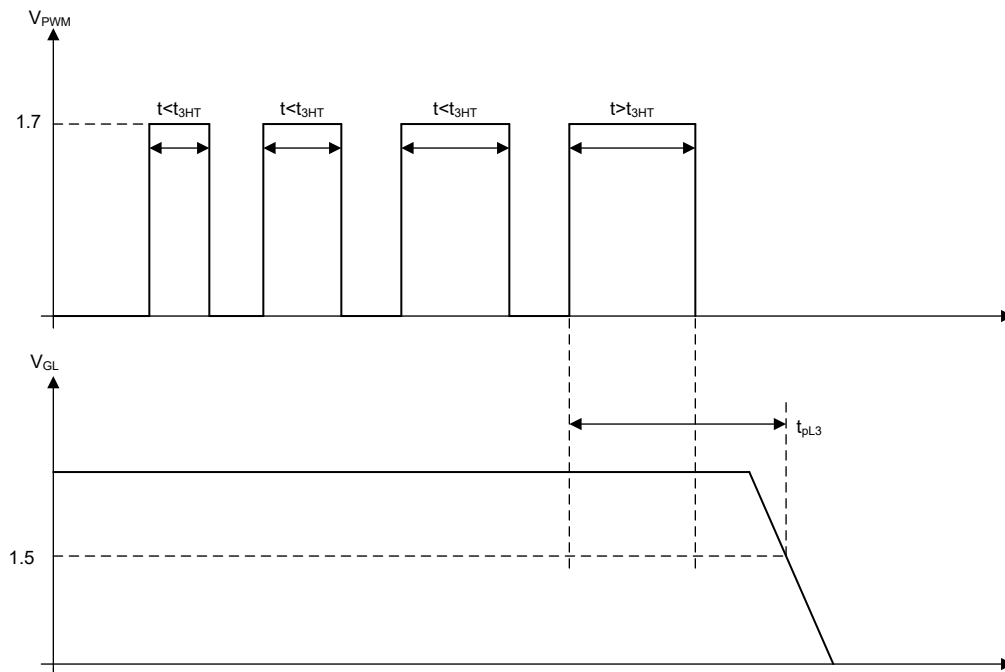


Figure 7-2. Hold Off Time Measurement - Low to Tri-state

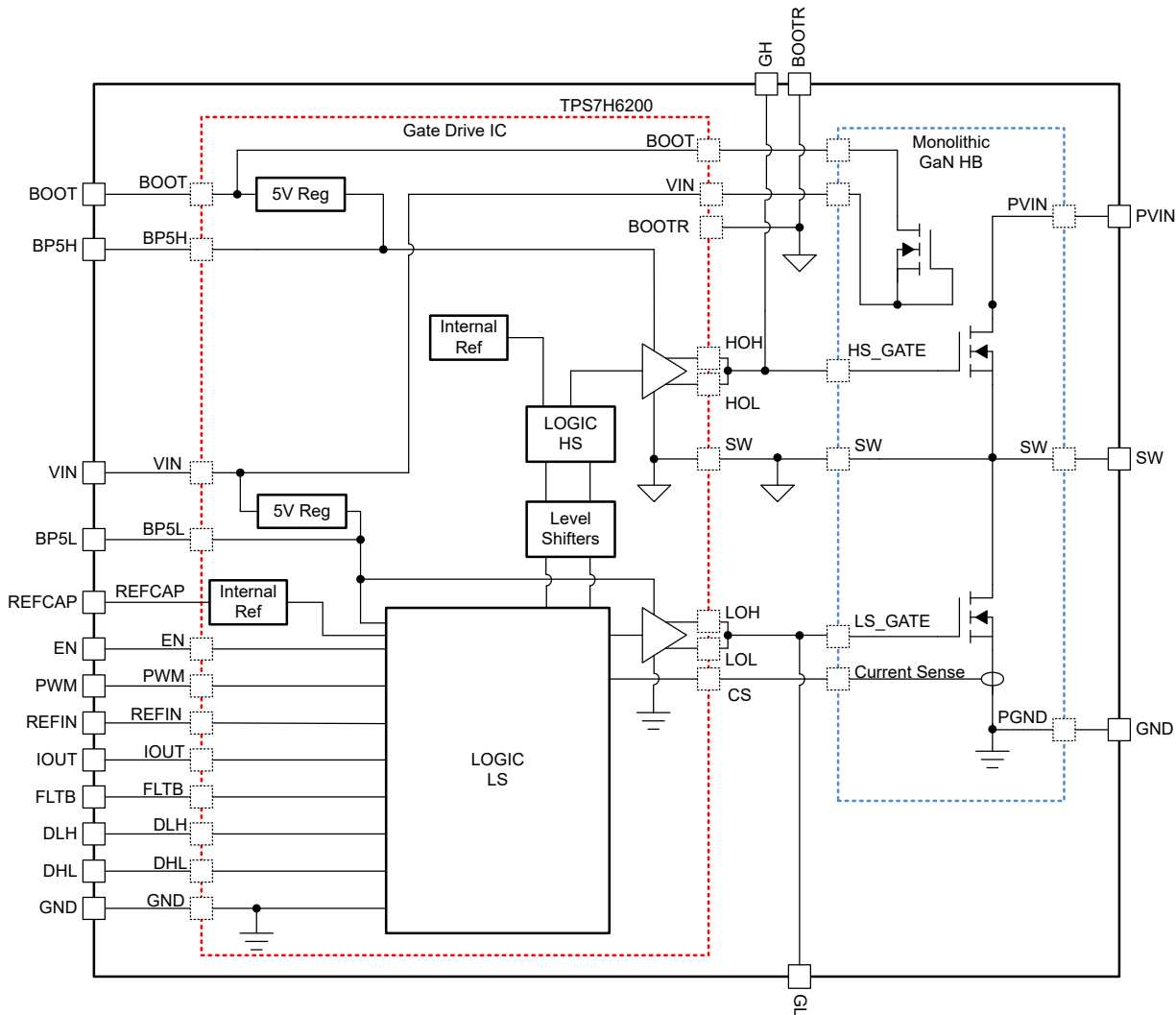
8 Detailed Description

8.1 Overview

The TPS7H6200-SEP is a highly integrated 15V GaN power stage that combines two dies—a silicon gate-driver and a half-bridge GaN die. Optimized for synchronous-buck converters, the TPS7H6200-SEP is designed for applications that step 12V down to sub-1V point-of-load supplies. The wide PVIN voltage range and low GaN FET $R_{DS(on)}$ facilitates additional conversion ratios.

Packaged in a compact 6mm × 6mm package with wettable flanks, the device supports tri-state PWM inputs, overcurrent and overtemperature monitoring, programmable dead-time, and fault indication. By integrating both the high-side and low-side GaN FETs on one die, the TPS7H6200-SEP achieves minimal parasitic inductance and improved efficiency.

8.2 Functional Block Diagram



ADVANCE INFORMATION

8.3 Feature Description

8.3.1 VIN PVIN

The VIN pin powers the internal control circuitry, while the PVIN pins and PVIN pad provide the input voltage to the internal high-side FET. Both VIN and PVIN have an input voltage range from 4.5V to 15V and are not internally connected.

Connect a minimum of one 100nF ceramic bypass capacitor to VIN. If supplemental bypass capacitance (for example, 10nF or 1nF) is required, place these capacitors as close to the VIN pin as possible.

The PVIN input capacitor network consists of an ascending array of bypass and bulk capacitors, using ceramic, tantalum, or polymer technologies.

8.3.2 Bootstrap Operation

To generate the power for the high-side gate driver circuitry the TPS7H6200-SEP incorporates an internal gate-to-source tied GaN FET to use the 3rd quadrant operation of the GaN FET as a bootstrap diode. TI recommends a ceramic 16V (minimum voltage rating) 100nF capacitor for C_{BOOT}.

8.3.3 Voltage Reference

The device generates an internal nominal 1.2V bandgap reference voltage which is present on the REFCAP pin during steady state operation. A 470nF capacitor to ground is required at the REFCAP pin for SET performance of the device.

8.3.4 Enable

When the enable pin, EN, is driven above V_{EN_TH(rising)}, 0.596V (typ), the TPS7H6200-SEP exits shutdown mode and commences switching upon exiting UVLO.

When the EN pin is driven below V_{EN_TH(falling)}, the device enters shutdown mode, ceasing operation.

Connecting VIN to EN requires an external resistor divider, as the maximum EN input voltage (7.5V) is lower than the recommended VIN (8.5V). The resistors can be appropriately sized to turn-on the device when a desired preset input voltage is reached (see [Equation 1](#)). The Enable voltage divider facilitates the creation of an adjustable UVLO to complement the default internal UVLO voltage on the VIN pin.

$$R_{EN_TOP} = R_{EN_BOT} \times \left(\frac{V_{EN(rising)}}{V_{VIN(rising)} - V_{EN(rising)}} \right) \quad (1)$$

where

- V_{IN(rising)} = the target VIN value that causes EN to go high, must be greater than 0.6V
- V_{EN(rising)} = 0.596V (typ)
- R_{EN_TOP} = feedback resistor from VIN to EN
- R_{EN_BOT} = feedback resistor from EN to GND

The EN pin has 100mV (typ) of hysteresis. Therefore, use [Equation 2](#) can to calculate the V_{IN(falling)} voltage.

$$V_{VIN(falling)} = V_{EN(falling)} \times \left(\frac{R_{EN_TOP} + R_{EN_BOT}}{R_{EN_BOT}} \right) \quad (2)$$

where

- V_{IN(falling)} = the target VIN value that causes EN to go low and turn-off the TPS7H6200-SEP
- V_{EN(falling)} = 0.496V (typ)

Alternatively, the EN pin can be driven directly from a microcontroller or FPGA. The low voltage threshold of the enable pin aids in support of 1.1, 1.8, 2.5, and 3.3V logic levels.

8.3.5 Start-Up and UVLO

The TPS7H6200-SEP has UVLO circuitry for VIN and regulators BP5H, BP5L which alters the state of gate drive outputs to provide robust protection of the GaN FETs and the external load.

Table 8-1. UVLO, ENABLE and FLTB Logic Operation

Condition					Output			
VIN	EN	PWM	BP5L ⁽¹⁾	BP5H ⁽¹⁾	FLT B ⁽²⁾	GH	GL	SW
VIN < V _{VIN(TH)_UVLO} (VIN UVLO)	x	x	x	x	OL	OL	OL	Tri-state
VIN > V _{VIN(TH)_UVLO}	V _{EN} < V _{EN_TH} (DISABLED)	x	NOM	NOM	OH	OL	OL	Tri-state
	V _{EN} > V _{EN_TH} (ENABLED)	x	UVLO	x	OL	OL	OL	Tri-state
		IL	NOM	UVLO	OL	OL	OH	Active LS
		TRI	NOM	UVLO	OL	OL	OL	Tri-state
		IH	NOM	ULVO	OL	OL	OH	Active LS ⁽³⁾
		IL	NOM	NOM	OH	OL	OH	Active LS
		TRI	NOM	NOM	OH	OL	OL	Tri-state
		IH	NOM	NOM	OH	OH	OL	Active HS

(1) Regulator is in UVLO when V_{BP5X} is less than minimum voltage stated in Electrical Characteristics table

(2) FLTB OL is driven low by internal pulldown FET when a fault is detected; otherwise FLTB is pulled up

(3) When BP5H is in UVLO, the low side FET remains on and the HS gate signal is interlocked and prevented from turning on while PWM has IH voltage present

8.3.6 Programmable Dead-Time

The DHL pin defines the dead-time interval from the time the high-side gate voltage reaches 1.5V (falling) to when the low-side gate voltage reaches 1.5V (rising); see [Figure 7-1](#). Tying a 10kΩ resistor from DHL to ground produces a typical dead-time of 7ns for this high-to-low transition.

The DLH pin sets the programmable dead-time between low-side gate voltage reaches 1.5V (falling) to when the high-side gate voltage reaches 1.5V (rising); see [Figure 7-1](#). Tying a 10kΩ resistor from DLH to ground produces a typical dead-time of 7ns for this low-to-high transition.

For designs that aim to reduce external component count, do not populate the dead-time resistors and connect DHL and DLH directly to a 5.5V supply (or to the low-side regulator BP5L) sets nominal dead-time values of 7ns for DHL and 12ns for DLH.

8.3.7 Current Sense

The TPS7H6200-SEP incorporates a lossless low-side current sense FET that outputs a differential voltage signal with the IOUT and REFIN pins.

Current Sense Gain

The current sense gain for the TPS7H6200-SEP is 5mV/A (typ), with a tolerance of ±0.5mV/A; using Equation 3 yields an error (ε_{Gain}) of ±10%.

$$\varepsilon_{Gain} = \frac{tol_G_{IOUT}\left(\frac{mV}{A}\right)}{G_{IOUT}\left(\frac{mV}{A}\right)} \times 100 \quad (3)$$

Offset

The offset accuracy is the no-load (0A) differential voltage output of the IOUT – REFIN pins, expressed as an absolute offset current $I_{ABS(OS)}$ is ±4.2A. Using Equation 4, the offset error contribution at an output current of 40A is ±10.5%.

$$\varepsilon_{Offset} = \frac{I_{ABS(OS)}(A)}{I_{IOUT}(A)} \times 100 \quad (4)$$

8.3.8 Over Temperature Protection (TSD)

The driver IC integrates temperature sensing circuitry to shutdown the device when the sensed temperature exceeds 175°C (typ). The thermal shutdown condition exits when the sensed temperature falls below 145°C (typ, resumption of normal operation).

8.3.9 Fault Reporting (FLT B)

The FLT B pin is an open-drain output that asserts when either the overtemperature event, overcurrent event or detection of UVLO conditions. Use a pull-up resistor on the FLT B pin to BP5L or to another voltage level within the device recommended operating conditions. Select the resistor size to keep the maximum current sunk by FLT B to under the recommended operating condition current maximum (less than 100µA when connected to BP5L); generally a pullup resistor of 10kΩ is sufficient. When connecting FLT B to an alternate pull-up voltage, size the resistor for a current maximum of 2mA. Using a larger value resistor reduces power dissipation but increases susceptibility to switching-noise coupling on the FLT B signal due to the weaker pull-up.

FLT B assertion ends when an overcurrent, overtemperature, or UVLO condition is no longer detected.

8.3.10 PWM

The PWM pin serves as the control input for the TPS7H6200-SEP. A voltage above 3V defines a logic high, while a voltage below 0.7V defines a logic low. Both $V_{PWM(rising_TH)}$ and $V_{PWM(falling_TH)}$ thresholds are compatible with 3.3V and 5V logic controllers.

The PWM input features a tri-state function: if the PWM pin floats for longer than the tri-state hold-off time (t_{3HT}), both the high-side and low-side FET gates are forced low. Enter tri-state mode can by actively driving the PWM input to V_{3T} or by placing the input in a high impedance state, allowing internal current sources to pull the pin to V_{3T} . The PWM pin can source up to I_{PWMH} and sink up to I_{PWML} to drive the signal to V_{3T} ; notably, these currents are not consumed while the pin is held at V_{3T} . Figure 7-1 shows the transitions into and out of tri-state mode. For reliable normal operation, drive the PWM signal with a maximum sink impedance of 500Ω and a maximum source impedance of 500Ω.

8.4 Device Functional Modes

The table below shows the device functional modes:

Table 8-2. Device Functional Modes

EN PIN	Device Status
High	Operation mode
Low	Shutdown mode

9 Application and Implementation

9.1 Application Information

9.2 Typical Application

The TPS7H6200-SEP is an integrated power stage with silicon gate driver and a monolithic GaN half bridge; the high level of integration reduces parasitic inductance and makes the power stage an excellent choice for high current point of load applications.

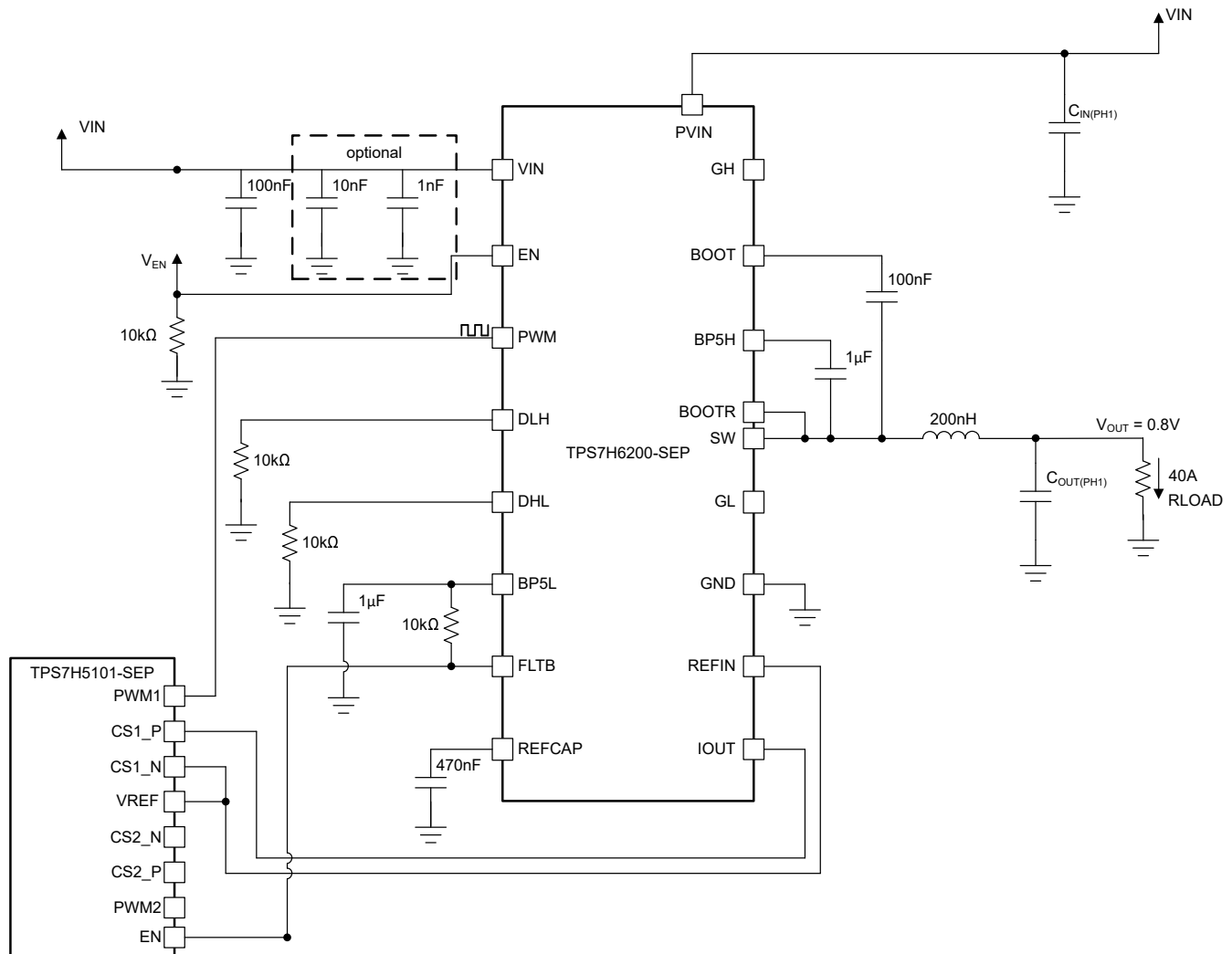


Figure 9-1. Typical Application

9.2.1 Design Requirements

The design parameters below are derived from using the TPS7H6200-SEP and TPS7H5101-SEP as a power stage and D-CAP+ controller chipset.

Table 9-1. Design Parameters

SYSTEM CONFIGURATION	VALUE
Input voltage	12V $\pm$ 5%
Output voltage	0.8V $\pm$ 5%
Maximum output current	40A
Switching frequency	500kHz
Inductor	200nH
Output bulk capacitance	1x 330 μ F, 6x 47 μ F
Output decoupling capacitance	10x 100nF
Start input voltage rising	10V

9.2.2 Detailed Design Procedure

9.2.2.1 Enable Configuration

The BOM shown in [Table 9-2](#) has the Enable pin connected directly to test-point in which a voltage can be directly applied, which includes a 10k Ω pull-down resistor.

The following example shows how to drive Enable from VIN by applying a resistor divider; note, this configuration is not present in the depicted EVM.

Using [Equation 1](#), select an enable turn-on voltage that exceeds the input voltage UVLO; for this example a selecting a $V_{IN(rising)}$ of 8.3V, the typical $V_{EN(rising)} = 0.6V$, and an $R_{EN(BOT)} = 100k\Omega$. $R_{EN_TOP} = 7.79k\Omega$, using standard resistor values select a 7.87k Ω resistor.

When Enable is driven using a microcontroller, V_{IN} UVLO (8.3V (max)) must be exceeded.

9.2.2.2 Dead Time Setting

The TPS7H6200-SEP can set dead times using two methods, the first utilizing a 10k Ω resistor connected dead-time pins DHL and DLH to ground and the second method alleviates the need for dead-time resistors by connecting dead-time pins DHL and DLH to BP5L. Using a dead-time setting resistor offers higher dead-time precision versus connecting to DHL and DLH to BP5L; using a 10k Ω resistor, the TPS7H6200-SEP provides the same nominal dead-time (7ns t_{DHL} , 7ns t_{DLH}) as when connected to BP5L, however the maximum dead times for the resistor set configuration are lower.

9.2.2.3 FLTB / Controller Connection

[Figure 9-1](#) depicts FLTB of the TPS7H6200-SEP connected to EN of the TPS7H5100.

[Table 8-1](#) details the conditions in which FLTB becomes active and pulls the applied pull-up voltage low. To facilitate appropriate start-up conditions for the TPS7H6200-SEP, TI recommends to connect FLTB to the Enable pin of the TPS7H5100.

9.2.2.4 Configuring Current Sense

When integrating the internal current sense with the TPS7H5101-SEP connect VREF and CSX_N (CS1_N or CS2_N) of the TPS7H5100 to the REFIN pin of the TPS7H6200-SEP, connect the TPS7H5101-SEP CSX_P pin (CS1_P or CS2_P) to IOUT.

During low-side conduction the current sense pin, IOUT, differential outputs with REFIN the currents sense signal. During high-side conduction, the current sense circuit sample-and-holds the output current information, and is reset upon re-entering low-side conduction.

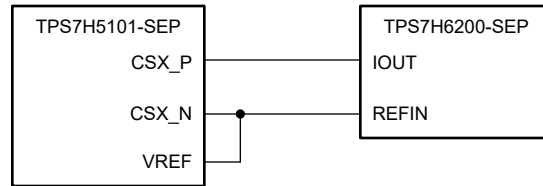


Figure 9-2. Simplified Current Sense Interface Diagram With TPS7H5101-SEP

9.2.2.4.1 Current Sense Accuracy

When combining multiple independent error sources, you can either add them directly (linear/arithmetic sum) or combine them using the root sum square (RSS) method, and the two give very different results. In practice, engineers use linear (worst-case) summation when a specified upper bound on total error is needed in safety-critical or high-reliability applications. While the RSS method is used when a statistically realistic estimate of combined error is more useful, such as when characterizing overall system accuracy under typical operating conditions.

Arithmetic Sum Error

Direct addition simply sums the magnitudes of each error term, which implicitly assumes that all errors are correlated and all occur simultaneously and in the same direction (worst case scenario, see Equation 5). Error sources (like offset, and gain) are typically uncorrelated and random, so the occurrence that all error terms occur at the same time and in the same direction is statistically unlikely.

$$\varepsilon_{total} = \varepsilon_{Gain} + \varepsilon_{Offset} \quad (5)$$

Applying Equation 5 results in a combined error of 20.5%:

$$\varepsilon_{total} = 10\% + 10.5\% = 20.5\% \quad (6)$$

RSS Error

The RSS method, by contrast, calculates the square root of the sum of the squares of each individual error term (see Equation 7), which is the statistically correct way to combine independent, uncorrelated random errors because variances (not standard deviations) add linearly. RSS of the total expected error under normal operating conditions, and the result is always smaller than or equal to the simple linear sum.

$$\varepsilon_{RSS} = \sqrt{\varepsilon_{Gain}^2 + \varepsilon_{Offset}^2} \quad (7)$$

Applying Equation 7 results in a combined error of 14.5%

$$\varepsilon_{RSS} = \sqrt{10\%^2 + 10.5\%^2} = 14.5\% \quad (8)$$

9.2.2.5 FET Thermal Impedance

The TPS7H6200-SEP incorporated GaN FETs are on a monolithic substrate and sized for wide V_{IN} to V_{OUT} point of load synchronous buck applications; therefore, the sizing of the FETs are not symmetrical. The low-side FET is three times larger than the high-side FET, this results in the high side FET having a thermal impedance that is three times larger than the low side.

Figure 9-3 and Figure 9-4 show the modeled thermal impedance of the low-side and high side FETs. This modeling represents the combined thermal impedance at thermal pads 45 and 46 for the low-side FET and pad 47 for the high side FET.

Also included are equivalent Foster network RC values that facilitate thermal simulations of the mission of the mission profile. In conjunction with electrical simulations the Foster network values establish a thermal domain. Include in the thermal domain the lumped thermal resistance and capacitance models associated PCB and

heat sink thermal characteristics. Figure 9-5 gives a simplified example of how to implement Foster network parameters with external thermal resistances, including PCB and other application considerations.

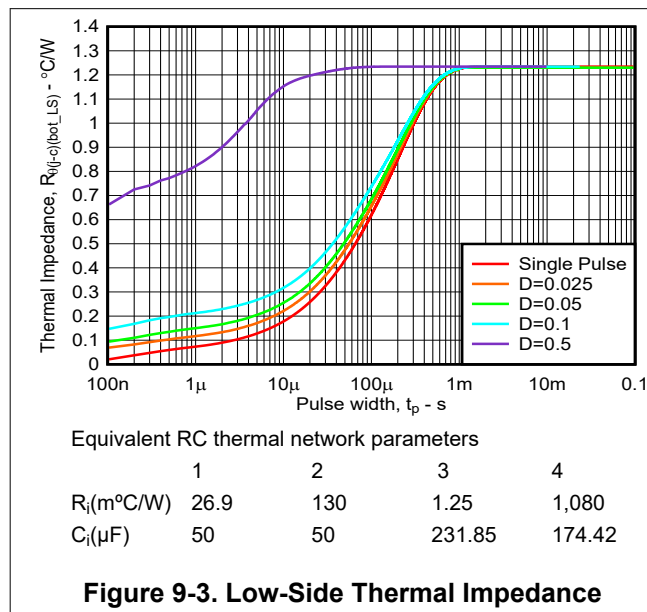


Figure 9-3. Low-Side Thermal Impedance

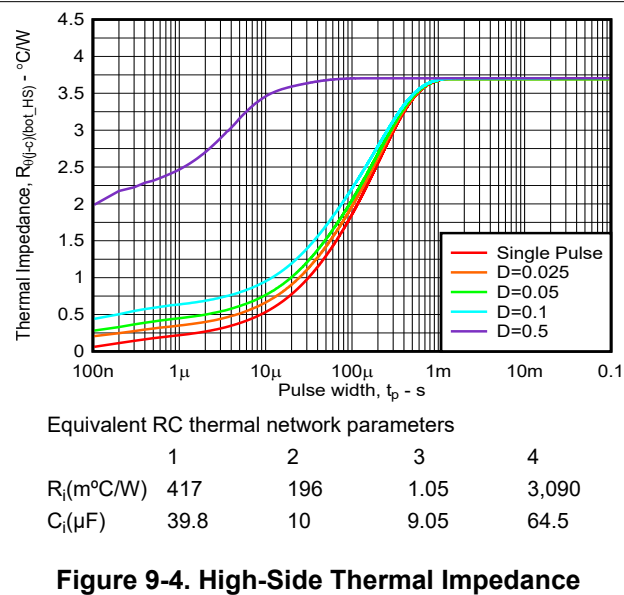


Figure 9-4. High-Side Thermal Impedance

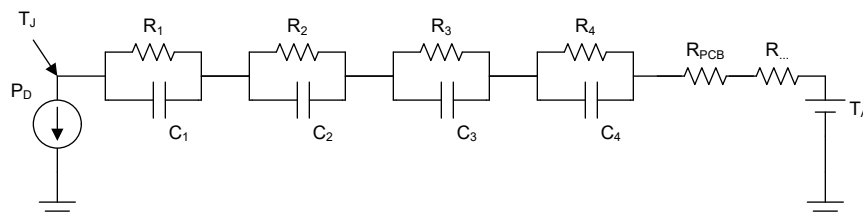


Figure 9-5. Foster Thermal RC Network

9.2.3 Application Curves

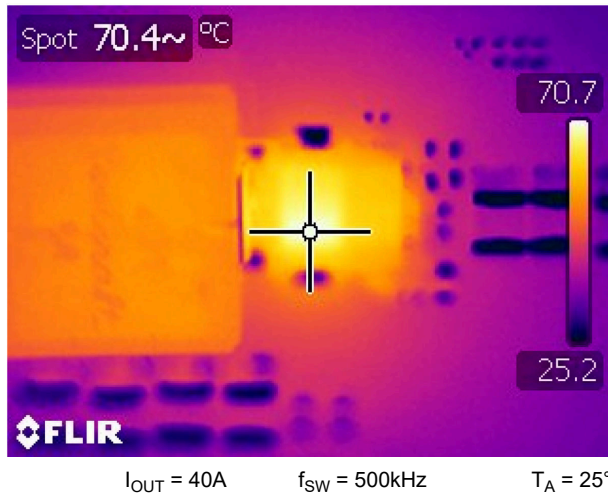


Figure 9-6. Thermal Image - High-Side

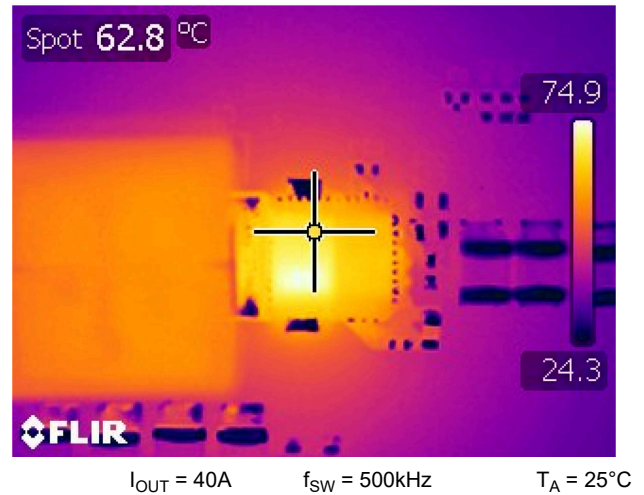


Figure 9-7. Thermal Image - Low-Side

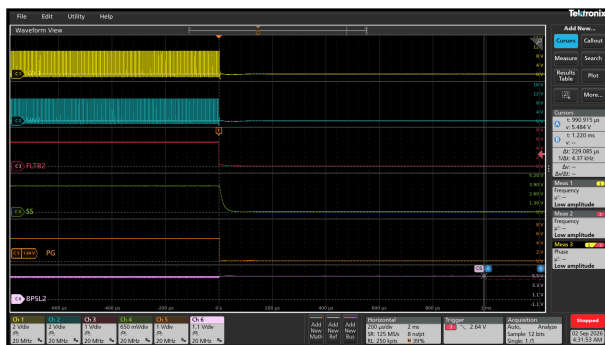


Figure 9-8. Thermal Shutdown Enter



Figure 9-9. Thermal Shutdown Enter (Zoomed)

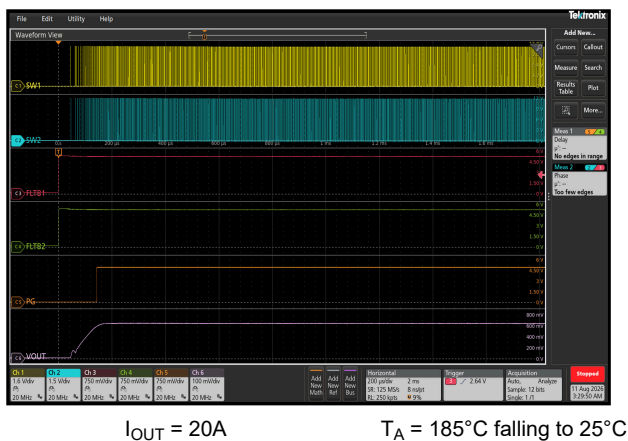


Figure 9-10. Thermal Shutdown Exit

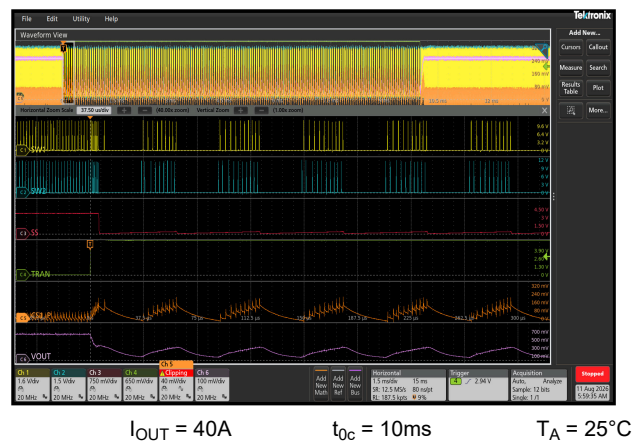


Figure 9-11. Overcurrent Response

9.3 Power Supply Recommendations

The TPS7H6200-SEP V_{IN} and V_{PVIN} pins support an input voltage range of 4.5V to 15V. Place adequate ceramic bypass capacitance networks as close as possible to each respective input pin, followed by bulk capacitance. The low-side regulator (BP5L) requires a 1 μ F ceramic capacitor connected across BP5L and GND. For bootstrap voltage generation (through the integrated gate-source tied GaN FET), connect a 0.1 μ F ceramic capacitor across BOOT and BOOTR (internally connected to SW). Finally, the high-side regulator requires a 1 μ F ceramic capacitor connected across BP5H and SW.

9.4 Layout

9.4.1 Layout Guidelines

- Use 2oz copper for high current carrying layers and use regions with a density of vias
- Position ceramic capacitors for internal regulators (BP5L, BP5H) and BOOT as close to the unit as possible
- Place ceramic input bypass capacitors as close as possible to PVIN
- Place ceramic bulk output capacitors closest to the TPS7H6200-SEP, followed by higher capacitance tantalum/polymer bulk output capacitors

Table 9-2. TPS7H6200-SEP Depicted Components

Alias	Description	Recommended Attributes
C11, C12	Input Capacitor	100 μ F, 25V, Tant/Polymer, 7343
C1, C2, C3, C4, C5, C6, C7, C8	Input Capacitor	22 μ F, 25V, Ceramic, 1210, 10%
C9, C10	Input Capacitor	22nF, 50V, Ceramic, 0603
C13	Input Capacitor	0.1 μ F, 50V, Ceramic, 0402
C14	Boot Capacitor	0.1 μ F, 50V, Ceramic, 0402
C15	High-side Regulator Capacitor	1 μ F, 50V, Ceramic, 0603
C17	Output Capacitor	220 μ F, 6.3V, Tantalum,
C18, C19, C20, C21, C22	Output Capacitor	47 μ F, 6.3v, Ceramic, 1210
C23	REFIN Capacitor	470pF, 100V, Ceramic, 0402
C24	Low-side Regulator Capacitor	1 μ F, 50V, Ceramic, 0603
C25	REFCAP	470nF, 16V, Ceramic, 0603
R2	R_{EN} pull-up	10k Ω , 0.1W, 0603
R3	R_{FLTB} pull-up	10k Ω , 0.1W, 0603
R4	R_{DHL}	10k Ω , 0.1W, 0603
R5	R_{DLH}	10k Ω , 0.1W, 0603
L1	Output Inductor	200nH, 55A, Surface Mount

9.4.2 Layout Example

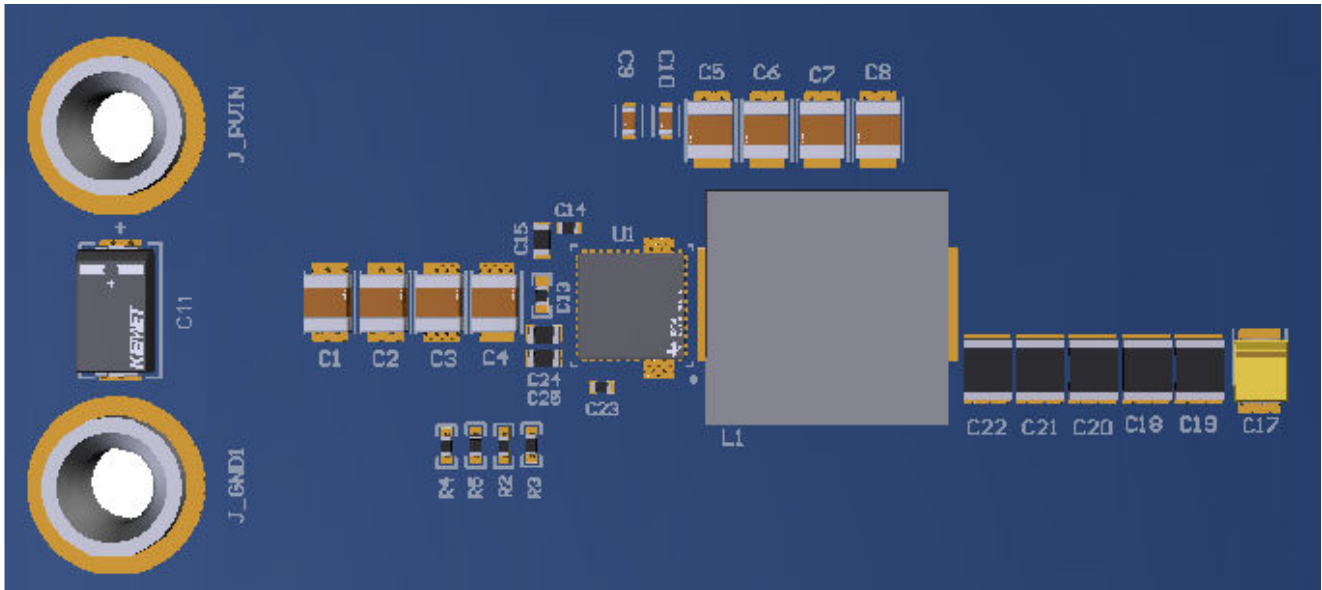


Figure 9-12. TPS7H6200-SEP Layout Example

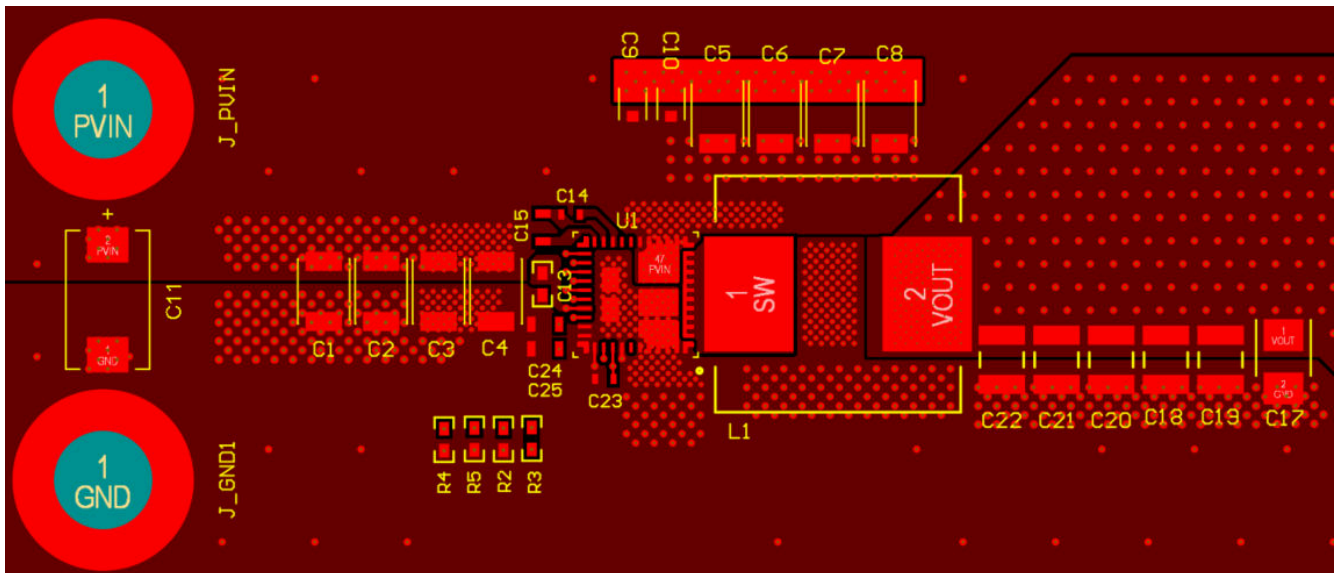


Figure 9-13. Top Layer Layout Example

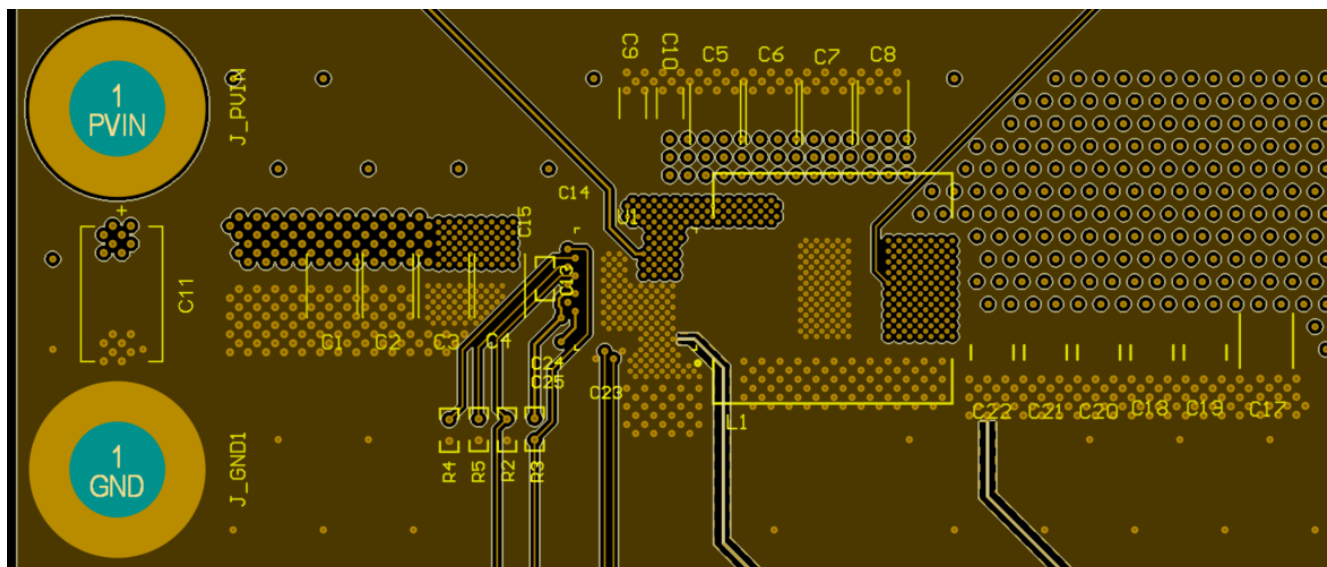


Figure 9-14. Signal Layer Layout Example

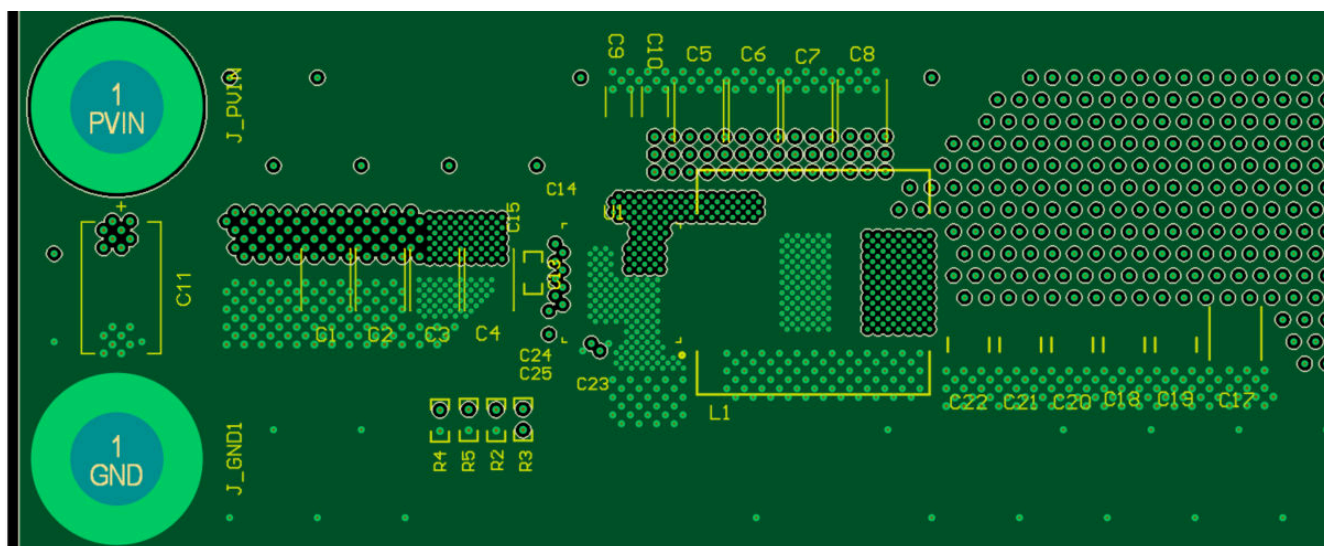


Figure 9-15. Ground Layer Layout Example

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.3 Trademarks

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All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

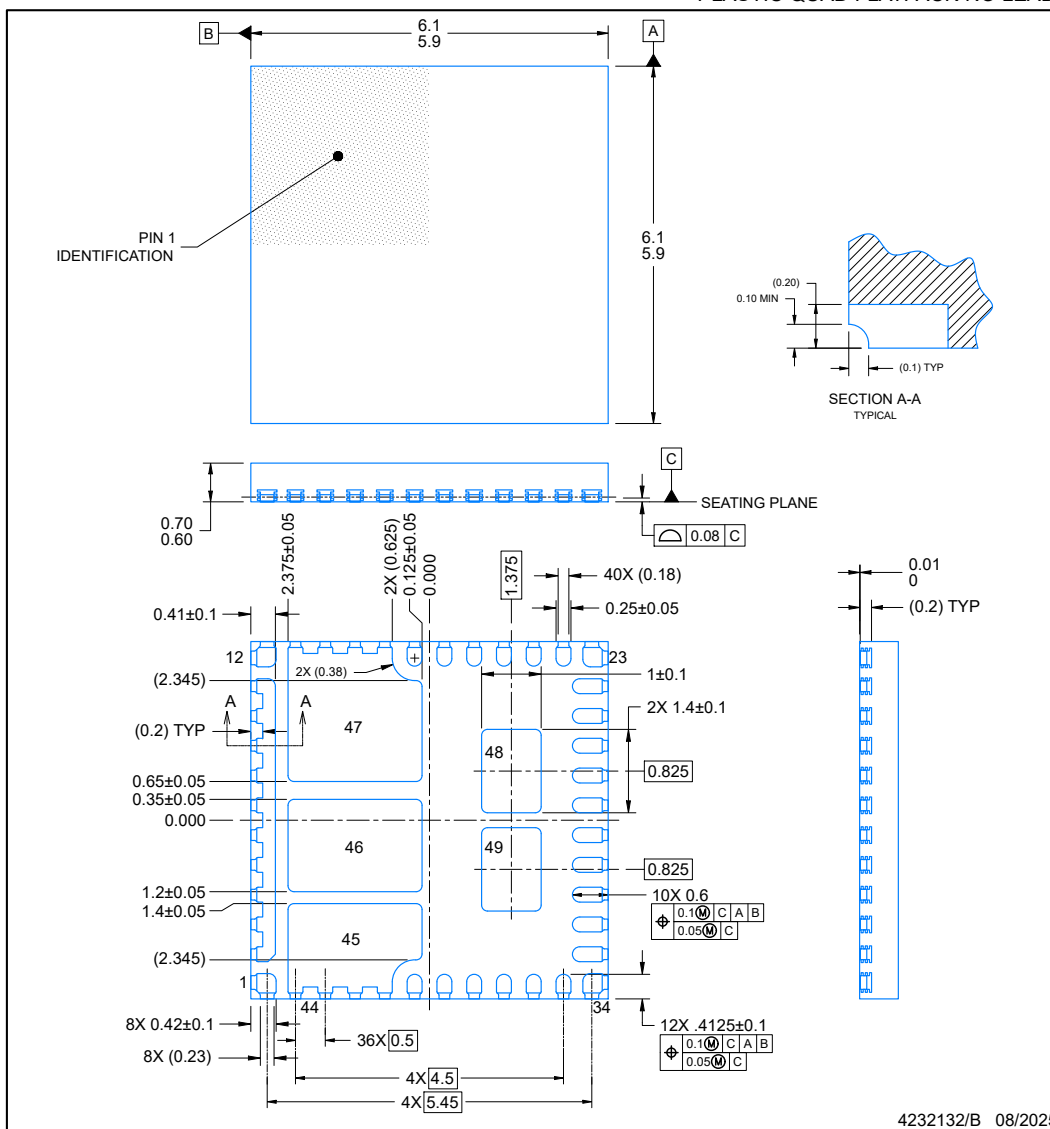
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-side navigation.

VEJ0049A

PACKAGE OUTLINE
WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



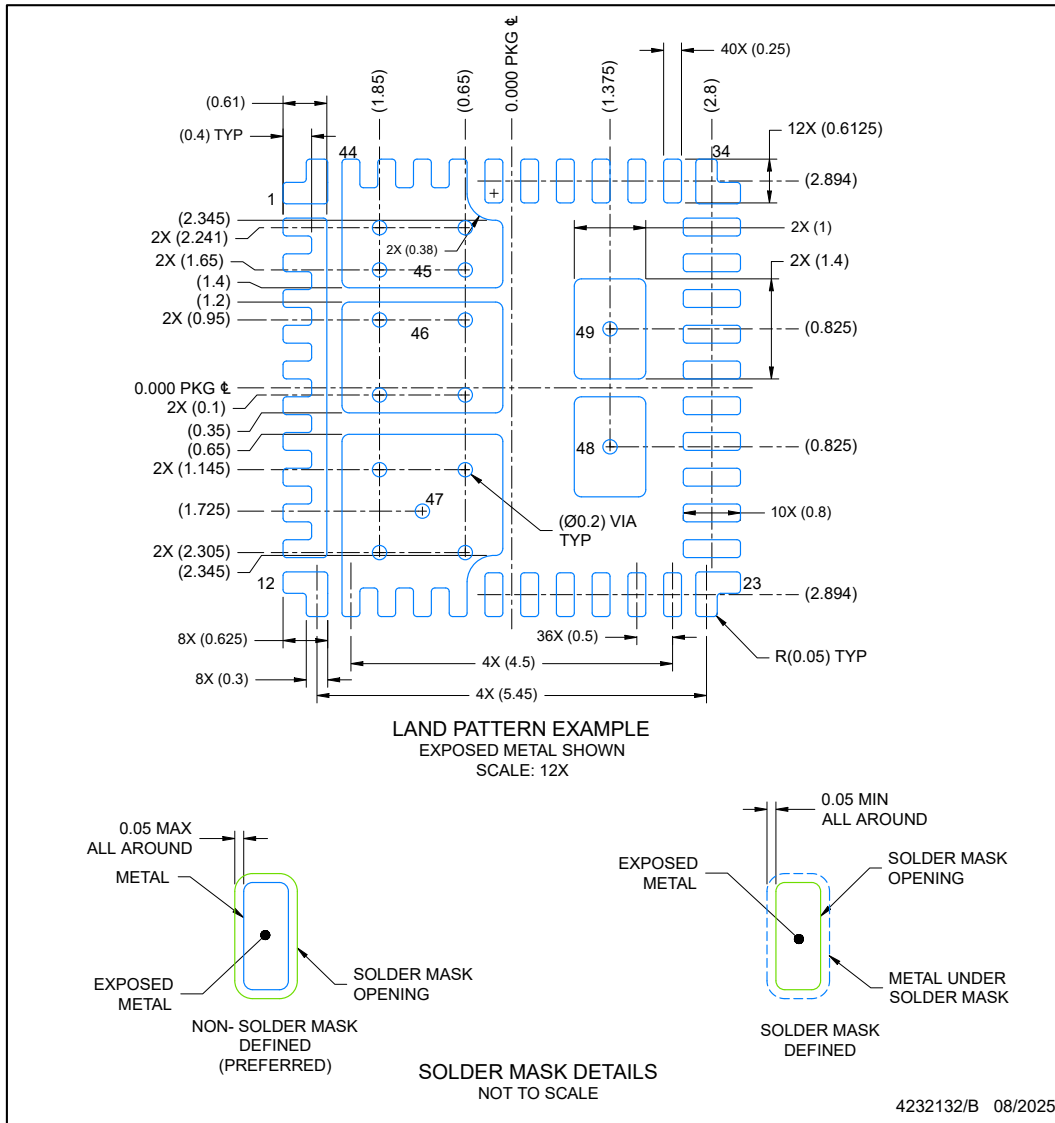
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

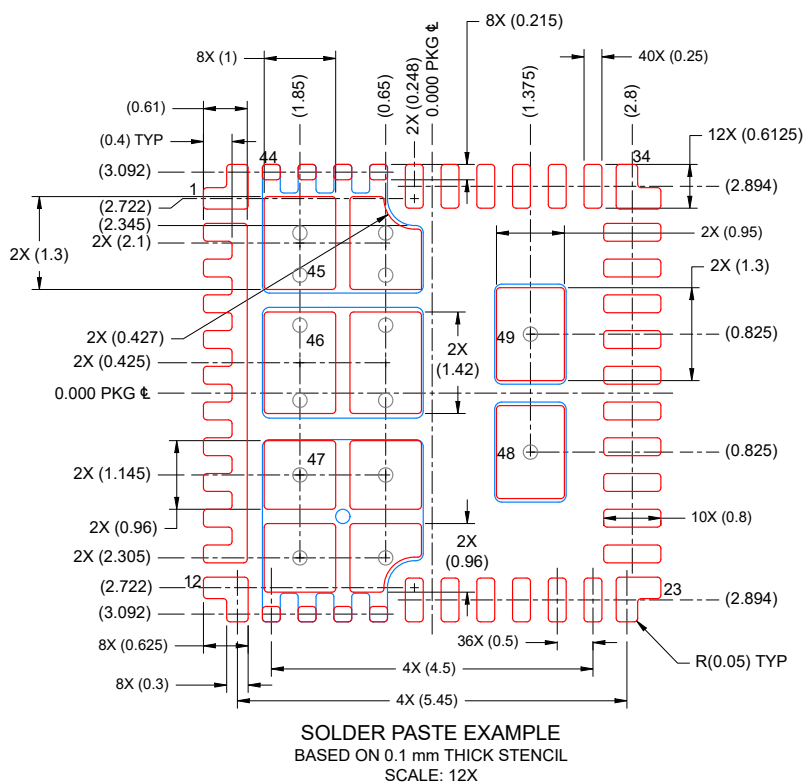
- For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

VEJ0049A

EXAMPLE STENCIL DESIGN

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



4232132/B 08/2025

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS7H6200MVEJTNSP	Active	Preproduction	WQFN-FCRLF (VEJ) 49	250 SMALL T&R	-	Call TI	Call TI	-55 to 125	

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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