TPS7B82-Q1 Automotive 300-mA, High-Voltage, Ultra-Low-I_Q Low-Dropout Regulator

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C ≤ T_A ≤ 125°C
  - Temperature grade 0: –40°C ≤ T_A ≤ 150°C
- Extended junction temperature range:
  - Grade 1: –40°C ≤ T_J ≤ 150°C
  - Grade 0: –40°C ≤ T_J ≤ 165°C
- Low quiescent current I_Q:
  - 300nA shutdown I_Q
  - 2.7µA typical at light loads
  - 5µA maximum at light loads
- 3V to 40V wide V_{IN} input voltage range with up to 45V transient
- Maximum output current: 300mA
- 2% output-voltage accuracy
- Maximum dropout voltage: 700mV at 200mA load current for fixed 5V output version
- Stable with low-ESR (0.001Ω to 5Ω) ceramic output-stability capacitor (1µF to 200µF)
- Fixed 2.5V, 3.3V, and 5V output voltage
- Packages:
  - 8-pin HVSSOP, $R_{\theta JA}$ = 63.9°C/W
  - 6-pin WSON, $R_{\theta JA}$ = 72.8°C/W
  - 6-pin WSON wettable flank, $R_{\theta JA}$ = 72.8°C/W
  - 5-pin TO-252, $R_{\theta JA}$ = 31.1°C/W
  - 14-pin HTSSOP, $R_{\theta JA}$ = 52.0°C/W

2 Applications

- Automotive head units
- Telematics control units
- Headlights
- Body control modules
- Inverter and motor controls

3 Description

In automotive battery-connected applications, low quiescent current (I_Q) is important to save power and extend battery lifetime. Ultra-low I_Q must be included for always-on systems.

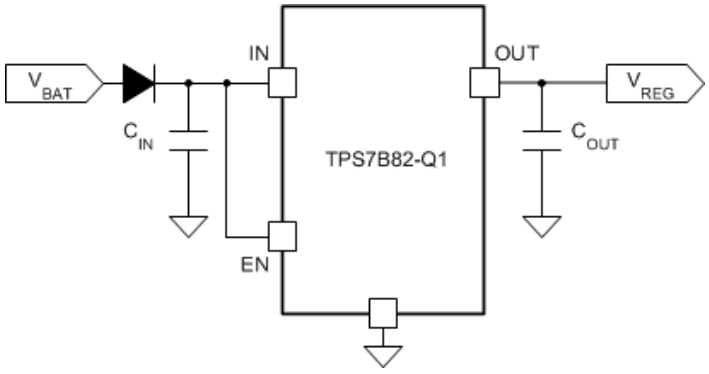
The TPS7B82-Q1 is a low-dropout linear regulator designed to operate with a wide input-voltage range from 3V to 40V (45V load dump protection). Operation down to 3V allows the TPS7B82-Q1 to continue operating during cold-crank and start and stop conditions. With only 2.7µA typical quiescent current at light load, this device is an optimum design for powering microcontrollers (MCUs) and CAN/LIN transceivers in standby systems.

The device features integrated short-circuit and overcurrent protection. This device operates in ambient temperatures from –40°C to +125°C and with junction temperatures from –40°C to +150°C. Additionally, this device uses a thermally conductive package to enable sustained operation despite significant dissipation across the device. Because of these features, the device is designed as a power supply for various automotive applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7B82-Q1	DGN (HVSSOP, 8)	3mm × 4.9mm
	DRV (WSON, 6)	2mm × 2mm
	DRV (WSON wettable flank, 6)	2mm × 2mm
	KVU (TO-252, 5)	6.6mm × 10.11mm
	PWP (HTSSOP, 14)	5mm × 6.4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

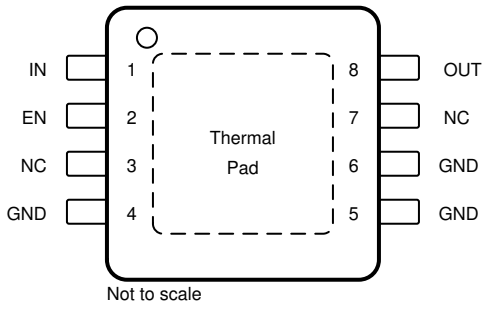


Figure 4-1. DGN Package, 8-Pin HVSSOP (Top View)

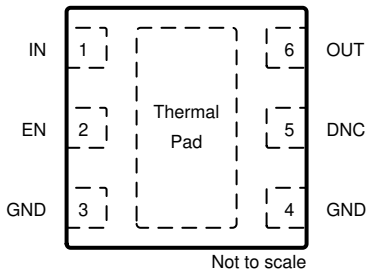


Figure 4-2. DRV Package, 6-Pin WSON (Top View)

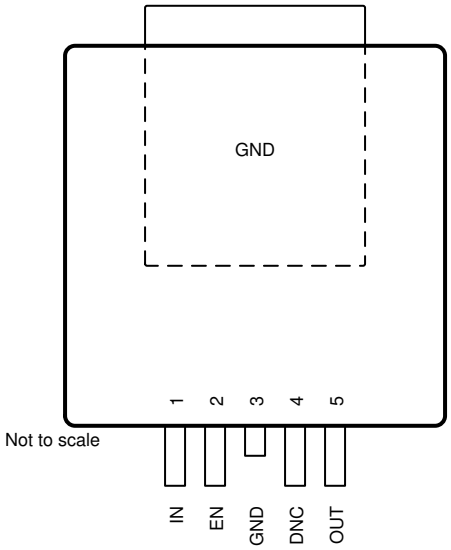


Figure 4-3. KVU Package, 5-Pin TO-252 (Top View)

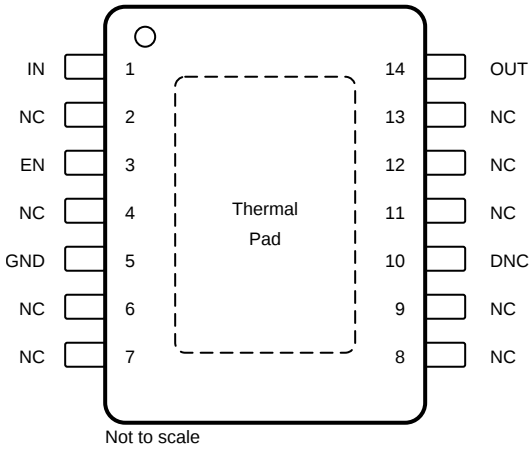


Figure 4-4. PWP Package, 14-Pin HTSSOP (Top View)

Table 4-1. Pin Functions

PIN					TYPE	DESCRIPTION
NAME	NO.					
	DGN	DRV	KVU	PWP		
DNC	—	5	4	10	—	Do not connect to a biased voltage. Tie this pin to ground or leave floating.
EN	2	2	2	3	I	Enable input pin
GND	4, 5, 6	3,4	3, TAB	5	—	Ground reference
IN	1	1	1	1	I	Input power-supply pin
NC	3, 7	—	—	2, 4, 6, 7, 8, 9, 11, 12, 13	—	Not internally connected
OUT	8	6	5	14	O	Regulated output voltage pin
Thermal pad					—	Connect the thermal pad to a large-area GND plane for improved thermal performance.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{IN}	Unregulated input(3)	–0.3	45	V
V_{EN}	Enable input(3)	–0.3	V_{IN}	V
V_{OUT}	Regulated output	–0.3	7	V
T_J	Junction temperature (grade 1)	–40	150	°C
	Junction temperature (grade 0)	–40	165	
T_{stg}	Storage temperature range	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Absolute maximum voltage, withstand 45 V for 200 ms.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD classification level H2		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C3B	Corner pins (1, 4, 5, and 8)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Unregulated input voltage	3	40	V
V_{EN}	Enable input voltage	0	V_{IN}	V
C_{OUT}	Output capacitor requirements(1)	1	200	µF
ESR	Output capacitor ESR requirements(2)	0.001	5	Ω
T_A	Ambient temperature (grade 1)	–40	125	°C
	Ambient temperature (grade 0)	–40	150	
T_J	Junction temperature (grade 1)	–40	150	°C
	Junction temperature (grade 0)	–40	165	

(1) The output capacitance range specified in the table is the effective value.
(2) Relevant equivalent series resistance (ESR) value at f = 10 kHz.

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5.4 Thermal Information

THERMAL METRIC[1]		TPS7B82-Q1				UNIT
		DGN (HVSSOP)	DRV (WSON)	KVU (TO-252)	PWP (HTSSOP)	
		8 PINS	6 PINS	5 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.9	72.8	31.1	52.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.2	85.8	39.9	48.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.6	37.4	9.9	28.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	2.7	4.2	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.3	37.3	9.9	28.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	13.8	2.8	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics: Grade 1 Options

V_{IN} = 14-V, 10-µF ceramic output capacitor, grade 1 options, T_J = –40°C to +150°C, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)							
V_{IN}	Input voltage			$V_{OUT(NOM)}$ + $V_{(Dropout)}$		40	V
$I_{(SD)}$	Shutdown current	EN = 0 V			0.3	1	µA
$I_{(Q)}$	Quiescent current	V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0 mA	DRV and KVU packages		1.9	3.5	µA
			DGN package		1.9	5	
		V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0.2 mA	DRV and KVU packages		2.7	4.5	
			DGN package		2.7	6.5	
$V_{(IN, UVLO)}$	V_{IN} undervoltage detection	Ramp V_{IN} down until the output turns OFF				2.7	V
		Hysteresis			200		mV
ENABLE INPUT (EN)							
V_{IL}	Logic-input low level					0.7	V
V_{IH}	Logic-input high level			2			V
REGULATED OUTPUT (OUT)							
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + $V_{(Dropout)}$ to 40 V, I_{OUT} = 1 mA to 300 mA	DRV, KVU packages	–1.5%		1.5%	
			DGN package for VOUT = 5.0 V	–1.5%		1.5%	
			DGN package for VOUT = 2.5 V and 3.3 V	–2%		2%	
$V_{(Line-Reg)}$	Line regulation	V_{IN} = 6 V to 40 V, I_{OUT} = 10 mA				10	mV
$V_{(Load-Reg)}$	Load regulation	V_{IN} = 14 V, I_{OUT} = 1 mA to 300 mA	DRV and KVU packages			10	mV
			DGN package			20	

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5.5 Electrical Characteristics: Grade 1 Options (continued)

V_{IN} = 14-V, 10-µF ceramic output capacitor, grade 1 options, T_J = –40°C to +150°C, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(Dropout)}$	Dropout voltage(1)	$V_{OUT(NOM)}$ = 5 V	I_{OUT} = 300 mA	DRV and KVU packages		630	1170	mV
				DGN package			1000	
			I_{OUT} = 200 mA	DRV and KVU packages		420	780	
				DGN package		400	700	
			I_{OUT} = 100 mA	DRV and KVU packages		210	390	
				DGN package		200	350	
		V_{OUT} = 3.3 V	I_{OUT} = 300 mA	DRV and KVU packages		730	1350	
				DGN package			1250	
			I_{OUT} = 200 mA	DRV and KVU packages		475	900	
				DGN package			850	
			I_{OUT} = 100 mA				450	
I_{OUT}	Output current	V_{OUT} in regulation			0		300	mA
$I_{(CL)}$	Output current limit	V_{OUT} short to 90% × V_{OUT}			310	510	690	mA
PSRR	Power-supply ripple rejection	$V_{(Ripple)}$ = 0.5 V_{PP}, I_{OUT} = 10 mA, frequency = 100 Hz, C_{OUT} = 2.2 µF				60		dB
OPERATING TEMPERATURE RANGE								
$T_{(SD)}$	Junction shutdown temperature					175		°C
$T_{(HYST)}$	Hysteresis of thermal shutdown					20		°C

(1) Dropout is not valid for the 2.5-V output because of the minimum input voltage limits.

5.6 Electrical Characteristics: Grade 0 Options

V_{IN} = 14-V, 10-µF ceramic output capacitor, grade 0 options (PWP package), T_J = –40°C to +165°C, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)						
V_{IN}	Input voltage		$V_{OUT(NOM)}$ + $V_{(Dropout)}$		40	V
$I_{(SD)}$	Shutdown current	EN = 0 V		0.3	1	µA
$I_{(Q)}$	Quiescent current	V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0 mA		1.9	5	
		V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0.2 mA		2.7	6.5	µA
$V_{(IN, UVLO)}$	V_{IN} undervoltage detection	Ramp V_{IN} down until the output turns OFF			2.7	V
		Hysteresis		200		mV
ENABLE INPUT (EN)						
V_{IL}	Logic-input low level				0.7	V
V_{IH}	Logic-input high level		2			V
REGULATED OUTPUT (OUT)						

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5.6 Electrical Characteristics: Grade 0 Options (continued)

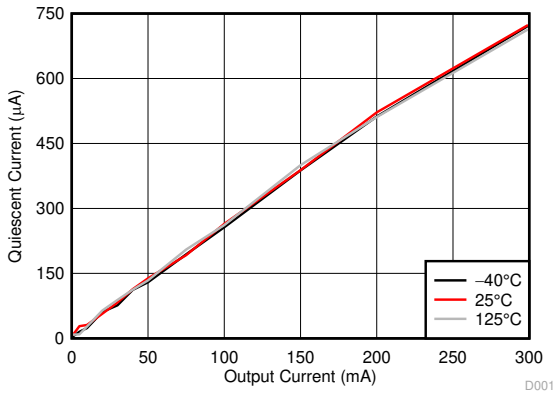
V_{IN} = 14-V, 10-µF ceramic output capacitor, grade 0 options (PWP package), T_J = –40°C to +165°C, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + $V_{(Dropout)}$ to 14 V, I_{OUT} = 1 mA to 300 mA		–1.5%		1.5%	
$V_{(Line-Reg)}$	Line regulation	V_{IN} = 6 V to 40 V, I_{OUT} = 10 mA				10	mV
$V_{(Load-Reg)}$	Load regulation	V_{IN} = 14 V, I_{OUT} = 1 mA to 300 mA				20	mV
$V_{(Dropout)}$	Dropout voltage[1]	$V_{OUT(NOM)}$ = 5 V	I_{OUT} = 300 mA		630	1170	mV
			I_{OUT} = 200 mA		420	780	
			I_{OUT} = 100 mA		210	390	
		V_{OUT} = 3.3 V	I_{OUT} = 300 mA		730	1350	
			I_{OUT} = 200 mA		475	900	
			I_{OUT} = 100 mA			450	
I_{OUT}	Output current	V_{OUT} in regulation		0		300	mA
$I_{(CL)}$	Output current limit	V_{OUT} short to 90% × V_{OUT}		310	510	690	mA
PSRR	Power-supply ripple rejection	$V_{(Ripple)}$ = 0.5 V_{PP}, I_{OUT} = 10 mA, frequency = 100 Hz, C_{OUT} = 2.2 µF			60		dB
OPERATING TEMPERATURE RANGE							
$T_{(SD)}$	Junction shutdown temperature				185		°C
$T_{(HYST)}$	Hysteresis of thermal shutdown				20		°C

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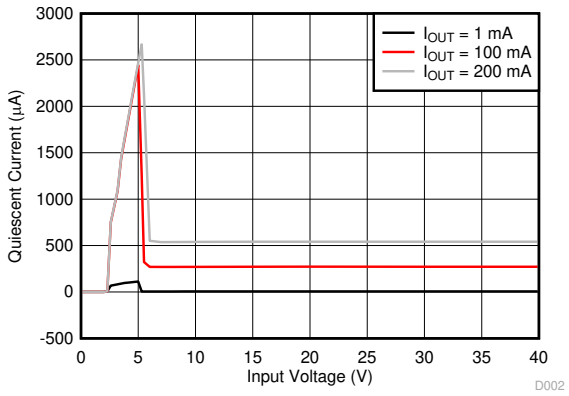
5.7 Typical Characteristics

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40°C to 150°C (unless otherwise noted)



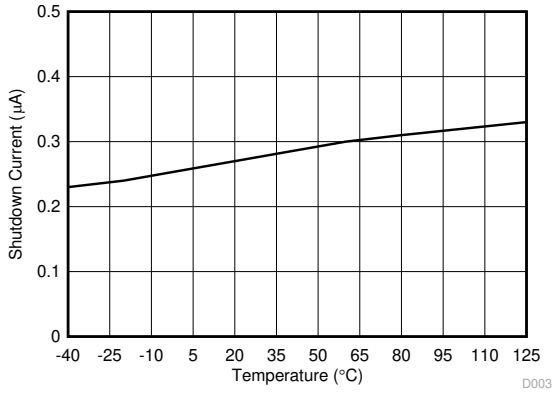
V_{OUT} = 5 V

Figure 5-1. Quiescent Current vs Output Current



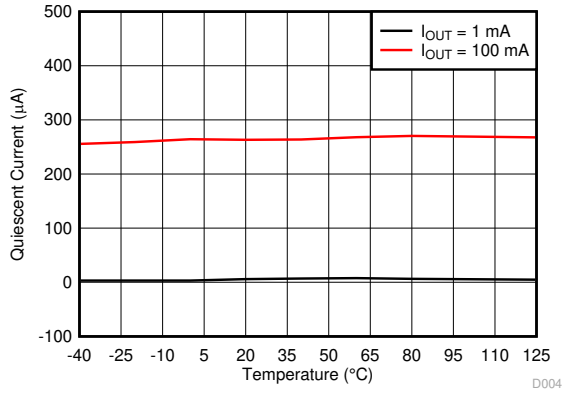
V_{OUT} = 5 V

Figure 5-2. Quiescent Current vs Input Voltage



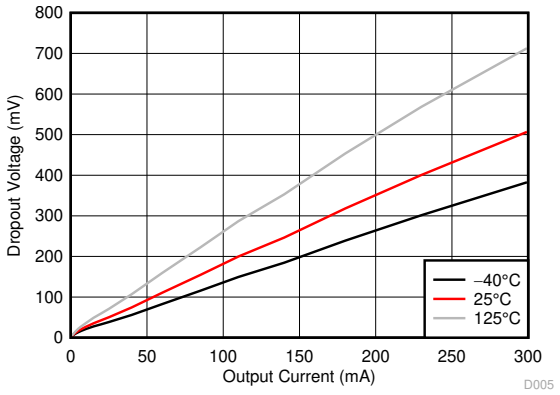
V_{EN} = 0 V

Figure 5-3. Shutdown Current vs Ambient Temperature



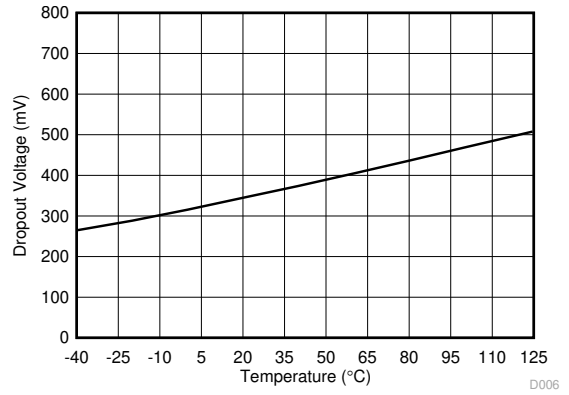
V_{OUT} = 5 V

Figure 5-4. Quiescent Current vs Ambient Temperature



V_{IN} = 5 V, 5-V fixed output, $V_{(Dropout)} = V_{IN} – V_{OUT}$

Figure 5-5. Dropout Voltage vs Output Current



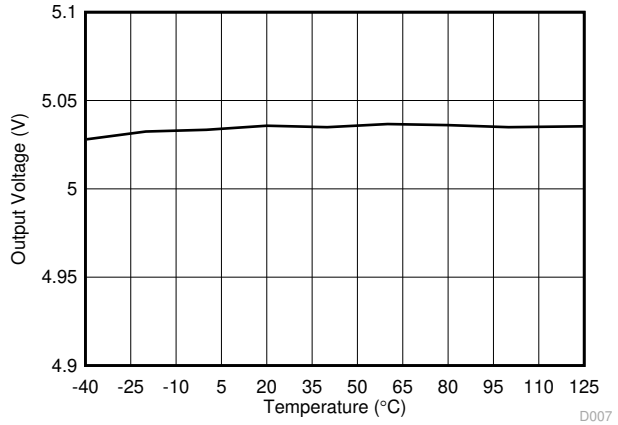
V_{IN} = 5 V, 5-V fixed output, $V_{(Dropout)} = V_{IN} – V_{OUT}$

Figure 5-6. Dropout Voltage vs Ambient Temperature

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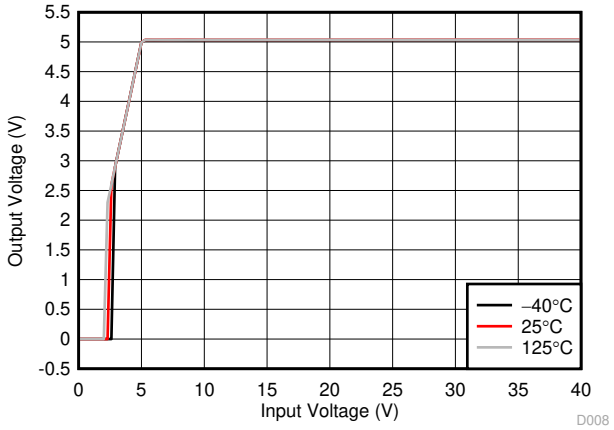
5.7 Typical Characteristics (continued)

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40°C to 150°C (unless otherwise noted)



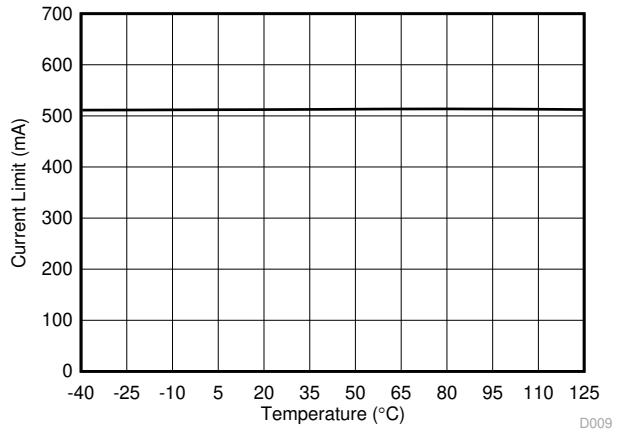
V_{OUT} = 5 V

Figure 5-7. Output Voltage vs Ambient Temperature



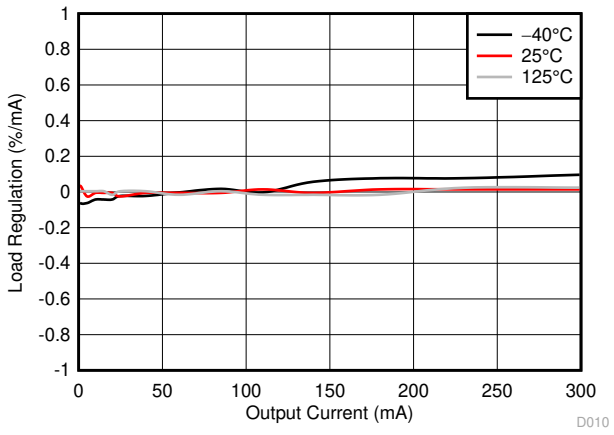
V_{OUT} = 5 V, I_{OUT} = 1 mA

Figure 5-8. Output Voltage vs Input Voltage



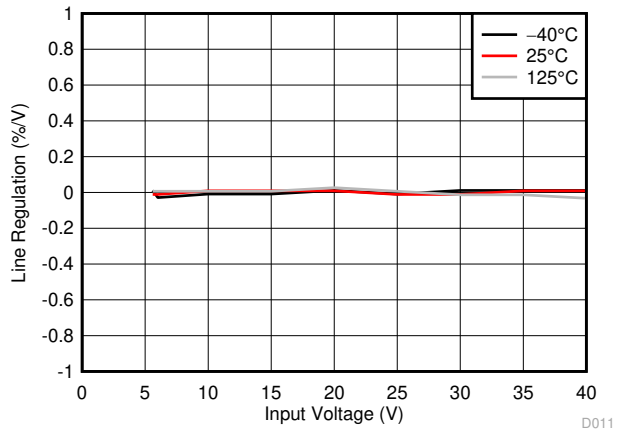
V_{IN} = 14 V, V_{OUT} is shorted to 90% × V_{OUT}

Figure 5-9. Output Current Limit vs Ambient Temperature



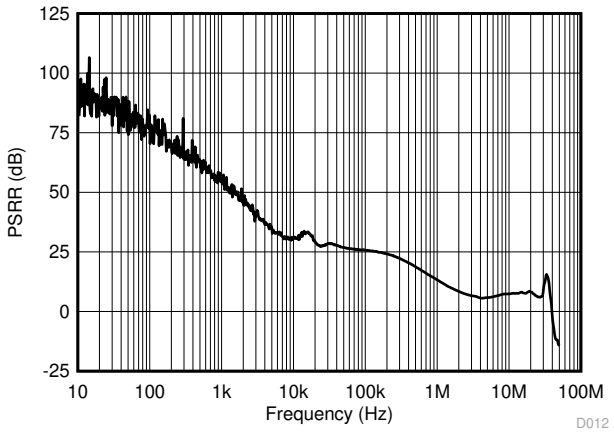
V_{OUT} = 5 V

Figure 5-10. Load Regulation



V_{OUT} = 5 V, I_{OUT} = 10 mA

Figure 5-11. Line Regulation



I_{OUT} = 10 mA

Figure 5-12. PSRR vs Frequency

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5.7 Typical Characteristics (continued)

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40°C to 150°C (unless otherwise noted)

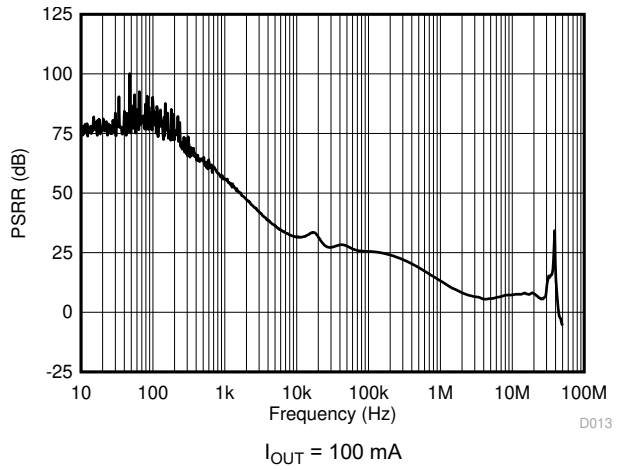


Figure 5-13. PSRR vs Frequency

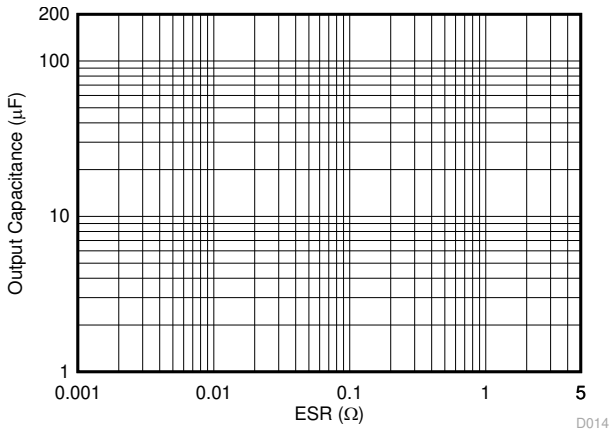


Figure 5-14. Output Capacitance vs ESR Stability

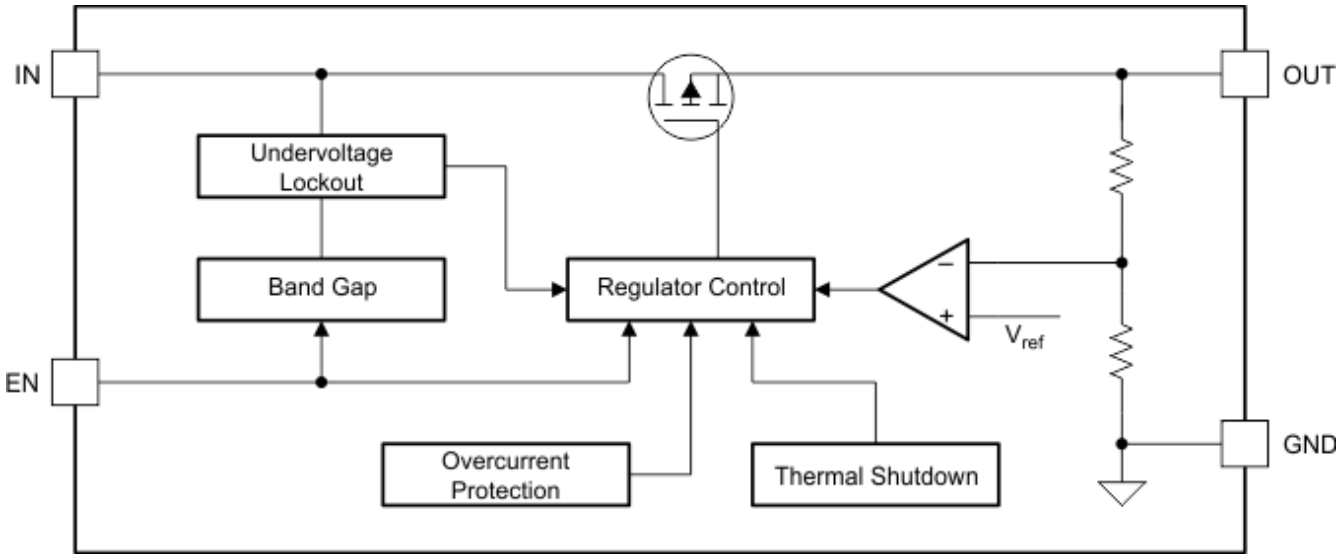
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6 Detailed Description

6.1 Overview

The TPS7B82-Q1 is a 40-V, 300-mA low-dropout (LDO) linear regulator with ultra-low quiescent current. This voltage regulator consumes only 3 µA of quiescent current at light load, and is designed for the automotive always-on application.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulation ON. Connect this pin to an external microcontroller or a digital circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

6.3.2 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internal UVLO threshold ($V_{(UVLO)}$). This threshold limit ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required level.

6.3.3 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This limit protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

6.3.4 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature must not exceed the TSD trip point. The junction temperature exceeding the TSD trip point causes the output to turn off. When the junction temperature falls below the TSD trip point minus thermal shutdown hysteresis, the output turns on again.

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6.4 Device Functional Modes

6.4.1 Operation With V_{IN} Lower Than 3 V

The device normally operates with input voltages above 3 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.7 V. At input voltages below the actual UVLO voltage, the device does not operate.

6.4.2 Operation With V_{IN} Larger Than 3 V

When V_{IN} is greater than 3 V, if V_{IN} is also higher than the output set value plus the device dropout voltage, V_{OUT} is equal to the set value. Otherwise, V_{OUT} is equal to V_{IN} minus the dropout voltage.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS7B82-Q1 is a 300-mA, 40-V low-dropout linear regulator with ultra-low quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

7.2 Typical Application

Figure 7-1 shows a typical application circuit for the TPS7B82-Q1. Different values of external components can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. Use a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

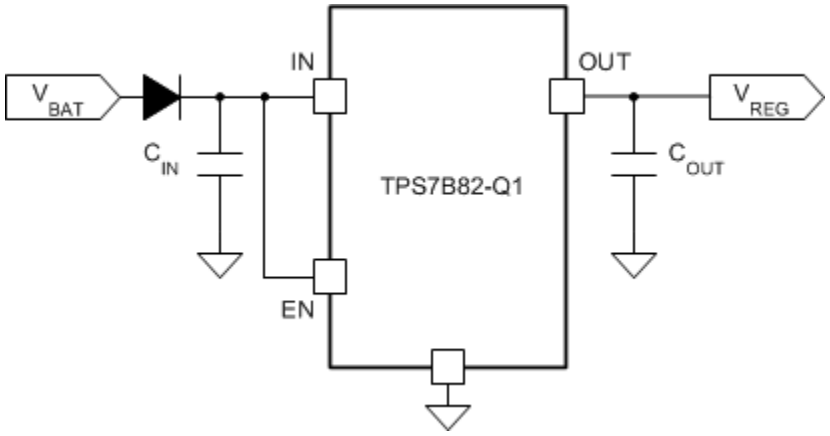


Figure 7-1. TPS7B82-Q1 Typical Application Schematic

7.2.1 Design Requirements

For this design example, use the parameters listed in Table 7-1.

Table 7-1. Design Requirements Parameters

PARAMETER	VALUE
Input voltage range	3 V to 40 V
Output voltage	5 V or 3.3 V
Output current	300 mA maximum

7.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current

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7.2.2.1 Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a 10-µF to 22-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR. The voltage rating must be greater than the maximum input voltage.

7.2.2.2 Output Capacitor

To ensure the stability of the TPS7B82-Q1, the device requires an output capacitor with a value in the range from 1 µF to 200 µF and with an ESR range between 0.001 Ω and 5 Ω. Select a ceramic capacitor with low ESR to improve the load transient response.

7.2.3 Application Curve

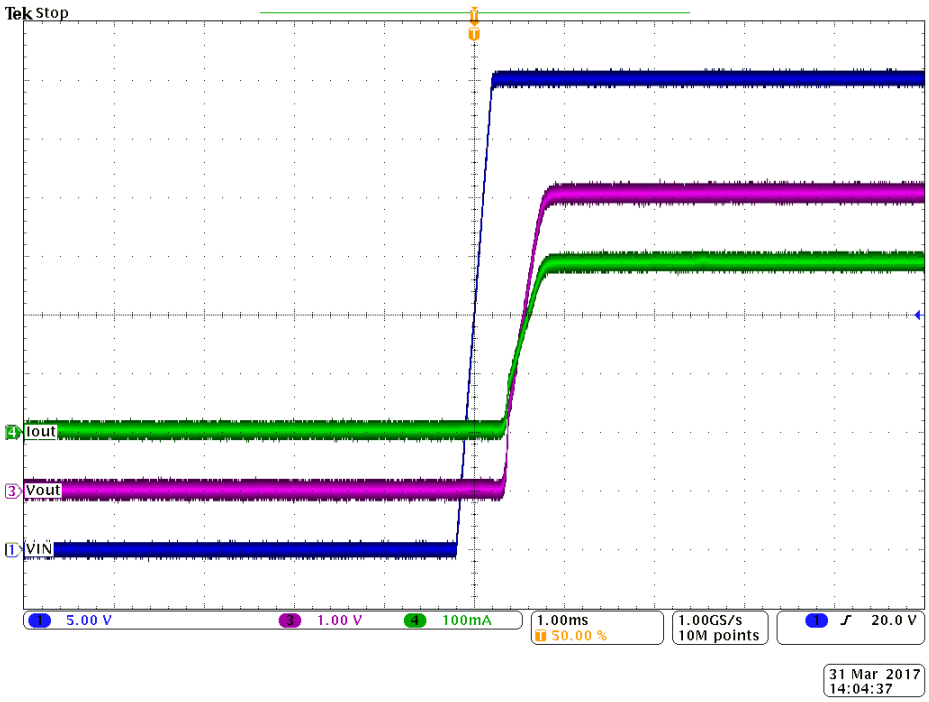


Figure 7-2. TPS7B82-Q1 Power-Up Waveform (5 V)

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B82-Q1, add a capacitor with a value greater than or equal to 10 µF with a 0.1-µF bypass capacitor in parallel at the input.

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7.4 Layout

7.4.1 Layout Guidelines

For LDO power supplies, especially high-voltage and large output current supplies, layout is an important step. If layout is not carefully designed, the regulator can fail to deliver enough output current because of thermal limitation. To improve the thermal performance of the device, and to maximize the current output at high ambient temperature, spread the copper under the thermal pad as far as possible and place enough thermal vias on the copper under the thermal pad. Figure 7-3 shows an example layout.

7.4.2 Layout Example

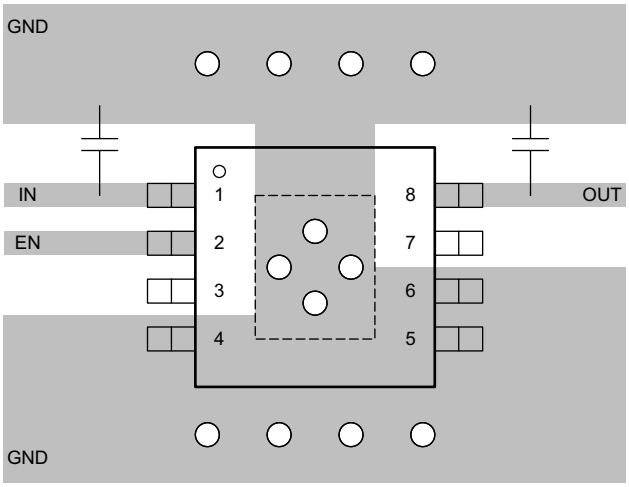


Figure 7-3. TPSB82-Q1 Example Layout Diagram

8 Device and Documentation Support

8.1 Device Nomenclature

Table 8-1. Available Options

PRODUCT(1)	DESCRIPTION
TPS7B82**xx**Q**(W)*yyyz***Q1	**xx** is the nominal output voltage (for example, 50 = 5.0V, 33 = 3.3V). **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **yyy** is the package designator. **z** is the reel quantity. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.
TPS7B82**xx**E ***yyyz***Q1	**xx** is the nominal output voltage (for example, 50 = 5.0V, 33 = 3.3V). **E** indicates that this device is a grade-0 device in accordance with the AEC-Q100 standard. **yyy** is the package designator. **z** is the reel quantity. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (August 2023) to Revision K (September 2025)	Page
• Added WSON wettable flank (DRV) package to document	1

Changes from Revision I (September 2017) to Revision J (August 2023)	Page
• Changed V_{OUT} parameter test conditions in *Electrical Characteristics* table	5

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- Added *Device Nomenclature* section..... 16

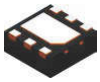
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

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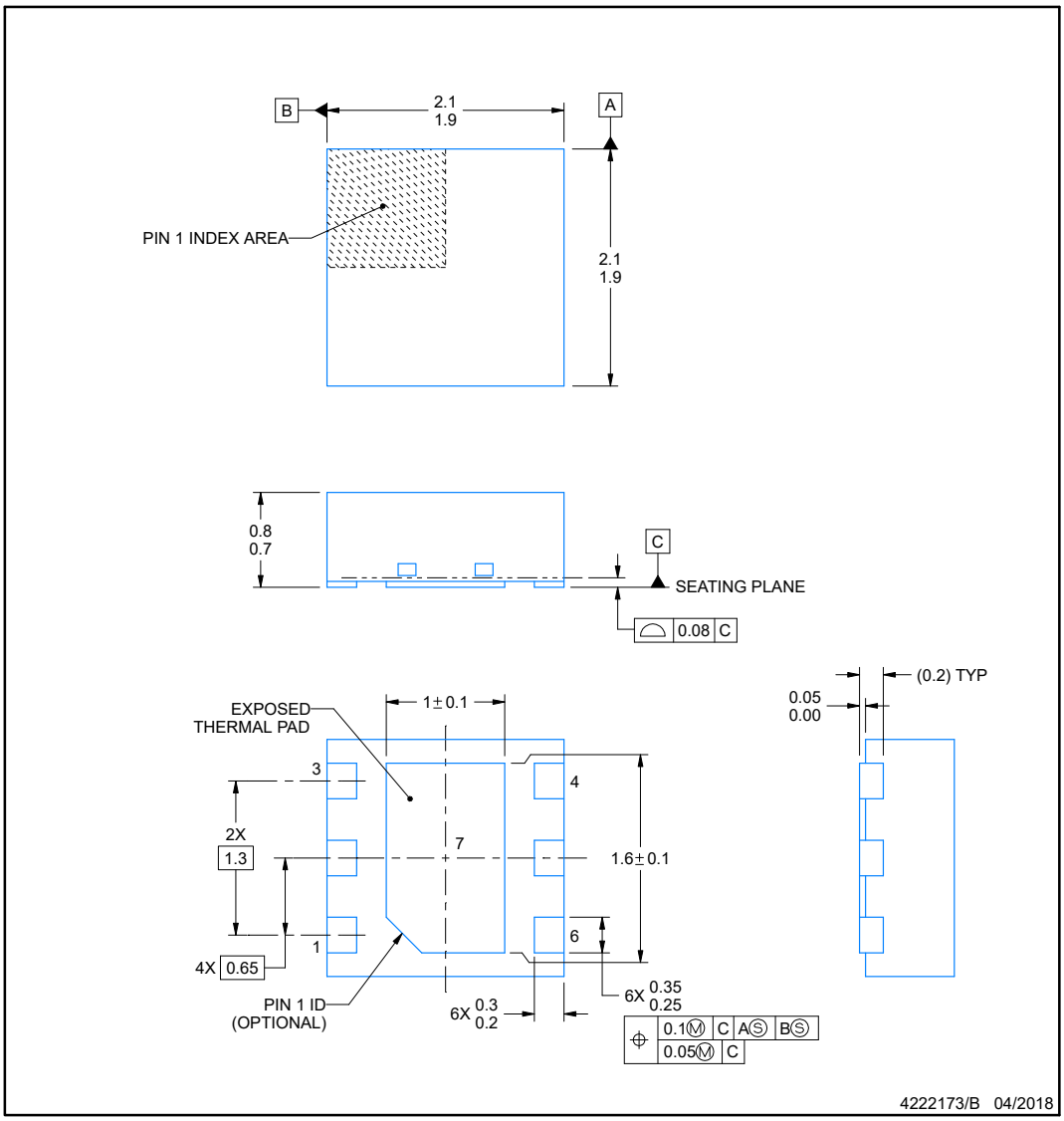
PACKAGE OUTLINE

DRV0006A



WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

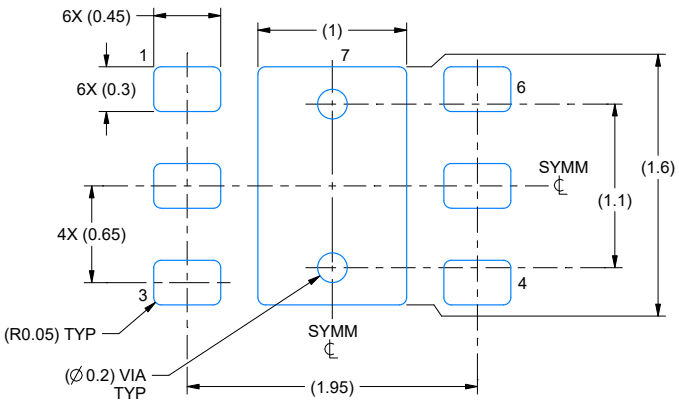
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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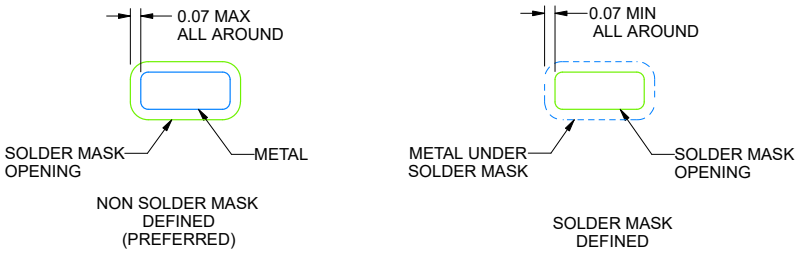
EXAMPLE BOARD LAYOUT

DRV0006A — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

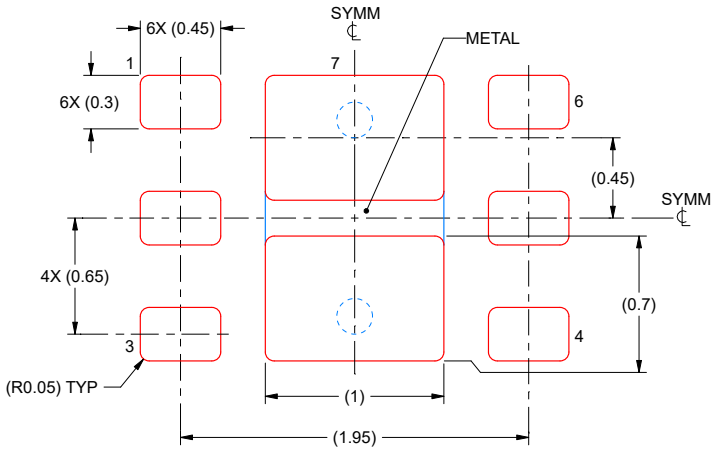
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

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EXAMPLE STENCIL DESIGN

DRV0006A — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7B8225QDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1QFX
TPS7B8225QDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	See TPS7B8225QDGNRQ1	1QFX
TPS7B8233EPWPRQ1	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 165	7B8233E
TPS7B8233EPWPRQ1.A	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	See TPS7B8233EPWPRQ1	7B8233E
TPS7B8233QDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1GGX
TPS7B8233QDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	See TPS7B8233QDGNRQ1	1GGX
TPS7B8233QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1ORH
TPS7B8233QDRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TPS7B8233QDRVRQ1	1ORH
TPS7B8233QKVURQ1	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8233Q1
TPS7B8233QKVURQ1.A	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	See TPS7B8233QKVURQ1	7B8233Q1
TPS7B8233QWDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	3NIH
TPS7B8250EPWPRQ1	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 165	7B8250E
TPS7B8250EPWPRQ1.A	Active	Production	HTSSOP (PWP) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	See TPS7B8250EPWPRQ1	7B8250E
TPS7B8250QDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	19TX
TPS7B8250QDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	See TPS7B8250QDGNRQ1	19TX
TPS7B8250QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1UFH
TPS7B8250QDRVRQ1.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TPS7B8250QDRVRQ1	1UFH
TPS7B8250QKVURQ1	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 150	7B8250Q1
TPS7B8250QKVURQ1.A	Active	Production	TO-252 (KVU) | 5	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	See TPS7B8250QKVURQ1	7B8250Q1
TPS7B8250QWDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	3NJH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

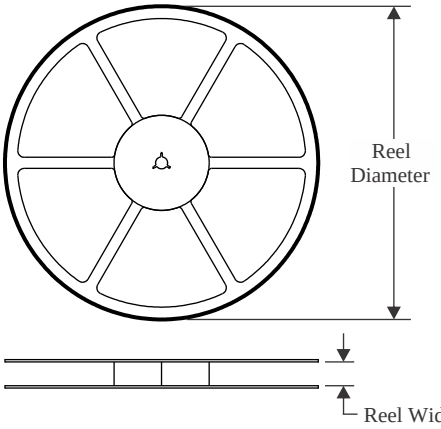
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

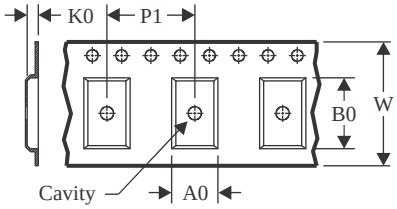
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

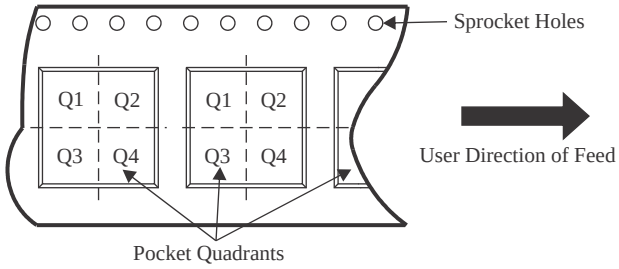


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

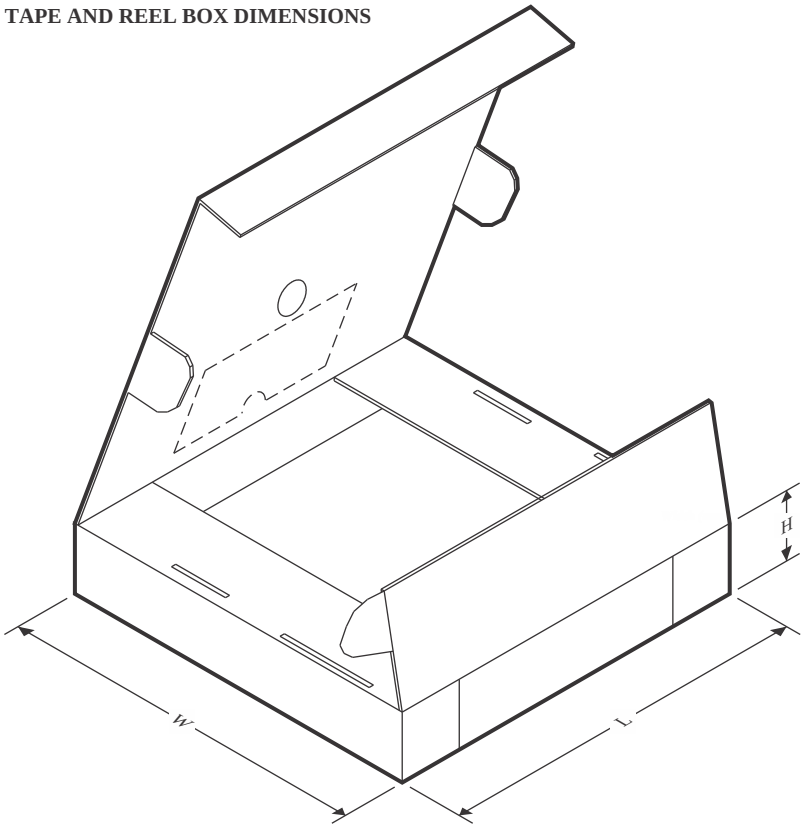
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B8225QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8233EPWPRQ1	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7B8233QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8233QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8233QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7B8233QWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8250EPWPRQ1	HTSSOP	PWP	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7B8250QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8250QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8250QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7B8250QWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B8225QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8233EPWPRQ1	HTSSOP	PWP	14	2500	353.0	353.0	32.0
TPS7B8233QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8233QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7B8233QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7B8233QWDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7B8250EPWPRQ1	HTSSOP	PWP	14	2500	353.0	353.0	32.0
TPS7B8250QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7B8250QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7B8250QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TPS7B8250QWDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

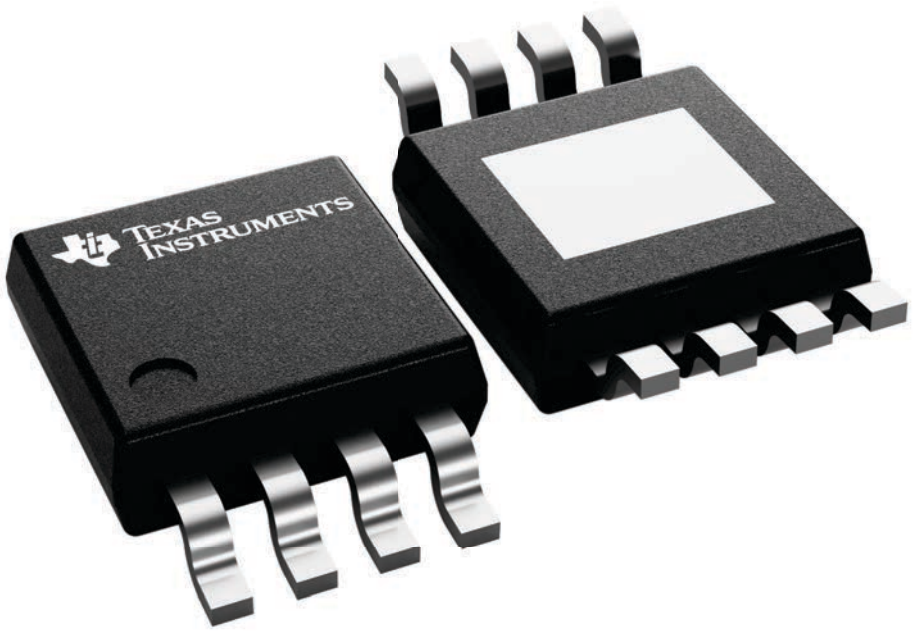
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

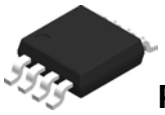
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

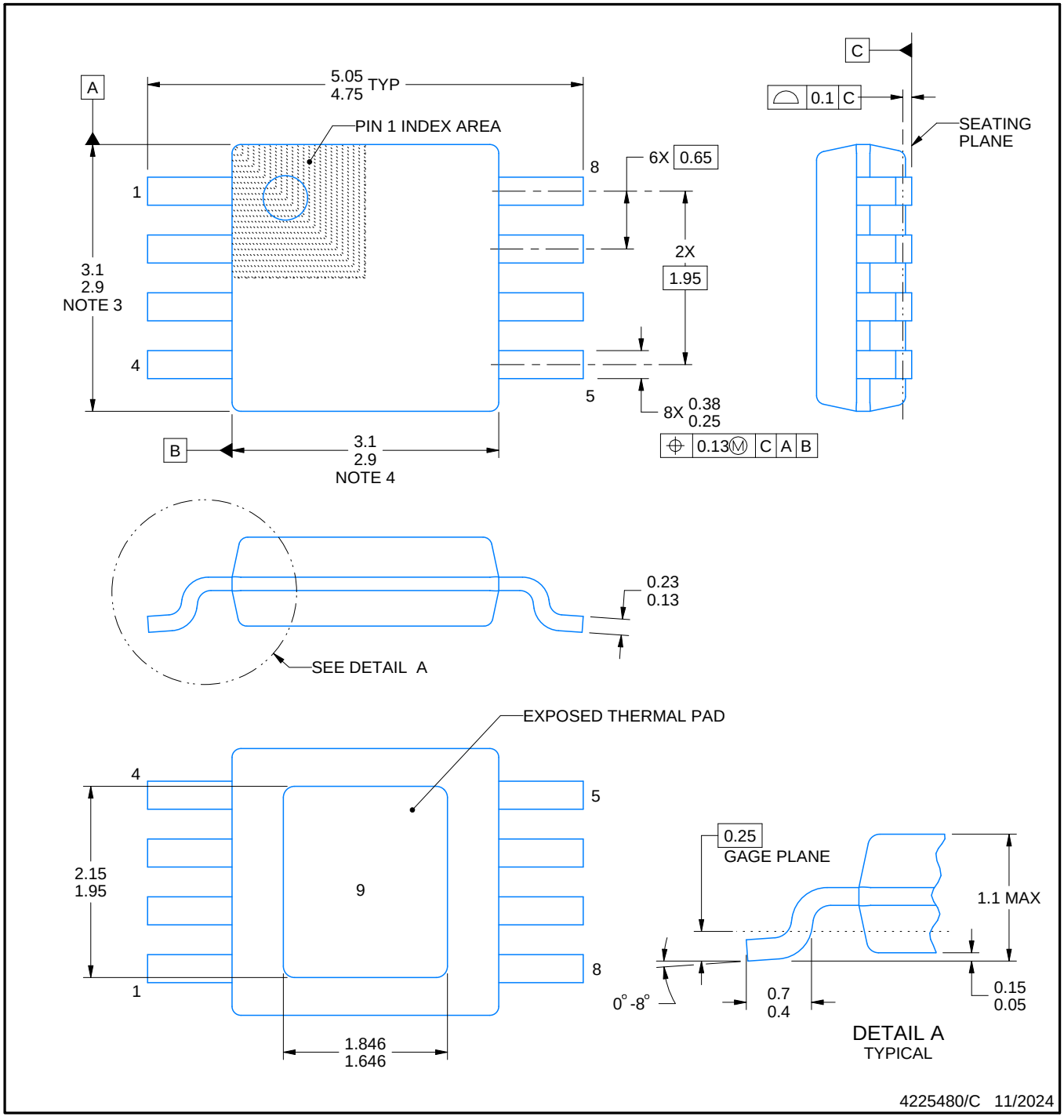
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

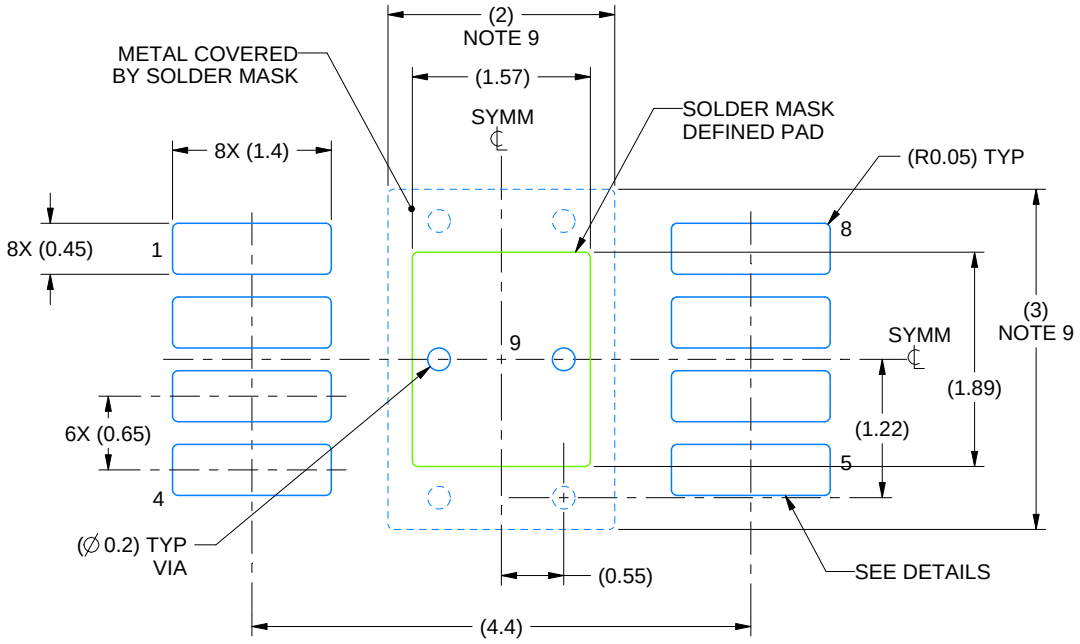
SMALL OUTLINE PACKAGE



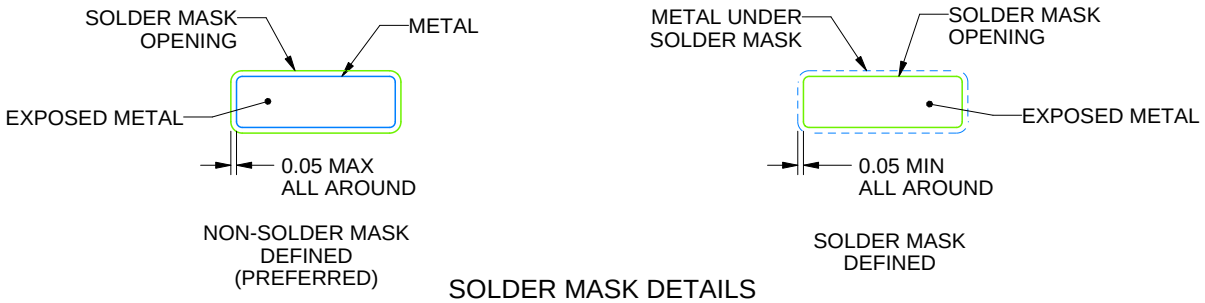
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

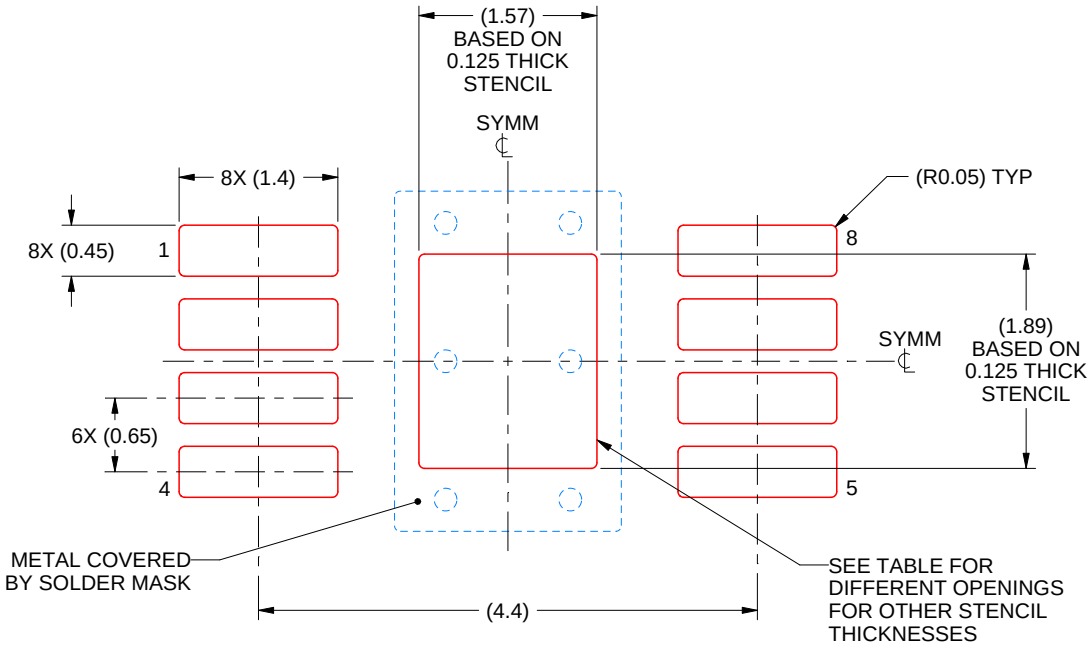


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

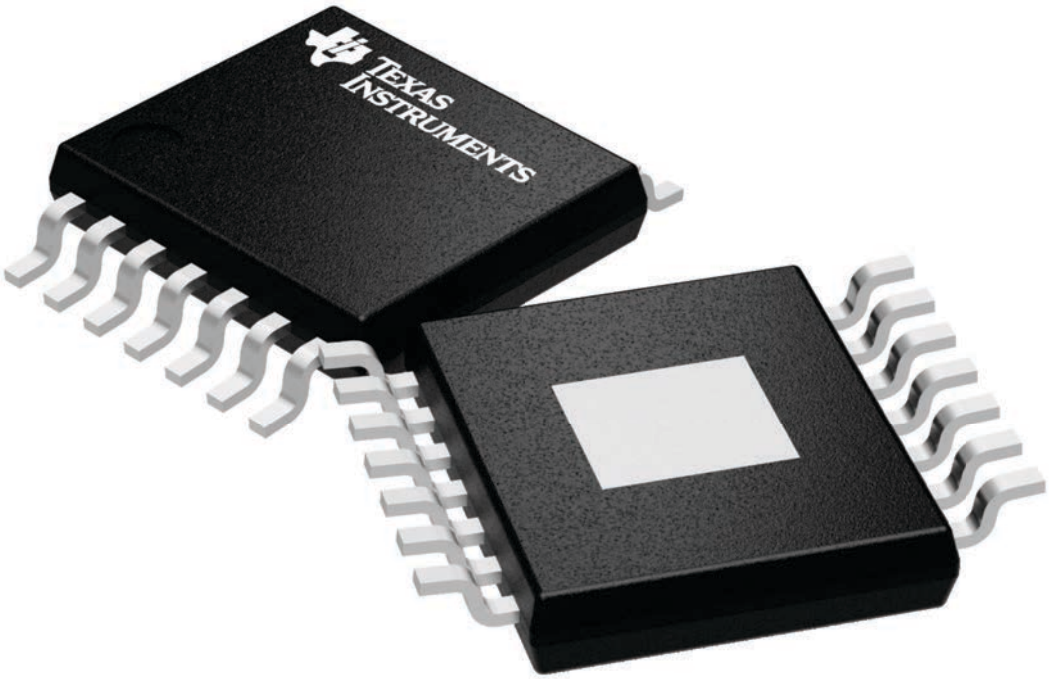
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



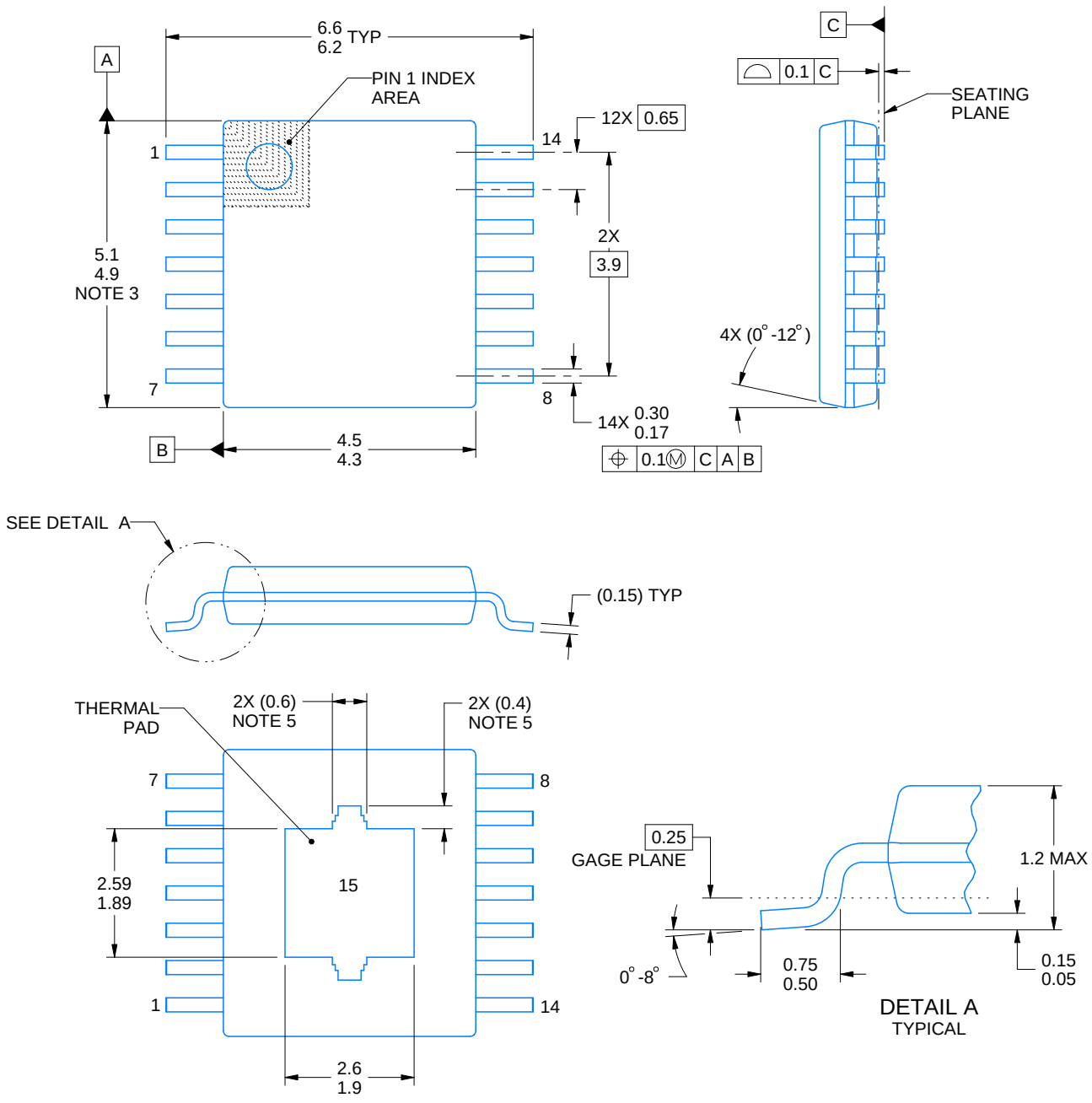
4224995/A

PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

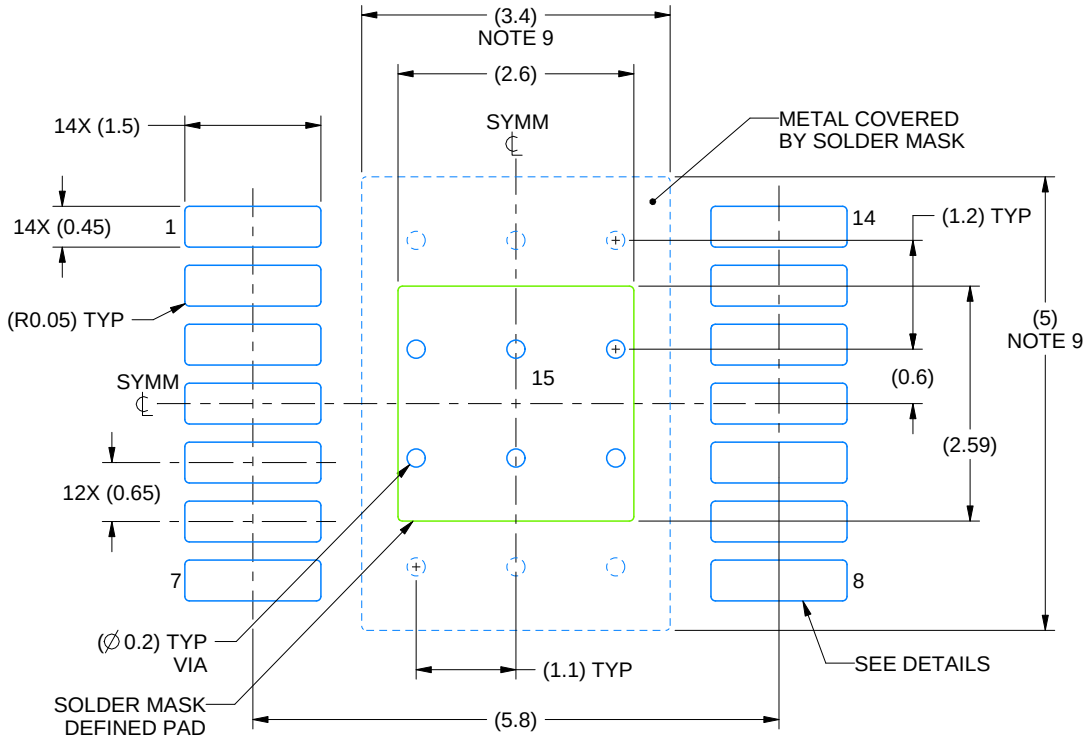
SMALL OUTLINE PACKAGE



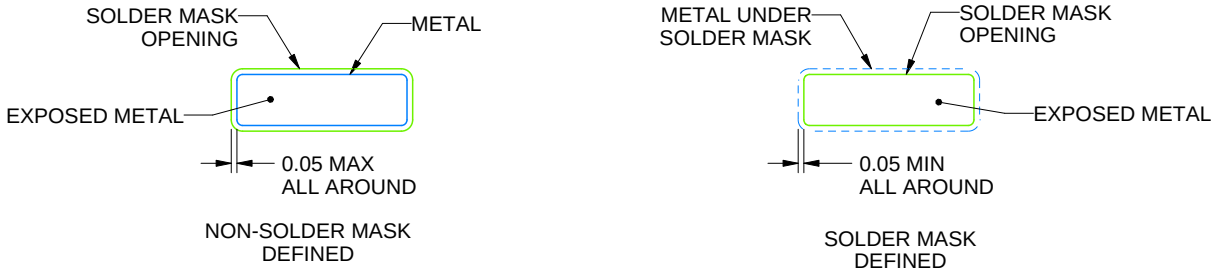
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

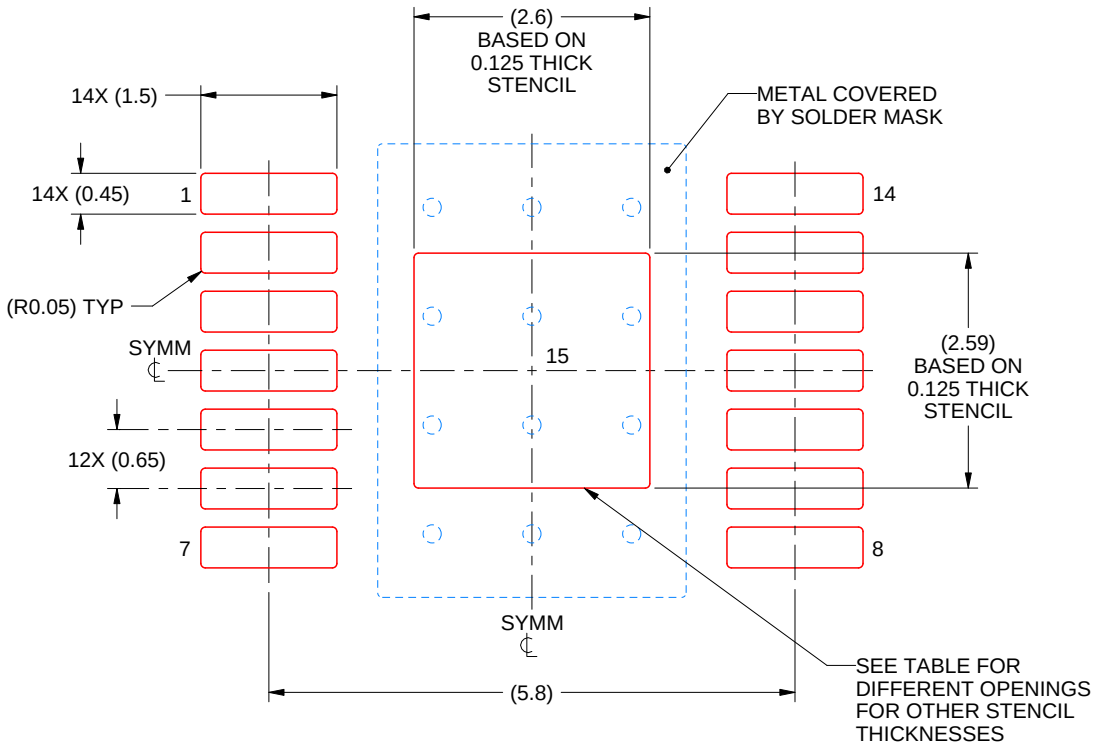


SOLDER MASK DETAILS

4229706/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

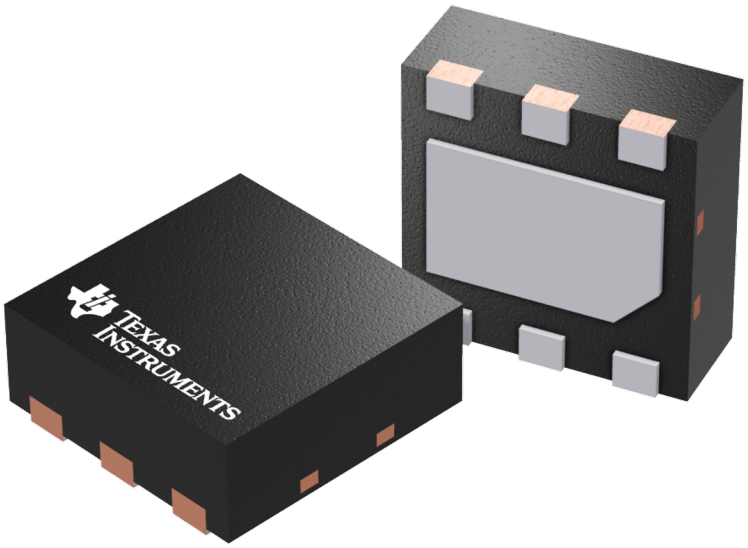
4229706/B 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

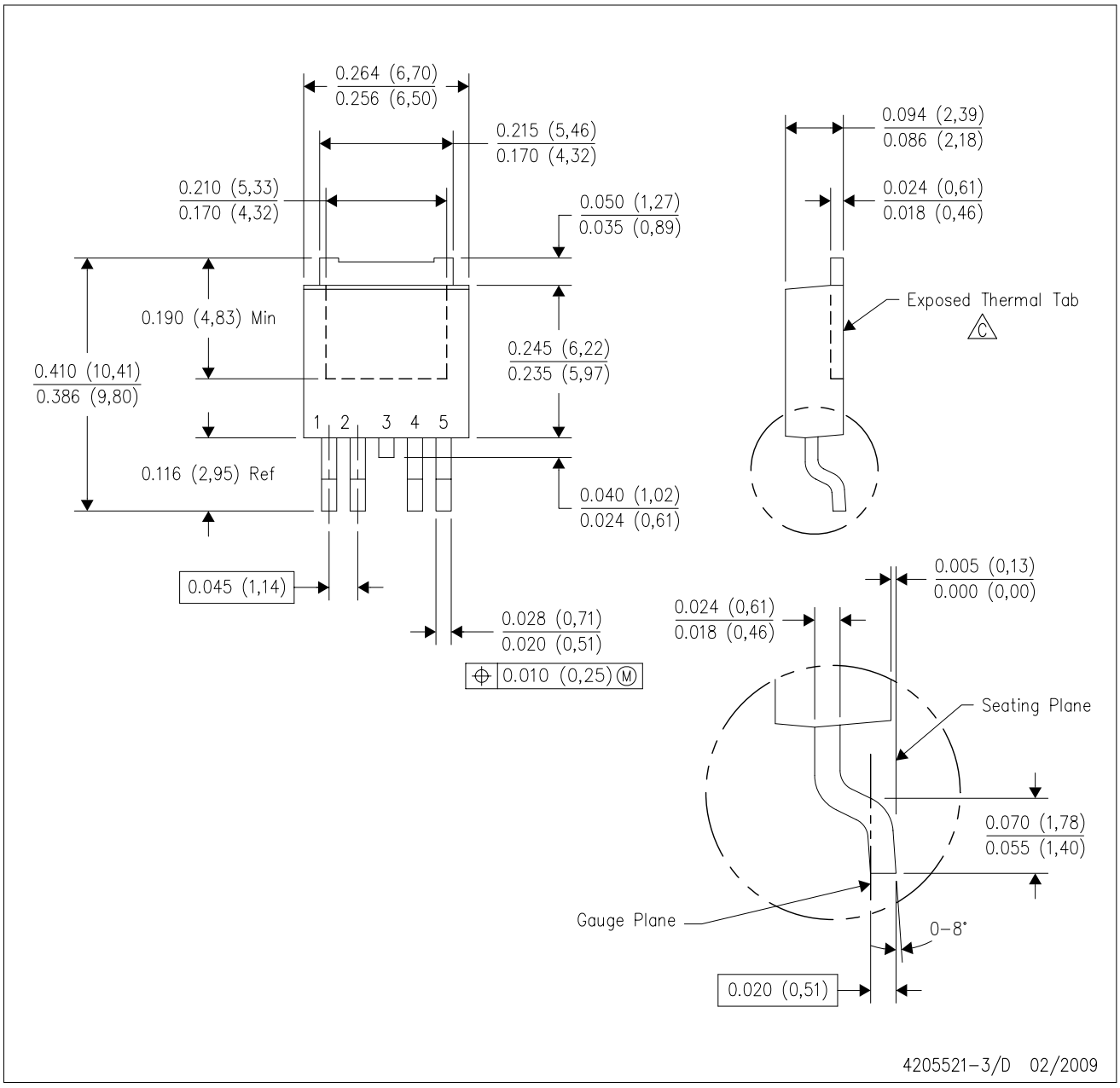
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

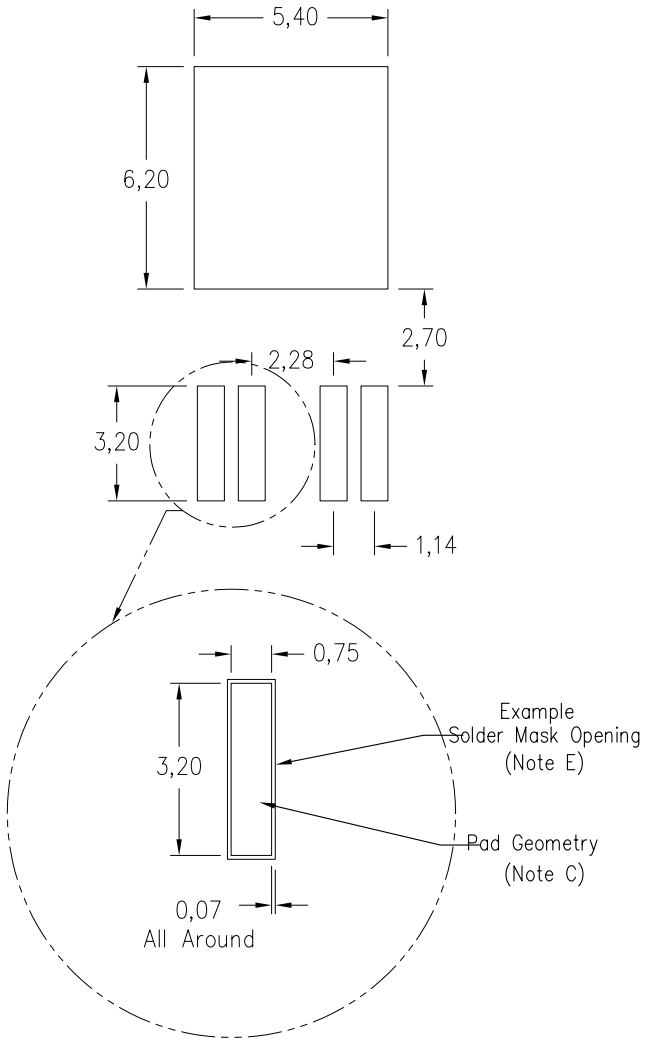
KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



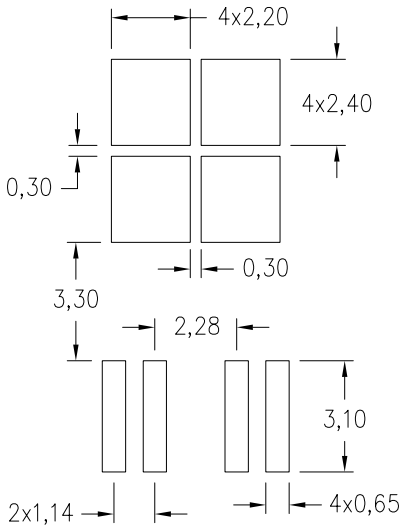
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AD.

KVU (R–PSFM–G5) PLASTIC FLANGE MOUNT PACKAGE

Example Board Layout



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



63% solder coverage on center pad

4211592–3/B 03/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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