TPS7A92 2A, High-Accuracy, Low-Noise LDO Voltage Regulator

1 Features

- 1.0% accuracy over line, load, and temperature
- Low output noise: 4.6µV_{RMS} (10Hz – 100kHz)
- Low dropout: 180mV (typical) at 2A
- Wide input voltage range: 1.4V to 6.5V
- Wide output voltage range: 0.8V to 5.2V
- High power-supply rejection ratio (PSRR):
  - 60dB at DC
  - 40dB at 100kHz
  - 40dB at 1MHz
- Fast transient response
- Adjustable start-up in-rush control with selectable soft-start charging current
- Open-drain power-good (PG) output
- $R_{\theta JC}$ = 3.2°C/W
- Stable with a 22µF or larger ceramic output capacitor
- 2.5mm × 2.5mm, 10-pin WSON package

2 Applications

- High-speed analog circuits:
  - VCO, ADC, DAC, LVDS
- Imaging: CMOS sensors, video ASICs
- Test and measurement
- Instrumentation, medical, and audio
- Digital loads: SerDes, FPGA, DSP

3 Description

The TPS7A92 is a low-noise (4.6µV_{RMS}), low-dropout (LDO) voltage regulator capable of sourcing 2A with only 180mV of maximum dropout.

The TPS7A92 output is adjustable with external resistors from 0.8V to 5.2V. The TPS7A92 wide input voltage range supports operation as low as 1.4V and up to 6.5V.

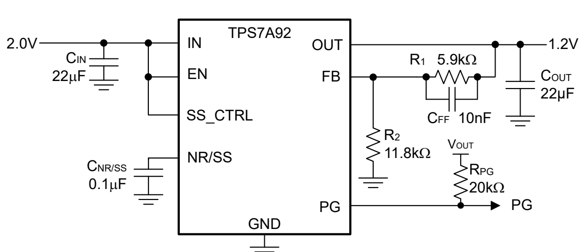
With 1% output voltage accuracy (over line, load, and temperature) and soft-start capabilities to reduce in-rush current, the TPS7A92 is designed for powering sensitive analog low-voltage devices [such as voltage-controlled oscillators (VCOs), analog-to-digital converters (ADCs), digital-to-analog converters (DACs), high-end processors, and field-programmable gate arrays (FPGAs)].

The TPS7A92 is designed to power noise-sensitive components such as components found in high-speed communication, video, medical, or test and measurement applications. The very low 4.6µV_{RMS} output noise and wideband PSRR (40dB at 1MHz) minimizes phase noise and clock jitter. These features maximize performance of clocking devices, ADCs, and DACs.

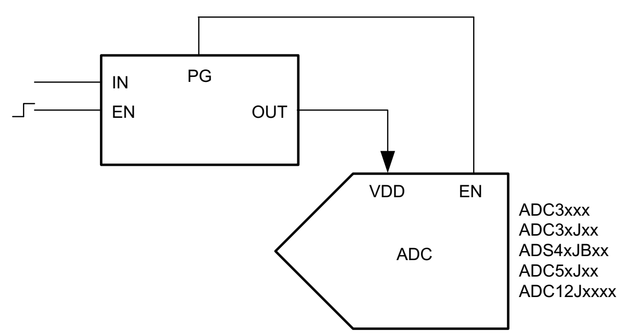
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7A92	DSK (WSON, 10)	2.5mm × 2.5mm

(1) For more information, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit



Typical Application Diagram

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4 Pin Configuration and Functions

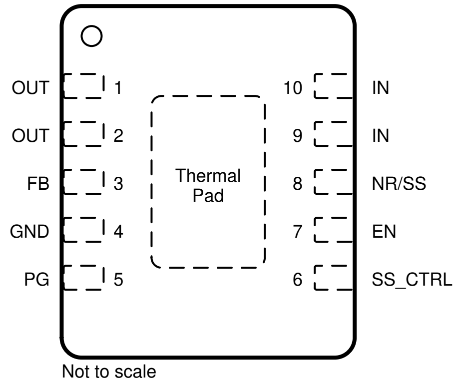


Figure 4-1. DSK Package, 2.5mm × 2.5mm, 10-Pin WSON (Top View)

Table 4-1. Pin Functions

PIN			DESCRIPTION
NAME	NO.	TYPE[(1)]	
EN	7	I	Enable pin. This pin turns the LDO on and off. If $V_{EN} \geq V_{IH(EN)}$, the regulator is enabled. If $V_{EN} \leq V_{IL(EN)}$, the regulator is disabled. The EN pin must connect to IN if the enable function is not used.
FB	3	I	Feedback pin. This pin is the input to the control loop error amplifier and is used to set the output voltage of the device.
GND	4	—	Device GND. Connect to the device thermal pad.
IN	9, 10	I	Input pin. A 10µF or greater input capacitor is required.
NR/SS	8	—	Noise reduction pin. Connect this pin to an external capacitor to bypass the noise generated by the internal band-gap reference. The capacitor reduces the output noise to very low levels and sets the output ramp rate to limit in-rush current.
OUT	1, 2	O	Regulated output. A 22µF or greater capacitor must connect from this pin to GND for stability.
PG	5	O	Open-drain, power-good indicator pin for the LDO output voltage. A from 10kΩ to 100kΩ external pullup resistor is required. This pin can be left floating or connected to GND if not used.
SS_CTRL	6	I	Soft-start control pin. Connect this pin either to GND or IN to change the NR/SS capacitor charging current. If a $C_{NR/SS}$ capacitor is not used, SS_CTRL must connect to GND to avoid output overshoot.
Thermal pad	Pad	—	Connect the thermal pad to the printed circuit board (PCB) ground plane. For an example layout, see Figure 7-5.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range and all voltages with respect to GND (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Voltage	IN, PG, EN	–0.3	7.0	V
	IN, PG, EN (5% duty cycle, pulse duration = 200µs)	–0.3	7.5	
	OUT	–0.3	V_{IN} + 0.3[(2)]	
	SS_CTRL	–0.3	V_{IN} + 0.3[(2)]	
	NR/SS, FB	–0.3	3.6	
Current	OUT	Internally limited		A
	PG (sink current into device)		5	mA
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The absolute maximum rating is V_{IN} + 0.3V or 7.0V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input supply voltage range	1.4	6.5	V
V_{OUT}	Output voltage range	0.8 - 1%	5.2 + 1%	V
I_{OUT}	Output current	0	2	A
C_{IN}	Input capacitor, each input	10		µF
C_{OUT}	Output capacitor[(1)(2)]	22		µF
$C_{NR/SS}$	Noise-reduction capacitor		1	µF
R_{PG}	Power-good pullup resistance	10	100	kΩ
T_J	Junction temperature range	–40	125	°C

(1) Effective output capacitance of 11µF (minimum) is required for stability.
(2) When I_{OUT} ≤ 1A, the C_{OUT} minimum is 10µF and the effective output capacitance of 5µF (minimum) is required for stability.

5.4 Thermal Information

THERMAL METRIC[(1)]		TPS7A92 DSK (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over operating temperature range (T_J = –40°C to +125°C), V_{IN} = 1.4V, $V_{OUT(TARGET)}$ = 0.8V, I_{OUT} = 50mA, V_{EN} = 1.4V, C_{OUT} = 22µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, SS_CTRL = GND, PG pin pulled up to V_{INx} with 100kΩ, and for each channel (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range		1.4		6.5	V
V_{REF}	Reference voltage			0.8		V
V_{UVLO}	Input supply UVLO	V_{IN} rising		1.31	1.39	V
V_{HYS}	V_{UVLO}			290		mV
V_{OUT}	Output voltage range		0.8 – 1.0%		5.2 + 1.0%	V
	Output voltage accuracy[(1)(2)]	0.8V ≤ V_{OUT} ≤ 5V, 5mA ≤ I_{OUT} ≤ 2A	–1.0%		1.0%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	I_{OUT}= 5mA, 1.4V ≤ V_{IN} ≤ 6.5V		0.003		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	5mA ≤ I_{OUT} ≤ 2A		0.03		%/A
V_{DO}	Dropout voltage	V_{IN} ≥ 1.4V, 0.8V ≤ V_{OUT} ≤ 5.0V, I_{OUT} = 2A, V_{FB} = 0.8V – 3%			400	mV
I_{LIM}	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(TARGET)}$, V_{IN} = $V_{OUT(TARGET)}$ + 300mV	2.3	2.6	2.9	A
I_{GND}	GND pin current	Both channels enabled, per channel, V_{IN} = 6.5V, I_{OUT} = 5mA		2.1	3.5	mA
		Both channels enabled, per channel, V_{IN} = 1.4V, I_{OUT} = 2A			4	
I_{SDN}	Shutdown GND pin current	Both channels shutdown, per channel, PGx = (open), V_{IN} = 6.5V, V_{EN} = 0.5V		0.1	15	µA
I_{EN}	EN pin current	V_{IN} = 6.5V, 0V ≤ V_{EN} ≤ 6.5V	–0.2		0.2	µA
$V_{IL(EN)}$	EN pin low-level input voltage (device disabled)		0		0.4	V
$V_{IH(EN)}$	EN pin high-level input voltage (device enabled)		1.1		6.5	V
I_{SS_CTRL}	SS_CTRL pin current	V_{IN} = 6.5V, 0V ≤ V_{SS_CTRL} ≤ 6.5V	–0.2		0.2	µA
$V_{IT(PG)}$	PG pin threshold	For PG transitioning low with falling V_{OUT}, expressed as a percentage of $V_{OUT(TARGET)}$	82%	88.9%	93%	
$V_{hys(PG)}$	PG pin hysteresis	For PG transitioning high with rising V_{OUT}, expressed as a percentage of $V_{OUT(TARGET)}$		1%		
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1mA (current into device)			0.4	V

5.5 Electrical Characteristics (continued)

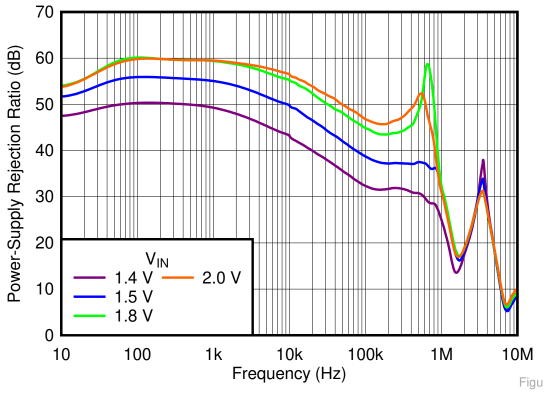
over operating temperature range (T_J = –40°C to +125°C), V_{IN} = 1.4V, $V_{OUT(TARGET)}$ = 0.8V, I_{OUT} = 50mA, V_{EN} = 1.4V, C_{OUT} = 22µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, SS_CTRL = GND, PG pin pulled up to V_{INx} with 100kΩ, and for each channel (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT} > $V_{IT(PG)}$, V_{PG} = 6.5V			1	µA
$I_{NR/SS}$	NR/SS pin charging current	$V_{NR/SS}$ = GND, 1.4V ≤ V_{IN} ≤ 6.5V, V_{SS_CTRL} = GND	4.0	6.2	9.0	µA
		$V_{NR/SS}$ = GND, 1.4V ≤ V_{IN} ≤ 6.5V, V_{SS_CTRL} = V_{IN}	65	100	150	
I_{FB}	FB pin leakage current	V_{IN} = 6.5V, V_{FB} = 0.8V	–100		100	nA
PSRR	Power-supply ripple rejection	f = 500kHz, V_{INx} = 2.0V, V_{OUT} = 1.2V, I_{OUT} = 2A, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF		40		dB
V_n	Output noise voltage	BW = 10Hz to 100kHz, V_{IN} = 1.8V, V_{OUT} = 0.8V, I_{OUT} = 2.0A, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF		4.6		μV_{RMS}
	Noise spectral density	f = 10kHz, V_{IN} = 1.8V, V_{OUT} = 0.8V, I_{OUT} = 2.0A, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF		15		$nV/\sqrt{Hz}$
R_{diss}	Output active discharge resistance	V_{EN} = GND		250		Ω
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		

(1) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
(2) The device is not tested under conditions where V_{IN} > V_{OUT} + 2.5V and I_{OUT} = 2A because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.

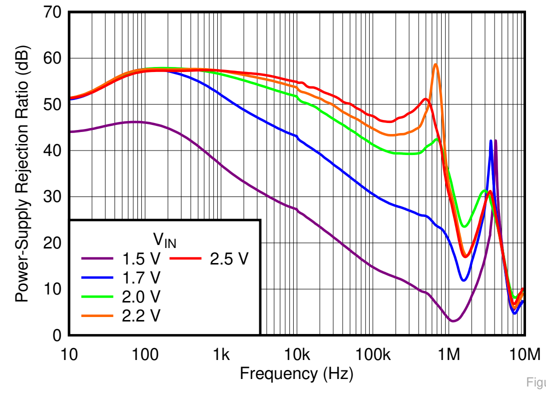
5.6 Typical Characteristics

at T_J = 25°C, 1.4V ≤ V_{IN} ≤ 6.5V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3V, V_{OUT} = 0.8V, SS_CTRL = GND, I_{OUT} = 5mA, V_{EN} = 1.1V, C_{OUT} = 22µF, $C_{NR/SS}$ = C_{FF} = 0nF, PG pin pulled up to V_{OUT} with 100kΩ, and SS_CTRL = GND (unless otherwise noted)



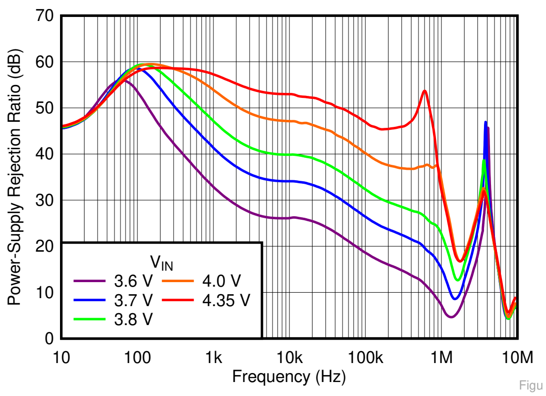
V_{OUT} = 0.8V, I_{OUT} = 2.0A, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10nF

Figure 5-1. PSRR vs Frequency and Input Voltage



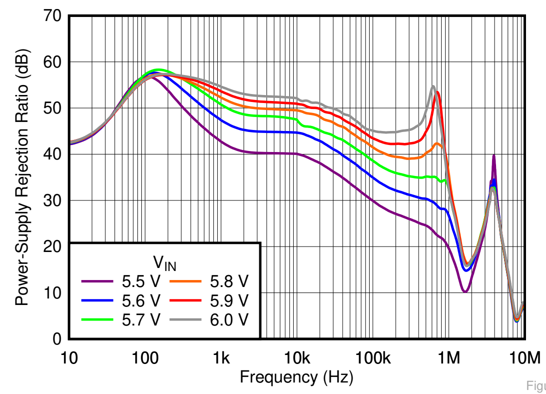
V_{OUT} = 1.2V, I_{OUT} = 2.0A, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10nF

Figure 5-2. PSRR vs Frequency and Input Voltage



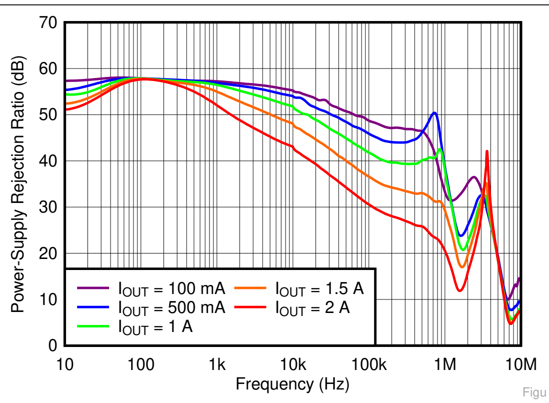
V_{OUT} = 3.3V, I_{OUT} = 2.0A, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10nF

Figure 5-3. PSRR vs Frequency and Input Voltage



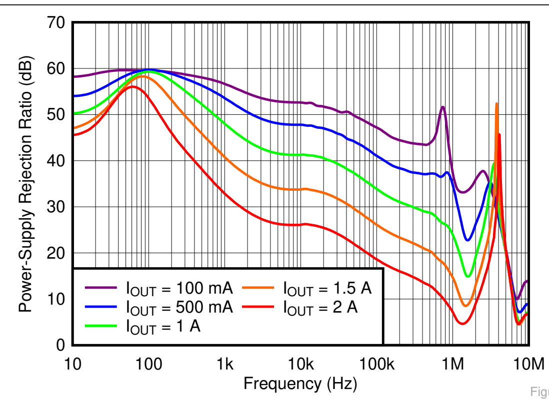
V_{OUT} = 5V, I_{OUT} = 2.0A, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10nF

Figure 5-4. PSRR vs Frequency and Input Voltage



V_{OUT} = 1.2V, V_{IN} = V_{EN} = 1.7V, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10nF

Figure 5-5. PSRR vs Frequency and Output Current

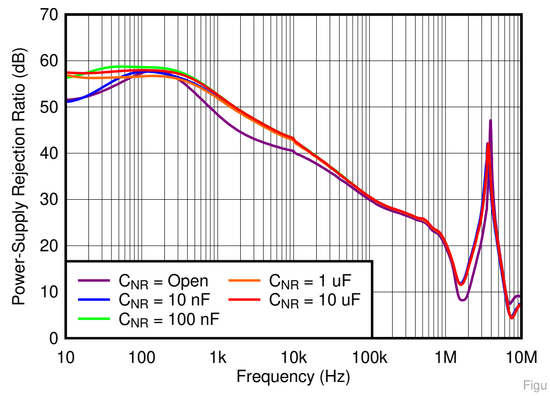


A. V_{OUT} = 3.3V, V_{IN} = V_{EN} = 3.8V, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10nF

Figure 5-6. PSRR vs Frequency and Output Current

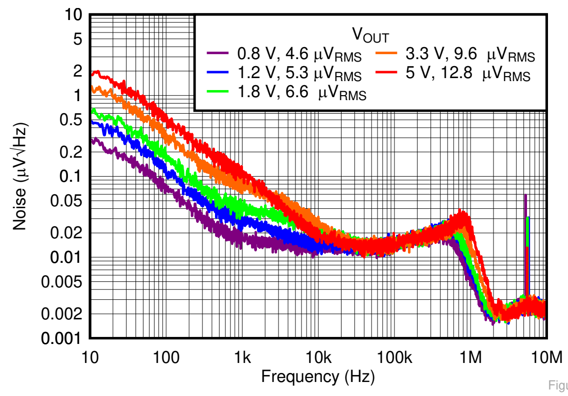
5.6 Typical Characteristics (continued)

at T_J = 25°C, 1.4V ≤ V_{IN} ≤ 6.5V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3V, V_{OUT} = 0.8V, SS_CTRL = GND, I_{OUT} = 5mA, V_{EN} = 1.1V, C_{OUT} = 22µF, $C_{NR/SS}$ = C_{FF} = 0nF, PG pin pulled up to V_{OUT} with 100kΩ, and SS_CTRL = GND (unless otherwise noted)



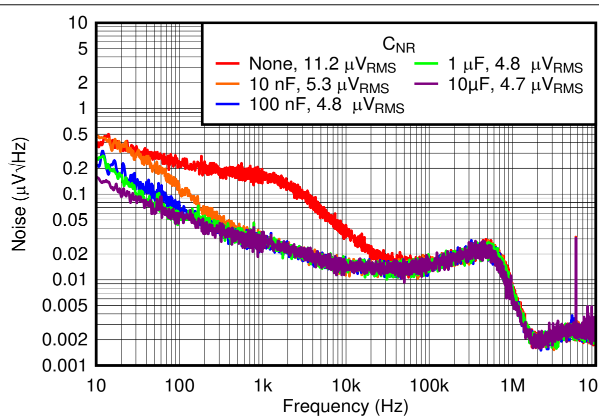
V_{OUT} = 1.2V, V_{IN} = V_{EN} = 1.7V, I_{OUT} = 2.0A, C_{OUT} = 22 µF, C_{FF} = 10 nF

Figure 5-7. PSRR vs Frequency and $C_{NR/SS}$



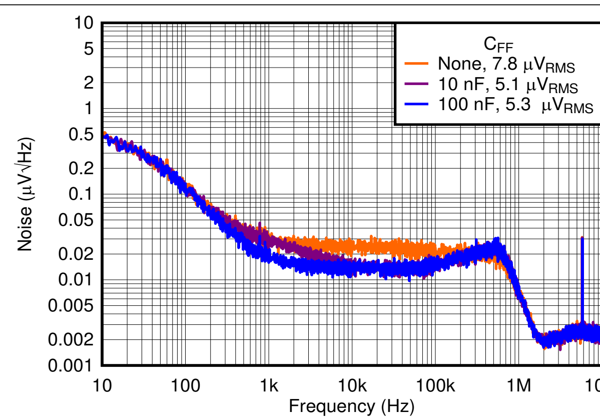
V_{IN} = V_{OUT} + 1.0V, I_{OUT} = 2.0A, C_{IN} = C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10nF, V_{RMS} BW = 10Hz to 100kHz

Figure 5-8. Spectral Noise Density vs Frequency and Output Voltage



V_{IN} = 2.2V, V_{OUT} = 1.2V, I_{OUT} = 2.0A, C_{IN} = C_{OUT} = 22 µF, C_{FF} = 10nF, V_{RMS} BW = 10Hz to 100kHz

Figure 5-9. Spectral Noise Density vs Frequency and $C_{NR/SS}$

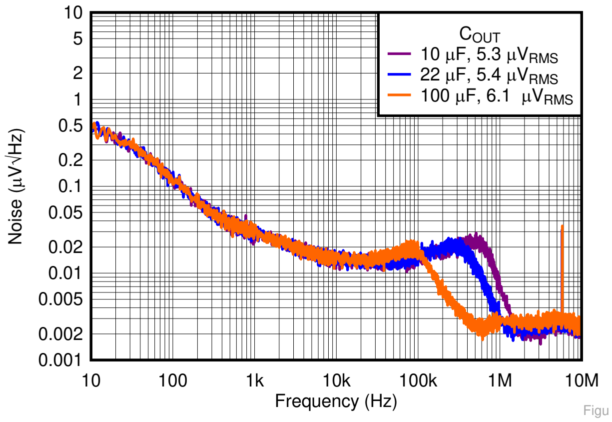


V_{IN} = 2.2V, V_{OUT} = 1.2V, I_{OUT} = 2.0A, C_{IN} = C_{OUT} = 22 µF, $C_{NR/SS}$ = 10nF, V_{RMS} BW = 10Hz to 100kHz

Figure 5-10. Spectral Noise Density vs Frequency and C_{FF}

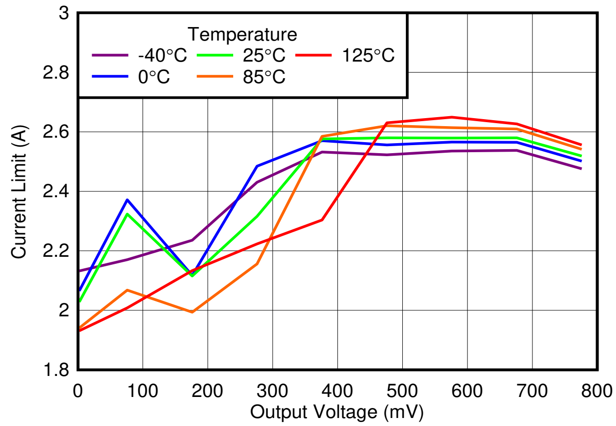
5.6 Typical Characteristics (continued)

at T_J = 25°C, 1.4V ≤ V_{IN} ≤ 6.5V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3V, V_{OUT} = 0.8V, SS_CTRL = GND, I_{OUT} = 5mA, V_{EN} = 1.1V, C_{OUT} = 22µF, $C_{NR/SS}$ = C_{FF} = 0nF, PG pin pulled up to V_{OUT} with 100kΩ, and SS_CTRL = GND (unless otherwise noted)



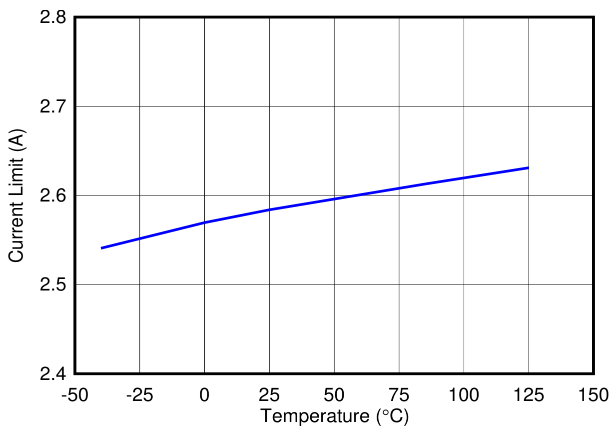
V_{IN} = 2.2V, V_{OUT} = 1.2V, I_{OUT} = 2.0A, C_{IN} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10nF, V_{RMS} BW = 10Hz to 100kHz

Figure 5-11. Spectral Noise Density vs Frequency and C_{OUT}



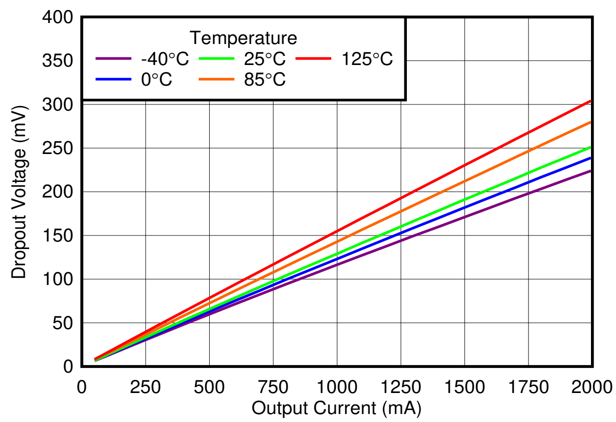
V_{IN} = 1.4V, V_{OUT} = 0.8V

Figure 5-12. Current Limit Foldback



V_{IN} = 1.4V, V_{OUT} = 0.8V

Figure 5-13. Current Limit vs Temperature



V_{IN} = 5.5V

Figure 5-14. Dropout Voltage vs Output Current

5.6 Typical Characteristics (continued)

at T_J = 25°C, 1.4V ≤ V_{IN} ≤ 6.5V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3V, V_{OUT} = 0.8V, SS_CTRL = GND, I_{OUT} = 5mA, V_{EN} = 1.1V, C_{OUT} = 22µF, $C_{NR/SS}$ = C_{FF} = 0nF, PG pin pulled up to V_{OUT} with 100kΩ, and SS_CTRL = GND (unless otherwise noted)

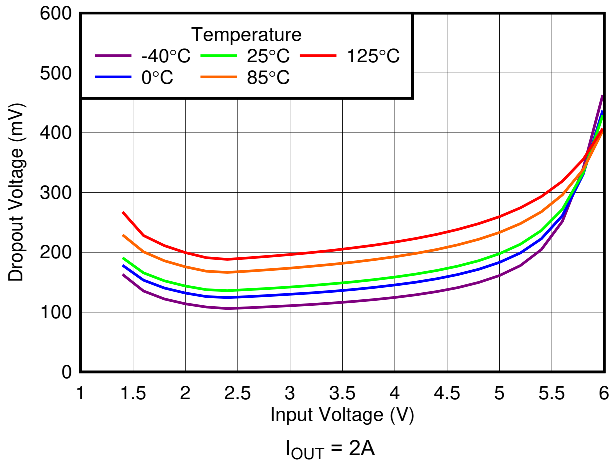


Figure 5-15. Dropout Voltage vs Input Voltage

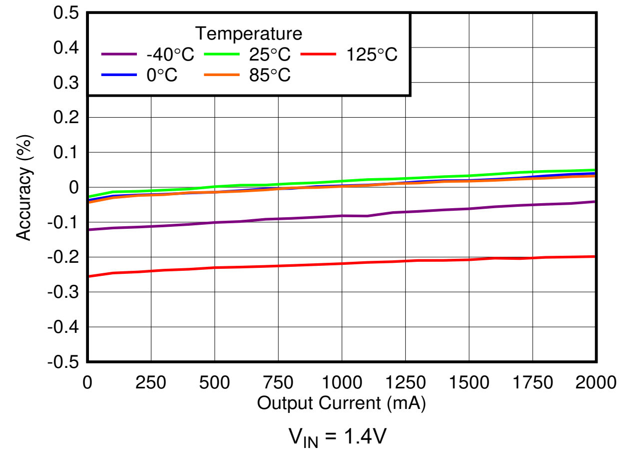


Figure 5-16. Load Regulation

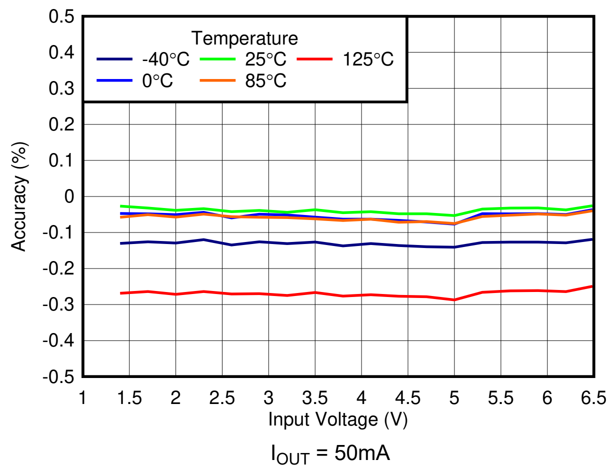


Figure 5-17. Line Regulation

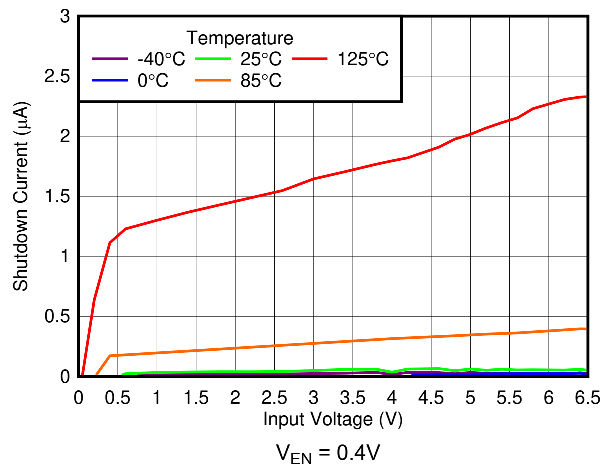


Figure 5-18. Shutdown Current vs Input Voltage

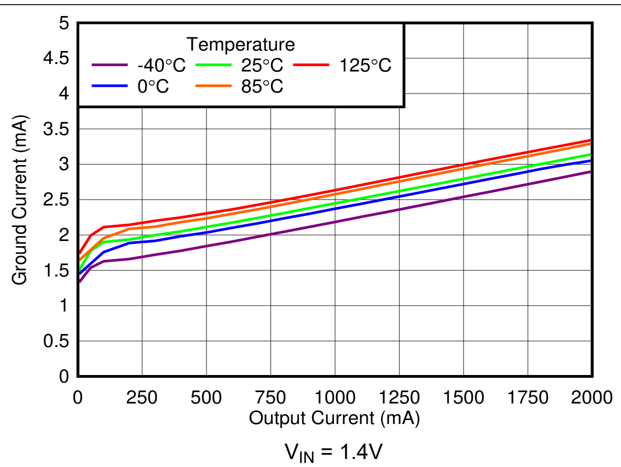


Figure 5-19. Ground Current vs Output Current

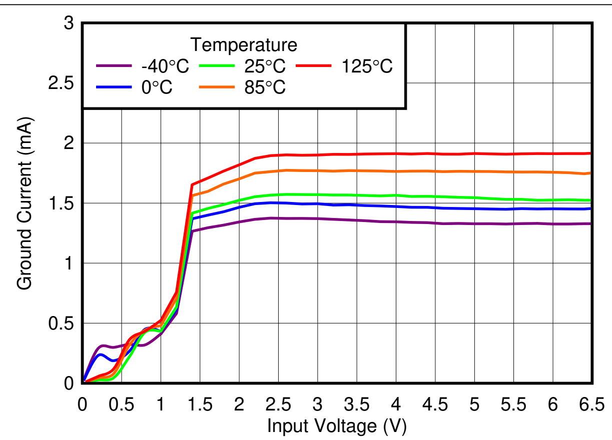


Figure 5-20. Ground Current vs Input Voltage

5.6 Typical Characteristics (continued)

at T_J = 25°C, 1.4V ≤ V_{IN} ≤ 6.5V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3V, V_{OUT} = 0.8V, SS_CTRL = GND, I_{OUT} = 5mA, V_{EN} = 1.1V, C_{OUT} = 22µF, $C_{NR/SS}$ = C_{FF} = 0nF, PG pin pulled up to V_{OUT} with 100kΩ, and SS_CTRL = GND (unless otherwise noted)

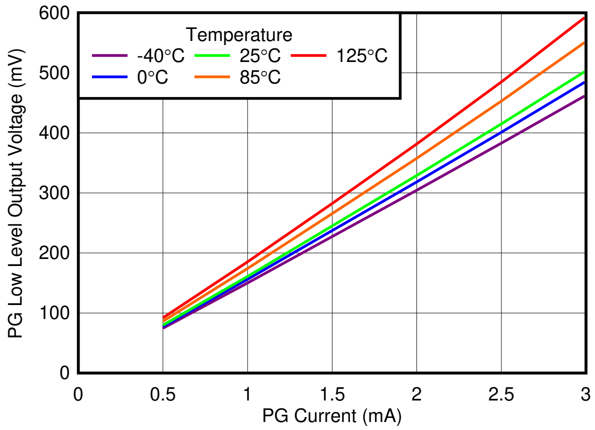


Figure 5-21. PG Low Level Voltage vs PG Current (V_{IN} = 1.4V)

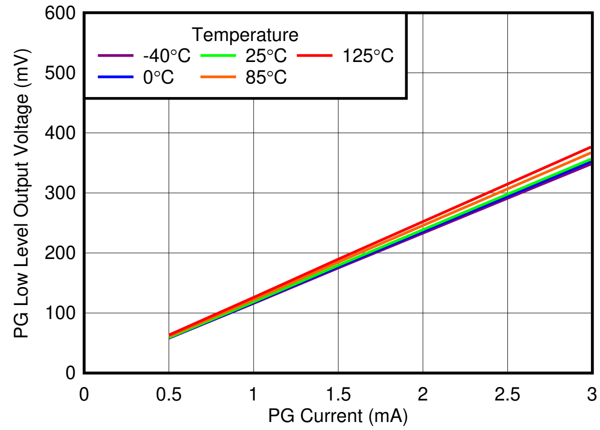


Figure 5-22. PG Low Level Voltage vs PG Current (V_{IN} = 6.5V)

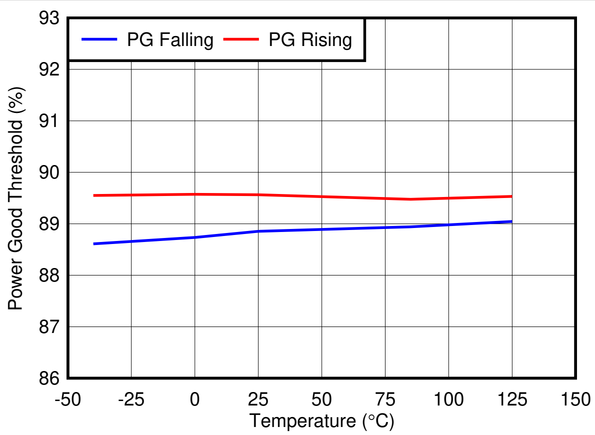
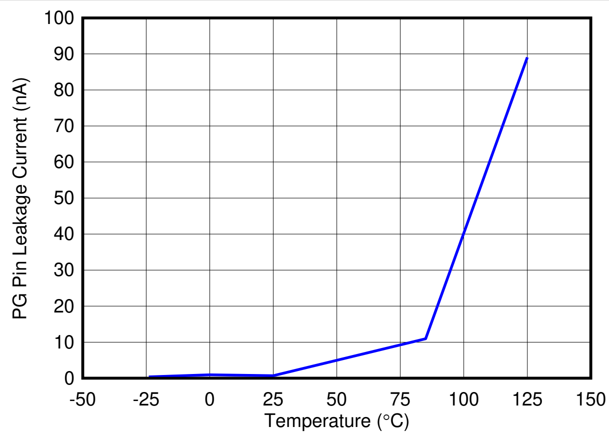


Figure 5-23. PG Threshold vs Temperature



V_{IN} = V_{PG} = 6.5V

Figure 5-24. PG Leakage Current vs Temperature

5.6 Typical Characteristics (continued)

at T_J = 25°C, 1.4V ≤ V_{IN} ≤ 6.5V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3V, V_{OUT} = 0.8V, SS_CTRL = GND, I_{OUT} = 5mA, V_{EN} = 1.1V, C_{OUT} = 22µF, $C_{NR/SS}$ = C_{FF} = 0nF, PG pin pulled up to V_{OUT} with 100kΩ, and SS_CTRL = GND (unless otherwise noted)

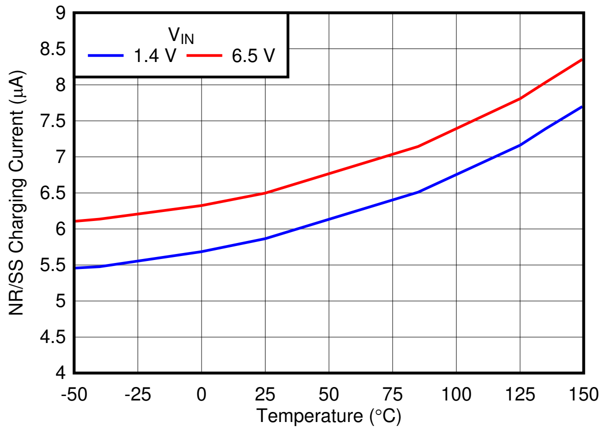


Figure 5-25. Soft-Start Current vs Temperature (SS_CTRL = GND)

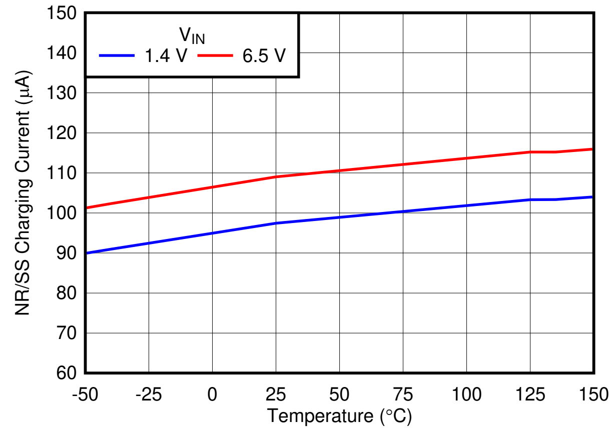


Figure 5-26. Soft-Start Current vs Temperature (SS_CTRL = V_{IN})

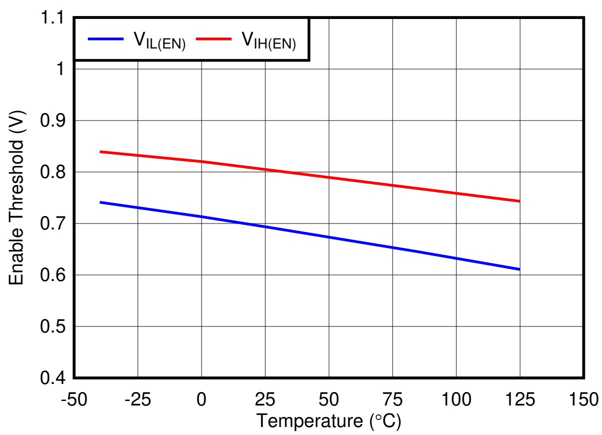


Figure 5-27. Enable Threshold vs Temperature

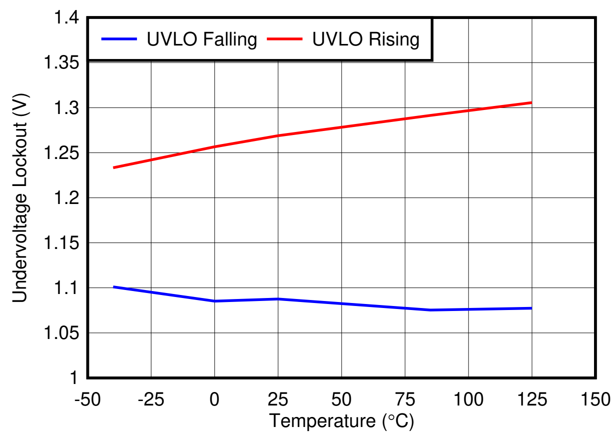
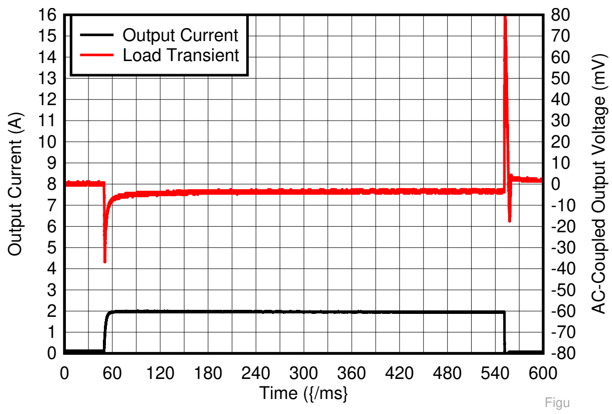


Figure 5-28. Input UVLO Threshold vs Temperature

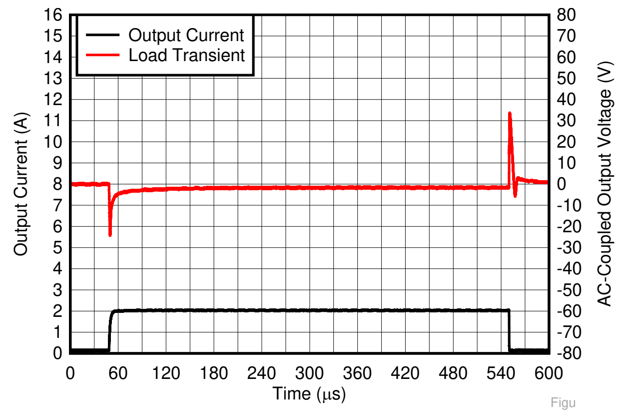
5.6 Typical Characteristics (continued)

at T_J = 25°C, 1.4V ≤ V_{IN} ≤ 6.5V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3V, V_{OUT} = 0.8V, SS_CTRL = GND, I_{OUT} = 5mA, V_{EN} = 1.1V, C_{OUT} = 22µF, $C_{NR/SS}$ = C_{FF} = 0nF, PG pin pulled up to V_{OUT} with 100kΩ, and SS_CTRL = GND (unless otherwise noted)



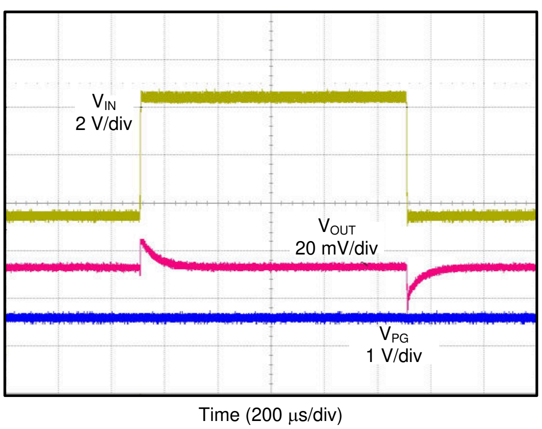
V_{IN} = 1.5V, I_{OUT} = 100mA to 2A to 100mA at 1A/µs, C_{OUT} = 22 µF, V_{PG} = V_{OUT}

Figure 5-29. Load Transient Response (V_{OUT} = 1.2V)



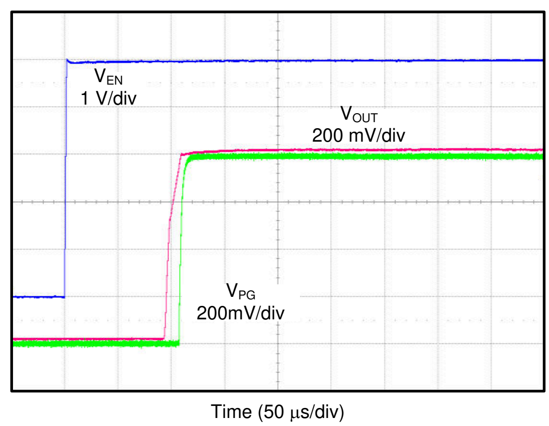
V_{IN} = 5.5V, I_{OUT} = 100mA to 2A to 100mA at 1A/µs, C_{OUT} = 22 µF, V_{PG} = V_{OUT}

Figure 5-30. Load Transient Response (V_{OUT} = 5.0V)



V_{IN} = 1.4V to 6.5V to 1.4V at 2V/µs, V_{OUT} = 0.8V, I_{OUT} = 2A, $C_{NR/SS}$ = C_{FF} = 10nF, V_{PG} = V_{OUT}

Figure 5-31. Line Transient

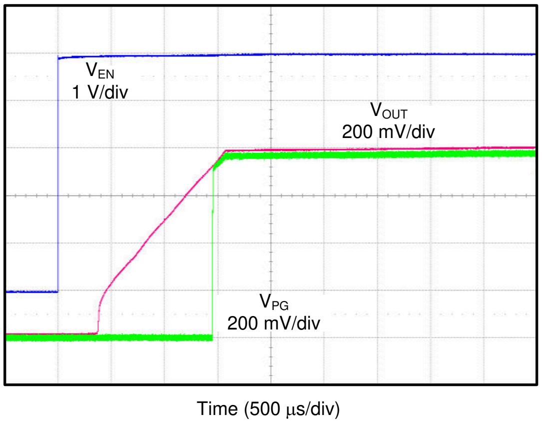


V_{IN} = 1.4V, V_{PG} = V_{OUT}

Figure 5-32. Start-Up (SS_CTRL = GND, $C_{NR/SS}$ = 0 nF)

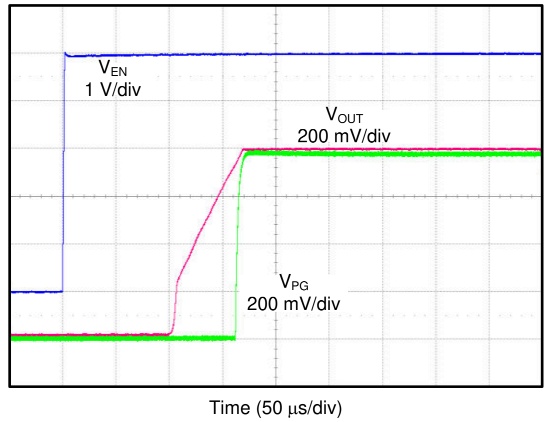
5.6 Typical Characteristics (continued)

at T_J = 25°C, 1.4V ≤ V_{IN} ≤ 6.5V, V_{IN} ≥ $V_{OUT(NOM)}$ + 0.3V, V_{OUT} = 0.8V, SS_CTRL = GND, I_{OUT} = 5mA, V_{EN} = 1.1V, C_{OUT} = 22µF, $C_{NR/SS}$ = C_{FF} = 0nF, PG pin pulled up to V_{OUT} with 100kΩ, and SS_CTRL = GND (unless otherwise noted)



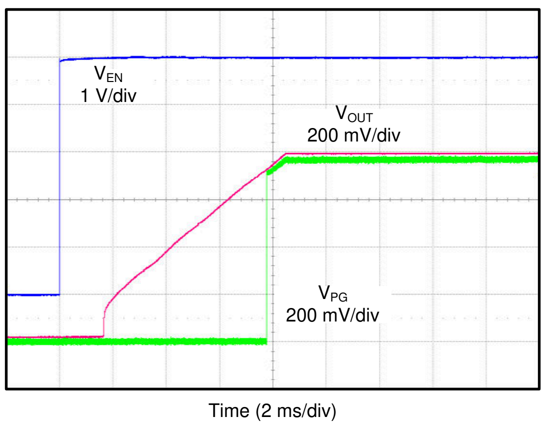
V_{IN} = 1.4V, V_{PG} = V_{OUT}

Figure 5-33. Start-Up (SS_CTRL = GND, $C_{NR/SS}$ = 10 nF)



V_{IN} = 1.4V, V_{PG} = V_{OUT}

Figure 5-34. Start-Up (SS_CTRL = V_{IN}, $C_{NR/SS}$ = 10nF)



V_{IN} = 1.4V, V_{PG} = V_{OUT}

Figure 5-35. Start-Up (SS_CTRL = V_{IN}, $C_{NR/SS}$ = 1 µF)

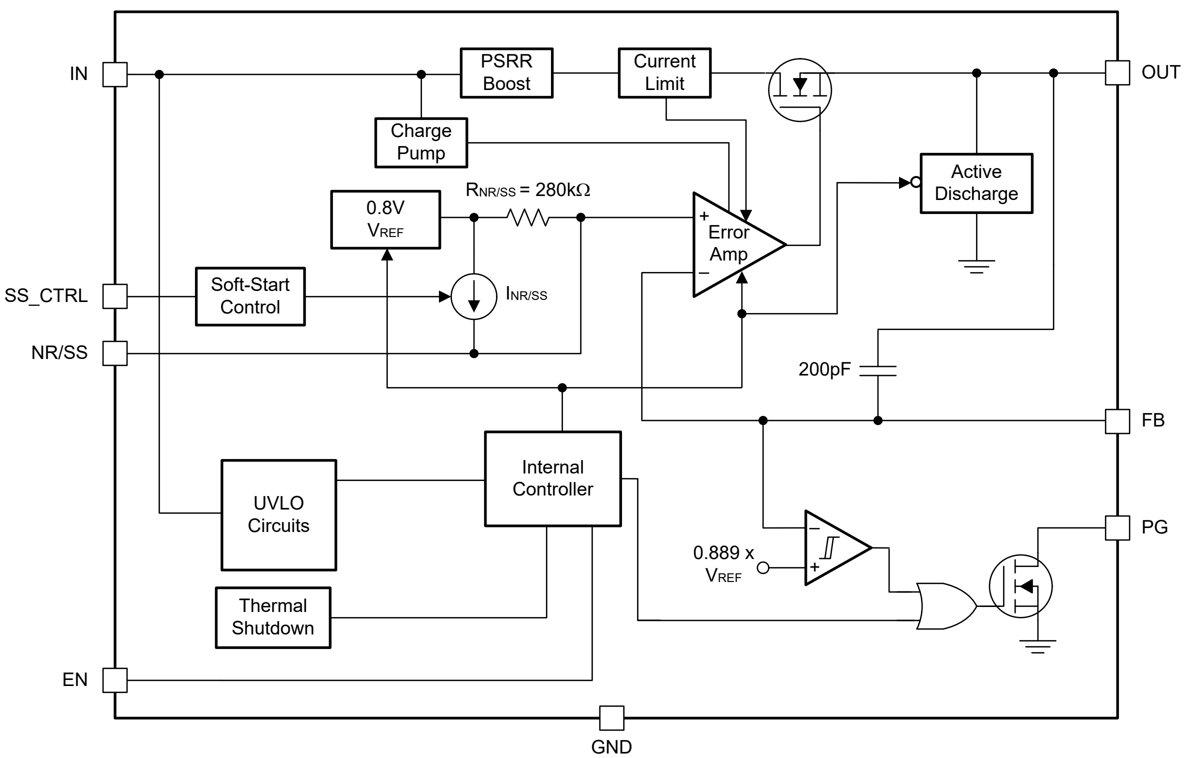
6 Detailed Description

6.1 Overview

The TPS7A92 is a low-noise, high PSRR, low dropout (LDO) regulator capable of sourcing a 2A load with only 400mV of maximum dropout. The TPS7A92 can operate down to a 1.4V input voltage and a 0.8V output voltage. This combination of low-noise, high PSRR, and low dropout voltage makes the device an appropriate LDO to power a multitude of loads from noise-sensitive communication components in high-speed communications applications to high-end microprocessors or field-programmable gate arrays (FPGAs).

As shown in *Functional Block Diagram*, the TPS7A92 linear regulator features a low-noise, 0.8V internal reference that can be filtered externally to obtain even lower output noise. The internal protection circuitry (such as the undervoltage lockout) prevents the device from turning on before the input is high enough to establish accurate regulation. Foldback current limiting is also included, allowing the output to source the rated output current when the output voltage is in regulation but reduces the allowable output current during short-circuit conditions. The internal power-good detection circuit allows down-stream supplies to be sequenced and alerts if the output voltage is below a regulation threshold.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Output Enable

The enable pin (EN) for the TPS7A92 is active high. The output voltage is enabled when the enable pin voltage is greater than $V_{IH(EN)}$ and disabled with the enable pin voltage is less than $V_{IL(EN)}$. If independent control of the output voltage is not needed, then connect the enable pin to the input.

The TPS7A92 has an internal pulldown MOSFET that connects a discharge resistor from V_{OUT} to ground when the device is disabled to actively discharge the output voltage.

6.3.2 Dropout Voltage (V_{DO})

Dropout voltage (V_{DO}) is defined as the V_{IN} – V_{OUT} voltage at the rated current (I_{RATED}) of 2A, where the pass-FET is fully on and in the ohmic region of operation. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain in regulation. If the input falls below the nominal output regulation, then the output follows the input.

The $R_{DS(ON)}$ of the pass-FET determines the dropout voltage. Therefore, if the LDO operates below the rated current, then the V_{DO} for that current scales accordingly. Use Equation 1 to calculate the $R_{DS(ON)}$ for the TPS7A92:

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

6.3.3 Output Voltage Accuracy

Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent. The TPS7A92 features an output voltage accuracy of 1% that includes the errors introduced by the internal reference, load regulation, and line regulation variance across the full range of rated load and line operating conditions overtemperature, as the electrical characteristics specifies. Output voltage accuracy also accounts for all variations between manufacturing lots.

6.3.4 High Power-Supply Rejection Ratio (PSRR)

PSRR is a measure of how well the LDO control loop rejects noise from the input source to make the dc output voltage as noise-free as possible across the frequency spectrum (usually measured from 10Hz to 10MHz). Even though PSRR is a loss in noise signal amplitude, the PSRR curves in typical characteristics are shown as positive values in decibels (dB) for convenience. Equation 2 shows the PSRR calculation as a function of frequency where input noise voltage (V_{IN}[f]) and output noise voltage (V_{OUT}[f]) are the amplitudes of the respective sinusoidal signals.

$$\text{PSRR (dB)} = 20 \log_{10}\left(\frac{V_{IN}(f)}{V_{OUT}(f)}\right) \tag{2}$$

Noise that couples from the input to the internal reference voltage is a primary contributor to reduced PSRR performance. TI recommends using a noise-reduction capacitor to filter unwanted noise from the input voltage, which creates a low-pass filter with an internal resistor to improve PSRR performance at lower frequencies.

LDOs are often employed not only as a step-down regulators, but also to provide exceptionally clean power rails for noise-sensitive components. This usage is especially true for the TPS7A92, which features a remarkable circuit to boost the PSRR from 200kHz to 1MHz. This boost circuit helps further filter switching noise from switching-regulators that operate in this region; see the typical characteristics. To achieve the maximum benefit of this PSRR boost circuit, TI recommends using a capacitor with a minimum impedance in the from 100kHz to 1MHz band.

6.3.5 Low Output Noise

LDO noise is defined as the internally-generated intrinsic noise created by the semiconductor circuits. The TPS7A92 is designed for system applications where minimizing noise on the power-supply rail is critical to system performance. This scenario is the case for phase-locked-loop (PLL)-based clocking circuits where minimum phase noise is all important, or in test and measurement systems where even small power-supply noise fluctuations can distort instantaneous measurement accuracy.

The TPS7A92 includes a low-noise reference establishing minimal output noise in normal operation. Make further improvements by adding a noise-reduction capacitor ($C_{NR/SS}$), a feedforward capacitor (C_{FF}), or a combination of the two. See the *Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)* and *Feed-Forward Capacitor (C_{FF})* sections for additional design information.

For more information on noise and noise measurement, see the *How to Measure LDO Noise* white paper.

6.3.6 Output Soft-Start Control

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after the EN and UVLO thresholds are exceeded. The noise-reduction capacitor ($C_{NR/SS}$) serves a dual purpose of both governing output noise reduction and programming the soft start ramp during turn-on. Larger values for the noise-reduction capacitors decrease the noise but also result in a slower output turn-on ramp rate.

The TPS7A92 features an SS_CTRL pin. When the SS_CTRL pin is grounded, the charging current for the NR/SS pin is 6.2µA (typical); when this pin connects to IN, the charging current for the NR/SS pin is increased to 100µA (typical). The higher current allows the use of a much larger noise-reduction capacitor and maintains a reasonable startup time. Figure 6-1 shows a simplified block diagram of the soft-start circuit. The switch SW is opened to turn off the $I_{NR/SS}$ current source after V_{FB} reaches approximately 97% of V_{REF}. The final 3% of $V_{NR/SS}$ is charged through the noise-reduction resistor (R_{NR}), which creates an RC delay. R_{NR} is approximately 280kΩ and applications that require the highest accuracy when using a large value $C_{NR/SS}$ must take this RC delay into account.

If a noise-reduction capacitor is not used on the NR/SS pin, tying the SS_CTRL pin to the IN pin can result in output voltage overshoot of approximately 10%. This overshoot is minimized by either connecting the SS_CTRL pin to GND or using a capacitor on the NR/SS pin.

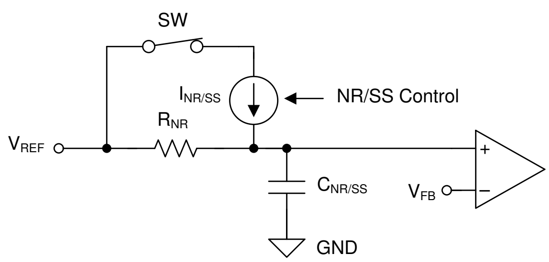


Figure 6-1. Simplified Soft-Start Circuit

6.3.7 Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the feedback pin voltage falls below the PG threshold voltage ($V_{IT(PG)}$), the PG pin open-drain output engages and pulls the PG pin close to GND. When the feedback voltage exceeds the $V_{IT(PG)}$ threshold by an amount greater than $V_{HYS(PG)}$, the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices. TI recommends using a pullup resistor from 10kΩ to 100kΩ. TI also recommends using an external reset device such as the TPS3890 in applications where high accuracy is needed or in applications where microprocessor induced resets are needed.

When using a feed-forward capacitor (C_{FF}), the time constant for the LDO startup is increased whereas the power-good output time constant stays the same, possibly resulting in an invalid status of the power-good output. To avoid this issue and to receive a valid PG output, make sure that the time constant of both the LDO startup and the power-good output are matching, which can be done by adding a capacitor in parallel with the power-good pullup resistor. See also the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note .

The state of PG is only valid when the device is operating above the minimum input voltage of the device and power-good is asserted regardless of the output voltage state when the input voltage falls below the UVLO threshold minus the UVLO hysteresis. Figure 6-2 shows a simplified block diagram of the power-good circuit. When the input voltage falls below approximately 0.8V, there is not enough gate drive voltage to keep the open-drain, power-good device turned on and the power-good output is pulled high. Connecting the power-good pullup resistor to the output voltage can help minimize this effect.

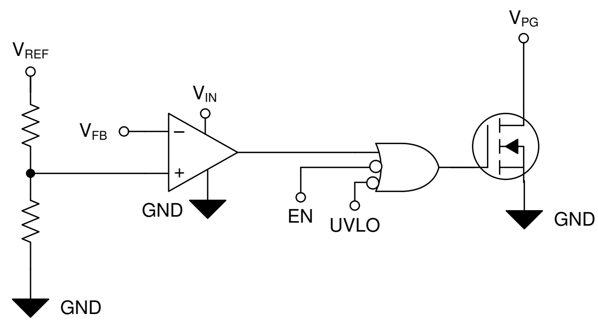


Figure 6-2. Simplified PG Circuit

6.3.8 Internal Protection Circuitry

6.3.8.1 Undervoltage Lockout (UVLO)

The TPS7A92 has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has approximately 290mV of hysteresis.

The UVLO circuit responds quickly to glitches on V_{IN} and disables the output of the device if this rail starts to collapse too quickly. Use an input capacitor that is large enough to slow input transients to less then two volts per microsecond.

6.3.8.2 Internal Current Limit (I_{CL})

The internal current-limit circuit is used to protect the LDO against transient high-load current faults or shorting events. The LDO is not designed to operate in current limit under steady-state conditions. During an overcurrent event where the output voltage is pulled 10% below the regulated output voltage, the LDO sources a constant current as specified in the electrical characteristics table. When the output voltage falls, the amount of output current is reduced to better protect the device. During a hard short-circuit event, the current is reduced to approximately 2.2A. See the current limit foldback in the typical characteristics section for more information about the current-limit foldback behavior. However, when a current-limit event occurs, the LDO begins to heat up because of the increase in power dissipation. The increase in heat can trigger the integrated thermal shutdown protection circuit.

6.3.8.3 Thermal Protection

The TPS7A92 contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. Thermal shut down occurs when the thermal junction temperature (T_J) of the pass-FET exceeds 160°C (typical). Thermal shutdown hysteresis assures that the LDO again resets (turns on) when the temperature falls to 140°C (typical). The thermal time-constant of the semiconductor die is fairly short, and thus the output turns on and off at a high rate when thermal shutdown is reached until power dissipation is reduced.

The internal protection circuitry of the TPS7A92 is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A92 into thermal shutdown degrades device reliability.

For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the thermal margin in a given layout, increase the ambient temperature until the thermal protection shutdown is triggered using worst-case load and highest input voltage conditions. For good reliability, thermal shutdown must occur at least 35°C above the maximum expected ambient temperature condition for the application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

6.4 Device Functional Modes

Table 6-1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 6-1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal(1)	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Dropout(1)	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Disabled(2)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{IL(EN)}$	—	$T_J > T_{sd}$

(1) All table conditions must be met.
(2) The device is disabled when any condition is met.

6.4.1 Normal Operation

The device regulates to the nominal output voltage when all of the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased below the enable falling threshold
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{sd}$)

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, right after being in a normal regulation state, but *not* during startup), the pass-FET is driven as hard as possible. When the input voltage returns to $V_{IN} \geq V_{OUT(NOM)} + V_{DO}$, V_{OUT} can overshoot for a short period of time if the input voltage slew rate is greater than 0.1V/µs.

6.4.3 Disabled

The output of the TPS7A92 can be shutdown by forcing the enable pin below 0.4V. When disabled, the pass device is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal resistor from the output to ground.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS7A92 is a linear voltage regulator operating from 1.4V to 6.5V on the input, and regulates voltages from 0.8V to 5.0V within 1% accuracy and a 2A maximum output current. Efficiency is defined by the ratio of output voltage to input voltage because the TPS7A92 is a linear voltage regulator. To achieve high efficiency, the dropout voltage (V_{IN} – V_{OUT}) must be as small as possible, thus requiring a very low dropout LDO. Successfully implementing an LDO in an application depends on the application requirements. This section describes key device features and how to best implement the features to achieve a reliable design.

7.1.1 Adjustable Output

As Figure 7-1 shows, the output voltage of the TPS7A92 can be adjusted from 0.8V to 5.2V by using a resistor divider network.

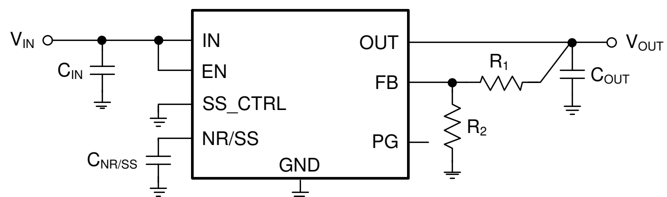


Figure 7-1. Adjustable Operation

Use Equation 3 to calculate R_1 and R_2 for any output voltage range. This resistive network must provide a current greater than or equal to 5µA for optimum noise performance.

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}} - 1\right) \quad (3)$$

where

$$\frac{|\,V_{REF(max)}\,|}{R_2} > 5\ \mu A \quad (4)$$

If greater voltage accuracy is required, take into account the output voltage offset contribution resulting from the feedback pin current (I_{FB}) and use 0.1%-tolerance resistors.

Table 7-1 lists the resistor combination required to achieve a few of the most common rails using commercially-available, 0.1%-tolerance resistors to maximize nominal voltage accuracy and also abiding to the formula given in Equation 3 and Equation 4.

Table 7-1. Recommended Feedback Resistor Values

$V_{OUT(TARGET)}$ (V)	FEEDBACK RESISTOR VALUES (1)		CALCULATED OUTPUT VOLTAGE (V)
	R_1 (kΩ)	R_2 (kΩ)	
0.8	Short	Open	0.800
1.00	2.55	10.2	1.000
1.20	5.9	11.8	1.200
1.50	9.31	10.7	1.496

Table 7-1. Recommended Feedback Resistor Values (continued)

$V_{OUT(TARGET)}$ (V)	FEEDBACK RESISTOR VALUES [(1)]		CALCULATED OUTPUT VOLTAGE (V)
	R_1 (kΩ)	R_2 (kΩ)	
1.80	1.87	1.5	1.797
1.90	15.8	11.5	1.899
2.50	2.43	1.15	2.490
3.00	3.16	1.15	2.998
3.30	3.57	1.15	3.283
5.00	10.5	2	5.00

(1) R_1 connects from OUT to FB; R_2 connects from FB to GND; see Figure 7-1.

7.1.2 Start-Up

7.1.2.1 Enable (EN) and Undervoltage Lockout (UVLO)

The TPS7A92 only turns on when EN and UVLO are above the respective voltage thresholds. The TPS7A92 has an independent UVLO circuit that monitors the input voltage to allow a controlled and consistent turn on and off. The UVLO has approximately 290mV of hysteresis to prevent the device from turning off if the input drops during turn on. The EN signal allows independent logic-level turn-on and shutdown of the LDO when the input voltage is present. Connecting EN directly to IN is recommended if independent turn-on is not needed.

The TPS7A92 has an internal pulldown MOSFET that connects a discharge resistor from V_{OUT} to ground when the device is disabled to actively discharge the output voltage.

7.1.2.2 Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

The $C_{NR/SS}$ capacitor serves a dual purpose of both reducing output noise and setting the soft-start ramp during turn-on.

7.1.2.2.1 Noise Reduction

For low-noise applications, the $C_{NR/SS}$ capacitor forms an RC filter for filtering output noise that is otherwise amplified by the control loop. For low-noise applications, a $C_{NR/SS}$ of from 10nF to 10µF is recommended. Larger values for $C_{NR/SS}$ can be used; however, above 1µF there is little benefit in lowering the output voltage noise for frequencies above 10Hz.

7.1.2.2.2 Soft-Start and In-Rush Current

Soft-start refers to the gradual ramp-up characteristic of the output voltage after the EN and UVLO thresholds are exceeded. Reducing how quickly the output voltage increases during startup also reduces the amount of current needed to charge the output capacitor, referred to as in-rush current. In-rush current is defined as the current going into the LDO during start-up. In-rush current consists of the load current, the current used to charge the output capacitor, and the ground pin current (that contributes very little to in-rush current). This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, use Equation 5 to estimate in-rush current:

$$I_{OUT}(t) = \left(\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right) + \left(\frac{V_{OUT}(t)}{R_{LOAD}}\right) \tag{5}$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t)$ / dt is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

The TPS7A92 features a monotonic, voltage-controlled soft-start that is set with an external capacitor ($C_{NR/SS}$). This soft-start helps reduce in-rush current, minimizing load transients to the input power bus that can cause potential start-up initialization problems when powering FPGAs, digital signal processors (DSPs), or other high current loads.

To achieve a monotonic start-up, the TPS7A92 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds approximately 97% of the internal reference. The final 3% of $V_{NR/SS}$ is charged through the noise-reduction resistor (R_{NR}), creating an RC delay. R_{NR} is approximately 280kΩ and applications that require the highest accuracy when using a large value $C_{NR/SS}$ must take this RC delay into account.

The soft-start ramp time depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference (V_{REF}). Use Equation 6 to calculate the approximate soft-start ramp time (t_{SS}):

$$t_{SS} = (V_{REF} \times C_{NR/SS}) / I_{NR/SS} \tag{6}$$

The value for $I_{NR/SS}$ is determined by the state of the SS_CTRL pin. When the SS_CTRL pin is connected to GND, the typical value for the $I_{NR/SS}$ current is 6.2µA. Connecting the SS_CTRL pin to IN increases the typical soft-start charging current to 100µA. The larger charging current for $I_{NR/SS}$ is useful if shorter start-up times are needed (such as when using a large noise-reduction capacitor).

7.1.3 Capacitor Recommendation

The TPS7A92 is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin. Multilayer ceramic capacitors are the industry standard for these types of applications and are recommended, but must be used with good understanding of the limitations. Ceramic capacitors that employ X7R-rated, X5R-rated, and COG-rated dielectric materials provide relatively good capacitive stability across temperature. The use of Y5V-rated capacitors is discouraged precisely because the capacitance varies so widely. In all cases, ceramic capacitors vary a great deal with operating voltage and temperature and the design engineer must be aware of these characteristics. As a general guideline, ceramic capacitors are recommended to be derated by 50%. The input and output capacitors recommended herein account for a capacitance derating of 50%.

7.1.3.1 Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The TPS7A92 is designed and characterized for operation with ceramic capacitors of 10µF or greater at the input and 22µF or greater at the output. Locate the input and output capacitors as near as practical to the input and output pins to minimize the trace inductance from the capacitor to the device.

Attention must be given to the input capacitance to minimize transient input droop during startup and load current steps. Simply using very large ceramic input capacitances can cause unwanted ringing at the output if the input capacitor (in combination with the wire-lead inductance) creates a high-Q peaking effect during transients, which is why short, well-designed interconnect traces to the upstream supply are needed to minimize ringing. Damping of unwanted ringing can be accomplished by using a tantalum capacitor, with a few hundred milliohms of ESR, in parallel with the ceramic input capacitor. The UVLO circuit responds quickly to glitches on V_{IN} and disables the output of the device if this rail starts to collapse too quickly. Use an input capacitor that is large enough to slow input transients to less then two volts per microsecond.

7.1.3.1.1 Load-Step Transient Response

The load-step transient response is the output voltage response by the LDO to a step change in load current. The depth of charge depletion immediately after the load step is directly proportional to the amount of output capacitance. However, although larger output capacitances decrease any voltage dip or peak occurring during a load step, the control-loop bandwidth is also decreased, thereby slowing the response time.

The LDO cannot sink charge, therefore when the output load is removed or greatly reduced, the control loop must turn off the pass-FET and wait for any excess charge to deplete.

7.1.3.2 Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}), from the FB pin to the OUT pin is not required to achieve stability, a 10nF, feed-forward capacitor improves the noise and PSRR performance. When using a higher capacitance C_{FF}, the startup time is longer and the power-good signal can incorrectly indicate that the output voltage has settled. For a detailed description, see the application note *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*.

7.1.4 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

To a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 7 calculates P_D:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{7}$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage necessary for proper output regulation.

The primary heat conduction path for the DSK package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to Equation 8, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (\theta_{JA} \times P_D) \tag{8}$$

Unfortunately, the thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the thermal information table is determined by the JEDEC standard, PCB, and copper-spreading area and is only used as a relative measure of package thermal performance.

7.1.5 Estimating Junction Temperature

The JEDEC standard recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 9 and are given in the thermal information table.

$$\begin{aligned} \Psi_{JT}&: T_J = T_T + \Psi_{JT} \times P_D \\ \Psi_{JB}&: T_J = T_B + \Psi_{JB} \times P_D \end{aligned} \tag{9}$$

where:

- P_D is the power dissipated as explained in Equation 7
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For a more detailed discussion on how to use thermal metrics, see the application note *Semiconductor and IC Package Thermal Metrics*.

7.2 Typical Application

This section describes the implementation of the TPS7A92 to regulate from a 2V input voltage to a 1.2V output voltage for noise-sensitive loads. Figure 7-2 shows the schematic for this application circuit.

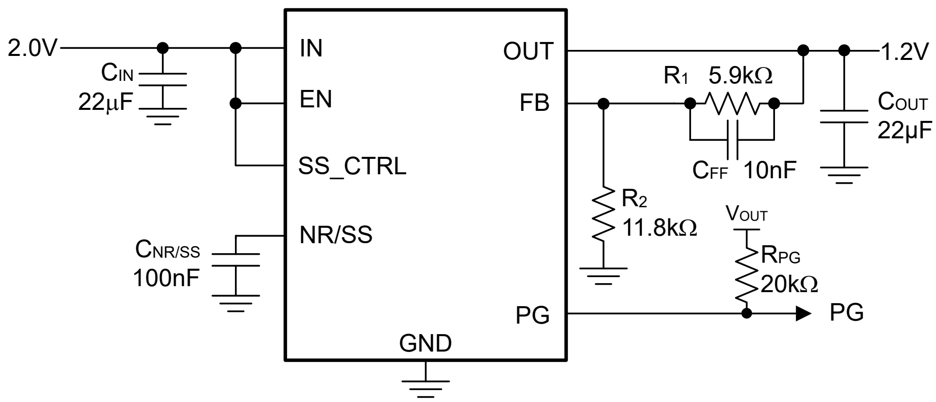


Figure 7-2. Application Example

7.2.1 Design Requirements

For the design example shown in Figure 7-2, use the parameters listed in Table 7-2 as the input parameters.

Table 7-2. Design Parameters

PARAMETER	APPLICATION REQUIREMENTS	DESIGN RESULTS
Input voltages (V_{IN})	2V, ±3%, provided by the DC-DC converter switching at 700kHz	1.4V to 6.5V
Maximum ambient operating temperature	55°C	124°C junction temperature
Output voltages (V_{OUT})	1.2V, ±1%	1.2V, ±1%
Output currents (I_{OUT})	1.5A (maximum), 50mA (minimum)	2.0A (maximum), 5mA (minimum)
RMS noise	< 5µV_{RMS}, bandwidth = 10Hz to 100kHz	4.8µV_{RMS}, bandwidth = 10Hz to 100kHz
PSRR at	> 40dB	42dB
Start-up time	< 2ms	800µs (typical) 1.48µs (maximum)

7.2.2 Detailed Design Procedure

Set the output voltage to 1.2V by selecting the correct values for R_1 and R_2; see Equation 3.

Input and output capacitors are selected in accordance with Capacitor Recommendation. Ceramic capacitances of 22µF for both input and output help balance the charge needed during start-up when charging the output capacitor, thus reducing the input voltage drop.

To satisfy the required start-up time (t_{SS}) and still maintain low-noise performance, a 0.1µF $C_{NR/SS}$ is selected for with SS_CTRL connected to V_{IN}. Equation 10 calculates this value. Using $I_{NR/SS(MAX)}$ and the smallest $C_{NR/SS}$ capacitance resulting from manufacturing variance (often ±20%) provides the fastest start-up time, whereas using $I_{NR/SS(MIN)}$ and the largest $C_{NR/SS}$ capacitance resulting from manufacturing variance provides the slowest start-up time.

$$t_{SS} = (V_{REF} \times C_{NR/SS}) / I_{NR/SS} \quad (10)$$

With a 1.5A maximum load, the internal power dissipation is 1.2W, corresponding to a 91°C junction temperature rise. With a 55°C maximum ambient temperature, the junction temperature is at 124°C on the JEDEC standard high-K board. Connecting the thermal pad to more metal on the PCB than the standard JEDEC high-K board decreases the thermal resistance to the board and causes a decrease in the junction temperature of the device for a given power dissipation.. To minimize noise, use a feed-forward capacitance (C_{FF}) of 10nF.

See Layout for an example of how to layout the TPS7A92 to achieve best PSRR and noise.

7.2.3 Application Curves

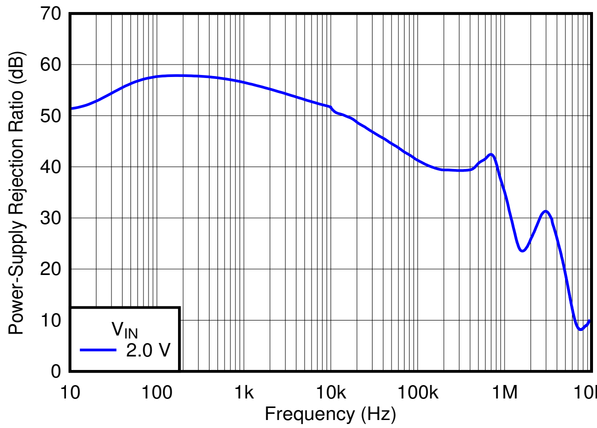


Figure 7-3. PSRR vs Frequency

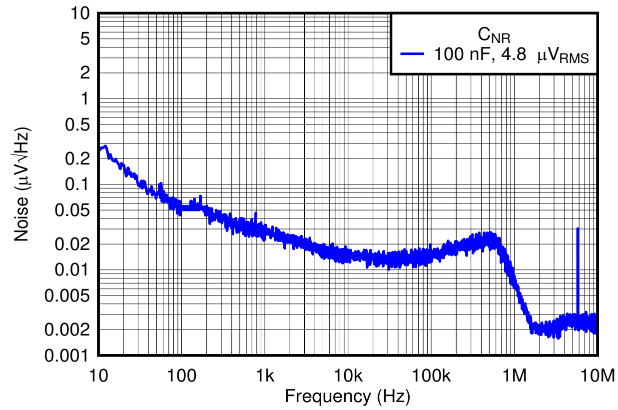


Figure 7-4. Output Noise vs Frequency

7.3 Power Supply Recommendations

The input of the TPS7A92 is designed to operate from an input voltage range from 1.4V to 6.5V and with an input capacitor of 10µF. The input voltage range must provide adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors can be used to improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

General guidelines for linear regulator designs are to place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance.

7.4.1.1 Board Layout

To maximize the ac performance of the TPS7A92, following the layout example shown in Figure 7-5 is recommended. This layout isolates the analog ground (AGND) from the noisy power ground. Components that must connect to the quiet analog ground are the noise-reduction capacitor ($C_{NR/SS}$) and the lower feedback resistor (R_2). These components must have a separate connection back to the thermal pad of the device for peak output noise performance. Connect the GND pin directly to the thermal pad and not to any external plane.

To maximize the output voltage accuracy, the connection from the output voltage back to top output divider resistors (R_1) must be made as close as possible to the load. This method of connecting the feedback trace eliminates the voltage drop from the device output to the load.

To improve thermal performance, use an array of thermal vias to connect the thermal pad to the ground planes. Larger ground planes improve the thermal performance of the device and lowering the operating temperature of the device.

7.4.2 Layout Example

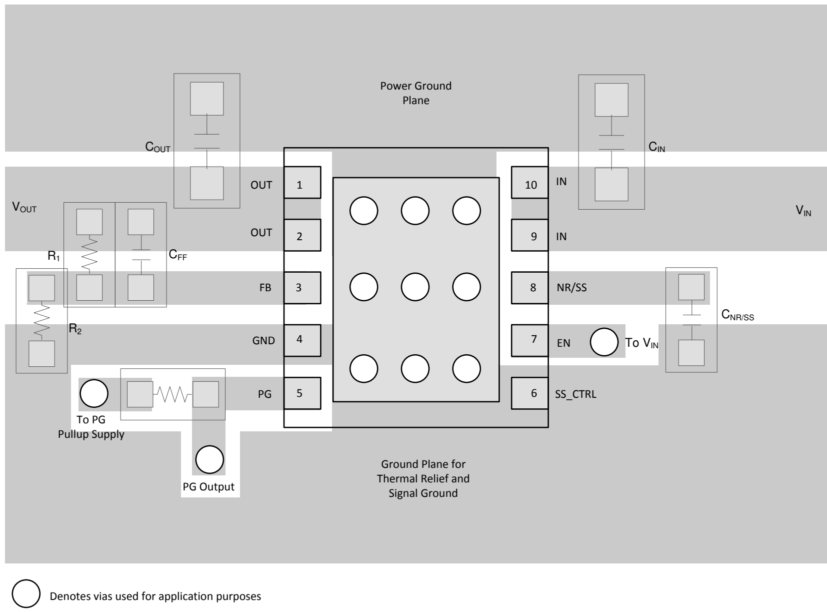


Figure 7-5. TPS7A92 Example Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Spice Models

Computer simulation of circuit performance using spice is often useful when analyzing the performance of analog circuits and systems. A spice model for the TPS7A92 is available through the TPS7A92 product folder under simulation models.

8.1.2 Device Nomenclature

Table 8-1. Ordering Information

PRODUCT#none#	DESCRIPTION
TPS7A92xx**YYYZ**	**YYY** is the package designator. **XX** represents the output voltage. 01 is the adjustable output version. **Z** is the package quantity.

8.2 Documentation Support

8.2.1 Related Documentation

Texas Instruments, *TPS37xx Dual-Channel, Low-Power, High-Accuracy Voltage Detectors* data sheet

Texas Instruments, *TPS7A88 Evaluation Module* user's guide

Texas Instruments, *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application report

Texas Instruments, *How to Measure LDO Noise* white paper

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2019) to Revision C (September 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated *Thermal Information* section	5

Changes from Revision A (April 2018) to Revision B (January 2019)	Page
• Added footnotes to *Recommended Operating Conditions* table	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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