# TPS7A80 Low-Noise, Wide-Bandwidth, High PSRR, Low-Dropout 1-A Linear Regulator

## 1 Features

- Low-Dropout 1-A Regulator With Enable
- Adjustable Output Voltages: 0.8 V to 6 V
- Fixed Output Voltages: 0.8 V to 6 V
- Wide-Bandwidth High PSRR:
  - 63 dB at 1 kHz
  - 57 dB at 100 kHz
  - 38 dB at 1 MHz
- Low Noise: (14 × $V_{OUT}$ ) $\mu V_{RMS}$ Typical (100 Hz to 100 kHz)
- Stable with a 4.7-µF Ceramic Capacitor
- Excellent Load/Line Transient Response
- 3% Overall Accuracy (Over Load/Line/Temp)
- Overcurrent and Overtemperature Protection
- Very Low Dropout: 170 mV Typical at 1 A
- 3-mm × 3-mm VSON-8 DRB Package

## 2 Applications

- Telecom Infrastructure
- Audio
- High-Speed I/F (PLL/VCO)

## 3 Description

The TPS7A80 family of low-dropout linear regulators (LDOs) offer very high power-supply ripple rejection (PSRR) at the output. This LDO family uses an advanced BiCMOS process and a PMOSFET pass device to achieve very low noise, excellent transient response, and excellent PSRR performance.

The TPS7A80 family is stable with a 4.7-µF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations.

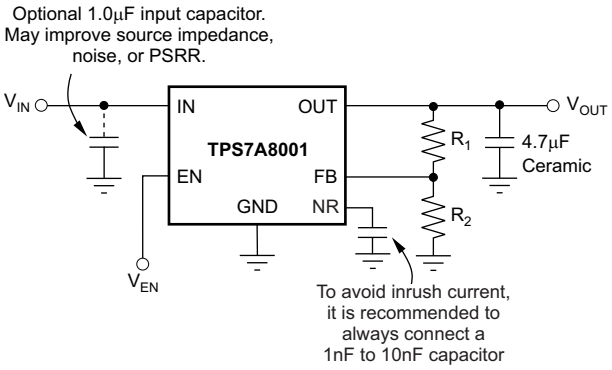
This family is fully specified over the temperature range of $T_J$ = –40°C to +125°C, and is offered in a 3-mm × 3-mm, VSON-8 package with a thermal pad.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS7A80 | VSON (8) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.

### Typical Application Diagram




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision I (August 2015) to Revision J** — **Page**

- Added new fixed voltage devices and associated content to data sheet ... 1
- Changed device name to generic part number to show new fixed voltage device options ... 1
- Added SNS pin and description to *Pin Functions* table ... 4
- Changed $T_A$ to $T_J$ in *Recommended Operating Conditions* table ... 5
- Added fixed-voltage-version values to *Electrical Characteristics* table ... 6
- Added test conditions to $V_{NR}$ parameter in *Electrical Characteristics* table ... 6
- Added new note (3) to output accuracy parameter in *Electrical Characteristics* table ... 6
- Deleted typical value for $I_{SHDN}$ in *Electrical Characteristics* table ... 6

**Changes from Revision H (January 2013) to Revision I** — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted "Fixed Output Voltages: 0.8 V to 5 V Using Innovating Facatory EEPROM Programming" bullet from *Features* ... 1
- Changed "12.6" to "14" in Low Noise bullet ... 1
- Deleted SNS row from *Pin Functions* table ... 4
- Deleted fixed version from $V_{OUT}$ row in *Electrical Characteristics* ... 6
- Deleted ISNS row from *Electrical Characteristics* ... 6

**Changes from Revision G (April 2012) to Revision H** — **Page**

- Updated Figure 8 ... 7


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**Changes from Revision F (March 2012) to Revision G** **Page**

- Changed Thermal Information table values, added new footnote 2, changed footnote 3 ..... 5

**Changes from Revision E (February 2012) to Revision F** **Page**

- Changed *Low Noise* Features bullet ..... 1
- Updated Equation 3 ..... 17

**Changes from Revision D (December 2010) to Revision E** **Page**

- Changed *Low Noise* Features bullet ..... 1
- Changed caption of front-page application circuit ..... 1
- Updated Figure 12 ..... 7
- Updated Figure 26 ..... 10
- Added Equation 1 note in *Start-up* section ..... 14
- Updated Equation 3 ..... 17

**Changes from Revision C (September, 2010) to Revision D** **Page**

- Updated front-page figure with new characteristic graph ..... 1
- Revised Figure 17 ..... 8
- Changed Figure 18 ..... 8

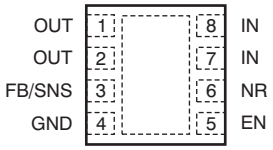
**Changes from Revision B (August, 2010) to Revision C** **Page**

- Changed data sheet title ..... 1
- Changed *ultra-high PSRR* to *wide-bandwidth lhgh PSRR* in *Features* list ..... 1
- Corrected typos in Figure 21 through Figure 23 ..... 9
- Revised first paragraph of *Application Information* to remove phrase *ultra-wide bandwidth* ..... 15

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# 5 Pin Configuration and Functions

**DRB Package**
**8-Pin VSON**
**Top View**




## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 5 | I | Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to *Shutdown* in the *Application and Implementation* section for more details. EN must not be left floating and can be connected to IN if not used. |
| FB/SNS | 3 | I | FB (adjustable version only): This pin is the input to the control loop error amplifier and is used to set the output voltage of the device.<br>SNS (fixed versions only): Output voltage sense pin.(1) |
| GND | 4, pad | — | Ground. |
| IN | 7, 8 | I | Unregulated input supply. |
| OUT | 1, 2 | O | Regulator output. A 4.7-μF or larger capacitor of any type is required for stability. |
| NR | 6 | — | Connect an external capacitor between this pin and ground to reduce output noise to very low levels. Also, the capacitor slows down the $V_{OUT}$ ramp (RC softstart). |

(1) In order to minimize the trace resistive drop, connect the SNS pin close to the load, and make sure that the trace inductance to the load is also minimized.


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | IN | –0.3 | 7 | V |
| | FB, NR | –0.3 | 3.6 | |
| | EN | –0.3 | $V_{IN}$ + 0.3(2) | |
| | OUT | –0.3 | 7 | |
| Current | OUT | Internally Limited | | A |
| Temperature | Operating virtual junction, $T_J$ | –55 | 150 | °C |
| | Operating free air temperature, $T_A$ | –40 | 125 | |
| | Storage, $T_{stg}$ | –55 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) $V_{EN}$ absolute maximum rating is $V_{IN}$ + 0.3 V or 7 V, whichever is smaller.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage(1) | 2.2 | 6.5 | V |
| $I_{OUT}$ | Output current | 0 | 1 | A |
| $T_J$ | Operating junction temperature | –40 | 125 | °C |
| $T_A$ | Operating free air temperature | –40 | 125 | °C |

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.2 V, whichever is greater.

## 6.4 Thermal Information

| THERMAL METRIC(1)(2) | | TPS7A80 DRB (VSON)(3) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 47.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 53.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 23.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 23.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 7.4 | °C/W |

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the DRB package are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) The exposed pad is connected to the PCB ground layer through a 2 × 2 thermal via array.
(b) The top and bottom copper layers are assumed to have a 5% thermal conductivity of copper representing a 20% copper coverage.
(c) This data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3 inches × 3 inches copper area. To understand the effects of the copper area on thermal performance, refer to the *Power Dissipation* and *Estimating Junction Temperature* sections.

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## 6.5 Electrical Characteristics

At $T_J$ = –40°C to +125°C, $V_{IN}$ = $V_{OUT(TYP)}$ + 0.5 V or 2.2 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = 2.2 V, $C_{OUT}$ = 4.7 µF, and $C_{NR}$ = 0.01 µF (unless otherwise noted). TPS7A8001 tested at $V_{OUT}$ = 0.8 V and $V_{OUT}$ = 6 V. Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{NR}$ | Internal reference | Adjustable and Fixed $V_{OUT}$ = 1.2 V | | 0.79 | 0.8 | 0.81 | V |
| | | Fixed $V_{OUT}$ ≥ 1.8 V | | 1.23 | 1.243 | 1.26 | V |
| $V_{OUT}$ | Output voltage | Adjustable version only (TPS7A8001) | | 0.8 | | 6 | V |
| | | Fixed versions only | | 1.2 | | 5 | V |
| | Output accuracy(1)(2) | $V_{OUT}$ + 0.5 V ≤ $V_{IN}$ ≤ 6 V, $V_{IN}$ ≥ 2.5 V, 100 mA ≤ $I_{OUT}$ ≤ 500 mA, 0°C ≤ $T_J$ ≤ 85°C | | –2% | | 2% | |
| | | $V_{OUT}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.5 V, $V_{IN}$ ≥ 2.2 V, 100 mA ≤ $I_{OUT}$ ≤ 1 A | | –3% | ±0.3% | 3% | |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation | $V_{OUT(NOM)}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.5 V, $V_{IN}$ ≥ 2.2 V, $I_{OUT}$ = 100 mA | | | 150 | | µV/V |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | 100 mA ≤ $I_{OUT}$ ≤ 1 A | | | 2 | | µV/mA |
| $V_{DO}$ | Dropout voltage(3) | $V_{OUT}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.5 V, $V_{IN}$ ≥ 2.2 V, $I_{OUT}$ = 500 mA, $V_{FB}$ = GND or $V_{SNS}$ = GND | | | | 250 | mV |
| | | $V_{OUT}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.5 V, $V_{IN}$ ≥ 2.5 V, $I_{OUT}$ = 750 mA, $V_{FB}$ = GND or $V_{SNS}$ = GND | | | | 350 | mV |
| | | $V_{OUT}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.5 V, $V_{IN}$ ≥ 2.5 V, $I_{OUT}$ = 1 A, $V_{FB}$ = GND or $V_{SNS}$ = GND | | | | 500 | mV |
| $I_{CL}$ | Output current limit | $V_{OUT}$ = 0.85 × $V_{OUT(NOM)}$, $V_{IN}$ ≥ 3.3 V | Adjustable | 1100 | 1400 | 2000 | mA |
| | | | Fixed | 1100 | | 2000 | |
| $I_{GND}$ | Ground pin current | $I_{OUT}$ = 1 mA, adjustable version only | | | 60 | 100 | µA |
| | | $I_{OUT}$ = 1 mA, fixed versions only | | | | 120 | µA |
| | | $I_{OUT}$ = 1 A | | | | 350 | µA |
| $I_{SHDN}$ | Shutdown current ($I_{GND}$) | $V_{EN}$ ≤ 0.4 V, $V_{IN}$ ≥ 2.2 V, $R_L$ = 1 kΩ, 0°C ≤ $T_J$ ≤ 85°C | | | | 2 | µA |
| $I_{FB}$ | Feedback pin current (TPS7A8001) | $V_{IN}$ = 6.5 V, $V_{FB}$ = 0.8 V | | | 0.02 | 1 | µA |
| PSRR | Power-supply rejection ratio | $V_{IN}$ = 4.3 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 750 mA | f = 100 Hz | | 48 | | dB |
| | | | f = 1 kHz | | 63 | | dB |
| | | | f = 10 kHz | | 63 | | dB |
| | | | f = 100 kHz | | 57 | | dB |
| | | | f = 1 MHz | | 38 | | dB |
| $V_N$ | Output noise voltage | BW = 100 Hz to 100 kHz, $V_{IN}$ = 4.3 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 100 mA | $C_{NR}$ = 0.001 µF | | 14.6 × $V_{OUT}$ | | $\mu V_{RMS}$ |
| | | | $C_{NR}$ = 0.01 µF | | 14.3 × $V_{OUT}$ | | $\mu V_{RMS}$ |
| | | | $C_{NR}$ = 0.1µF | | 13.9 × $V_{OUT}$ | | $\mu V_{RMS}$ |
| $V_{EN(HI)}$ | Enable high (enabled) | 2.2 V ≤ $V_{IN}$ ≤ 3.6 V, $R_L$ = 1 kΩ | | 1.2 | | | V |
| | | 3.6 V < $V_{IN}$ ≤ 6.5 V, $R_L$ = 1 kΩ | | 1.35 | | | V |
| $V_{EN(LO)}$ | Enable low (shutdown) | $R_L$ = 1 kΩ | | 0 | | 0.4 | V |
| $I_{EN(HI)}$ | Enable pin current, enabled | $V_{IN}$ = $V_{EN}$ = 6.5 V | | | 0.02 | 1 | µA |
| $t_{STR}$ | Start-up time | $V_{OUT(NOM)}$ = 3.3 V, $V_{OUT}$ = 0%–90% $V_{OUT(NOM)}$, $R_L$ = 3.3 kΩ, $C_{OUT}$ = 4.7 µF | $C_{NR}$ = 1 nF | | 0.1 | | ms |
| | | | $C_{NR}$ = 10 nF | | 1.6 | | ms |
| UVLO | Undervoltage lockout | $V_{IN}$ rising, $R_L$ = 1 kΩ | | 1.86 | 2 | 2.10 | V |
| | UVLO hysteresis | $V_{IN}$ falling, $R_L$ = 1 kΩ | | | 75 | | mV |
| $T_{SD}$ | Thermal shutdown temperature | Shutdown, temperature increasing | | | 160 | | °C |
| | | Reset, temperature decreasing | | | 140 | | °C |

(1) The TPS7A8001 (adjustable) does not include external resistor tolerances and is not tested at these conditions: $V_{OUT}$ = 0.8 V, 4.5 V ≤ $V_{IN}$ ≤ 6.5 V, and 750 mA ≤ $I_{OUT}$ ≤ 1 A because power dissipation is higher than maximum rating of the package.
(2) The TPS7A8012, TPS7A8018, and TPS7A8033 are not tested at these conditions: 4.5 V ≤ $V_{IN}$ ≤ 6.5 V, and 750 mA ≤ $I_{OUT}$ ≤ 1 A because power dissipation is higher than maximum rating of the package.
(3) $V_{DO}$ is not measured for fixed output voltage devices with VOUT < 1.7 V because minimum $V_{IN}$ = 2.2 V.


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## 6.6 Typical Characteristics

At $V_{OUT(TYP)}$ = 3.3 V, $V_{IN}$ = $V_{OUT(TYP)}$ + 0.5 V or 2.2 V (whichever is greater), $I_{OUT}$ = 100 mA, $V_{EN}$ = $V_{IN}$, $C_{IN}$ = 1 µF, $C_{OUT}$ = 4.7 µF, and $C_{NR}$ = 0.01 µF, all temperature values refer to $T_J$ (unless otherwise noted).

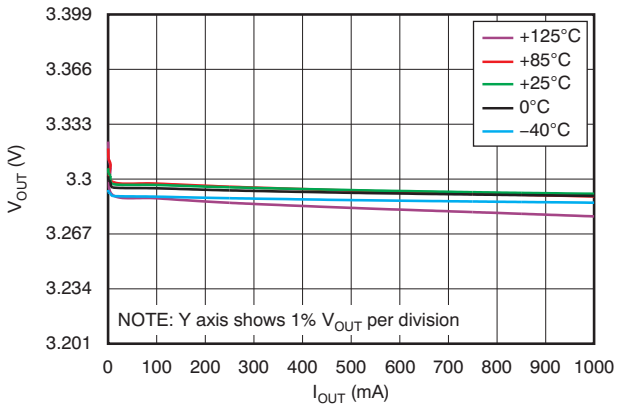



**Figure 1. Load Regulation**

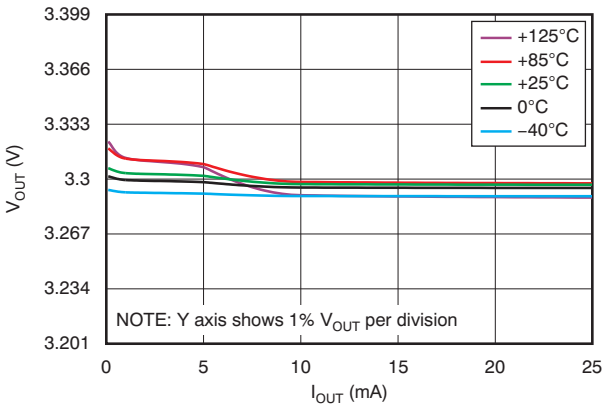



**Figure 2. Load Regulation Under Light Loads**

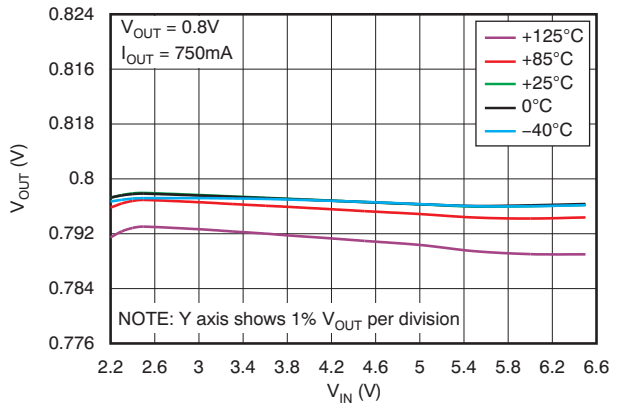



**Figure 3. Line Regulation**

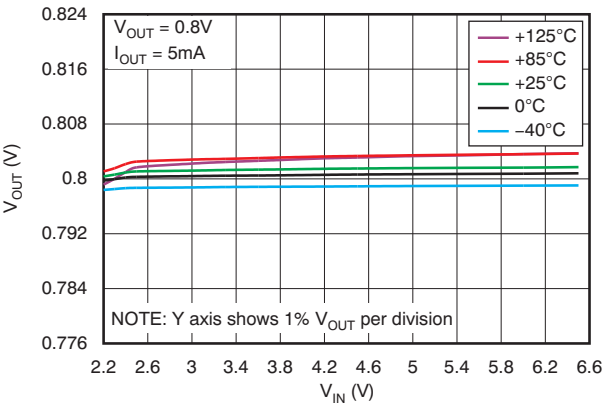



**Figure 4. Line Regulation Under Light Loads**

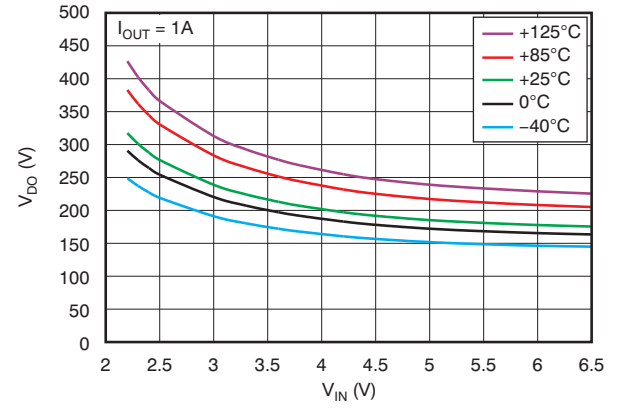



**Figure 5. Dropout Voltage vs Input Voltage**

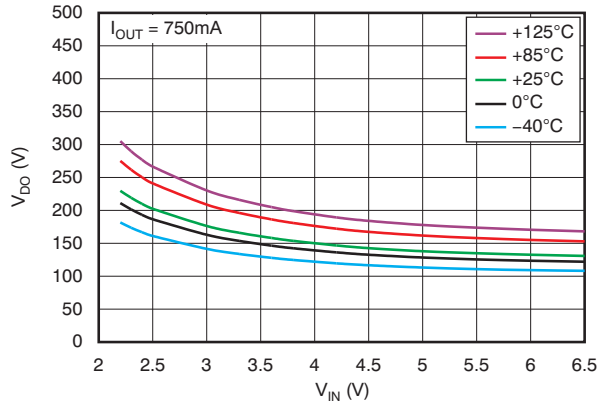



**Figure 6. Dropout Voltage vs Input Voltage**

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## Typical Characteristics (continued)

At $V_{OUT(TYP)}$ = 3.3 V, $V_{IN}$ = $V_{OUT(TYP)}$ + 0.5 V or 2.2 V (whichever is greater), $I_{OUT}$ = 100 mA, $V_{EN}$ = $V_{IN}$, $C_{IN}$ = 1 µF, $C_{OUT}$ = 4.7 µF, and $C_{NR}$ = 0.01 µF, all temperature values refer to $T_J$ (unless otherwise noted).

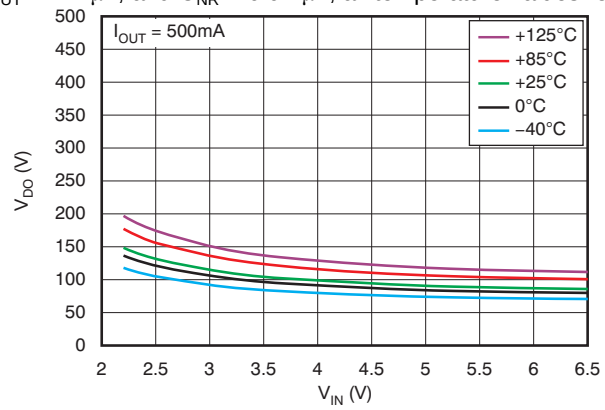



**Figure 7. Dropout Voltage vs Input Voltage**

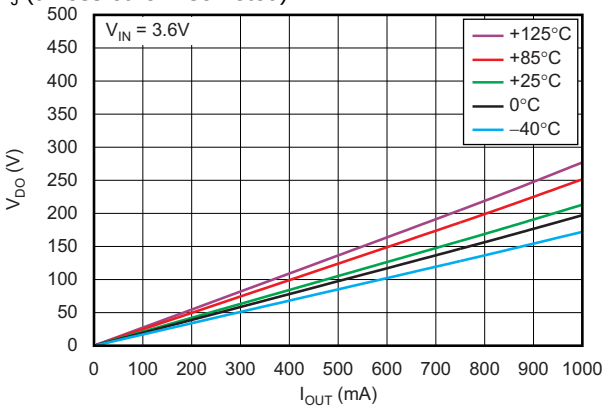



**Figure 8. Dropout Voltage vs Load Current**

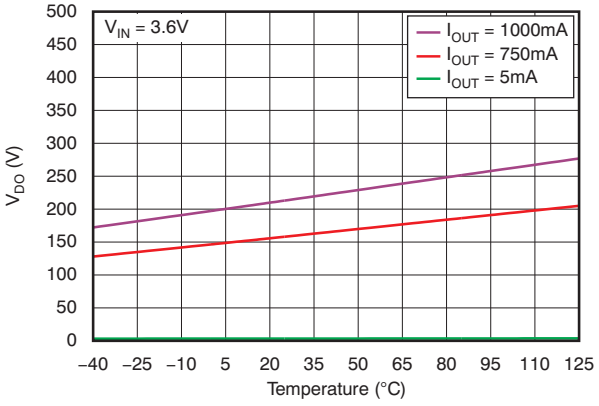



**Figure 9. Dropout Voltage vs Temperature**

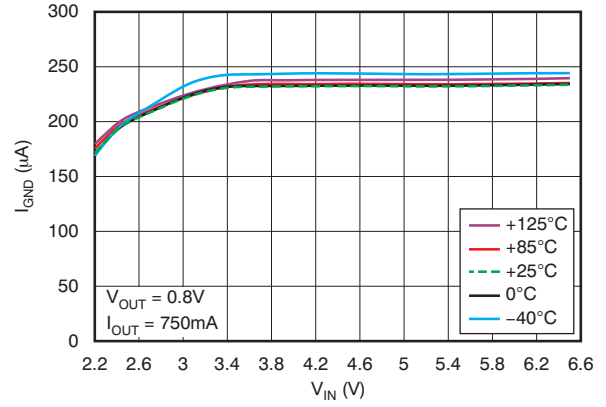



**Figure 10. Ground Pin Current vs Input Voltage**

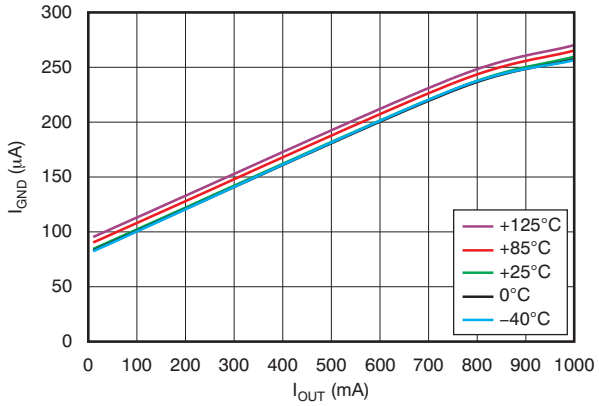



**Figure 11. Ground Pin Current vs Load Current**

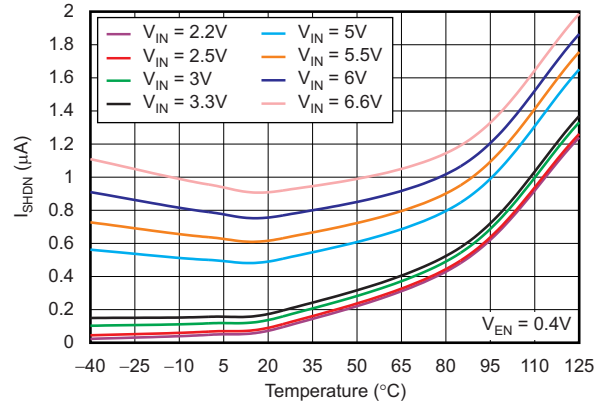



**Figure 12. Shutdown Current vs Temperature**


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## Typical Characteristics (continued)

At $V_{OUT(TYP)}$ = 3.3 V, $V_{IN}$ = $V_{OUT(TYP)}$ + 0.5 V or 2.2 V (whichever is greater), $I_{OUT}$ = 100 mA, $V_{EN}$ = $V_{IN}$, $C_{IN}$ = 1 µF, $C_{OUT}$ = 4.7 µF, and $C_{NR}$ = 0.01 µF, all temperature values refer to $T_J$ (unless otherwise noted).

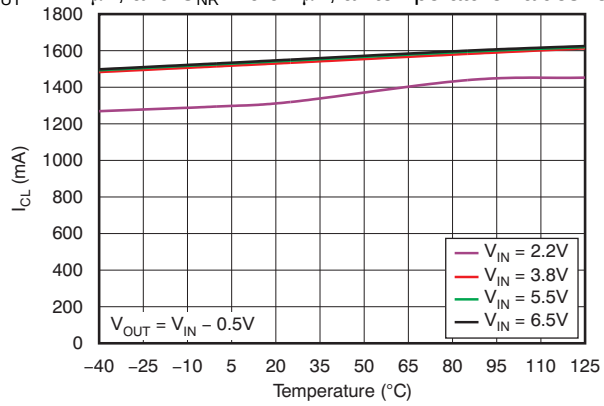



**Figure 13. Current Limit vs Temperature**

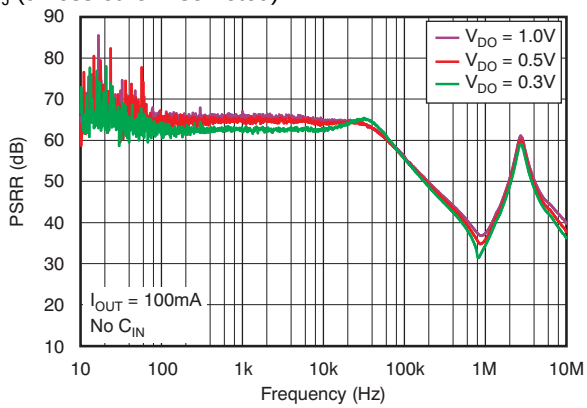



**Figure 14. Power-Supply Ripple Rejection vs Frequency**

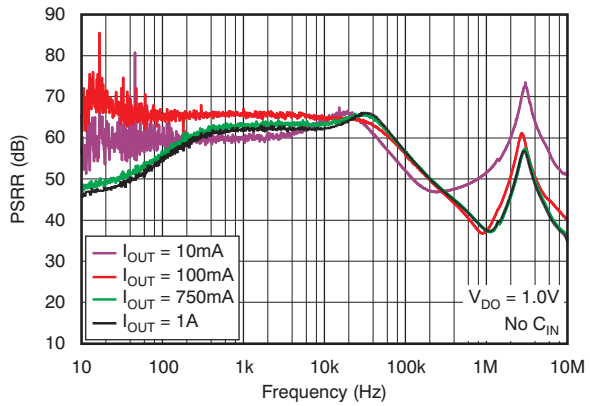



**Figure 15. Power-Supply Ripple Rejection vs Frequency**

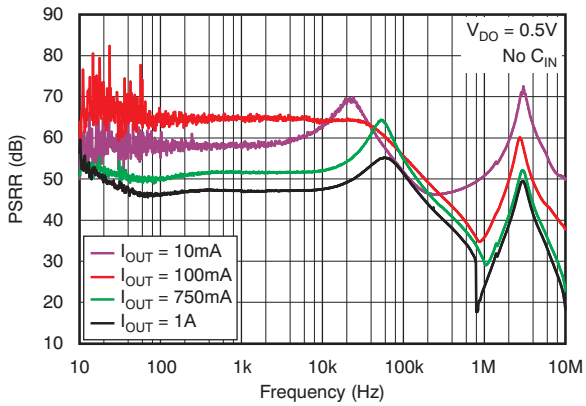



**Figure 16. Power-Supply Ripple Rejection vs Frequency**

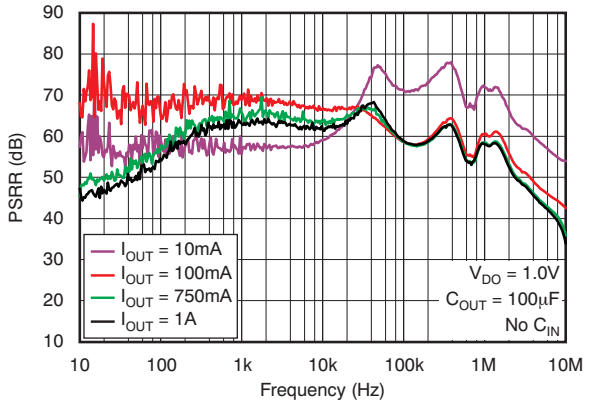



**Figure 17. Power-Supply Ripple Rejection vs Frequency**

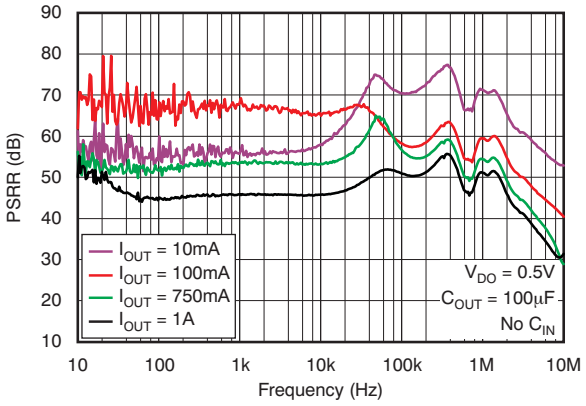



**Figure 18. Power-Supply Ripple Rejection vs Frequency**

## Typical Characteristics (continued)

At $V_{OUT(TYP)}$ = 3.3 V, $V_{IN}$ = $V_{OUT(TYP)}$ + 0.5 V or 2.2 V (whichever is greater), $I_{OUT}$ = 100 mA, $V_{EN}$ = $V_{IN}$, $C_{IN}$ = 1 µF, $C_{OUT}$ = 4.7 µF, and $C_{NR}$ = 0.01 µF, all temperature values refer to $T_J$ (unless otherwise noted).

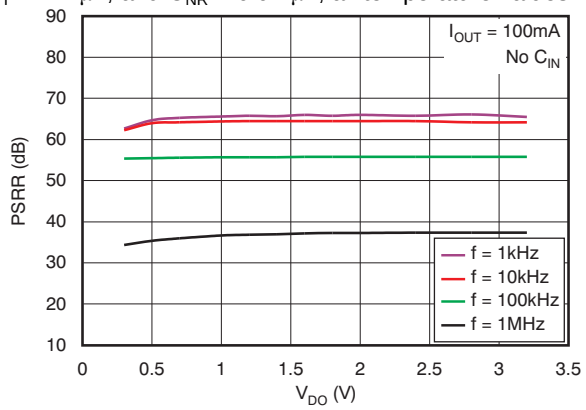



**Figure 19. Power-Supply Ripple Rejection vs Dropout Voltage**

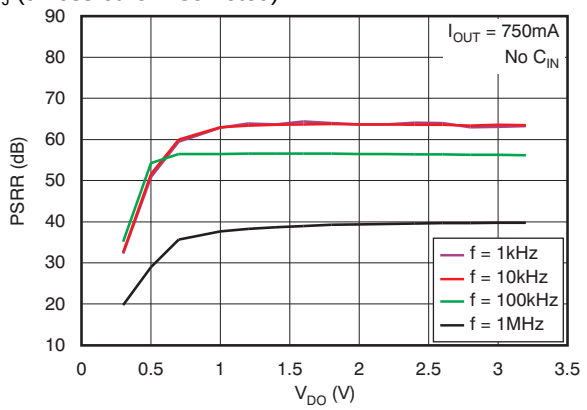



**Figure 20. Power-Supply Ripple Rejection vs Dropout Voltage**

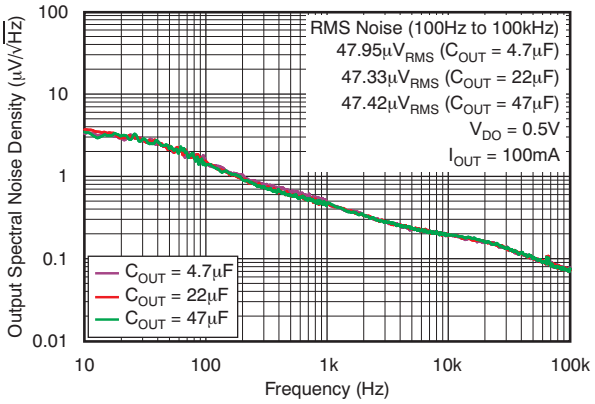



**Figure 21. Output Spectral Noise Density vs Frequency**

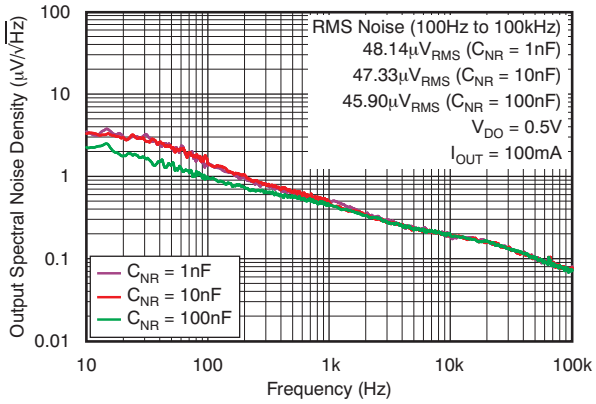



**Figure 22. Output Spectral Noise Density vs Frequency**

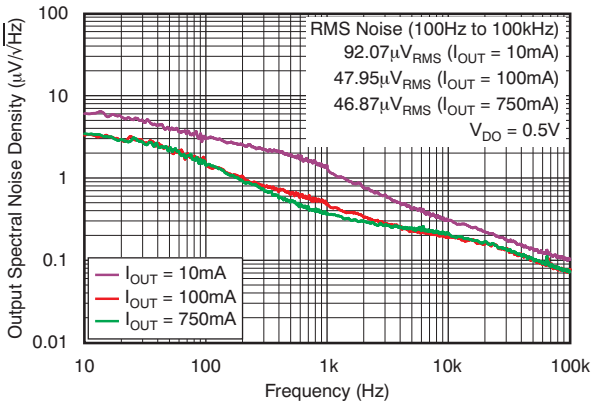



**Figure 23. Output Spectral Noise Density vs Frequency**

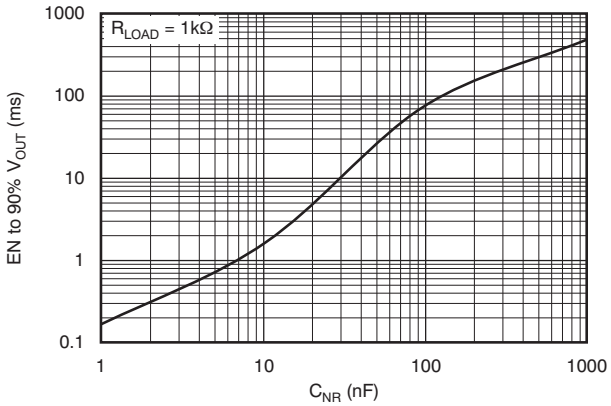



**Figure 24. Start-Up Time vs Noise Reduction Capacitance**


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## Typical Characteristics (continued)

At $V_{OUT(TYP)}$ = 3.3 V, $V_{IN}$ = $V_{OUT(TYP)}$ + 0.5 V or 2.2 V (whichever is greater), $I_{OUT}$ = 100 mA, $V_{EN}$ = $V_{IN}$, $C_{IN}$ = 1 µF, $C_{OUT}$ = 4.7 µF, and $C_{NR}$ = 0.01 µF, all temperature values refer to $T_J$ (unless otherwise noted).

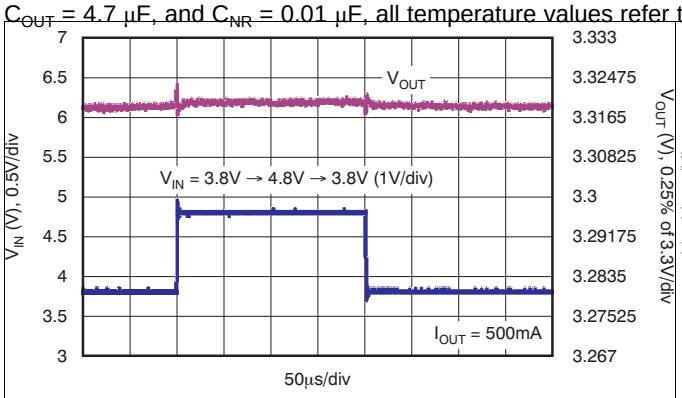



**Figure 25. Line Transient Response**

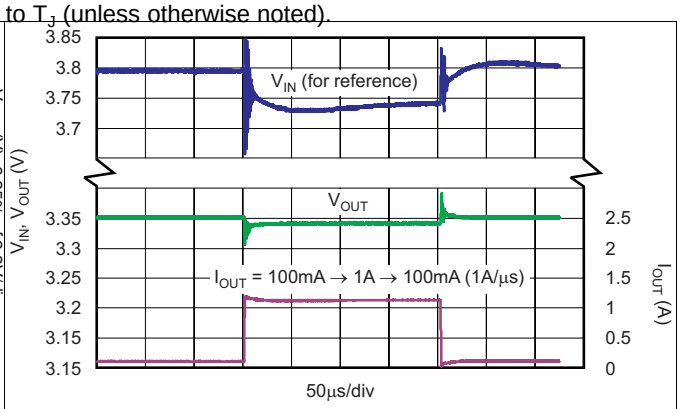



**Figure 26. Load Transient Response**

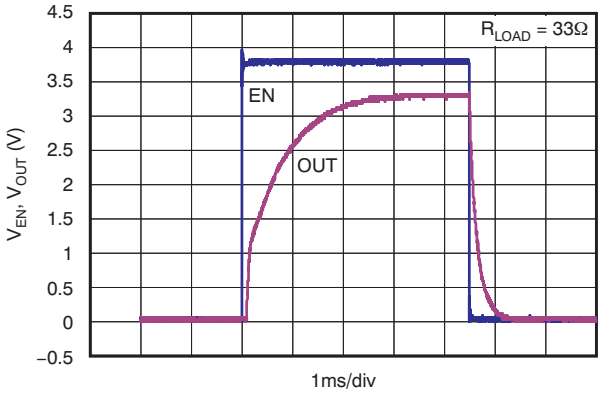
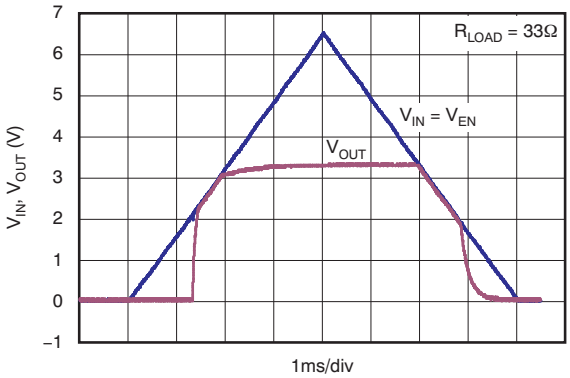



**Figure 27. Enable Pulse Response**




The internal reference requires approximately 2 ms of rampup time (see *Start-Up*); therefore, $V_{OUT}$ fully reaches the target output voltage of 3.3 V in 2 ms from start-up.

**Figure 28. Power-Up and Power-Down Response**

# 7 Detailed Description

## 7.1 Overview

The TPS7A80 devices belong to a family of new-generation LDO regulators that uses innovative circuitry to achieve wide bandwidth and high loop gain, resulting in extremely high PSRR (over a 1-MHz range), even with very low headroom ($V_{IN}$ – $V_{OUT}$). A noise-reduction capacitor ($C_{NR}$) at the NR pin and a bypass capacitor ($C_{BYPASS}$) decrease noise generated by the band-gap reference to improve PSRR, while a quick-start circuit fastcharges the noise-reduction capacitor. This family of regulators offers sub-band-gap output voltages, current limit, and thermal protection, and is fully specified from –40°C to +125°C.

## 7.2 Functional Block Diagram

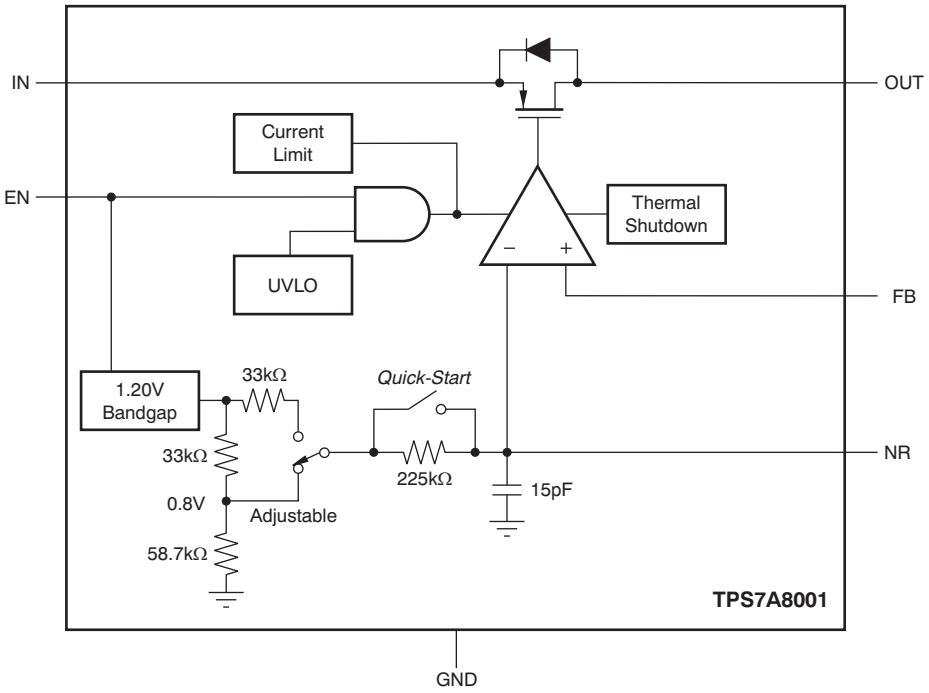



**Figure 29. Adjustable Voltage Version**


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## Functional Block Diagram (continued)

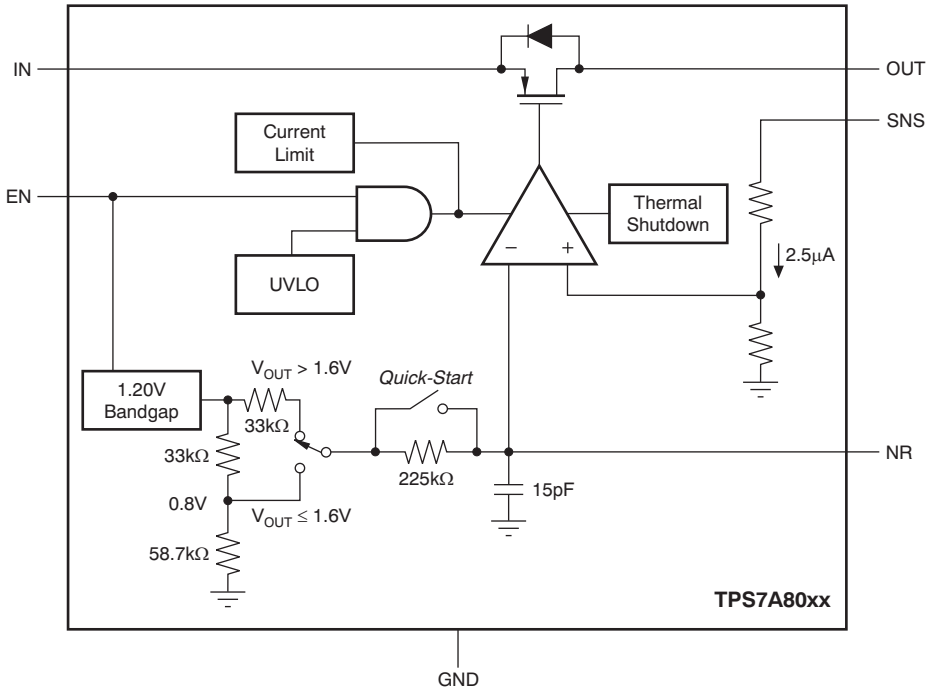



**Figure 30. Fixed Voltage Versions**

## 7.3 Feature Description

### 7.3.1 Internal Current Limit

The TPS7A80 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, do not operate these devices in a current limit state for extended periods of time.

The PMOS pass element in the TPS7A80 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting is required.

### 7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

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## Feature Description (continued)

### 7.3.3 Start-Up

Through a lower resistance, the band-gap reference can quickly charge the noise reduction capacitor ($C_{NR}$). The TPS7A80 have a *quick-start* circuit to quickly charge $C_{NR}$, if present; see the *Functional Block Diagram*. At start-up, this quick-start switch is closed, with only 33 kΩ of resistance between the band-gap reference and the NR pin. The quick-start switch opens approximately 2ms after any device enabling event, and the resistance between the band-gap reference and the NR pin becomes higher in value (approximately 250 kΩ) to form a very good low-pass (RC) filter. This low-pass filter achieves very good noise reduction for the reference voltage.

Inrush current can be a problem in many applications. The 33-kΩ resistance during the start-up period is intentionally put there to slow down the reference voltage ramp up, thus reducing the inrush current. For example, the capacitance of connecting the recommended $C_{NR}$ value of 0.01 µF along with the 33-kΩ resistance causes approximately 1-ms RC delay. Start-up time with the other $C_{NR}$ values can be calculated as Equation 1:

$$t_{STR}\ (s) = 76{,}000 \times C_{NR}\ (F) \quad (1)$$

Equation 1 is valid up to $t_{STR}$ = 2 ms or $C_{NR}$ = 26 nF, whichever is smaller.

Although the noise reduction effect is nearly saturated at 0.01 µF, connecting a $C_{NR}$ value greater than 0.01 µF can help reduce noise slightly more; however, start-up time will be extremely long because the quick-start switch opens after approximately 2 ms. That is, if $C_{NR}$ is not fully charged during this 2 ms period, $C_{NR}$ finishes charging through a higher resistance of 250 kΩ, and takes much longer to fully charge.

A low leakage $C_{NR}$ should be used; most ceramic capacitors are suitable.

### 7.3.4 Undervoltage Lockout (UVLO)

The TPS7A80 use an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that it typically ignores undershoot transients on the input if they are less than 50-µs duration.

## 7.4 Device Functional Modes

Driving the EN pin over 1.2 V for $V_{IN}$ from 2.2 V to 3.6 V or 1.35 V for $V_{IN}$ from 3.6 V to 6.5 V turns on the regulator. Driving the EN pin below 0.4 V causes the regulator to enter shutdown mode.

In shutdown, the current consumption of the device is reduced to 0.02 µA, typically.


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS7A80 devices belong to a family of new generation LDO regulators that use innovative circuitry to achieve wide bandwidth and high loop gain, resulting in extremely high PSRR (over a 1-MHz range) at very low headroom ($V_{IN}$ – $V_{OUT}$). A noise reduction capacitor ($C_{NR}$) at the NR pin bypasses noise generated by the band-gap reference to improve PSRR, while a quick-start circuit fast-charges this capacitor. This family of regulators offers sub-band-gap output voltages, current limit, and thermal protection, and is fully specified from –40°C to 125°C.

Figure 31 gives the connections for the adjustable-output version (TPS7A8001). Figure 32 shows the connections for the fixed-voltage versions.

## 8.2 Typical Application

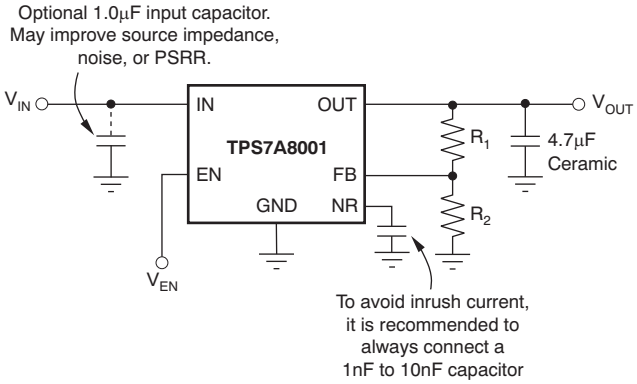



**Figure 31. Typical Application Circuit: Adjustable-Voltage Version**

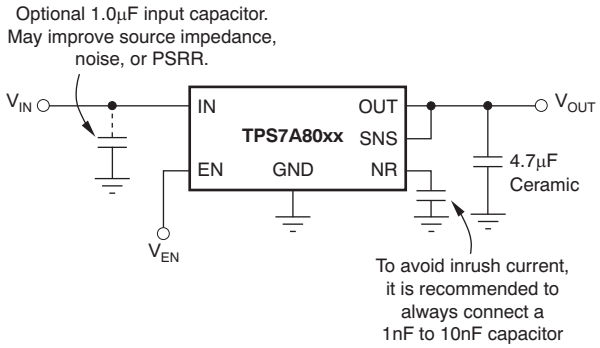



**Figure 32. Typical Application Circuit: Fixed-Voltage Versions**

## Typical Application (continued)

### 8.2.1 Design Requirements

#### *8.2.1.1 Dropout Voltage*

The TPS7A80 use a PMOS pass transistor to achieve low dropout. When ($V_{IN}$ – $V_{OUT}$) is less than the dropout voltage ($V_{DO}$), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. $V_{DO}$ scales approximately with output current because the PMOS device in dropout behaves the same way as a resistor.

As with any linear regulator, PSRR and transient response are degraded as ($V_{IN}$ – $V_{OUT}$) approaches dropout. This effect is shown in Figure 19 and Figure 20 in the *Typical Characteristics* section.

#### *8.2.1.2 Minimum Load*

The TPS7A80 are stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS7A80 employ an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

#### *8.2.1.3 Input and Output Capacitor Requirements*

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-μF to 1-μF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor may be necessary to provide stability.

The TPS7A80 are designed to be stable with standard ceramic capacitors of capacitance values 4.7 μF or larger. These devices is evaluated using a 4.7-μF ceramic capacitor of 10-V rating, 10% tolerance, X5R type, and 0805 size (2 mm × 1.25 mm).

X5R- and X7R-type capacitors are highly recommended because they have minimal variation in value and ESR over temperature. Maximum ESR should be < 1 Ω.

The TPS7A80 implement an innovative internal compensation circuit that does not require a feedback capacitor across $R_2$ for stability. Do not use a feedback capacitor for this device.

#### *8.2.1.4 Transient Response*

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude, but increases duration of the transient response.


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## Typical Application (continued)

### 8.2.2 Detailed Design Procedure

The voltage on the FB pin sets the output voltage and is determined by the values of $R_1$ and $R_2$. The values of $R_1$ and $R_2$ can be calculated for any voltage using the formula given in Equation 2:

$$V_{OUT} = \frac{(R_1 + R_2)}{R_2} \times 0.800 \quad (2)$$

Sample resistor values for common output voltages are shown in Table 1. In Table 1, E96 series resistors are used, and all values meet 1% of the target $V_{OUT}$, assuming resistors with zero error. For the actual design, pay attention to any resistor error factors. Using lower values for $R_1$ and $R_2$ reduces the noise injected from the FB pin.

**Table 1. Sample 1% Resistor Values for Common Output Voltages**

| $V_{OUT}$ | $R_1$ | $R_2$ |
|---|---|---|
| 0.8 V | 0 Ω (Short) | Do not populate |
| 1 V | 2.49 kΩ | 10 kΩ |
| 1.2 V | 4.99 kΩ | 10 kΩ |
| 1.5 V | 8.87 kΩ | 10 kΩ |
| 1.8 V | 12.5 kΩ | 10 kΩ |
| 2.5 V | 21 kΩ | 10 kΩ |
| 3.3 V | 30.9 kΩ | 10 kΩ |
| 5 V | 52.3 kΩ | 10 kΩ |

#### *8.2.2.1 Output Noise*

In most LDOs, the band gap is the dominant noise source. If a noise reduction capacitor ($C_{NR}$) is used with the TPS7A80, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-µF (minimum) noise-reduction capacitor.

Equation 3 approximates the total noise when $C_{NR}$ = 0.01 µF:

$$V_N = 14.6 \times V_{OUT} + (\mu V_{RMS}) \quad (3)$$

### 8.2.3 Application Curve

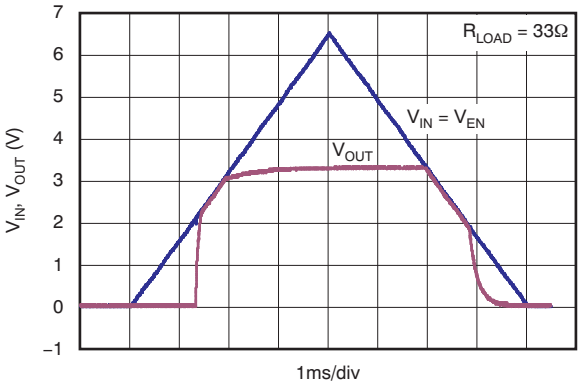



**Figure 33. Power-Up and Power-Down Response**

# 9 Power Supply Recommendations

These devices are designed to operate with an input voltage supply range from 2.2 V to 6.5 V. The input voltage range should provide adequate headroom for the device to have a regulated output. Use a well-regulated input supply. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

# 10 Layout

## 10.1 Layout Guidelines

### 10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

### 10.1.2 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A80 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A80 into thermal shutdown degrades device reliability.

### 10.1.3 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

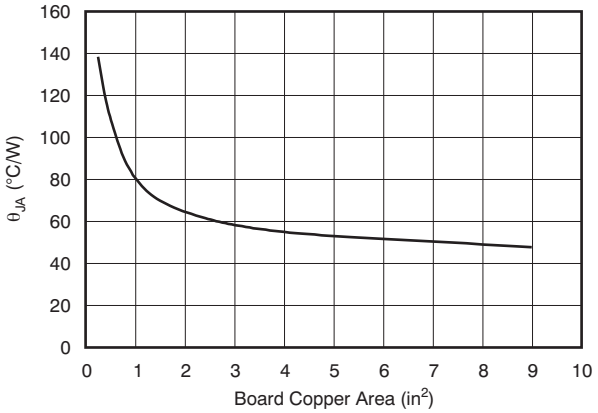
On the VSON (DRB) package, the primary conduction path for heat is through the exposed pad to the printed-circuit-board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to make sure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and is calculated using Equation 5:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \quad (5)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking is estimated using Figure 34.


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## Layout Guidelines (continued)




NOTE: $\theta_{JA}$ value at board size of 9 $in^2$ (that is, 3 inches × 3 inches) is a JEDEC standard.

**Figure 34. $R_{\theta JA}$ vs Board Size**

Figure 34 shows the variation of $\theta_{JA}$ as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

**NOTE**

When the device is mounted on an application PCB, it is strongly recommended to use $\Psi_{JT}$ and $\Psi_{JB}$, as explained in the section.

### 10.1.4 Estimating Junction Temperature

Using the thermal metrics $\Psi_{JT}$ and $\Psi_{JB}$, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 6). For backwards compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{6}$$

Where $P_D$ is the power dissipation shown by Equation 5, $T_T$ is the temperature at the center-top of the IC package, and $T_B$ is the PCB temperature measured 1 mm away from the IC package *on the PCB surface* (as Figure 36 shows).

**NOTE**

Both $T_T$ and $T_B$ can be measured on actual application boards using a thermo gun (an infrared thermometer).

For more information about measuring $T_T$ and $T_B$, see *Using New Thermal Metrics*.

By looking at Figure 35, the new thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) have very little dependency onboard size. That is, using $\Psi_{JT}$ or $\Psi_{JB}$ with Equation 6 is a good way to estimate $T_J$ by simply measuring $T_T$ or $T_B$, regardless of the application board size.

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## Layout Guidelines (continued)

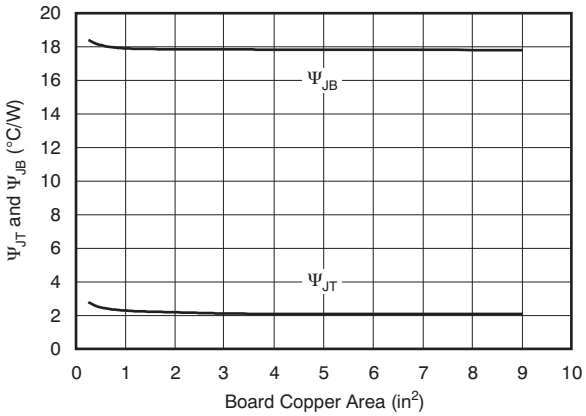



**Figure 35. $\Psi_{JT}$ and $\Psi_{JB}$ vs Board Size**

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see *Using New Thermal Metrics*. For further information, see *Semiconductor and IC Package Thermal Metrics*.

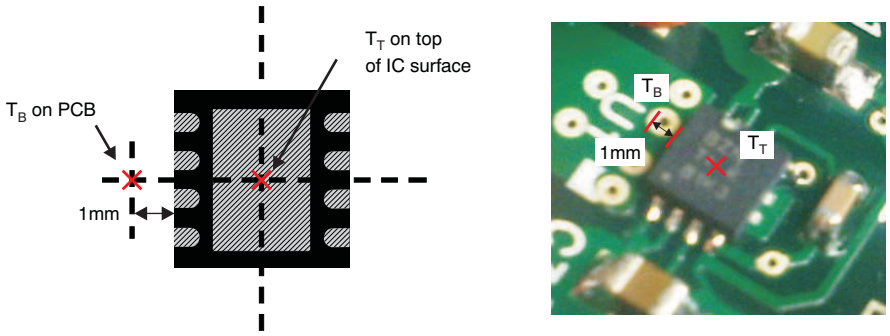



**Figure 36. Measuring Points for $T_T$ and $T_B$**


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## 10.2 Layout Example

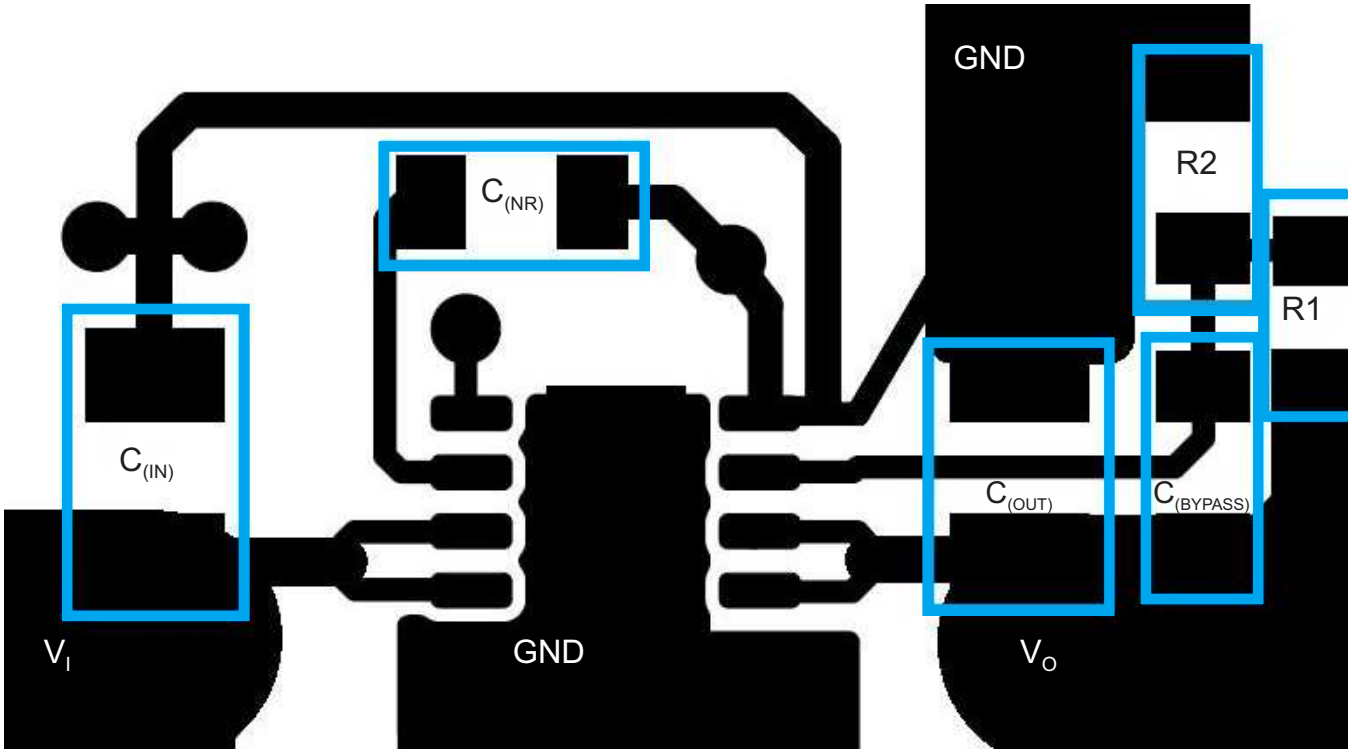



**Figure 37. Layout Example**

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation see the following:

*TPS7A80xxDRBEVM User's Guide*

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS7A8001DRBR | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OFU |
| TPS7A8001DRBR.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OFU |
| TPS7A8001DRBT | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OFU |
| TPS7A8001DRBT.A | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OFU |
| TPS7A8001DRBTG4 | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OFU |
| TPS7A8001DRBTG4.A | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OFU |
| TPS7A8012DRBR | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G1H |
| TPS7A8012DRBR.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G1H |
| TPS7A8012DRBT | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G1H |
| TPS7A8012DRBT.A | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G1H |
| TPS7A8018DRBR | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G2H |
| TPS7A8018DRBR.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G2H |
| TPS7A8018DRBT | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G2H |
| TPS7A8018DRBT.A | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G2H |
| TPS7A8033DRBR | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G3H |
| TPS7A8033DRBR.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G3H |
| TPS7A8033DRBT | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G3H |
| TPS7A8033DRBT.A | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G3H |
| TPS7A8050DRBR | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G4H |
| TPS7A8050DRBR.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G4H |
| TPS7A8050DRBRG4 | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1G4H |
| TPS7A8050DRBRG4.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1G4H |
| TPS7A8050DRBT | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G4H |
| TPS7A8050DRBT.A | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1G4H |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

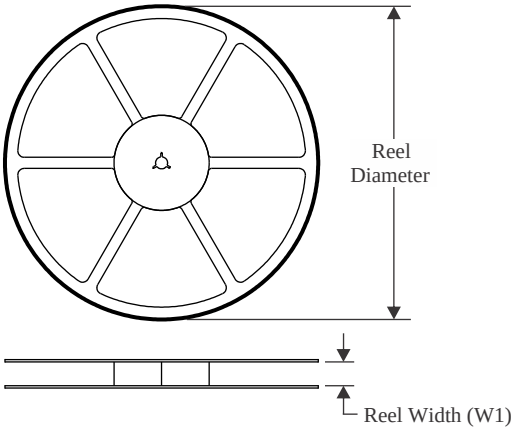
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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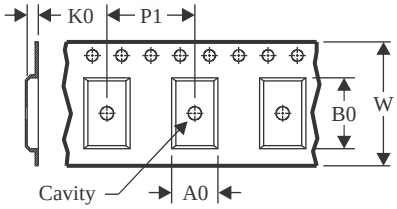
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

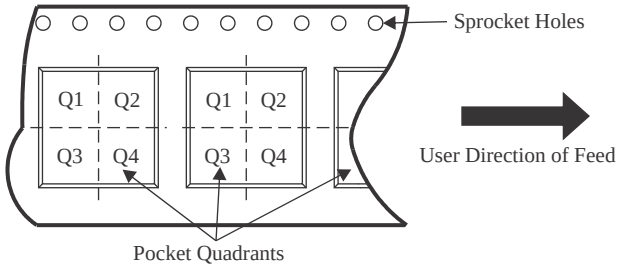



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

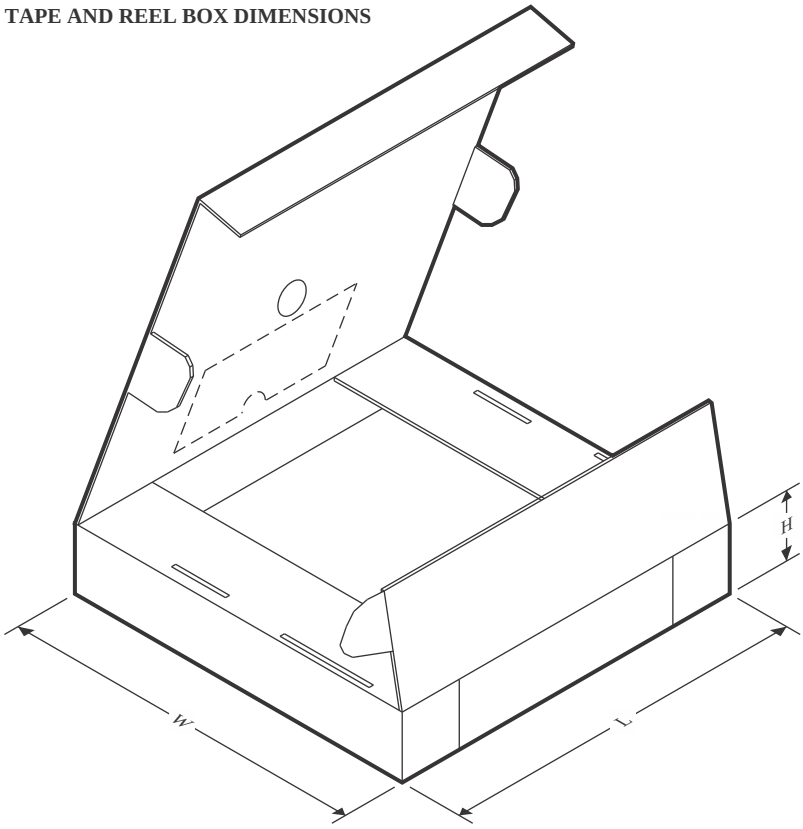
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7A8001DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A8001DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A8001DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A8001DRBTG4 | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A8012DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A8012DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A8018DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A8018DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A8033DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A8033DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A8050DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A8050DRBRG4 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A8050DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7A8001DRBR | SON | DRB | 8 | 3000 | 360.0 | 360.0 | 36.0 |
| TPS7A8001DRBT | SON | DRB | 8 | 250 | 213.0 | 191.0 | 35.0 |
| TPS7A8001DRBT | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TPS7A8001DRBTG4 | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TPS7A8012DRBR | SON | DRB | 8 | 3000 | 360.0 | 360.0 | 36.0 |
| TPS7A8012DRBT | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TPS7A8018DRBR | SON | DRB | 8 | 3000 | 360.0 | 360.0 | 36.0 |
| TPS7A8018DRBT | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TPS7A8033DRBR | SON | DRB | 8 | 3000 | 360.0 | 360.0 | 36.0 |
| TPS7A8033DRBT | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TPS7A8050DRBR | SON | DRB | 8 | 3000 | 360.0 | 360.0 | 36.0 |
| TPS7A8050DRBRG4 | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS7A8050DRBT | SON | DRB | 8 | 250 | 210.0 | 185.0 | 35.0 |

## GENERIC PACKAGE VIEW

# DRB 8

# VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

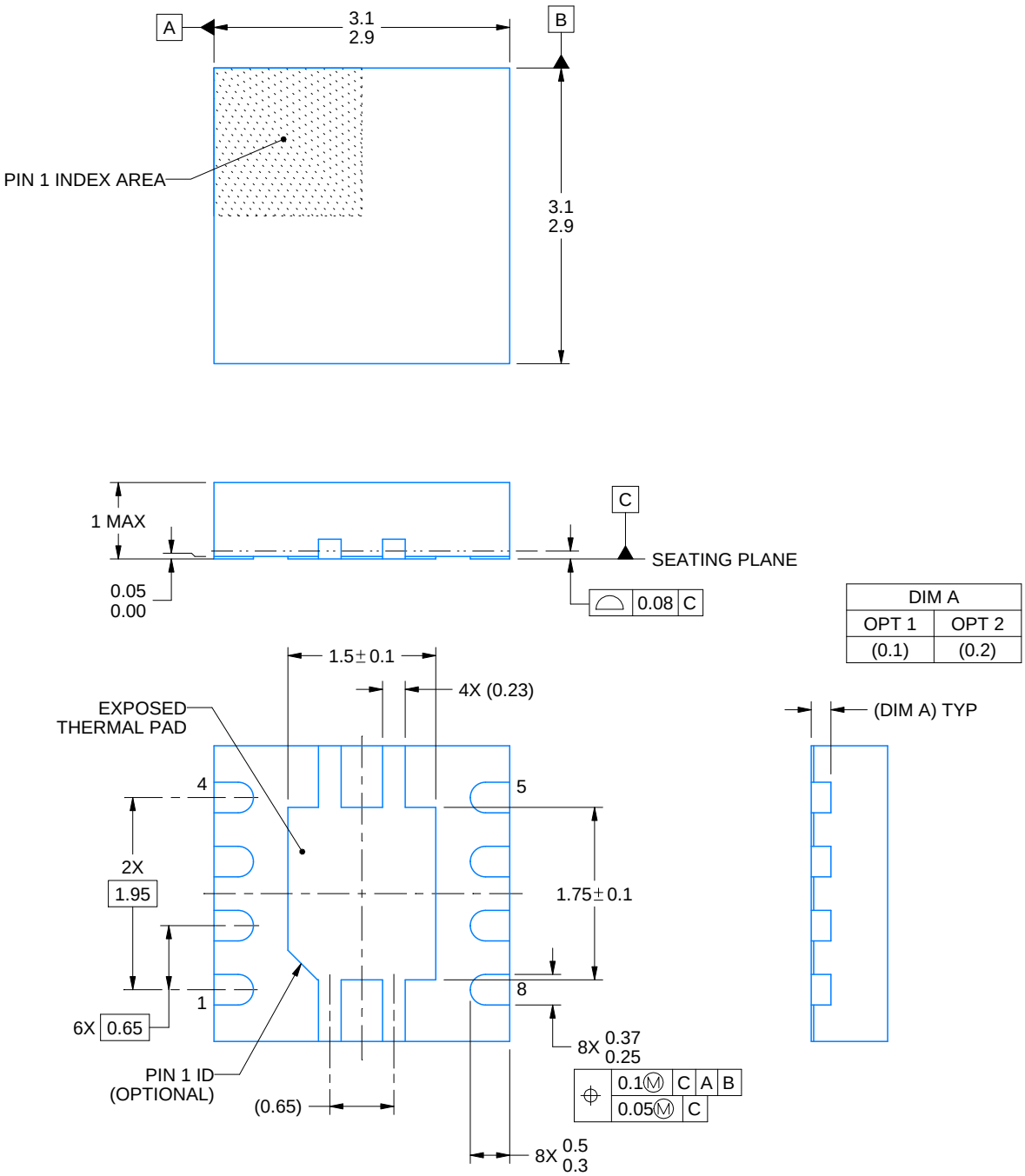
4203482/L

# PACKAGE OUTLINE

## DRB0008A

## VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




NOTES:

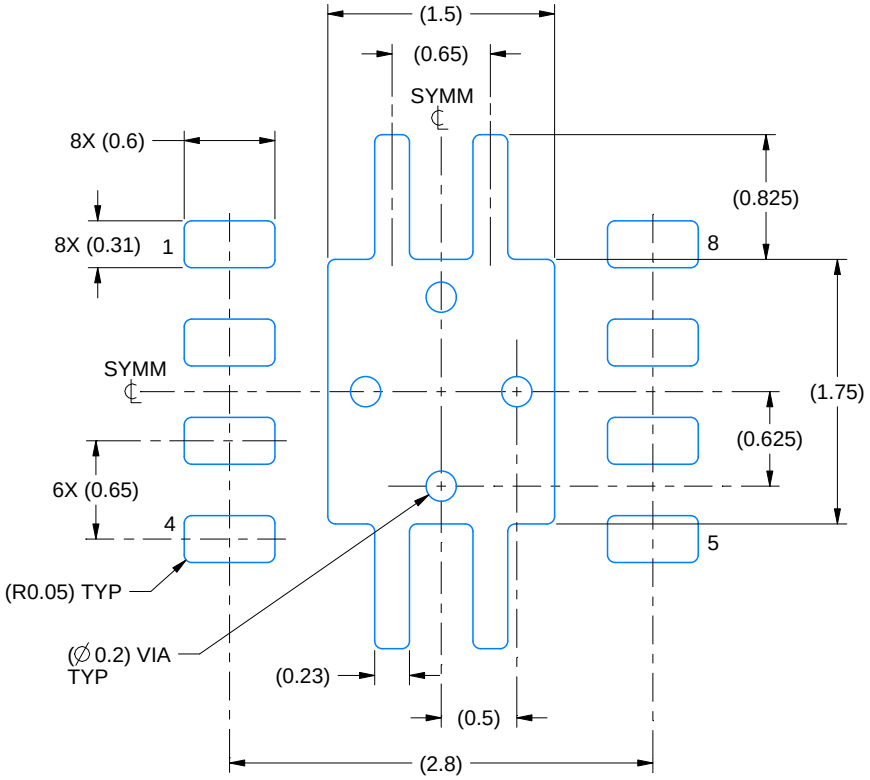
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

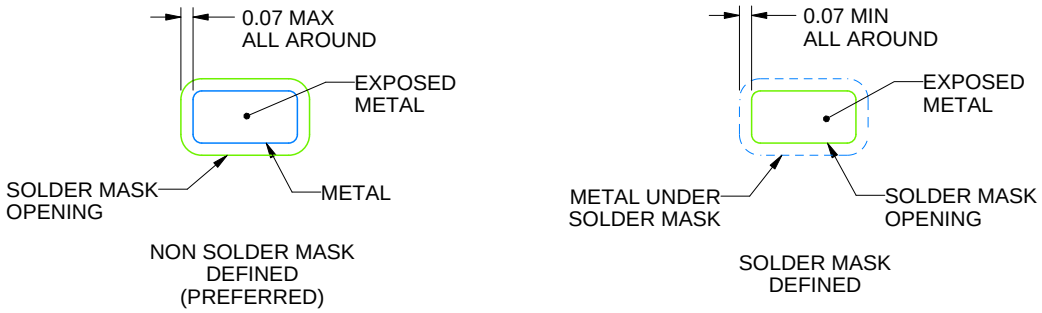
## DRB0008A

## VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

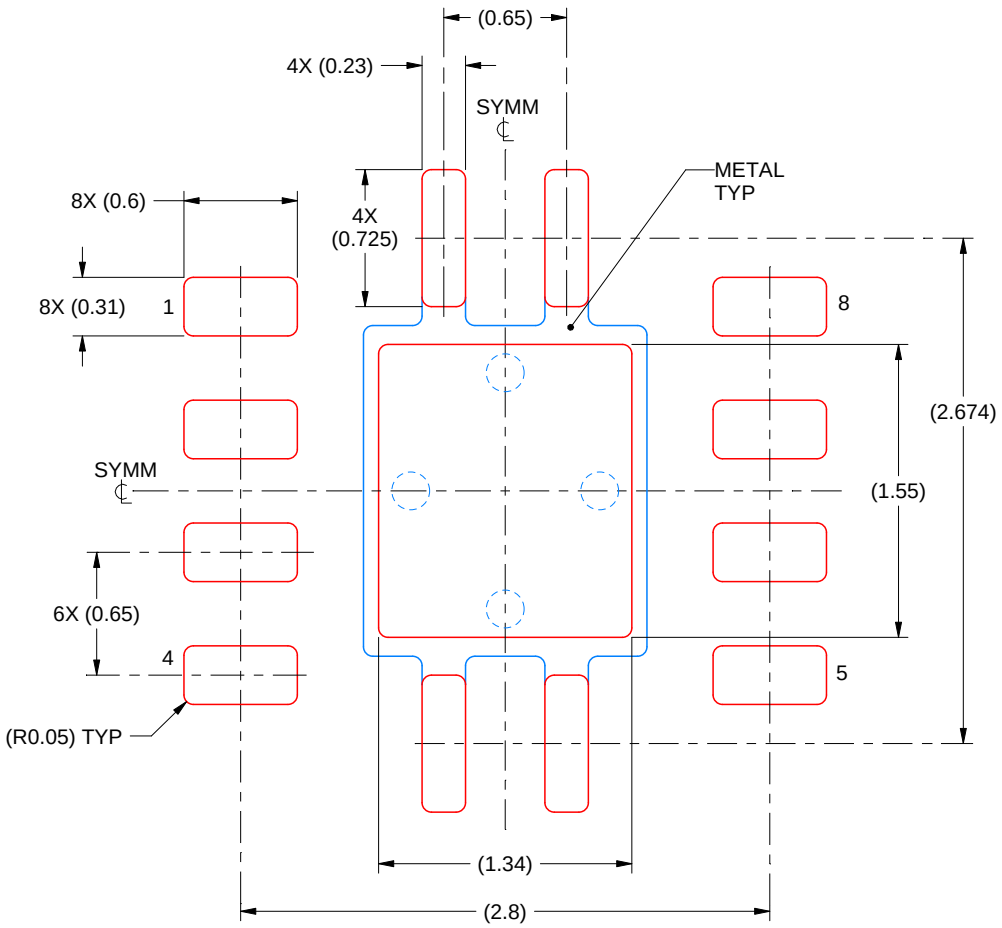



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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